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LAN9252

2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs

Highlights

- 2/3-port EtherCAT slave controller with 3 Fieldbus Memory Management Units (FMMUs) and 4 SyncManagers
- Interfaces to most 8/16-bit embedded controllers and 32-bit embedded controllers with an 8/16-bit bus
- Integrated Ethernet PHYs with HP Auto-MDIX
- Wake on LAN (WoL) support
- Low power mode allows systems to enter sleep mode until addressed by the Master
- Cable diagnostic support
- 1.8V to 3.3V variable voltage I/O
- Integrated 1.2V regulator for single 3.3V operation
- Low pin count and small body size package

Target Applications

- Motor Motion Control
- Process/Factory Automation
- Communication Modules, Interface Cards
- Sensors
- Hydraulic & Pneumatic Valve Systems
- Operator Interfaces

Key Benefits

- Integrated high-performance 100Mbps Ethernet transceivers
  - Compliant with IEEE 802.3/802.3u (Fast Ethernet)
  - 100BASE-FX support via external fiber transceiver
  - Loop-back modes
  - Automatic polarity detection and correction
  - HP Auto-MDIX
- EtherCAT slave controller
  - Supports 3 FMMUs
  - Supports 4 SyncManagers
  - Distributed clock support allows synchronization with other EtherCAT devices
  - 4K bytes of DPRAM
- 8/16-Bit Host Bus Interface
  - Indexed register or multiplexed bus
  - Allows local host to enter sleep mode until addressed by EtherCAT Master
  - SPI / Quad SPI support
- Digital I/O Mode for optimized system cost
- 3rd port for flexible network configurations
- Comprehensive power management features
  - 3 power-down levels
  - Wake on link status change (energy detect)
  - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
  - Wakeup indicator event signal
- Power and I/O
  - Integrated power-on reset circuit
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
  - Single 3.3V power supply (integrated 1.2V regulator)
- Additional Features
  - Multifunction GPIOs
  - Ability to use low cost 25MHz crystal for reduced BOM
- Packaging
  - Pb-free RoHS compliant 64-pin QFN or 64-pin TQFP-EP
- Available in commercial, industrial, and extended industrial* temp. ranges

*Extended temp. (105ºC) is supported only in the 64-QFN with an external voltage regulator (internal regulator must be disabled) and 2.5V (typ) Ethernet magnetics.

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-T	10 Mbps Ethernet, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE802.3u compliant
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
AN	Auto-Negotiation
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8 bits
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32 bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
LVDS	Low Voltage Differential Signaling
MDI	Medium Dependent Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLD	Multicast Listening Discovery
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8 mA sink and 8 mA source
VOD8	Variable voltage open-drain output with 8 mA sink
VO12	Variable voltage output with 12 mA sink and 12 mA source
VOD12	Variable voltage open-drain output with 12 mA sink
VOS12	Variable voltage open-source output with 12 mA source
VO16	Variable voltage output with 16 mA sink and 16 mA source
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
ILVPECL	Low voltage PECL input pin
OLVPECL	Low voltage PECL output pin
P	Power pin

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

2.0 GENERAL DESCRIPTION

The LAN9252 is a 2/3-port EtherCAT slave controller with dual integrated Ethernet PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. The LAN9252 supports HP Auto-MDIX, allowing the use of direct connect or cross-over LAN cables. 100BASE-FX is supported via an external fiber transceiver.

The LAN9252 includes an EtherCAT slave controller with 4K bytes of Dual Port memory (DPRAM) and 3 Fieldbus Memory Management Units (FMMUs). Each FMMU performs the task of mapping logical addresses to physical addresses. The EtherCAT slave controller also includes 4 SyncManagers to allow the exchange of data between the EtherCAT master and the local application. Each SyncManager's direction and mode of operation is configured by the EtherCAT master. Two modes of operation are available: buffered mode or mailbox mode. In the buffered mode, both the local microcontroller and EtherCAT master can write to the device concurrently. The buffer within the LAN9252 will always contain the latest data. If newer data arrives before the old data can be read out, the old data will be dropped. In mailbox mode, access to the buffer by the local microcontroller and the EtherCAT master is performed using handshakes, guaranteeing that no data will be dropped.

Two user selectable host bus interface options are available:

- ***Indexed register access***
  This implementation provides three index/data register banks, each with independent Byte/WORD to DWORD conversion. Internal registers are accessed by first writing one of the three index registers, followed by reading or writing the corresponding data register. Three index/data register banks support up to 3 independent driver threads without access conflicts. Each thread can write its assigned index register without the issue of another thread overwriting it. Two 16-bit cycles or four 8-bit cycles are required within the same 32-bit index/data register - however, these access can be interleaved. Direct (non-indexed) read and write accesses are supported to the process data FIFOs. The direct FIFO access provides independent Byte/WORD to DWORD conversion, supporting interleaved accesses with the index/data registers.
- ***Multiplexed address/data bus***
  This implementation provides a multiplexed address and data bus with both single phase and dual phase address support. The address is loaded with an address strobe followed by data access using a read or write strobe. Two back to back 16-bit data cycles or 4 back to back 8-bit data cycles are required within the same 32-bit DWORD. These accesses must be sequential without any interleaved accesses to other registers. Burst read and write accesses are supported to the process data FIFOs by performing one address cycle followed by multiple read or write data cycles.

The HBI supports 8/16-bit operation with big, little, and mixed endian operations. Two process data RAM FIFOs interface the HBI to the EtherCAT slave controller and facilitate the transferring of process data information between the host CPU and the EtherCAT slave. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

An SPI / Quad SPI slave controller provides a low pin count synchronous slave interface that facilitates communication between the device and a host system. The SPI / Quad SPI slave allows access to the System CSRs, internal FIFOs and memories. It supports single and multiple register read and write commands with incrementing, decrementing and static addressing. Single, Dual and Quad bit lanes are supported with a clock rate of up to 80 MHz.

The LAN9252 supports numerous power management and wakeup features. The LAN9252 can be placed in a reduced power mode and can be programmed to issue an external wake signal (IRQ) via several methods, including “Magic Packet”, “Wake on LAN”, wake on broadcast, wake on perfect DA, and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command or one of the wake events.

For simple digital modules without microcontrollers, the LAN9252 can also operate in Digital I/O Mode where 16 digital signals can be controlled or monitored by the EtherCAT master.

To enable star or tree network topologies, the device can be configured as a 3-port slave, providing an additional MII port. This port can be connected to an external PHY, forming a tap along the current daisy chain, or to another LAN9252 creating a 4-port solution. The MII port can point upstream (as Port 0) or downstream (as Port 2).

LED support consists of a standard RUN indicator and a LINK / Activity indicator per port. A 64-bit distributed clock is included to enable high-precision synchronization and to provide accurate information about the local timing of data acquisition.

The LAN9252 can be configured to operate via a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN9252 is available in commercial, industrial, and extended industrial temperature ranges. Figure 2-1 details a typical system application, while Figure 2-2 provides an internal block diagram of the LAN9252.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM

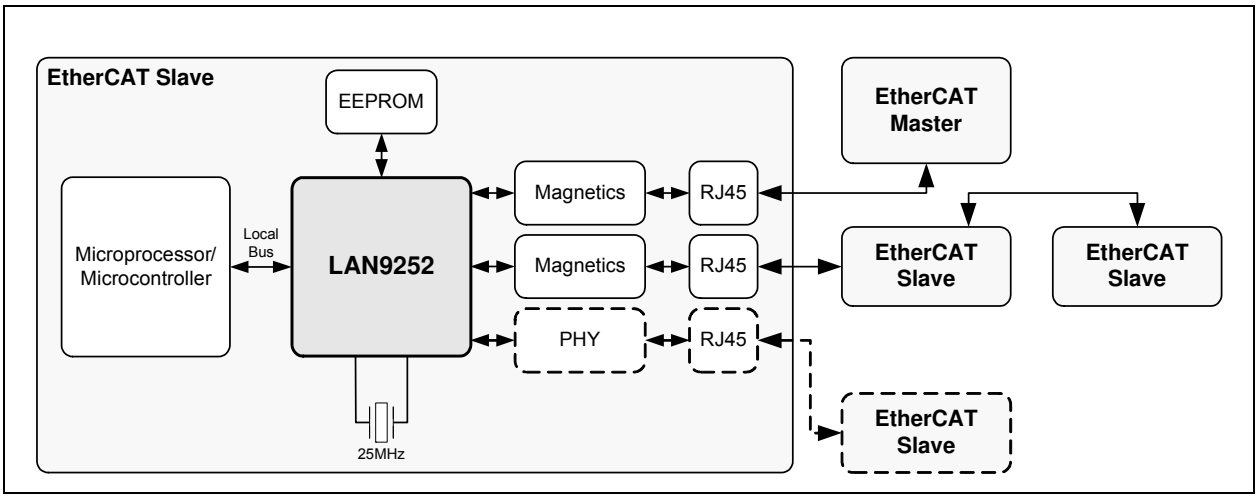
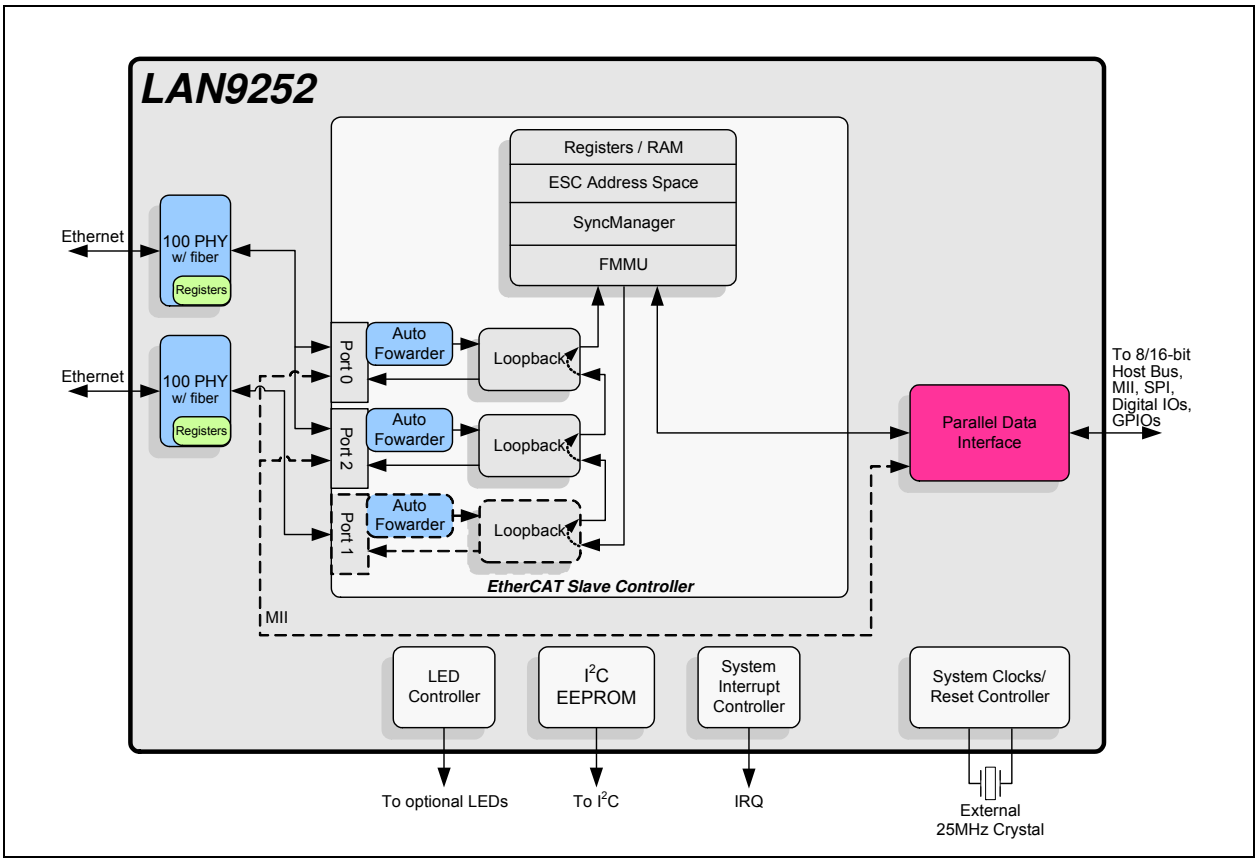


FIGURE 2-2: INTERNAL BLOCK DIAGRAM



The LAN9252 can operate in Microcontroller, Expansion, or Digital I/O mode:

Microcontroller Mode: The LAN9252 communicates with the microcontroller through an SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 8 or 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with an 8 or 16-bit external bus.

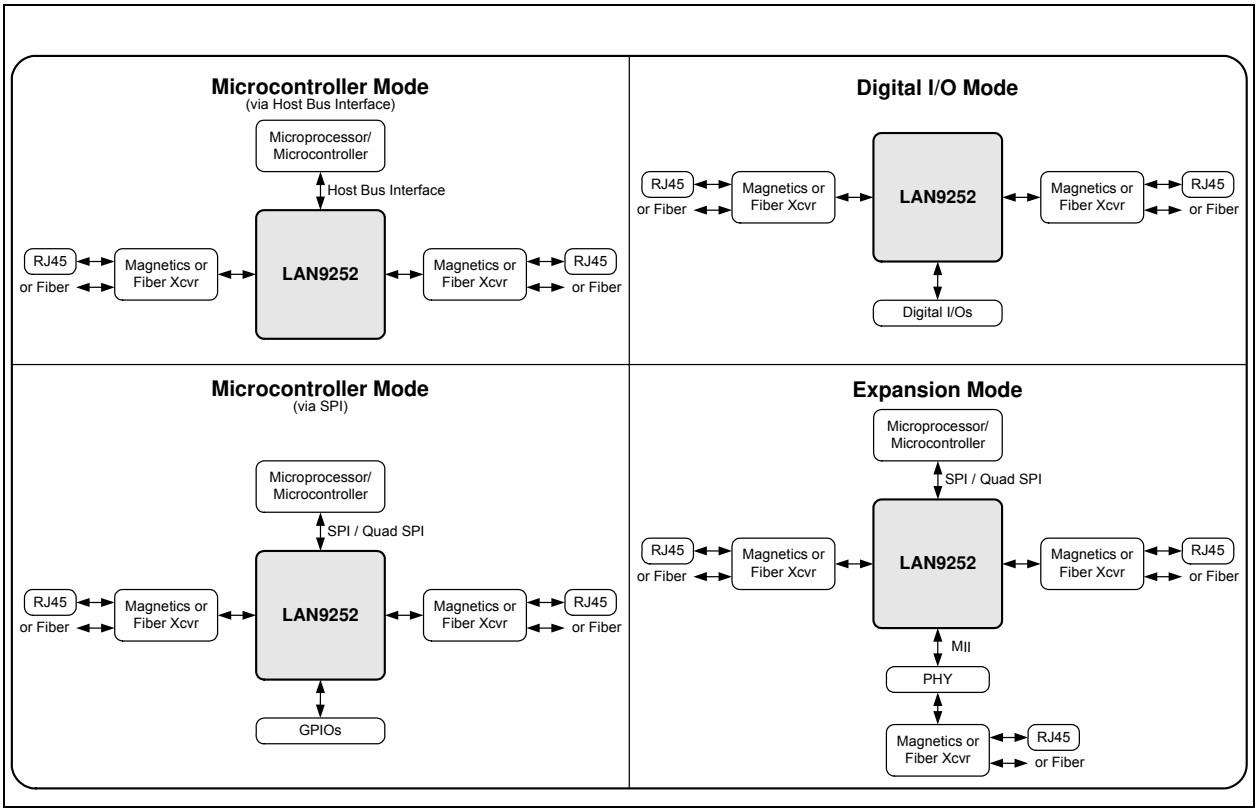
Alternatively, the device can be accessed via SPI or Quad SPI, while also providing up to 16 inputs or outputs for general purpose usage.

Expansion Mode: While the device is in SPI or Quad SPI mode, a third networking port can be enabled to provide an additional MII port. This port can be connected to an external PHY, to enable star or tree network topologies, or to another LAN9252 to create a four port solution. This port can be configured for the upstream or downstream direction.

Digital I/O Mode: For simple digital modules without microcontrollers, the LAN9252 can operate in Digital I/O Mode where 16 digital signals can be controlled or monitored by the EtherCAT master. Six control signals are also provided.

Figure 2-3 provides a system level overview of each mode of operation.

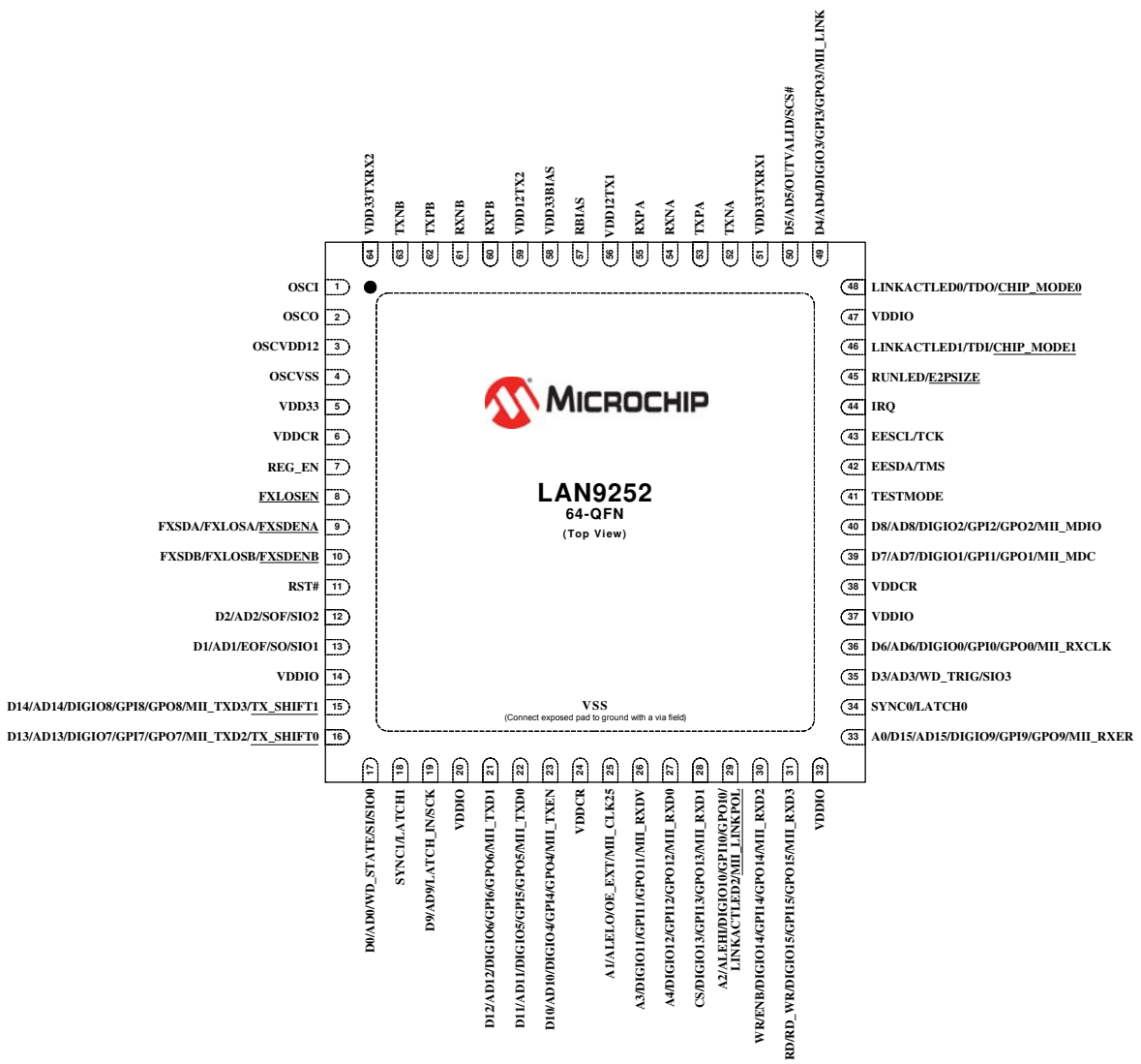
FIGURE 2-3: MODES OF OPERATION



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 64-QFN Pin Assignments

FIGURE 3-1: 64-QFN PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Note: When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-1 details the 64-QFN package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

TABLE 3-1: 64-QFN PACKAGE PIN ASSIGNMENTS

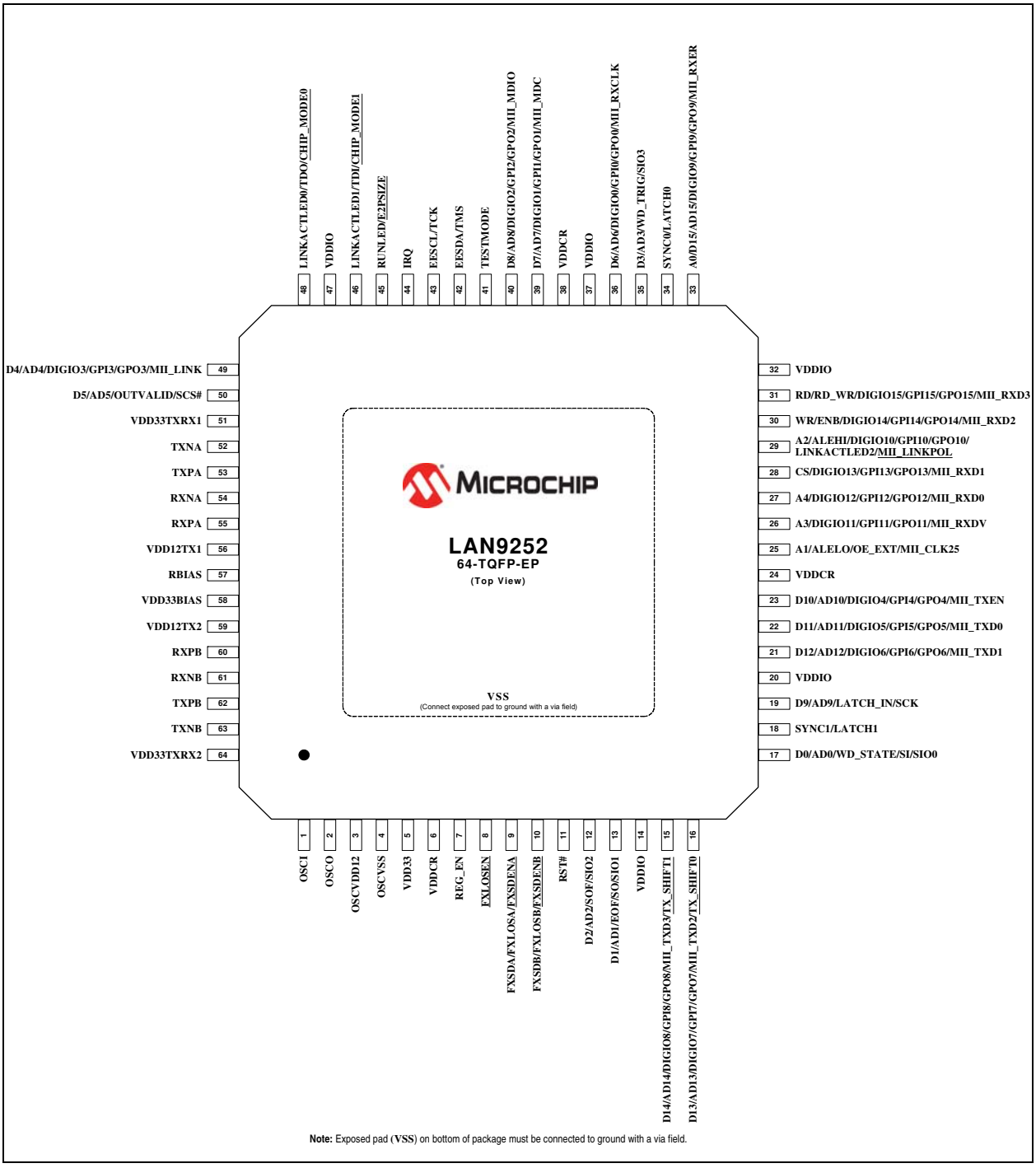
Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	Digital I/O Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name
1	OSCI				
2	OSCO				
3	OSCVDD12				
4	OSCVSS				
5	VDD33				
6	VDDCR				
7	REG_EN				
8	FXLOSEN				
9	FXSDA/FXLOSA/FXSDENA				
10	FXSDB/FXLOSB/FXSDENB				
11	RST#				
12	D2	AD2	SOF	SIO2	
13	D1	AD1	EOF	SO/SIO1	
14	VDDIO				
15	D14	AD14	DIGIO8	GPI8/GPO8	MII_TXD3/ TX_SHIFT1
16	D13	AD13	DIGIO7	GPI7/GPO7	MII_TXD2/ TX_SHIFT0
17	D0	AD0	WD_STATE	SI/SIO0	
18	SYNC1/LATCH1				
19	D9	AD9	LATCH_IN	SCK	
20	VDDIO				
21	D12	AD12	DIGIO6	GPI6/GPO6	MII_TXD1
22	D11	AD11	DIGIO5	GPI5/GPO5	MII_TXD0
23	D10	AD10	DIGIO4	GPI4/GPO4	MII_TXEN
24	VDDCR				
25	A1	ALELO	OE_EXT	-	MII_CLK25
26	A3	-	DIGIO11	GPI11/GPO11	MII_RXDV
27	A4	-	DIGIO12	GPI12/GPO12	MII_RXD0
28	CS		DIGIO13	GPI13/GPO13	MII_RXD1
29	A2	ALEHI	DIGIO10	GPI10/GPO10	LINKACTLED2/ MII_LINKPOL
30	WR/ENB		DIGIO14	GPI14/GPO14	MII_RXD2

TABLE 3-1: 64-QFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	Digital I/O Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name
31	RD/RD_WR		DIGIO15	GPI15/GPO15	MII_RXD3
32	VDDIO				
33	A0/D15	AD15	DIGIO9	GPI9/GPO9	MII_RXER
34	SYNC0/LATCH0				
35	D3	AD3	WD_TRIG	SIO3	
36	D6	AD6	DIGIO0	GPI0/GPO0	MII_RXCLK
37	VDDIO				
38	VDDCR				
39	D7	AD7	DIGIO1	GPI1/GPO1	MII_MDC
40	D8	AD8	DIGIO2	GPI2/GPO2	MII_MDIO
41	TESTMODE				
42	EESDA/TMS				
43	EESCL/TCK				
44	IRQ				
45	RUNLED/E2PSIZE				
46	LINKACTLED1/TDI/CHIP_MODE1				
47	VDDIO				
48	LINKACTLED0/TDO/CHIP_MODE0				
49	D4	AD4	DIGIO3	GPI3/GPO3	MII_LINK
50	D5	AD5	OUTVALID	SCS#	
51	VDD33TXRX1				
52	TXNA				
53	TXPA				
54	RXNA				
55	RXPA				
56	VDD12TX1				
57	RBIAS				
58	VDD33BIAS				
59	VDD12TX2				
60	RXPB				
61	RXNB				
62	TXPB				
63	TXNB				
64	VDD33TXRX2				
Exposed Pad	VSS				

3.2 64-TQFP-EP Pin Assignments

FIGURE 3-2: 64-TQFP-EP PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (**VSS**) on bottom of package must be connected to ground with a via field.

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Note: When an "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-2 details the 64-TQFP-EP package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

TABLE 3-2: 64-TQFP-EP PACKAGE PIN ASSIGNMENTS

Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	Digital I/O Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name
1	OSCI				
2	OSCO				
3	OSCVDD12				
4	OSCVSS				
5	VDD33				
6	VDDCR				
7	REG_EN				
8	FXLOSEN				
9	FXSDA/FXLOSA/FXSDENA				
10	FXSDB/FXLOSB/FXSDENB				
11	RST#				
12	D2	AD2	SOF	SIO2	
13	D1	AD1	EOF	SO/SIO1	
14	VDDIO				
15	D14	AD14	DIGIO8	GPI8/GPO8	MII_TXD3/ TX_SHIFT1
16	D13	AD13	DIGIO7	GPI7/GPO7	MII_TXD2/ TX_SHIFT0
17	D0	AD0	WD_STATE	SI/SIO0	
18	SYNC1/LATCH1				
19	D9	AD9	LATCH_IN	SCK	
20	VDDIO				
21	D12	AD12	DIGIO6	GPI6/GPO6	MII_TXD1
22	D11	AD11	DIGIO5	GPI5/GPO5	MII_TXD0
23	D10	AD10	DIGIO4	GPI4/GPO4	MII_TXEN
24	VDDCR				
25	A1	ALELO	OE_EXT	-	MII_CLK25
26	A3	-	DIGIO11	GPI11/GPO11	MII_RXDV
27	A4	-	DIGIO12	GPI12/GPO12	MII_RXD0
28	CS		DIGIO13	GPI13/GPO13	MII_RXD1
29	A2	ALEHI	DIGIO10	GPI10/GPO10	LINKACTLED2/ MII_LINKPOL
30	WR/ENB		DIGIO14	GPI14/GPO14	MII_RXD2

TABLE 3-2: 64-TQFP-EP PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	Digital I/O Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name
31	RD/RD_WR		DIGIO15	GPI15/GPO15	MII_RXD3
32	VDDIO				
33	A0/D15	AD15	DIGIO9	GPI9/GPO9	MII_RXER
34	SYNC0/LATCH0				
35	D3	AD3	WD_TRIG	SIO3	
36	D6	AD6	DIGIO0	GPI0/GPO0	MII_RXCLK
37	VDDIO				
38	VDDCR				
39	D7	AD7	DIGIO1	GPI1/GPO1	MII_MDC
40	D8	AD8	DIGIO2	GPI2/GPO2	MII_MDIO
41	TESTMODE				
42	EESDA/TMS				
43	EESCL/TCK				
44	IRQ				
45	RUNLED/E2PSIZE				
46	LINKACTLED1/TDI/CHIP_MODE1				
47	VDDIO				
48	LINKACTLED0/TDO/CHIP_MODE0				
49	D4	AD4	DIGIO3	GPI3/GPO3	MII_LINK
50	D5	AD5	OUTVALID	SCS#	
51	VDD33TXRX1				
52	TXNA				
53	TXPA				
54	RXNA				
55	RXPA				
56	VDD12TX1				
57	RBIAS				
58	VDD33BIAS				
59	VDD12TX2				
60	RXPB				
61	RXNB				
62	TXPB				
63	TXNB				
64	VDD33TXRX2				
Exposed Pad	VSS				

3.3 Pin Descriptions

This section contains descriptions of the various LAN9252 pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port A Pin Descriptions
- LAN Port B Pin Descriptions
- LAN Port A & B Power and Common Pin Descriptions
- EtherCAT MII Port & Configuration Strap Pin Descriptions
- Host Bus Pin Descriptions
- SPI/SQI Pin Descriptions
- EtherCAT Distributed Clock Pin Descriptions
- EtherCAT Digital I/O and GPIO Pin Descriptions
- EEPROM Pin Descriptions
- LED & Configuration Strap Pin Descriptions
- Miscellaneous Pin Descriptions
- JTAG Pin Descriptions
- Core and I/O Power Pin Descriptions

TABLE 3-3: LAN PORT A PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port A TP TX/RX Positive Channel 1	TXPA	AIO	Port A Twisted Pair Transmit/Receive Positive Channel 1. See Note 1
	Port A FX TX Positive		OLVPECL	Port A Fiber Transmit Positive.
1	Port A TP TX/RX Negative Channel 1	TXNA	AIO	Port A Twisted Pair Transmit/Receive Negative Channel 1. See Note 1.
	Port A FX TX Negative		OLVPECL	Port A Fiber Transmit Negative.
1	Port A TP TX/RX Positive Channel 2	RXPA	AIO	Port A Twisted Pair Transmit/Receive Positive Channel 2. See Note 1.
	Port A FX RX Positive		AI	Port A Fiber Receive Positive.
1	Port A TP TX/RX Negative Channel 2	RXNA	AIO	Port A Twisted Pair Transmit/Receive Negative Channel 2. See Note 1.
	Port A FX RX Negative		AI	Port A Fiber Receive Negative.

TABLE 3-3: LAN PORT A PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port A FX Signal Detect (SD)	**FXSDA**	ILVPECL	Port A Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
	Port A FX Loss Of Signal (LOS)	**FXLOSA**	IS (PU)	Port A Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_1), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
	Port A FX-SD Enable Strap	**FXSDENA**	AI	Port A FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD. When FX-LOS mode is selected, the input buffer is disabled. See Note 2.

Note 1: In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Note 2: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 51 for more information.

Note: Port A is connected to the EtherCAT port 0 or 2.

TABLE 3-4: LAN PORT B PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port B TP TX/RX Positive Channel 1	**TXPB**	AIO	Port B Twisted Pair Transmit/Receive Positive Channel 1. See Note 3
	Port B FX TX Positive		OLVPECL	Port B Fiber Transmit Positive.
1	Port B TP TX/RX Negative Channel 1	**TXNB**	AIO	Port B Twisted Pair Transmit/Receive Negative Channel 1. See Note 3.
	Port B FX TX Negative		OLVPECL	Port B Fiber Transmit Negative.

TABLE 3-4: LAN PORT B PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port BTP TX/RX Positive Channel 2	**RXPB**	AIO	Port B Twisted Pair Transmit/Receive Positive Channel 2. See Note 3.
	Port B FX RX Positive		AI	Port B Fiber Receive Positive.
1	Port B TP TX/RX Negative Channel 2	**RXNB**	AIO	Port B Twisted Pair Transmit/Receive Negative Channel 2. See Note 3.
	Port B FX RX Negative		AI	Port B Fiber Receive Negative.
1	Port B FX Signal Detect (SD)	**FXSDB**	ILVPECL	Port B Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
	Port B FX Loss Of Signal (LOS)	**FXLOSB**	IS (PU)	Port B Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_2), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
	Port B FX-SD Enable Strap	**FXSDENB**	AI	Port B FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD. When FX-LOS mode is selected, the input buffer is disabled. See Note 4.

Note 3: In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Note 4: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 51 for more information.

Note: Port B is connected to EtherCAT port 1.

TABLE 3-5: LAN PORT A & B POWER AND COMMON PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Bias Reference	**RBIAS**	AI	Used for internal bias circuits. Connect to an external 12.1 kΩ, 1% resistor to ground. Refer to the device reference schematic for connection information. **Note:** The nominal voltage is 1.2 V and the resistor will dissipate approximately 1 mW of power.
1	Port A and B FX-LOS Enable Strap	**FXLOSEN**	AI	Port A and B FX-LOS Enable. This 3 level strap input selects between FX-LOS and FX-SD / copper twisted pair mode. A level below 1 V (typ.) selects FX-SD / copper twisted pair for ports A and B, further determined by FXSDENA and FXSDENB. A level of 1.5 V selects FX-LOS for port A and FX-SD / copper twisted pair for port B, further determined by FXSDENB. A level above 2 V (typ.) selects FX-LOS for ports A and B.
1	+3.3 V Port A Analog Power Supply	**VDD33TXRX1**	P	See Note 5.
1	+3.3 V Port B Analog Power Supply	**VDD33TXRX2**	P	See Note 5.
1	+3.3 V Master Bias Power Supply	**VDD33BIAS**	P	See Note 5.
1	Port A Transmitter +1.2 V Power Supply	**VDD12TX1**	P	This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX2** pin for proper operation. See Note 5.
1	Port B Transmitter +1.2 V Power Supply	**VDD12TX2**	P	This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX1** pin for proper operation. See Note 5.

Note 5: Refer to Section 4.0, "Power Connections," on page 29, the device reference schematics, and the device LANCheck schematic checklist for additional connection information.

TABLE 3-6: ETHERCAT MII PORT & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	25 MHz Clock	**MII_CLK25**	VO12 Note 6	This pin is a free-running 25 MHz clock that can be used as the clock input to the PHY.
4	Receive Data MII Port	**MII_RXD[3:0]**	VIS (PD)	These pins are the receive data from the external PHY.
1	Receive Data Valid MII Port	**MII_RXDV**	VIS (PD)	This pin is the receive data valid signal from the external PHY.
1	Receive Error MII Port	**MII_RXER**	VIS (PD)	This pin is the receive error signal from the external PHY.
1	Receive Clock MII Port	**MII_RXCLK**	VIS (PD)	This pin is the receive clock from the external PHY.
4	Transmit Data MII Port	**MII_TXD[3:0]**	VO8	These pins are the transmit data to the external PHY.
	MII Transmit Timing Shift Configuration Strap	**TX_SHIFT[1:0]**	VIS (PU) Note 7	These straps configure the value of the external MII Bus TX timing shift hard-strap. See Note 8. **TX_SHIFT[1]** is on **MII_TXD[3]** and **TX_SHIFT[0]** is on **MII_TXD[2]**.
1	Transmit Data Enable MII Port	**MII_TXEN**	VO8	This pin is the transmit data enable signal to the external PHY.
1	Link Status MII Port	**MII_LINK**	VIS	This pin is the provided by the PHY to indicate that a 100 Mbit/s Full Duplex link is established. The polarity is configurable via the link_pol_strap_mii strap.
1	SMI Clock	**MII_MDC**	VO8	This pin is the serial management clock to the external PHY.
1	SMI Data	**MII_MDIO**	VIS/VO8	This pin is the serial management interface data input/output to the external PHY. **Note:** An external pull-up is required to ensure that the non-driven state of the MDIO signal is a logic one.

Note 6: A series terminating resistor is recommended for the best PCB signal integrity.

Note 7: An external supplemental pull-up may be needed, depending upon the input current loading of the external MAC/PHY device.

Note 8: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 51 for more information.

TABLE 3-7: HOST BUS PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Read	**RD**	VIS	This pin is the host bus read strobe. Normally active low, the polarity can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI Modes).
	Read or Write	**RD_WR**	VIS	This pin is the host bus direction control. Used in conjunction with the ENB pin, it indicates a read or write operation. The normal polarity is read when 1, write when 0 (R/nW) but can be changed via the HBI Read, Read/Write Polarity bit of the PDI Configuration Register (HBI Modes).
1	Write	**WR**	VIS	This pin is the host bus write strobe. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI Modes).
	Enable	**ENB**	VIS	This pin is the host bus data enable strobe. Used in conjunction with the RD_WR pin it indicates the data phase of the operation. Normally active low, the polarity can be changed via the HBI Write, Enable Polarity bit of the PDI Configuration Register (HBI Modes).
1	Chip Select	**CS**	VIS	This pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via the HBI Chip Select Polarity bit of the PDI Configuration Register (HBI Modes).
5	Address	**A[4:0]**	VIS	These pins provide the address for non-multiplexed address mode. In 16-bit data mode, bit 0 is not used.

TABLE 3-7: HOST BUS PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
16	Data	**D[15:0]**	VIS/VO8	These pins are the host bus data bus for non-multiplexed address mode. In 8-bit data mode, bits 15-8 are not used and their input and output drivers are disabled.
	Address & Data	**AD[15:0]**	VIS/VO8	These pins are the host bus address / data bus for multiplexed address mode. Bits 15-8 provide the upper byte of address for single phase multiplexed address mode. Bits 7-0 provide the lower byte of address for single phase multiplexed address mode and both bytes of address for dual phase multiplexed address mode. In 8-bit data dual phase multiplexed address mode, bits 15-8 are not used and their input and output drivers are disabled.
1	Address Latch Enable High	**ALEHI**	VIS	This pin indicates the address phase for multiplexed address modes. It is used to load the higher address byte in dual phase multiplexed address mode. Normally active low (address saved on rising edge), the polarity can be changed via the HBI ALE Polarity bit of the PDI Configuration Register (HBI Modes).
1	Address Latch Enable Low	**ALELO**	VIS	This pin indicates the address phase for multiplexed address modes. It is used to load both address bytes in single phase multiplexed address mode and the lower address byte in dual phase multiplexed address mode. Normally active low (address saved on rising edge), the polarity can be changed via the HBI ALE Polarity bit of the PDI Configuration Register (HBI Modes).

TABLE 3-8: SPI/SQI PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	SPI/SQI Slave Chip Select	**SCS#**	VIS (PU)	This pin is the SPI/SQI slave chip select input. When low, the SPI/SQI slave is selected for SPI/SQI transfers. When high, the SPI/SQI serial data output(s) is(are) 3-stated.
1	SPI/SQI Slave Serial Clock	**SCK**	VIS (PU)	This pin is the SPI/SQI slave serial clock input.
4	SPI/SQI Slave Serial Data Input/Output	**SIO[3:0]**	VIS/VO8 (PU)	These pins are the SPI/SQI slave data input and output for multiple bit I/O.
	SPI Slave Serial Data Input	**SI**	VIS (PU)	This pin is the SPI slave serial data input. **SI** is shared with the **SIO0** pin.
	SPI Slave Serial Data Output	**SO**	VO8 (PU) Note 9	This pin is the SPI slave serial data output. **SO** is shared with the **SIO1** pin.

Note 9: Although this pin is an output for SPI instructions, it includes a pull-up since it is also SIO bit 1.

TABLE 3-9: ETHERCAT DISTRIBUTED CLOCK PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
2	Sync	**SYNC[1]** **SYNC[0]**	VO8	These pins are the Distributed Clock Sync (OUT) or Latch (IN) signals. The direction is bitwise configurable. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.
	Latch	**LATCH[1]** **LATCH[0]**	VIS	

TABLE 3-10: ETHERCAT DIGITAL I/O AND GPIO PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
16	General Purpose Input	**GPI[15:0]**	VIS	These pins are the general purpose inputs and are directly mapped into the **General Purpose Inputs Register**. Consistency of the general purpose inputs is not provided.
	General Purpose Output	**GPO[15:0]**	VO8	These pins are the general purpose outputs and reflect the values of the **General Purpose Outputs Register** without watchdog protection. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.
16	Digital I/O	**DIGIO[15:0]**	VIS/VO8	These pins are the input/output or bidirectional data. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.
1	Output Valid	**OUTVALID**	VO8	This pin indicates that the outputs are valid and can be captured into external registers. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.

TABLE 3-10: ETHERCAT DIGITAL I/O AND GPIO PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Latch In	**LATCH_IN**	VIS	This pin is the external data latch signal. The input data is sampled each time a rising edge of **LATCH_IN** is recognized.
1	Watchdog Trigger	**WD_TRIG**	VO8	This pin is the SyncManager Watchdog Trigger output. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
1	Watchdog State	**WD_STATE**	VO8	This pin is the SyncManager Watchdog State output. A 0 indicates the watchdog has expired. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
1	Start of Frame	**SOF**	VO8	This pin is the Start of Frame output and indicates the start of an Ethernet/EtherCAT frame. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
1	End of Frame	**EOF**	VO8	This pin is the End of Frame output and indicates the end of an Ethernet/EtherCAT frame. **Note:** The signal is not driven (high impedance) until the EEPROM is loaded.
1	Output Enable	**OE_EXT**	VIS	This pin is the Output Enable input. When low, it clears the output data.

TABLE 3-11: EEPROM PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	EEPROM I^2C Serial Data Input/Output	**EESDA**	VIS/VOD8	When the device is accessing an external EEPROM this pin is the I^2C serial data input/open-drain output. **Note:** This pin must be pulled-up by an external resistor at all times.
1	EEPROM I^2C Serial Clock	**EESCL**	VOD8	When the device is accessing an external EEPROM this pin is the I^2C clock open-drain output. **Note:** This pin must be pulled-up by an external resistor at all times.