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SMSC® SUCCESS BY DESIGN

LAN9303/LAN9303i

Small Form Factor Three Port 10/100 Managed Ethernet Switch with Single MII/RMII/Turbo MII

PRODUCT FEATURES

Datasheet

Highlights

- Up to 200Mbps via Turbo MII Interface
- High performance, full featured 3 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Serial management via I^2C or SMI
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port PHY

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 512 entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1D spanning tree protocol support
  - 4 separate transmit queues available per port
  - Fixed or weighted egress priority servicing
  - QoS/CoS Packet prioritization
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable Traffic Class map based on input priority on per port basis
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress with coloring and random early discard, per port / priority
    - Programmable rate limiting at the egress with leaky bucket algorithm, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable broadcast storm protection with global % control and enable per port
  - Programmable buffer usage limits
  - Dynamic queues on internal memory
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any port or port pair
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - Port 0 - MII MAC, MII PHY, RMII PHY modes
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - 200Mbps Turbo MII (PHY or MAC mode)
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Full LED support per port
  - Auto-negotiation
  - Automatic polarity correction
  - Automatic MDI/MDI-X
  - Loop-back mode
- Serial Management
  - I^2C (slave) access to all internal registers
  - MIIM (MDIO) access to PHY related registers
  - SMI (extended MIIM) access to all internal registers
- Other Features
  - General Purpose Timer
  - I^2C Serial EEPROM interface
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- ESD Protection Levels
  - ±8kV HBM without External Protection Devices
  - ±8kV contact mode (IEC61000-4-2)
  - ±15kV air-gap discharge mode (IEC61000-4-2)
- Latch-up exceeds ±150mA per EIA/JESD 78
- 56-pin QFN (8x8 mm) Lead-Free RoHS Compliant Package
- Available in Commercial & Industrial Temp. Ranges

Order Number(s):

LAN9303-ABZJ for 56-Pin, QFN Lead-Free RoHS Compliant Package (0 to 70°C Temp Range)

LAN9303i-ABZJ for 56-Pin, QFN Lead-Free RoHS Compliant Package (-40 to 85°C Temp Range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Preface

1.1 General Terms

10BASE-T	10BASE-T (10Mbps Ethernet, IEEE 802.3)
100BASE-TX	100BASE-TX (100Mbps Fast Ethernet, IEEE 802.3u)
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8-bits
CSMA/CD	Carrier Sense Multiple Access / Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32-bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
MDI	Medium Dependant Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface

MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16-bits

Chapter 2 Introduction

2.1 General Description

The LAN9303/LAN9303i is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9303/LAN9303i combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and serial management. The LAN9303/LAN9303i complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9303/LAN9303i provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9303/LAN9303i provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the MII/Turbo MII interface. In PHY mode, the device can be connected to an external MAC via the MII/RMII/Turbo MII interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The integrated I^2C and SMI slave controllers allow for full serial management of the device via the integrated I^2C or MII interface, respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the device into various designs. It is this flexibility which allows the device to operate in 2 different modes and under various management conditions. In both MAC and PHY modes, the device can be SMI managed or I^2C managed. This flexibility in management makes the LAN9303/LAN9303i a candidate for virtually all switch applications.

The LAN9303/LAN9303i contains an I^2C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset. The I^2C management slave and master EEPROM controller share common pins.

In addition to the primary functionality described above, the LAN9303/LAN9303i provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, and 6-bit configurable GPIO/LED interface.

The LAN9303/LAN9303i's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment.

2.2 Block Diagram

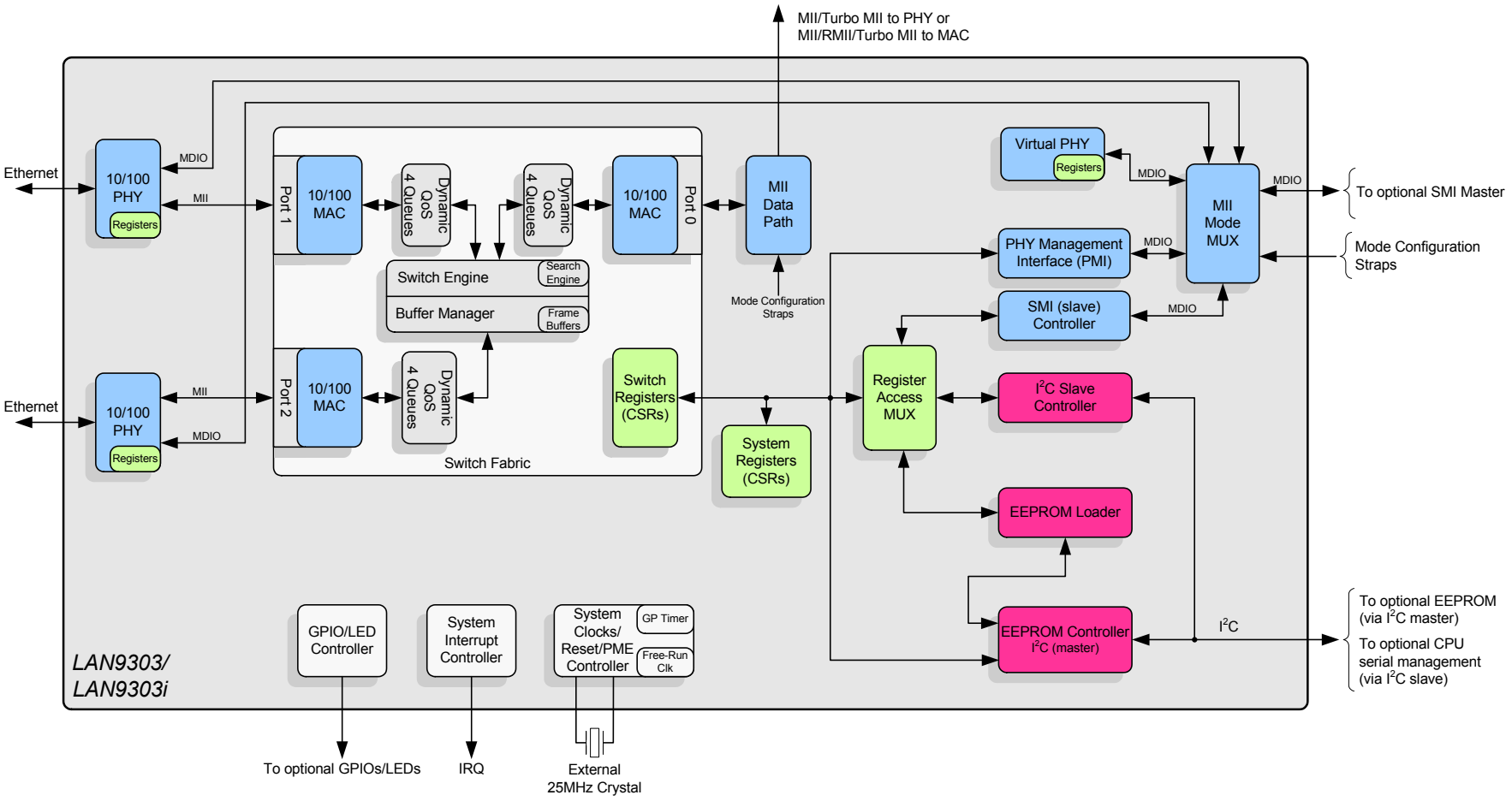


Figure 2.1 Internal Block Diagram

2.2.1 System Clocks/Reset/PME Controller

A clock module generates all the system clocks required by the device. This module interfaces directly with the external 25MHz crystal/oscillator to generate the required clock divisions for each internal module. A 16-bit general purpose timer and 32-bit free-running clock are provided by this module for general purpose use. The Port 1 & 2 PHYs provide general power-down and energy detect power-down modes, which allow a reduction in PHY power consumption.

The device reset events are categorized as chip-level resets, multi-module resets, and single-module resets. These reset events are summarized below:

- **Chip Level Resets**
  —Power-On Reset (Entire chip reset)
  —nRST Pin Reset (Entire chip reset)
- **Multi-Module Reset**
  —Digital Reset (All sub-modules except Ethernet PHYs)
- **Single-Module Resets**
  —Port 2 PHY Reset
  —Port 1 PHY Reset
  —Virtual PHY Reset

2.2.2 System Interrupt Controller

The device provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. Top level interrupt registers aggregate and control all interrupts from the various sub-modules. The device is capable of generating interrupt events from the following:

- **Switch Fabric**
- **Ethernet PHYs**
- **GPIOs**
- **General Purpose Timer**
- **Software (general purpose)**

A dedicated programmable IRQ interrupt output pin is provided for external indication of any device interrupts. The IRQ buffer type, polarity, and de-assertion interval are register configurable.

2.2.3 Switch Fabric

The Switch Fabric consists of the following major function blocks:

- **10/100 MACs**
  There is one 10/100 Ethernet MAC per Switch Fabric port, which provides basic 10/100 Ethernet functionality, including transmission deferral, collision back-off/retry, TX/RX FCS checking/generation, TX/RX pause flow control, and transmit back pressure. The 10/100 MACs act as an interface between the Switch Engine and the 10/100 PHYs (for ports 1 and 2). The port 0 10/100 MAC interfaces the Switch Engine to the external MAC/PHY (see Section 2.3, "Modes of Operation"). Each 10/100 MAC includes RX and TX FIFOs and per port statistic counters.
- **Switch Engine**
  This block, consisting of a 3 port VLAN layer 2 switching engine, provides the control for all forwarding/filtering rules and supports untagged, VLAN tagged, and priority tagged frames. The Switch Engine provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, and port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. A 512 entry forwarding table provides ample room for MAC address forwarding tables.

- **Buffer Manager**
  This block controls the free buffer space, multi-level transmit queues, transmission scheduling, and packet dropping of the Switch Fabric. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block.
- **Switch CSRs**
  This block contains all switch related control and status registers, and allows all aspects of the Switch Fabric to be managed. These registers are indirectly accessible via the system control and status registers.

2.2.4 Ethernet PHYs

The device contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the Switch Fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of an external MAC to port 0 of the Switch Fabric as if it was connected to a single port PHY. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set.

2.2.5 PHY Management Interface (PMI)

The PHY Management Interface (PMI) is used to serially access the internal PHYs as well as the external PHY on the MII pins (in MAC mode only, see Section 2.3, "Modes of Operation"). The PMI implements the IEEE 802.3 management protocol, providing read/write commands for PHY configuration.

2.2.6 I^2C Slave Controller

This module provides an I^2C slave interface which can be used for CPU serial management of the device. The I^2C slave controller implements the low level I^2C slave serial interface (start and stop condition detection, data bit transmission/reception, and acknowledge generation/reception), handles the slave command protocol, and performs system register reads and writes. The I^2C slave controller conforms to the NXP *I^2C-Bus Specification*. A list of management modes and configurations settings for these modes is discussed in Section 2.3, "Modes of Operation"

2.2.7 SMI Slave Controller

This module provides a SMI slave interface which can be used for CPU management of the device via the MII pins, and allows CPU access to all system CSRs. SMI uses the same pins and protocol of the IEEE MII management function, and differs only in that SMI provides access to all internal registers by using a non-standard extended addressing map. The SMI protocol co-exists with the MII management protocol by using the upper half of the PHY address space (16 through 31). A list of management modes and configurations settings for these modes is discussed in Section 2.3, "Modes of Operation"

2.2.8 EEPROM Controller/Loader

The EEPROM Controller is an I^2C master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple sizes of external EEPROMs are supported along with various EEPROM commands, allowing for the efficient storage and retrieval of static data. The I^2C interface conforms to the NXP *I^2C-Bus Specification*.

The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs. The EEPROM Loader provides the automatic loading of configuration settings from the

EEPROM into the device at reset, allowing the device to operate unmanaged. The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset, or upon the issuance of a EEPROM RELOAD command.

2.2.9 GPIO/LED Controller

Six configurable general-purpose input/output pins are provided which are controlled via this module. These pins can be individually configured via the GPIO/LED CSRs to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. The GPIO pins can be alternatively configured as LED outputs to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

2.3 Modes of Operation

The LAN9303/LAN9303i is designed to integrate into various embedded environments. To accomplish compatibility with a wide range of applications, the LAN9303/LAN9303i ports can operate in the following modes:

- Port 0 - Independently configured for MII MAC, MII PHY, RMII PHY modes
- Port 1 - Internal PHY mode
- Port 2 - Internal PHY mode

The mode of the device is determined by the P0_MODE[2:0] (Port 0) pin straps.

The device can also be placed into the following management modes:

- SMI managed
- I^2C managed

The management mode is determined by the MNGT1_LED4P and MNGT0_LED3P pin straps. These modes are detailed in the following sections. Figure 2.4 displays a typical system configuration for each Port 0 mode and management type supported by the device. Refer to Chapter 9, "MII Data Interface," on page 123 for additional information on the usage of MII signals in each supported mode.

2.3.1 Internal PHY Mode

Internal PHY mode (Port 1 and Port 2) utilizes the internal PHY for the network connection. The Switch Engine MAC's MII port is connected internally to the internal PHY in this mode. Internal PHY mode can operate at 10Mbps or 100Mbps.

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C interface. Once operational, if managed, the CPU can use the I^2C interface to read or write the EEPROM.

2.3.2 MAC Mode

MAC mode utilizes an external PHY, which is connected to the Port 0 MII pins, to provide an Ethernet network connection. In this mode, the port acts as a MAC, providing a communication path between the Switch Fabric and the external PHY. MAC mode can operate at 10, 100, or 200Mbps (Turbo mode). In MAC mode, the device may be SMI managed or I^2C managed as detailed in Section 2.3.4, "Management Modes".

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C interface. Once operational, if managed, the CPU can use the I^2C interface to read or write the EEPROM.

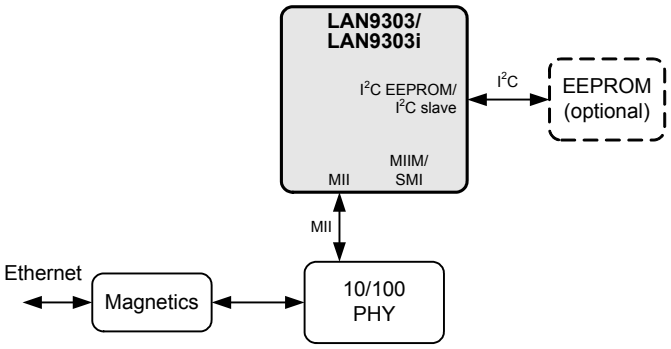


Figure 2.2 MII MAC Mode

2.3.3 PHY Mode

PHY mode utilizes an external MAC to provide a network path for the CPU. PHY mode supports MII and RMII interfaces. The external MII/RMII pins must be connected to an external MAC, providing a communication path to the Switch Fabric. MII PHY mode can operate at 10, 100, or 200Mbps (Turbo mode). RMII PHY mode can operate at 10 or 100Mbps. In PHY mode, the device may be SMI managed or I^2C managed as detailed in Section 2.3.4, "Management Modes".

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C interface. Once operational, if managed, the CPU can use the I^2C interface to read or write the EEPROM.

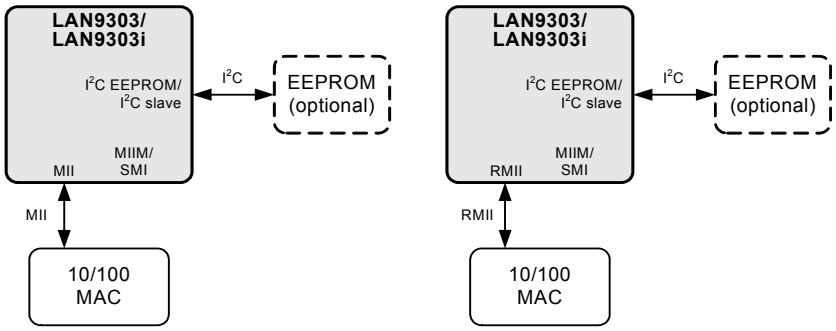


Figure 2.3 MII/RMII PHY Mode

2.3.4 Management Modes

Various modes of management are provided in both MAC and PHY modes of operation. Two separate interfaces may be used for management: the I^2C interface or the SMI/MIIM (Media Independent Interface Management) slave interface.

The I^2C interface runs as an I^2C slave. The slave mode is used as a register access path for an external CPU. The I^2C slave and I^2C master EEPROM interface are shared interfaces.

The SMI/MIIM interface runs as either an SMI/MIIM slave or MIIM master. The master mode is used to access an external PHYs registers under CPU control (assuming the CPU is using I^2C). The slave mode is used for register access by the CPU or external MAC and provides access to either the internal Port 1&2 PHY registers or to all non-PHY registers (using addresses 16-31 and a non-standard extended address map). MIIM and SMI use the same pins and protocol and differ only in that SMI provides access to all internal registers while MIIM provides access to only the Port 1&2 PHY registers. A special mode provides access to the Virtual PHY, which mimics the register operation of a single port standalone PHY. This is used for software compatibility in managed operation.

The selection of management modes is determined at startup via the P0_MODE[2:0], MNGT1_LED4P, and MNGT0_LED3P straps as detailed in Table 2.1. System configuration diagrams for each mode are provided in Figure 2.4.

Table 2.1 Device Modes

MODE	I^2C INTERFACE (MASTER/SLAVE)	SMI/MIIM INTERFACE	P0_MODE[2:0] STRAP VALUE	MNGT1_LED4P, MNGT0_LED3PSTRAP VALUE
MAC SMI	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	SMI/MIIM slave, used for CPU access to internal PHYs and non-PHY registers	000	01
MAC I^2C	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM I^2C slave used for management	MIIM master, used for CPU access to external PHY registers	000	10
PHY SMI	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	SMI/MIIM slave, used for CPU access to internal PHYs, Virtual PHY, and non-PHY registers	001, 010, 011, 100, 101, or 110	01
PHY I^2C	I^2C master used to load initial configuration from EEPROM and for CPU R/W access to EEPROM I^2C slave used for management	Virtual MIIM slave, used for external MAC access to Virtual PHY registers	001, 010, 011, 100, 101, or 110	10

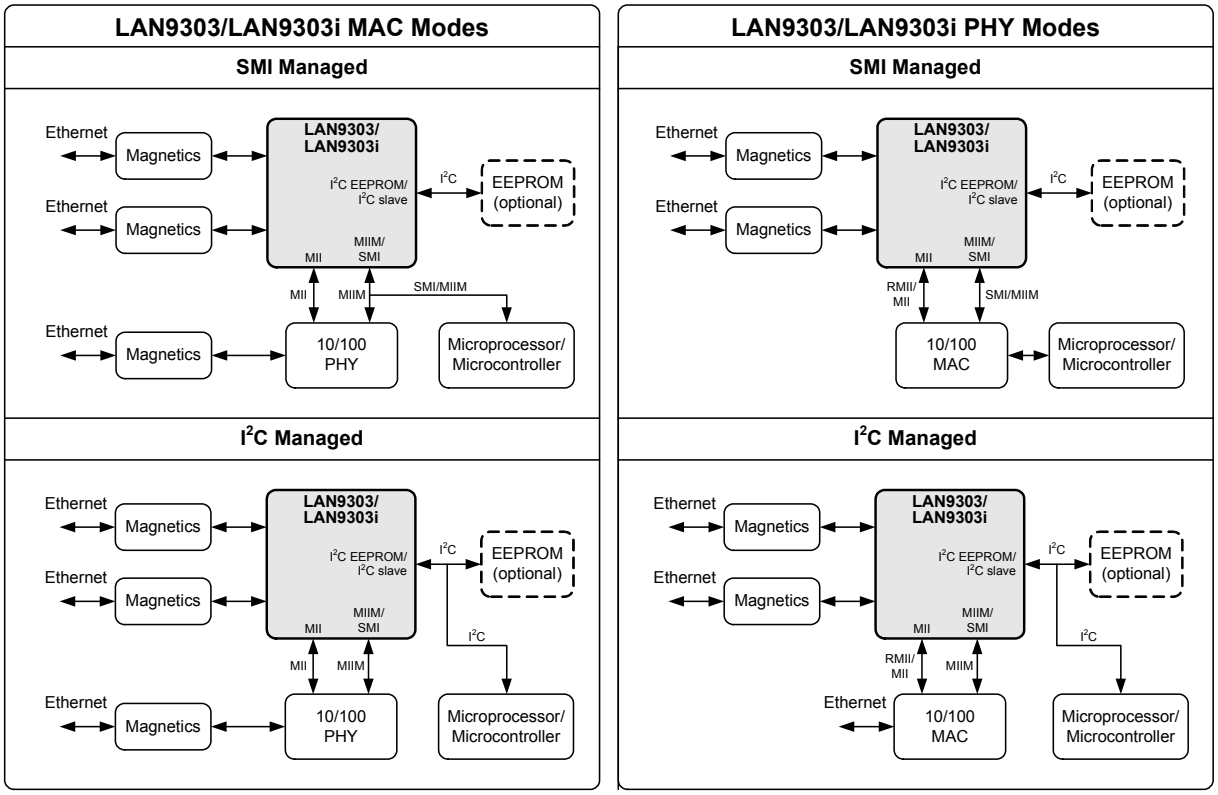
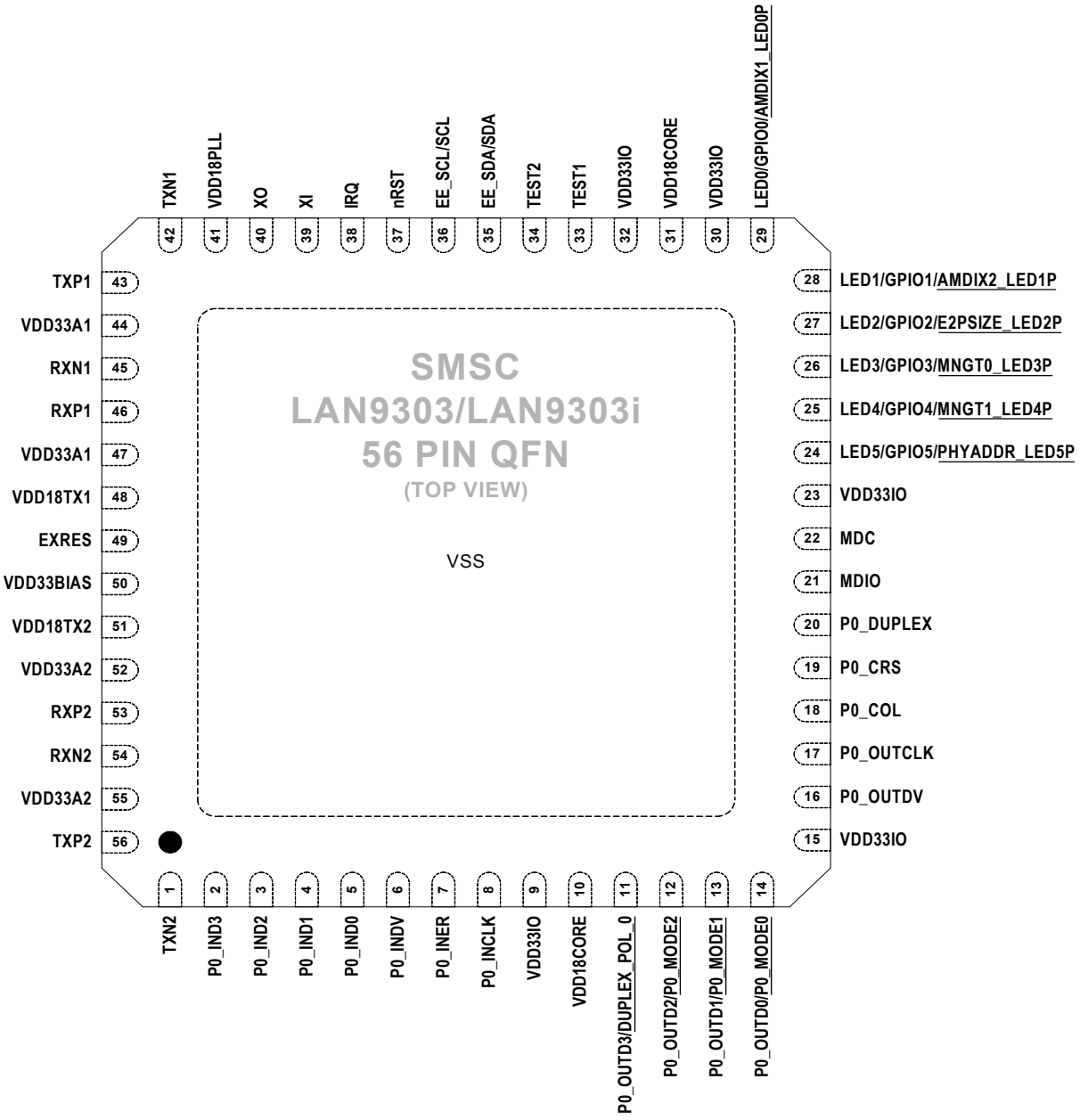


Figure 2.4 Port 0 MAC/PHY Management Modes

Chapter 3 Pin Description and Configuration

3.1 Pin Diagram

3.1.1 56-QFN Pin Diagram



NOTE: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa

NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Figure 3.1 Pin Assignments (TOP VIEW)

3.2 Pin Descriptions

This section contains the descriptions of the device pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port 1 Pins
- LAN Port 2 Pins
- LAN Port 1 & 2 Power and Common Pins
- Port 0 MII/RMII Pins
- GPIO/LED/Configuration Straps
- Serial Management/EEPROM Pins
- Miscellaneous Pins
- PLL Pins
- Core and I/O Power and Ground Pins

Note: A list of buffer type definitions is provided in Section 3.3, "Buffer Types," on page 41.

Note: Please refer to the LAN9303/LAN9303i Reference Schematic and LANCheck Schematic Checklist on the SMSC website for additional connection information.

Table 3.1 LAN Port 1 Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 Ethernet TX Negative	TXN1	AIO	Negative output of Port 1 Ethernet transmitter. See Note 3.1.
1	Port 1 Ethernet TX Positive	TXP1	AIO	Positive output of Port 1 Ethernet transmitter. See Note 3.1.
1	Port 1 Ethernet RX Negative	RXN1	AIO	Negative input of Port 1 Ethernet receiver. See Note 3.1.
1	Port 1 Ethernet RX Positive	RXP1	AIO	Positive input of Port 1 Ethernet receiver. See Note 3.1.

Note 3.1 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Table 3.2 LAN Port 2 Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 2 Ethernet TX Negative	TXN2	AIO	Negative output of Port 2 Ethernet transmitter. See Note 3.2.
1	Port 2 Ethernet TX Positive	TXP2	AIO	Positive output of Port 2 Ethernet transmitter. See Note 3.2.
1	Port 2 Ethernet RX Negative	RXN2	AIO	Negative input of Port 2 Ethernet receiver. See Note 3.2.
1	Port 2 Ethernet RX Positive	RXP2	AIO	Positive input of Port 2 Ethernet receiver. See Note 3.2.

Note 3.2 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Table 3.3 LAN Port 1 & 2 Power and Common Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Bias Reference	EXRES	AI	Used for internal bias circuits. Connect to an external 12.4K ohm, 1% resistor to ground.
2	+3.3V Port 1 Analog Power Supply	VDD33A1	P	See Note 3.3.
2	+3.3V Port 2 Analog Power Supply	VDD33A2	P	See Note 3.3.
1	+3.3V Master Bias Power Supply	VDD33BIAS	P	See Note 3.3.
1	Port 2 Transmitter +1.8V Power Supply	VDD18TX2	P	This pin is supplied from the internal PHY voltage regulator. This pin must be tied to the VDD18TX1 pin for proper operation. See Note 3.3.
1	Port 1 Transmitter +1.8V Power Supply	VDD18TX1	P	This pin must be connected directly to the VDD18TX2 pin for proper operation. See Note 3.3.

Note 3.3 Please refer to the LAN9303/LAN9303i Reference Schematic and LANCheck Schematic Checklist on the SMSC website for additional connection information.

Table 3.4 Port 0 MII/RMII Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 0 MII Input Data 3	P0_IND3	IS (PD)	**MII MAC Mode:** This pin is the receive data 3 bit from the external PHY to the switch.
			IS (PD)	**MII PHY Mode:** This pin is the transmit data 3 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
			-	**RMII PHY Mode:** This pin is not used.