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LAN9311/LAN9311i

Two Port 10/100 Managed Ethernet Switch with 16-Bit Non-PCI CPU Interface

Highlights

- High performance and full featured 2 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Easily interfaces to most 16-bit embedded CPU's
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port MAC/PHY
- Integrated IEEE 1588 Hardware Time Stamp Unit

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 1K entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1d spanning tree protocol support
  - QoS/CoS Packet prioritization
    - 4 dynamic QoS queues per port
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable class of service map based on input priority
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress/egress ports with random early discard, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any ports or port pairs
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Auto-negotiation
  - Automatic MDI/MDI-X
  - Loop-back mode
- High-performance host bus interface
  - Provides in-band network communication path
  - Access to management registers
  - Simple, SRAM-like interface
  - 16-bit data bus
  - Big, little, and mixed endian support
  - Large TX and RX FIFO's for high latency applications
  - Programmable water marks and threshold levels
  - Host interrupt support
- IEEE 1588 Hardware Time Stamp Unit
  - Global 64-bit tunable clock
  - Master or slave mode per port
  - Time stamp on TX or RX of Sync and Delay_req packets per port, Timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive Power Management Features
  - Wake on LAN
  - Wake on link status change (energy detect)
  - Magic packet wakeup
  - Wakeup indicator event signal
- Other Features
  - General Purpose Timer
  - Serial EEPROM interface (I^2C master or Microwire™ master) for non-managed configuration
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- Available in Commercial & Industrial Temp. Ranges

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1.0 PREFACE

1.1 General Terms

100BT	100BASE-T (100Mbps Fast Ethernet, IEEE 802.3u)
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8-bits
CSMA/CD	Carrier Sense Multiple Access / Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32-bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
HBI	Host Bus Interface. The physical bus connecting the LAN9311/LAN9311i to the host. Also referred to as the Host Bus.
HBIC	Host Bus Interface Controller. The hardware module that interfaces theLAN9311/LAN9311i to the HBI.
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the LAN9311/LAN9311i from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
MDI	Medium Dependant Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier

Outbound	Refers to data output from the LAN9311/LAN9311i to the host
PIO cycle	Program I/O cycle. An SRAM-like read or write cycle on the HBI.
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16-bits

1.2 Buffer Types

Table 1-1 describes the pin buffer type notation used in Section 3.0, "Pin Description and Configuration," on page 13 and throughout this document.

TABLE 1-1: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered Input
O8	Output with 8mA sink and 8mA source
OD8	Open-drain output with 8mA sink
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the LAN9311/LAN9311i. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the LAN9311/LAN9311i. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

1.3 Register Nomenclature

Table 1-2 describes the register bit attribute notation used throughout this document.

TABLE 1-2: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Some examples of this are shown below:

- **R/W:** Can be written. Will return current setting on a read.
- **R/WAC:** Will return current setting on a read. Writing anything clears the bit.

2.0 INTRODUCTION

2.1 General Description

The LAN9311/LAN9311i is a full featured, 2 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9311/LAN9311i combines all the functions of a 10/100 switch system, including the switch fabric, packet buffers, buffer manager, media access controllers (MACs), PHY transceivers, and host bus interface. The LAN9311/LAN9311i complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the LAN9311/LAN9311i is the high performance, high efficiency 3 port Ethernet switch fabric. The switch fabric contains a 3 port VLAN layer 2 switch engine that supports untagged, VLAN tagged, and priority tagged frames. The switch fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 1K entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the buffer manager block within the switch fabric. All aspects of the switch fabric are managed via the switch fabric configuration and status registers, which are indirectly accessible via the memory mapped system control and status registers.

The LAN9311/LAN9311i provides 2 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9311/LAN9311i provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the Host MAC are used to connect the LAN9311/LAN9311i switch fabric to the host bus interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. Automatic 32-bit CRC generation/checking and automatic payload padding are supported to further reduce CPU overhead. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while deceasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the LAN9311/LAN9311i.

The integrated Host Bus Interface (HBI) easily interfaces to most 16-bit embedded CPU's via a simple SRAM like interface, enabling switch fabric access via the internal Host MAC and allowing full control over the LAN9311/LAN9311i via memory mapped system control and status registers. The HBI supports 16-bit operation with big, little, and mixed endian operations. Four separate FIFO mechanisms (TX/RX Data FIFO's, TX/RX Status FIFO's) interface the HBI to the Host MAC and facilitate the transferring of packet data and status information between the host CPU and the switch fabric. The LAN9311/LAN9311i also provides power management features which allow for wake on LAN, wake on link status change (energy detect), and magic packet wakeup detection. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

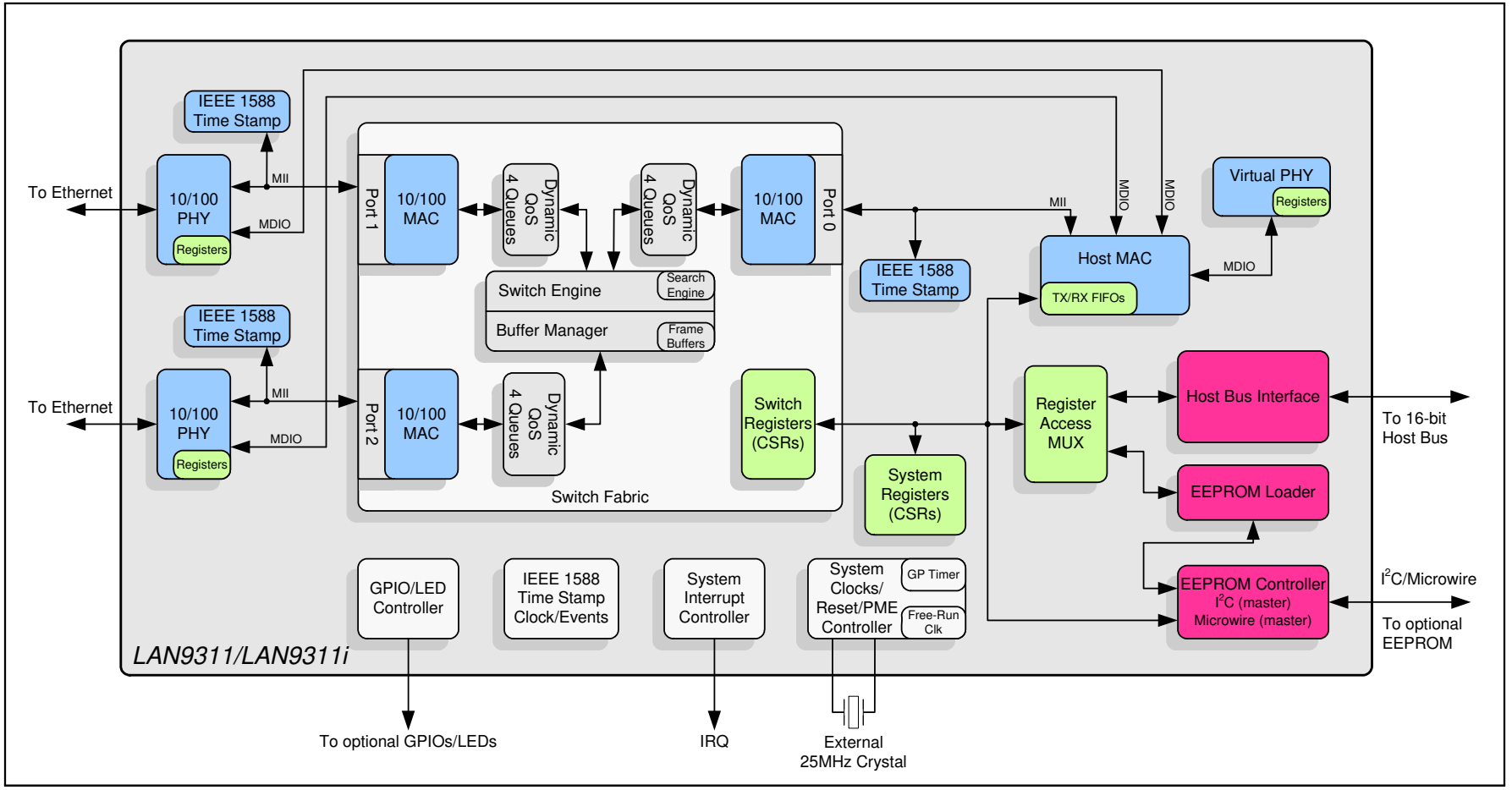
The LAN9311/LAN9311i contains an I^2C/Microwire master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the LAN9311/LAN9311i at reset.

In addition to the primary functionality described above, the LAN9311/LAN9311i provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a 12-bit configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and select GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9311/LAN9311i's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment.

2.2 Block Diagram

FIGURE 2-1: INTERNAL LAN9311/LAN9311I BLOCK DIAGRAM



2.2.1 SYSTEM CLOCKS/RESET/PME CONTROLLER

A clock module contained within the LAN9311/LAN9311i generates all the system clocks required by the device. This module interfaces directly with the external 25MHz crystal/oscillator to generate the required clock divisions for each internal module, with the exception of the 1588 clocks, which are generated in the 1588 Time Stamp Clock/Events module. A 16-bit general purpose timer and 32-bit free-running clock are provided by this module for general purpose use.

The LAN9311/LAN9311i reset events are categorized as chip-level resets, multi-module resets, and single-module resets.

A chip-level reset is initiated by assertion of any of the following input events:

- Power-On Reset
- nRST Pin Reset

A multi-module reset is initiated by assertion of the following:

- **Digital Reset** - DIGITAL_RST (bit 0) in the Reset Control Register (RESET_CTL)
  - Resets all LAN9311/LAN9311i sub-modules except the Ethernet PHYs (Port 1 PHY, Port 2 PHY, and Virtual PHY)
- **Soft Reset** - SRST (bit 0) in the Hardware Configuration Register (HW_CFG)
  - Resets the HBI, Host MAC, and System CSRs below address 100h

A single-module reset is initiated by assertion of the following:

- **Port 2 PHY Reset** - PHY2_RST (bit 2) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)
  - Resets the Port 2 PHY
- **Port 1 PHY Reset** - PHY1_RST (bit 1) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)
  - Resets the Port 1 PHY
- **Virtual PHY Reset** - VPHY_RST (bit 0) in the Reset Control Register (RESET_CTL), (bit 10) in the Power Management Control Register (PMT_CTRL), or Reset (bit 15) in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)
  - Resets the Virtual PHY

The LAN9311/LAN9311i supports numerous power management and wakeup features. The Port 1 & 2 PHYs provide general power-down and energy detect power-down modes, which allow a reduction in PHY power consumption. The Host MAC provides wake-up frame detection and magic packet detection modes. The LAN9311/LAN9311i can be programmed to issue an external wake signal (PME) via several methods, including wake on LAN, wake on link status change (energy detect), and magic packet wakeup. The PME signal is ideal for triggering system power-up using remote Ethernet wakeup events.

2.2.2 SYSTEM INTERRUPT CONTROLLER

The LAN9311/LAN9311i provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. At the top level are the Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). These registers aggregate and control all interrupts from the various LAN9311/LAN9311i sub-modules. The LAN9311/LAN9311i is capable of generating interrupt events from the following:

- 1588 Time Stamp
- Switch Fabric
- Ethernet PHYs
- GPIOs
- Host MAC (FIFOs, power management)
- General Purpose Timer
- Software (general purpose)

A dedicated programmable IRQ interrupt output pin is provided for external indication of any LAN9311/LAN9311i interrupts. The IRQ pin is controlled via the Interrupt Configuration Register (IRQ_CFG), which allows configuration of the IRQ buffer type, polarity, and de-assertion interval.

2.2.3 SWITCH FABRIC

The Switch Fabric consists of the following major function blocks:

- **10/100 MACs**
  There is one 10/100 Ethernet MAC per switch fabric port, which provides basic 10/100 Ethernet functionality, including transmission deferral, collision back-off/retry, TX/RX FCS checking/generation, TX/RX pause flow control, and transmit back pressure. The 10/100 MACs act as an interface between the switch engine and the 10/100 PHYs (for ports 1 and 2). The port 0 10/100 MAC interfaces the switch engine to the Host MAC. Each 10/100 MAC includes RX and TX FIFOs and per port statistic counters.
- **Switch Engine**
  This block, consisting of a 3 port VLAN layer 2 switching engine, provides the control for all forwarding/filtering rules and supports untagged, VLAN tagged, and priority tagged frames. The switch engine provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, and port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. A 1K entry forwarding table provides ample room for MAC address forwarding tables.
- **Buffer Manager**
  This block controls the free buffer space, multi-level transmit queues, transmission scheduling, and packet dropping of the switch fabric. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed. Each port is allocated 1a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block.
- **Switch CSRs**
  This block contains all switch related control and status registers, and allows all aspects of the switch fabric to be managed. These registers are indirectly accessible via the memory mapped system control and status registers

2.2.4 ETHERNET PHYS

The LAN9311/LAN9311i contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the switch fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of the Host MAC to port 0 of the switch fabric as if it was connected to a single port PHY. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set.

2.2.5 HOST BUS INTERFACE (HBI)

The Host Bus Interface (HBI) module provides a high-speed asynchronous SRAM-like slave interface that facilitates communication between the LAN9311/LAN9311i and a host system. The HBI allows access to the System CSRs and handles byte swapping based on the dynamic endianess select. The HBI interfaces to the switch fabric via the Host MAC, which contains the TX/RX Data and Status FIFOs, Host MAC registers and power management features. The main features of the HBI are:

- Asynchronous 16-bit Host Bus Interface
  - Host Data Bus Endianess Control
  - Direct FIFO Access Modes
- System CSRs Access
- Interrupt Support

2.2.6 HOST MAC

The Host MAC incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface between the Host Bus Interface (HBI) and the Ethernet PHYs and Switch Fabric. On the front end, the Host MAC interfaces to the HBI via 2 sets of FIFO's (TX Data FIFO, TX Status FIFO, RX Data FIFO, RX Status FIFO). The FIFOs are a conduit between the HBI and the Host MAC through which all transmitted and received data and status information is passed. An additional bus is used to access the Host MAC CSR's via the Host MAC CSR Interface Command Register (MAC_CSR_CMD) and Host MAC CSR Interface Data Register (MAC_CSR_DATA) system registers.

On the back end, the Host MAC interfaces with the 10/100 Ethernet PHY's (Virtual PHY, Port 1 PHY, Port 2 PHY) via an internal SMI (Serial Management Interface) bus. This allows the Host MAC access to the PHY's internal registers via the Host MAC MII Access Register (HMAC_MII_ACC) and Host MAC MII Data Register (HMAC_MII_DATA). The Host MAC interfaces to the Switch Engine Port 0 via an internal MII (Media Independent Interface) connection allowing for incoming and outgoing Ethernet packet transfers.

The Host MAC can operate at either 100Mbps or 10Mbps in both half-duplex or full-duplex modes. When operating in half-duplex mode, the Host MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in full-duplex mode, the Host MAC complies with IEEE 802.3 full-duplex operation standard.

2.2.7 EEPROM CONTROLLER/LOADER

The EEPROM Controller is an I^2C/Microwire master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple types (I^2C/Microwire) and sizes of external EEPROMs are supported. Configuration of the EEPROM type and size are accomplished via the eeprom_type_strap and eeprom_size_strap[1:0] configuration straps respectively. Various commands are supported for each EEPROM type, allowing for the storage and retrieval of static data. The I^2C interface conforms to the Philips *I^2C-Bus Specification*.

The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs. The EEPROM Loader provides the automatic loading of configuration settings from the EEPROM into the LAN9311/LAN9311i at reset. The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset (DIGITAL_RST bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD).

2.2.8 1588 TIME STAMP

The IEEE 1588 Time Stamp modules provide hardware support for the IEEE 1588 Precision Time Protocol (PTP), allowing clock synchronization with remote Ethernet devices, packet time stamping, and time driven event generation. Time stamping is supported on all ports, with an individual IEEE 1588 Time Stamp module connected to each port via the MII bus. Any port may function as a master or a slave clock per the IEEE 1588 specification, and the LAN9311/LAN9311i as a whole may function as a boundary clock.

A 64-bit tunable clock is provided that is used as the time source for all IEEE 1588 time stamp related functions. The IEEE 1588 Clock/Events block provides IEEE 1588 clock comparison based interrupt generation and time stamp related GPIO event generation. Two LAN9311/LAN9311i GPIO pins (GPIO[8:9]) can be used to trigger a time stamp capture when configured as an input, or output a signal from the GPIO based on an IEEE 1588 clock target compare event when configured as an output. All features of the IEEE 1588 hardware time stamp unit can be monitored and configured via their respective IEEE 1588 configuration and status registers (CSRs).

2.2.9 GPIO/LED CONTROLLER

The LAN9311/LAN9311i provides 12 configurable general-purpose input/output pins which are controlled via this module. These pins can be individually configured via the GPIO/LED CSRs to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. Two of the GPIO pins (GPIO[9:8]) can be used for IEEE 1588 timestamp functions, allowing GPIO driven 1588 time clock capture when configured as an input, or GPIO output generation based on an IEEE 1588 clock target compare event.

In addition, 8 of the GPIO pins can be alternatively configured as LED outputs. These pins, GPIO[7:0] (nP1LED[3:0] and nP2LED[3:0]), may be enabled to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

2.3 System Configuration

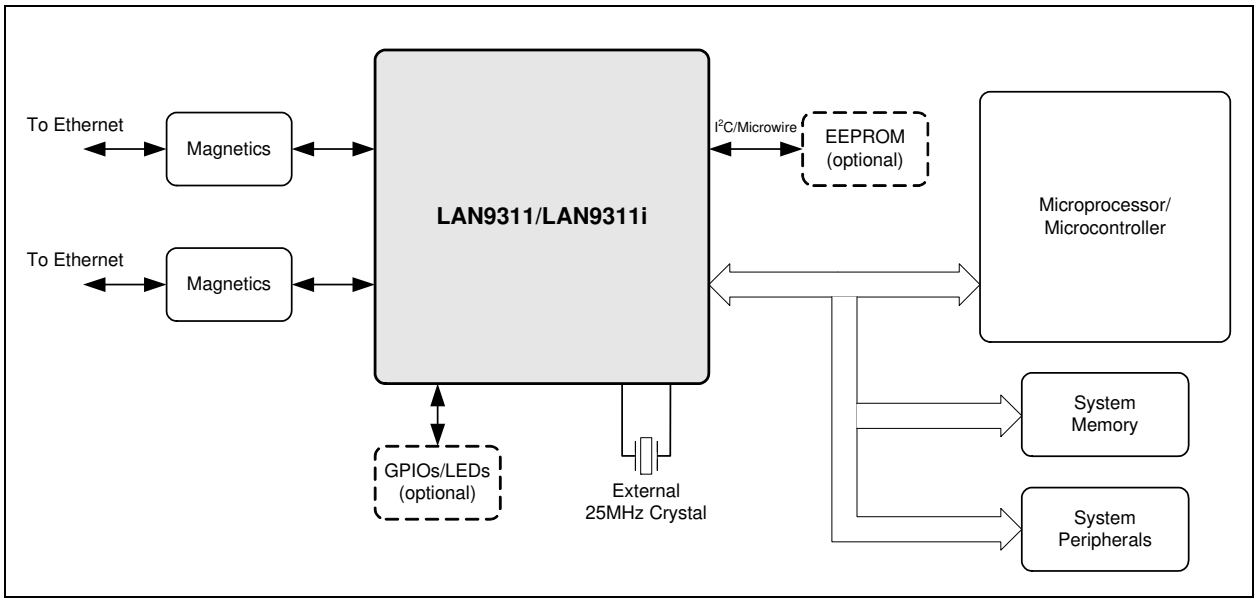
In a typical application, the LAN9311/LAN9311i Host Bus Interface (HBI) is connected to the host microprocessor/microcontroller via the asynchronous 16-bit interface, allowing access to the LAN9311/LAN9311i system configuration and status registers. The LAN9311/LAN9311i utilizes the internal Host MAC to provide a network path for the host CPU. The LAN9311/LAN9311i may share the host bus with additional system memory and/or peripherals. For more information on the HBI, refer to Section 8.0, "Host Bus Interface (HBI)," on page 76.

The 2 Ethernet ports of the LAN9311/LAN9311i must be connected to Auto-MDIX style magnetics for proper operation on the Ethernet network. Refer to the Microchip Application Note 8.13 “Suggested Magnetics” for further details.

The LAN9311/LAN9311i also supports optional EEPROM and GPIOs/LEDs. When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C/Microwire interface.

A system configuration diagram of the LAN9311/LAN9311i in a typical embedded environment can be seen in Figure 2-2.

FIGURE 2-2: SYSTEM BLOCK DIAGRAM

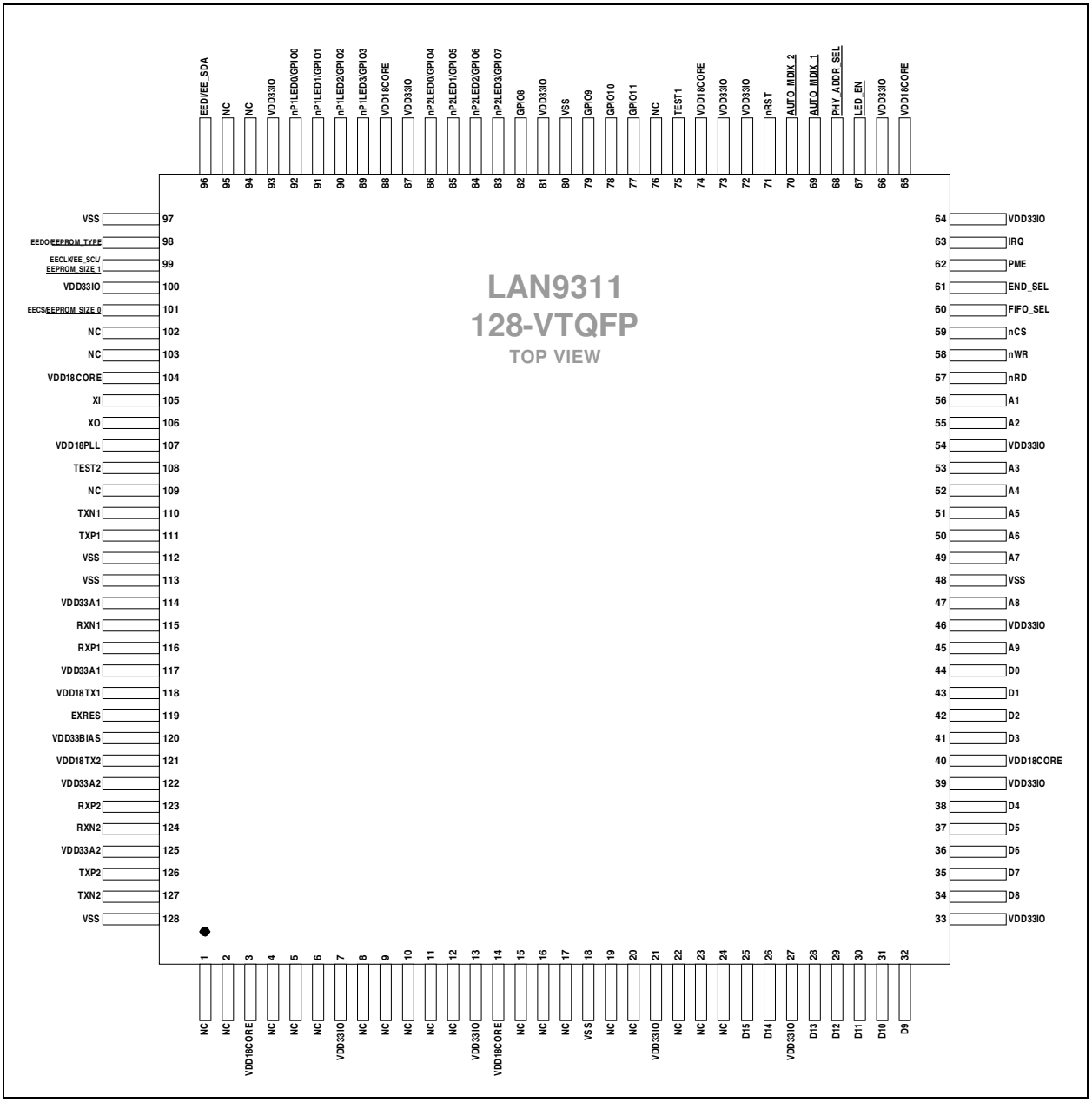


3.0 PIN DESCRIPTION AND CONFIGURATION

3.1 Pin Diagrams

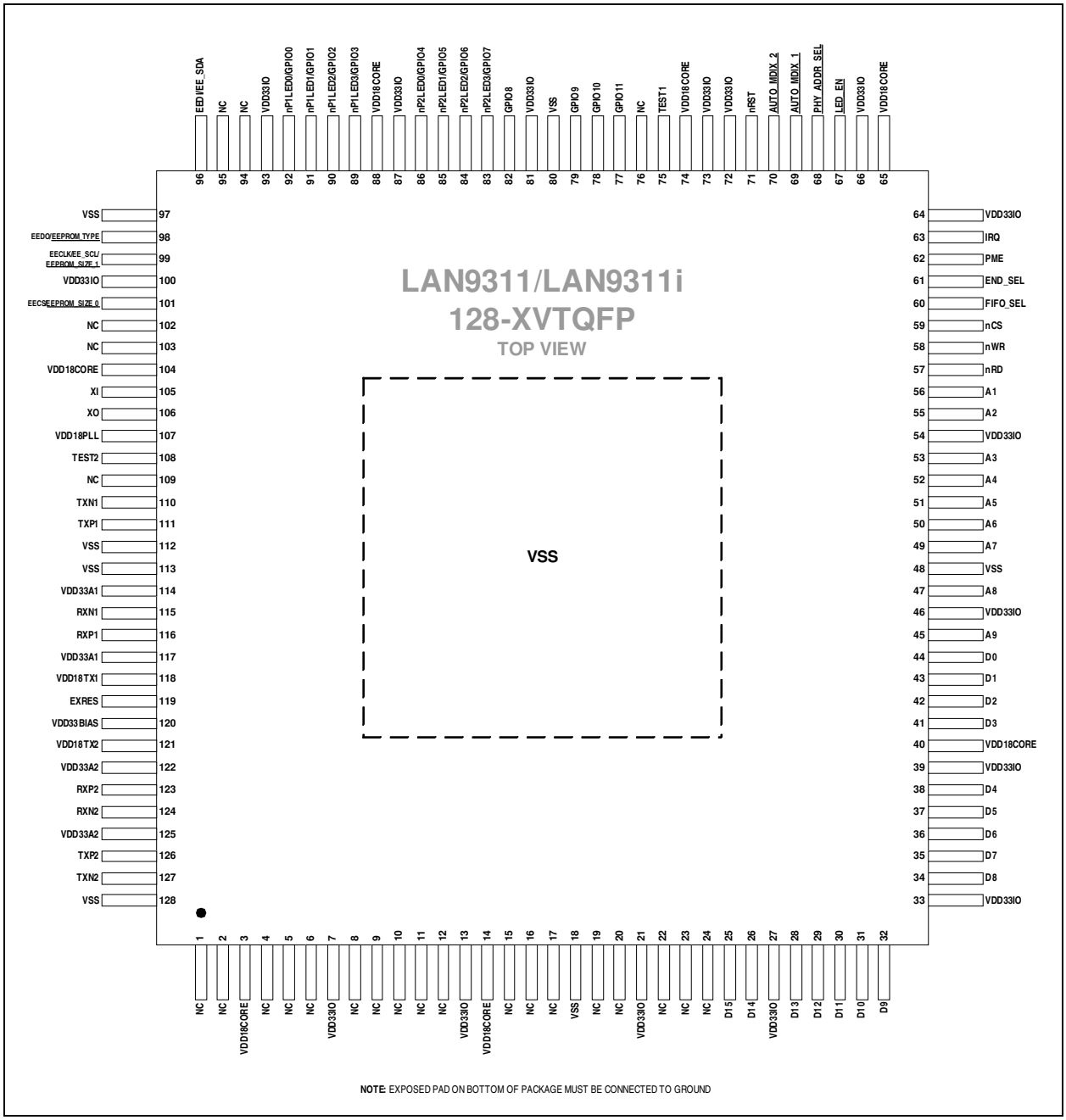
3.1.1 128-VTQFP PIN DIAGRAM

FIGURE 3-1: LAN9311 128-VTQFP PIN ASSIGNMENTS (TOP VIEW)



3.1.2 128-XVTQFP PIN DIAGRAM

FIGURE 3-2: LAN9311/LAN9311I 128-XVTQFP PIN ASSIGNMENTS (TOP VIEW)



NOTE: EXPOSED PAD ON BOTTOM OF PACKAGE MUST BE CONNECTED TO GROUND

3.2 Pin Descriptions

This section contains the descriptions of the LAN9311/LAN9311i pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port 1 Pins
- LAN Port 2 Pins
- LAN Port 1 & 2 Power and Common Pins
- Host Bus Interface Pins
- EEPROM Pins
- Dedicated Configuration Strap Pins
- Miscellaneous Pins
- PLL Pins
- Core and I/O Power and Ground Pins
- No-Connect Pins

Note: A list of buffer type definitions is provided in Section 1.2, "Buffer Types," on page 5.

TABLE 3-1: LAN PORT 1 PINS

Pin	Name	Symbol	Buffer Type	Description
89-92	Port 1 LED Indicators	nP1LED[3:0]	OD12	**LED Indicators:** When configured as LED outputs via the LED Configuration Register (LED_CFG), these pins are open-drain, active low outputs and the pull-ups and input buffers are disabled. The functionality of each pin is determined via the LED_CFG[9:8] bits.
	General Purpose I/O Data	GPIO[3:0]	IS/O12/OD12 (PU)	**General Purpose I/O Data:** When configured as GPIO via the LED Configuration Register (LED_CFG), these general purpose signals are fully programmable as either push-pull outputs, open-drain outputs or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The pull-ups are enabled in GPIO mode. The input buffers are disabled when set as an output. **Note:** See Section 13.0, "GPIO/LED Controller," on page 133 for additional details.
110	Port 1 Ethernet TX Negative	TXN1	AIO	**Ethernet TX Negative:** Negative output of Port 1 Ethernet transmitter. See Note 3-1 for additional information.
111	Port 1 Ethernet TX Positive	TXP1	AIO	**Ethernet TX Positive:** Positive output of Port 1 Ethernet transmitter. See Note 3-1 for additional information.
115	Port 1 Ethernet RX Negative	RXN1	AIO	**Ethernet RX Negative:** Negative input of Port 1 Ethernet receiver. See Note 3-1 for additional information.
116	Port 1 Ethernet RX Positive	RXP1	AIO	**Ethernet RX Positive:** Positive input of Port 1 Ethernet receiver. See Note 3-1 for additional information.

Note 3-1 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

TABLE 3-2: LAN PORT 2 PINS

Pin	Name	Symbol	Buffer Type	Description
83-86	Port 2 LED Indicators	nP2LED[3:0]	OD12	**LED indicators:** When configured as LED outputs via the LED Configuration Register (LED_CFG), these pins are open-drain, active low outputs and the pull-ups and input buffers are disabled. The functionality of each pin is determined via the LED_CFG[9:8] bits.
	General Purpose I/O Data	GPIO[7:4]	IS/O12/OD12 (PU)	**General Purpose I/O Data:** When configured as GPIO via the LED Configuration Register (LED_CFG), these general purpose signals are fully programmable as either push-pull outputs, open-drain outputs or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The pull-ups are enabled in GPIO mode. The input buffers are disabled when set as an output. **Note:** See Section 13.0, "GPIO/LED Controller," on page 133 for additional details.
127	Port 2 Ethernet TX Negative	TXN2	AIO	**Ethernet TX Negative:** Negative output of Port 2 Ethernet transmitter. See Note 3-2 for additional information.
126	Port 2 Ethernet TX Positive	TXP2	AIO	**Ethernet TX Positive:** Positive output of Port 2 Ethernet transmitter. See Note 3-2 for additional information.
124	Port 2 Ethernet RX Negative	RXN2	AIO	**Ethernet RX Negative:** Negative input of Port 2 Ethernet receiver. See Note 3-2 for additional information.
123	Port 2 Ethernet RX Positive	RXP2	AIO	**Ethernet RX Positive:** Positive input of Port 2 Ethernet receiver. See Note 3-2 for additional information.

Note 3-2 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

TABLE 3-3: LAN PORT 1 & 2 POWER AND COMMON PINS

Pin	Name	Symbol	Buffer Type	Description
119	Bias Reference	EXRES	AI	**Bias Reference:** Used for internal bias circuits. Connect to an external 12.4K ohm, 1% resistor to ground.
114,117	+3.3V Port 1 Analog Power Supply	VDD33A1	P	**+3.3V Port 1 Analog Power Supply** Refer to the LAN9311/LAN9311i reference schematic for additional connection information.
122,125	+3.3V Port 2 Analog Power Supply	VDD33A2	P	**+3.3V Port 2 Analog Power Supply** Refer to the LAN9311/LAN9311i reference schematic for additional connection information.
120	+3.3V Master Bias Power Supply	VDD33BIAS	P	**+3.3V Master Bias Power Supply** Refer to the LAN9311/LAN9311i reference schematic for additional connection information.

TABLE 3-3: LAN PORT 1 & 2 POWER AND COMMON PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Description
121	Port 2 Transmitter +1.8V Power Supply	VDD18TX2	P	**Port 2 Transmitter +1.8V Power Supply:** This pin is supplied from the internal PHY voltage regulator. This pin must be tied to the VDD18TX1 pin for proper operation. Refer to the LAN9311/LAN9311i reference schematic for additional connection information.
118	Port 1 Transmitter +1.8V Power Supply	VDD18TX1	P	**Port 1 Transmitter +1.8V Power Supply:** This pin must be connected directly to the VDD18TX2 pin for proper operation. Refer to the LAN9311/LAN9311i reference schematic for additional connection information.

TABLE 3-4: HOST BUS INTERFACE PINS

Pin	Name	Symbol	Buffer Type	Description
25,26, 28-32, 34-38, 41-44	Host Bus Data	D[15:0]	IS/O8	**Host Bus Data:** Bits 15-0 of the Host Bus data port. **Note:** Big and little endianess is supported.
45,47, 49-53, 55,56	Host Bus Address	A[9:1]	IS	**Host Bus Address:** 9-bit Host Bus Address Port used to select Internal CSR's and TX and RX FIFO's. **Note:** The A0 bit is not used because the LAN9311/LAN9311i must be accessed on WORD boundaries.
57	Read Strobe	nRD	IS	**Read Strobe:** Active low strobe to indicate a read cycle. This signal is qualified by the nCS chip select.
58	Write Strobe	nWR	IS	**Write Strobe:** Active low strobe to indicate a write cycle. This signal is qualified by the nCS chip select.
59	Chip Select	nCS	IS	**Chip Select:** Active low signal used to qualify read and write operations.
60	Data FIFO Direct Access Select	FIFO_SEL	IS	**Data FIFO Direct Access Select:** When driven high, all accesses to the LAN9311/LAN9311i are directed to the RX and TX Data FIFO's. All reads are from the RX Data FIFO, and all writes are to the TX Data FIFO. In this mode, the address input is ignored. Refer to Section 14.1.3, "Direct FIFO Access Mode," on page 138 for additional information.
61	Endianess Select	END_SEL	IS	**Endianess Select:** When this signal is set high, big endian mode is selected. When low, little endian mode is selected. This signal may be dynamically changed or held static. Refer to Section 8.0, "Host Bus Interface (HBI)," on page 76 for additional information.

Note: Refer to Section 8.0, "Host Bus Interface (HBI)," on page 76 for additional information regarding the use of these signals.

TABLE 3-5: EEPROM PINS

Pin	Name	Symbol	Buffer Type	Description
96	EEPROM Microwire Data Input	EEDI	IS (PD)	**EEPROM Microwire Data Input (EEDI):** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM serial data input.
	EEPROM I²C Serial Data Input/Output	EE_SDA	IS/OD8	**EEPROM I²C Serial Data Input/Output (EE_SDA):** In I²C EEPROM mode (EEPROM_TYPE = 1), this pin is the I²C EEPROM serial data input/output. **Note:** If I²C is selected, an external pull-up is required when using an EEPROM and is recommended if no EEPROM is attached.
98	EEPROM Microwire Data Output	EEDO	O8	**EEPROM Microwire Data Output:** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM serial data output. **Note:** In I²C mode (EEPROM_TYPE=1), this pin is not used and is driven low. **Note:** When not using a Microwire or I²C EEPROM, an external pull-down resistor is recommended on this pin.
	EEPROM Type Strap	EEPROM_TYPE	IS Note 3-3	**EEPROM Type Strap:** Configures the EEPROM type. See Note 3-4 **0 = Microwire Mode** **1 = I²C Mode** **Note:** When not using a Microwire or I²C EEPROM, an external pull-down resistor is recommended on this pin.
99	EEPROM Microwire Serial Clock	EECLK	O8	**EEPROM Microwire Serial Clock (EECLK):** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM clock output.
	EEPROM I²C Serial Clock	EE_SCL	IS/OD8	**EEPROM I²C Serial Clock (EE_SCL):** In I²C EEPROM mode (EEPROM_TYPE=1), this pin is the I²C EEPROM clock input/open-drain output. **Note:** If I²C is selected, an external pull-up is required when using an EEPROM and is recommended if no EEPROM is attached.
	EEPROM Size Strap 1	EEPROM_SIZE_1	IS Note 3-5	**EEPROM Size Strap 1:** Configures the high bit of the EEPROM size range as specified in Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 110. This bit is not used for I²C EEPROMs. See Note 3-4.
101	EEPROM Microwire Chip Select	EECS	O8	**EEPROM Microwire Chip Select:** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM chip select output. **Note:** In I²C mode (EEPROM_TYPE=1), this pin is not used and is driven low.
	EEPROM Size Strap 0	EEPROM_SIZE_0	IS Note 3-3	**EEPROM Size Strap 0:** Configures the low bit of the EEPROM size range as specified in Section 10.2, "I2C/Microwire Master EEPROM Controller," on page 110. See Note 3-4.

Note 3-3 The IS buffer type is valid only during the time specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 294.

Note 3-4 Configuration strap values are latched on power-on reset or nRST de-assertion. Configuration strap pins are identified by an underlined symbol name. Refer to Section 4.2.4, "Configuration Straps," on page 25 for more information.

Note 3-5 The IS buffer type is valid only during the time specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 294 and when in I^2C mode.

TABLE 3-6: DEDICATED CONFIGURATION STRAP PINS

Pin	Name	Symbol	Buffer Type	Description
67	LED Enable Strap	LED_EN	IS (PU)	**LED Enable Strap:** Configures the default value for the LED_EN bits in the LED Configuration Register (LED_CFG). When latched low, all 8 LED/GPIO pins are configured as GPIOs. When latched high, all 8 LED/GPIO pins are configured as LEDs. See Note 3-6.
68	PHY Address Strap	PHY_ADDR_SEL	IS (PU)	**PHY Address Select Strap:** Configures the default MII management address values for the PHYs (Virtual, Port 1, and Port 2) as detailed in Section 7.1.1, "PHY Addressing," on page 62. PHY_ADDR_SEL VALUE / VIRTUAL PHY ADDRESS / PORT 1 PHY ADDRESS / PORT 2 PHY ADDRESS **0** / 0 / 1 / 2 **1** / 1 / 2 / 3 See Note 3-6.
69	Port 1 Auto-MDIX Enable Strap	AUTO_MDIX_1	IS (PU)	**Port 1 Auto-MDIX Enable Strap:** Configures the Auto-MDIX functionality on Port 1. When latched low, Auto-MDIX is disabled. When latched high, Auto-MDIX is enabled. See Note 3-6.
70	Port 2 Auto-MDIX Enable Strap	AUTO_MDIX_2	IS (PU)	**Port 2 Auto-MDIX Enable Strap:** Configures the Auto-MDIX functionality on Port 2. When latched low, Auto-MDIX is disabled. When latched high, Auto-MDIX is enabled. See Note 3-6.

Note: For more information on configuration straps, refer to Section 4.2.4, "Configuration Straps," on page 25. Additional strap pins, which share functionality with the EEPROM pins, are described in Table 3-5.

Note 3-6 Configuration strap values are latched on power-on reset or nRST de-assertion. Configuration strap pins are identified by an underlined symbol name. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 25 for more information.

TABLE 3-7: MISCELLANEOUS PINS

Pin	Name	Symbol	Buffer Type	Description
77-79, 82	General Purpose I/O Data	GPIO[11:8]	IS/OD12/ O12 (PU) Note 3-7	**General Purpose I/O Data:** These general purpose signals are fully programmable as either push-pull outputs, open-drain outputs, or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). For more information, refer to Section 13.0, "GPIO/LED Controller," on page 133. **Note:** The remaining GPIO[7:0] pins share functionality with the LED output pins, as described in Table 3-1 and Table 3-2.
63	Interrupt Output	IRQ	O8/OD8	**Interrupt Output:** Interrupt request output. The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). For more information, refer to Section 5.0, "System Interrupts," on page 34.
71	System Reset Input	nRST	IS (PU)	**System Reset Input:** This active low signal allows external hardware to reset the LAN9311/LAN9311i. The LAN9311/LAN9311i also contains an internal power-on reset circuit. Thus, this signal may be left unconnected if an external hardware reset is not needed. When used, this signal must adhere to the reset timing requirements as detailed in Section 15.5.2, "Reset and Configuration Strap Timing," on page 294. **Note:** The LAN9311/LAN9311i must always be read at least once after power-up or reset to ensure that write operations function properly.
75	Test 1	TEST1	AI	**Test 1:** This pin must be tied to VDD33IO for proper operation.
108	Test 2	TEST2	AI	**Test 2:** This pin must be tied to VDD33IO for proper operation.
62	Power Management Event	PME	O8/OD8	**Power Management Event:** When programmed accordingly, this signal is asserted upon detection of a wakeup event. The polarity and buffer type of this signal is programmable via the PME_EN bit of the Power Management Control Register (PMT_CTRL). Refer to Section 4.0, "Clocking, Resets, and Power Management," on page 22 for additional information on the LAN9311/LAN9311i power management features.

Note 3-7 The input buffers are enabled when configured as GPIO inputs only.

TABLE 3-8: PLL PINS

Pin	Name	Symbol	Buffer Type	Description
107	PLL +1.8V Power Supply	VDD18PLL	P	**PLL +1.8V Power Supply:** This pin must be connected to VDD18CORE for proper operation. Refer to the LAN9311/LAN9311i reference schematic for additional connection information.
105	Crystal Input	XI	ICLK	**Crystal Input:** External 25MHz crystal input. This signal can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
106	Crystal Output	XO	OCLK	**Crystal Output:** External 25MHz crystal output.

TABLE 3-9: CORE AND I/O POWER AND GROUND PINS

Pin	Name	Symbol	Buffer Type	Description
7,13,21,27,33,39,46, 54,64,66, 72,73,81, 87,93,100	+3.3V I/O Power	VDD33IO	P	**+3.3V Power Supply for I/O Pins and Internal Regulator** Refer to the LAN9311/LAN9311i reference schematic for additional connection information.
3,14,40,65,74,88,104	Digital Core +1.8V Power Supply Output	VDD18CORE	P	**Digital Core +1.8V Power Supply Output:** +1.8V power from the internal core voltage regulator. All VDD18CORE pins must be tied together for proper operation. Refer to the LAN9311/LAN9311i reference schematic for additional connection information.
18,48,80, 97,112,113,128 Note 3-8	Common Ground	VSS	P	**Common Ground**

Note 3-8 Plus external pad for 128-XVTQFP package only.

TABLE 3-10: NO-CONNECT PINS

Pin	Name	Symbol	Buffer Type	Description
1,2, 4-6, 8-12, 15-17,19, 20,22-24, 76,94,95, 102,103, 109	No Connect	NC	-	**No Connect:** These pins must be left floating for normal device operation.

4.0 CLOCKING, RESETS, AND POWER MANAGEMENT

4.1 Clocks

The LAN9311/LAN9311i includes a clock module which provides generation of all system clocks as required by the various sub-modules of the device. The LAN9311/LAN9311i requires a fixed-frequency 25MHz clock source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25MHz crystal to the XI and XO pins as specified in Section 15.6, "Clock Circuit," on page 302. Optionally, this clock can be provided by driving the XI input pin with a single-ended 25MHz clock source. If a single-ended source is selected, the clock input must run continuously for normal device operation. The internal PLL generates a fixed 200MHz base clock which is used to derive all LAN9311/LAN9311i sub-system clocks.

In addition to the sub-system clocks, the clock module is also responsible for generating the clocks used for the general purpose timer and free-running clock. Refer to Section 12.0, "General Purpose Timer & Free-Running Clock," on page 132 for additional details.

Note: Crystal specifications are provided in Table 15-15, “LAN9311/LAN9311iCrystal Specifications,” on page 302.

4.2 Resets

The LAN9311/LAN9311i provides multiple hardware and software reset sources, which allow varying levels of the LAN9311/LAN9311i to be reset. All resets can be categorized into three reset types as described in the following sections:

- Chip-Level Resets
  - Power-On Reset (POR)
  - nRST Pin Reset
- Multi-Module Resets
  - Digital Reset (DIGITAL_RST)
  - Soft Reset (SRST)
- Single-Module Resets
  - Port 2 PHY Reset
  - Port 1 PHY Reset
  - Virtual PHY Reset

The LAN9311/LAN9311i supports the use of configuration straps to allow automatic custom configurations of various LAN9311/LAN9311i parameters. These configuration strap values are set upon de-assertion of all chip-level resets and can be used to easily set the default parameters of the chip at power-on or pin (nRST) reset. Refer to Section 4.2.4, "Configuration Straps," on page 25 for detailed information on the usage of these straps.

Note: The LAN9311/LAN9311i EEPROM Loader is run upon a power-on reset, nRST pin reset, and digital reset. Refer to Section 10.2.4, "EEPROM Loader," on page 120 for additional information.

Table 4-1 summarizes the effect of the various reset sources on the LAN9311/LAN9311i. Refer to the following sections for detailed information on each of these reset types.

TABLE 4-1: RESET SOURCES AND AFFECTED LAN9311/LAN9311I CIRCUITRY

Reset Source	System Clocks/Reset/PME	Sys Interrupts	Switch Fabric	Ethernet PHYs	HBI	Host MAC	EEPROM Controller	1588 Time Stamp	GPIO/LED Controller	Config. Straps Latched	EEPROM Loader Run
POR	X	X	X	X	X	X	X	X	X	X	X
nRST Pin	X	X	X	X	X	X	X	X	X	X	X
Digital Reset	X	X	X		X	X	X	X	X		X
Soft Reset					X	X					Note 4-1
Port 2 PHY				X							
Port 1 PHY				X							
Virtual PHY				X							

Note 4-1 In the case of a soft reset, the EEPROM Loader is run, but loads only the MAC address into the Host MAC. No other values are loaded by the EEPROM Loader in this case.

4.2.1 CHIP-LEVEL RESETS

A chip-level reset event activates all internal resets, effectively resetting the entire LAN9311/LAN9311i. Configuration straps are latched, and the EEPROM Loader is run as a result of chip-level resets. A chip-level reset is initiated by assertion of any of the following input events:

- Power-On Reset (POR)
- nRST Pin Reset

Chip-level reset completion/configuration can be determined by polling the READY bit of the Hardware Configuration Register (HW_CFG) or Power Management Control Register (PMT_CTRL) until it is set. When set, the READY bit indicates that the reset has completed and the device is ready to be accessed.

With the exception of the Hardware Configuration Register (HW_CFG), Power Management Control Register (PMT_CTRL), Byte Order Test Register (BYTE_TEST), and Reset Control Register (RESET_CTL), read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until the READY bit is set.

Note: The LAN9311/LAN9311i must be read at least once after any chip-level reset to ensure that write operations function properly.

4.2.1.1 Power-On Reset (POR)

A power-on reset occurs whenever power is initially applied to the LAN9311/LAN9311i, or if the power is removed and reapplied to the LAN9311/LAN9311i. This event resets all circuitry within the device. Configuration straps are latched, and the EEPROM Loader is run as a result of this reset.

A POR reset typically takes approximately 23mS, plus additional time (91uS for I^2C, 28uS for Microwire) per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load (64KB for I^2C, 2KB for Microwire) will complete in approximately 6.0 seconds for I^2C EEPROM, and 80mS for Microwire EEPROM.

4.2.1.2 nRST Pin Reset

Driving the nRST input pin low initiates a chip-level reset. This event resets all circuitry within the device. Use of this reset input is optional, but when used, it must be driven for the period of time specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 294. Configuration straps are latched, and the EEPROM Loader is run as a result of this reset.

A nRST pin reset typically takes approximately 760uS, plus additional time (91uS for I^2C, 28uS for Microwire) per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load (64KB for I^2C, 2KB for Microwire) will complete in approximately 6.0 seconds for I^2C EEPROM, and 58mS for Microwire EEPROM.

Note:	The nRST pin is pulled-high internally. If unused, this signal can be left unconnected. Do not rely on internal pull-up resistors to drive signals external to the device.

Please refer to Table 3-7, "Miscellaneous Pins" for a description of the nRST pin.

4.2.2 MULTI-MODULE RESETS

Multi-module resets activate multiple internal resets, but do not reset the entire chip. Configuration straps are *not* latched upon multi-module resets. A multi-module reset is initiated by assertion of the following:

- Digital Reset (DIGITAL_RST)
- Soft Reset (SRST)

Chip-level reset completion/configuration can be determined by polling the READY bit of the Hardware Configuration Register (HW_CFG) or Power Management Control Register (PMT_CTRL) until it is set. When set, the READY bit indicates that the reset has completed and the device is ready to be accessed.

With the exception of the Hardware Configuration Register (HW_CFG), Power Management Control Register (PMT_CTRL), Byte Order Test Register (BYTE_TEST), and Reset Control Register (RESET_CTL), read access to any internal resources is forbidden while the READY bit is cleared. Writes to any address are invalid until the READY bit is set.

Note:	The digital reset and soft reset do not reset register bits designated as NASR.

Note:	The LAN9311/LAN9311i must be read at least once after a multi-module reset to ensure that write operations function properly.

4.2.2.1 Digital Reset (DIGITAL_RST)

A digital reset is performed by setting the DIGITAL_RST bit of the Reset Control Register (RESET_CTL). A digital reset will reset all LAN9311/LAN9311i sub-modules except the Ethernet PHYs (Port 1 PHY, Port 2 PHY, and Virtual PHY). The EEPROM Loader will automatically run following this reset. Configuration straps are *not* latched as a result of a digital reset.

A digital reset typically takes approximately 760uS, plus additional time (91uS for I^2C, 28uS for Microwire) per byte of data loaded from the EEPROM via the EEPROM Loader. A full EEPROM load (64KB for I^2C, 2KB for Microwire) will complete in approximately 6.0 seconds for I^2C EEPROM, and 58mS for Microwire EEPROM.

4.2.2.2 Soft Reset (SRST)

A soft reset is performed by setting the SRST bit of the Hardware Configuration Register (HW_CFG). A soft reset will reset the HBI, Host MAC, and System CSRs below address 100h. The soft reset also clears any TX or RX errors in the Host MAC transmitter and receiver (TXE/RXE). This reset does *not* latch the configuration straps. On soft reset, the EEPROM Loader is run, but loads only the MAC address into the Host MAC. No other values are loaded by the EEPROM Loader in this case.

A soft reset typically takes 590uS, plus an additional time (550uS for I^2C, 170uS for Microwire) when data is loaded from the EEPROM via the EEPROM Loader.

4.2.3 SINGLE-MODULE RESETS

A single-module reset will reset only the specified module. Single-module resets do *not* latch the configuration straps or initiate the EEPROM Loader. A single-module reset is initiated by assertion of the following:

- Port 2 PHY Reset
- Port 1 PHY Reset
- Virtual PHY Reset

4.2.3.1 Port 2 PHY Reset

A Port 2 PHY reset is performed by setting the PHY2_RST bit of the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Upon completion of the Port 2 PHY reset, the PHY2_RST and Reset bits are automatically cleared. No other modules of the LAN9311/LAN9311i are affected by this reset.

In addition to the methods above, the Port 2 PHY is automatically reset after returning from a PHY power-down mode. This reset differs in that the PHY power-down mode reset does not reload or reset any of the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 72 for additional information.

Port 2 PHY reset completion can be determined by polling the PHY2_RST bit in the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) until it clears. Under normal conditions, the PHY2_RST and Reset bit will clear approximately 110uS after the Port 2 PHY reset occurrence.

Note: When using the Reset bit to reset the Port 2 PHY, register bits designated as NASR are not reset.

Refer to Section 7.2.10, "PHY Resets," on page 73 for additional information on Port 2 PHY resets.

4.2.3.2 Port 1 PHY Reset

A Port 1 PHY reset is performed by setting the PHY1_RST bit of the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x). Upon completion of the Port 1 PHY reset, the PHY1_RST and Reset bits are automatically cleared. No other modules of the LAN9311/LAN9311i are affected by this reset.

In addition to the methods above, the Port 1 PHY is automatically reset after returning from a PHY power-down mode. This reset differs in that the PHY power-down mode reset does not reload or reset any of the PHY registers. Refer to Section 7.2.9, "PHY Power-Down Modes," on page 72 for additional information.

Port 1 PHY reset completion can be determined by polling the PHY1_RST bit in the Reset Control Register (RESET_CTL) or the Reset bit in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x) until it clears. Under normal conditions, the PHY1_RST and Reset bit will clear approximately 110uS after the Port 1 PHY reset occurrence.

Note: When using the Reset bit to reset the Port 1 PHY, register bits designated as NASR are not reset.

Refer to Section 7.2.10, "PHY Resets," on page 73 for additional information on Port 1 PHY resets.

4.2.3.3 Virtual PHY Reset

A Virtual PHY reset is performed by setting the VPHY_RST bit of the Reset Control Register (RESET_CTL), VPHY_RST bit in the Power Management Control Register (PMT_CTRL), or Reset in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). No other modules of the LAN9311/LAN9311i are affected by this reset.

Virtual PHY reset completion can be determined by polling the VPHY_RST bit in the Reset Control Register (RESET_CTL), the VPHY_RST bit in the Power Management Control Register (PMT_CTRL), or the Reset bit in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) until it clears. Under normal conditions, the VPHY_RST and Reset bit will clear approximately 1uS after the Virtual PHY reset occurrence.

Refer to Section 7.3.2, "Virtual PHY Resets," on page 75 for additional information on Virtual PHY resets.

4.2.4 CONFIGURATION STRAPS

Configuration straps allow various features of the LAN9311/LAN9311i to be automatically configured to user defined values. Configuration straps can be organized into two main categories: hard-straps and soft-straps. Both hard-straps and soft-straps are latched upon Power-On Reset (POR) or pin reset (nRST). The primary difference between these strap types is that soft-strap default values can be overridden by the EEPROM Loader, while hard-straps cannot.

Configuration straps which have a corresponding external pin include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down resistor should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note: The system designer must ensure that configuration strap pins meet the timing requirements specified in Section 15.5.2, "Reset and Configuration Strap Timing," on page 294. If configuration strap pins are not at the correct voltage level prior to being latched, the LAN9311/LAN9311i may capture incorrect strap values.