Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LAN9313/LAN9313i

Three Port 10/100 Managed Ethernet Switch with MII

Highlights

- High performance and full featured 3 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Serial management via SPI/I^2C or SMI
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port PHY
- Integrated IEEE 1588 Hardware Time Stamp Unit

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 1K entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1d spanning tree protocol support
  - QoS/CoS Packet prioritization
    - 4 dynamic QoS queues per port
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable class of service map based on input priority
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress/egress ports with random early discard, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any ports or port pairs
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - 1 MII - PHY mode or MAC mode
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Auto-negotiation
  - Automatic MDI/MDI-X
  - Loop-back mode
- Serial Management
  - SPI/I^2C (slave) access to all internal registers
  - MIIM (MDIO) access to PHY related registers
  - SMI (extended MIIM) access to all internal registers
- IEEE 1588 Hardware Time Stamp Unit
  - Global 64-bit tunable clock
  - Master or slave mode per port
  - Time stamp on TX or RX of Sync and Delay_req packets per port, Timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Other Features
  - General Purpose Timer
  - Serial EEPROM interface (I^2C master or Microwire™ master) for non-managed configuration
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- Available in Commercial & Industrial Temp. Ranges

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 PREFACE

1.1 General Terms

100BT	100BASE-T (100Mbps Fast Ethernet, IEEE 802.3u)
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8-bits
CSMA/CD	Carrier Sense Multiple Access / Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32-bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the LAN9313/LAN9313i from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
MDI	Medium Dependant Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the LAN9313/LAN9313i to the host
PIO cycle	Program I/O cycle. An SRAM-like read or write cycle on the HBI.
PISO	Parallel In Serial Out

PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16-bits

1.2 Buffer Types

Table 1-1 describes the pin buffer type notation used in Section 3.0, "Pin Description and Configuration," on page 15 and throughout this document.

TABLE 1-1: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered Input
O8	Output with 8mA sink and 8mA source
OD8	Open-drain output with 8mA sink
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the LAN9313/LAN9313i. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the LAN9313/LAN9313i. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

1.3 Register Nomenclature

Table 1-2 describes the register bit attribute notation used throughout this document.

TABLE 1-2: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Some examples of this are shown below:

- **R/W:** Can be written. Will return current setting on a read.
- **R/WAC:** Will return current setting on a read. Writing anything clears the bit.

2.0 INTRODUCTION

2.1 General Description

The LAN9313/LAN9313i is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9313/LAN9313i combines all the functions of a 10/100 switch system, including the switch fabric, packet buffers, buffer manager, media access controllers (MACs), PHY transceivers, and serial management. The LAN9313/LAN9313i complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the LAN9313/LAN9313i is the high performance, high efficiency 3 port Ethernet switch fabric. The switch fabric contains a 3 port VLAN layer 2 switch engine that supports untagged, VLAN tagged, and priority tagged frames. The switch fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 1K entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the buffer manager block within the switch fabric. All aspects of the switch fabric are managed via the switch fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9313/LAN9313i provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9313/LAN9313i provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the LAN9313/LAN9313i switch fabric to an external MAC or PHY. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while deceasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the LAN9313/LAN9313i.

The integrated SPI, I^2C and SMI slave controllers allow for full serial management of the LAN9313/LAN9313i via the integrated SPI/I^2C serial interface or MII interface respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the LAN9313/LAN9313i into various designs. It is this flexibility which allows the LAN9313/LAN9313i to operate in 2 different modes and under various management conditions. In MAC mode, the LAN9313/LAN9313i can be connected to an external PHY via the MII interface. In PHY mode, the LAN9313/LAN9313i can be connected to an external MAC via the MII interface. In both MAC and PHY modes, the LAN9313/LAN9313i can be unmanaged, SMI managed, I^2C managed or SPI managed. This flexibility in management makes the LAN9313/LAN9313i a candidate for virtually all switch applications.

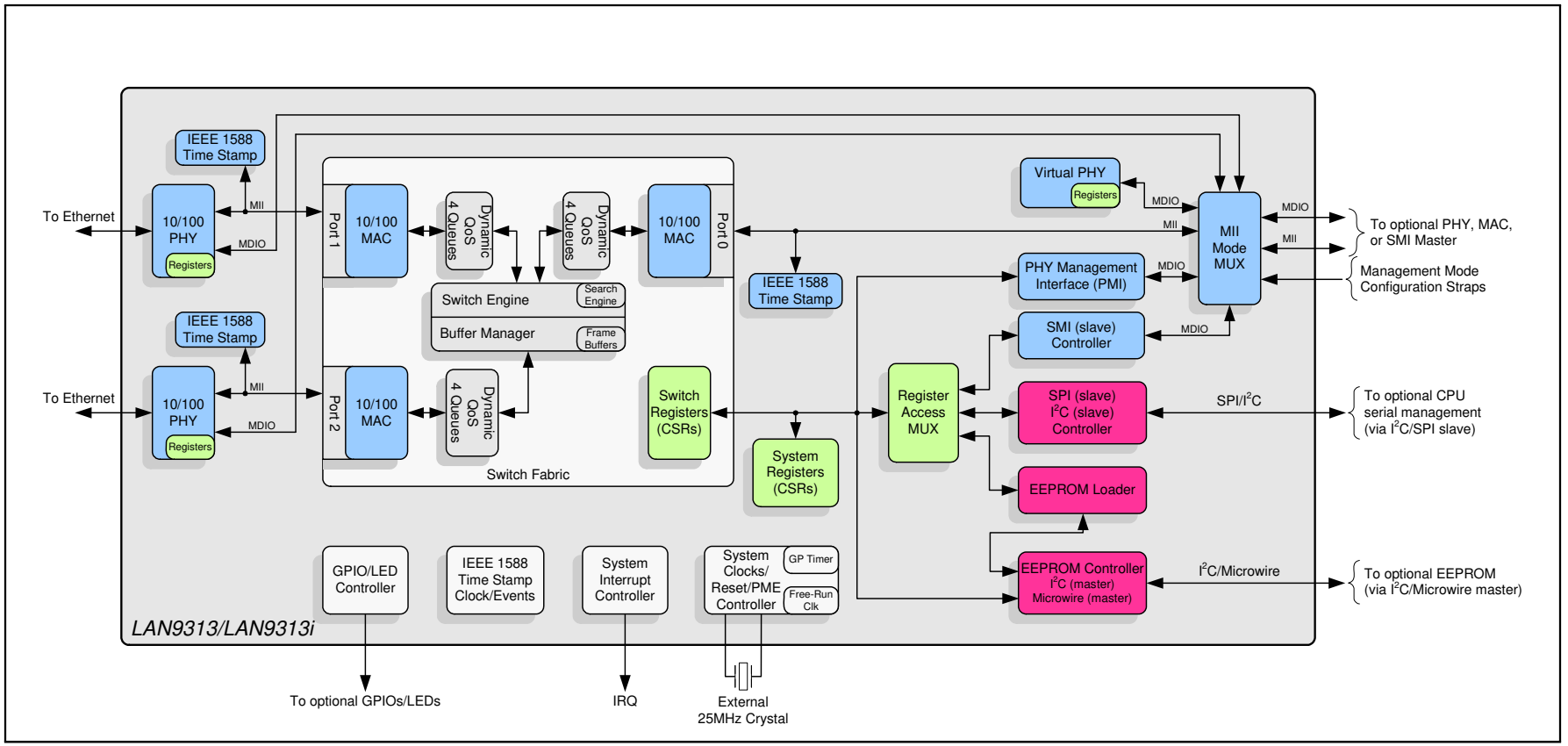
The LAN9313/LAN9313i contains an I^2C/Microwire master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the LAN9313/LAN9313i at reset, allowing the LAN9313/LAN9313i to operate unmanaged.

In addition to the primary functionality described above, the LAN9313/LAN9313i provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a 12-bit configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and select GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9313/LAN9313i's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment.

2.2 Block Diagram

FIGURE 2-1: INTERNAL LAN9313/LAN9313I BLOCK DIAGRAM



2.2.1 SYSTEM CLOCKS/RESET/PME CONTROLLER

A clock module contained within the LAN9313/LAN9313i generates all the system clocks required by the device. This module interfaces directly with the external 25MHz crystal/oscillator to generate the required clock divisions for each internal module, with the exception of the 1588 clocks, which are generated in the 1588 Time Stamp Clock/Events module. A 16-bit general purpose timer and 32-bit free-running clock are provided by this module for general purpose use. The Port 1 & 2 PHYs provide general power-down and energy detect power-down modes, which allow a reduction in PHY power consumption.

The LAN9313/LAN9313i reset events are categorized as chip-level resets, multi-module resets, and single-module resets.

A chip-level reset is initiated by assertion of any of the following input events:

- Power-On Reset
- nRST Pin Reset

A multi-module reset is initiated by assertion of the following:

- **Digital Reset** - DIGITAL_RST (bit 0) in the Reset Control Register (RESET_CTL)
  - Resets all LAN9313/LAN9313i sub-modules except the Ethernet PHYs (Port 1 PHY, Port 2 PHY, and Virtual PHY)

A single-module reset is initiated by assertion of the following:

- **Port 2 PHY Reset** - PHY2_RST (bit 2) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)
  - Resets the Port 2 PHY
- **Port 1 PHY Reset** - PHY1_RST (bit 1) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Port x PHY Basic Control Register (PHY_BASIC_CONTROL_x)
  - Resets the Port 1 PHY
- **Virtual PHY Reset** - VPHY_RST (bit 0) in the Reset Control Register (RESET_CTL) or Reset (bit 15) in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL)
  - Resets the Virtual PHY

2.2.2 SYSTEM INTERRUPT CONTROLLER

The LAN9313/LAN9313i provides a multi-tier programmable interrupt structure which is controlled by the System Interrupt Controller. At the top level are the Interrupt Status Register (INT_STS) and Interrupt Enable Register (INT_EN). These registers aggregate and control all interrupts from the various LAN9313/LAN9313i sub-modules. The LAN9313/LAN9313i is capable of generating interrupt events from the following:

- 1588 Time Stamp
- Switch Fabric
- Ethernet PHYs
- GPIOs
- General Purpose Timer
- Software (general purpose)

A dedicated programmable IRQ interrupt output pin is provided for external indication of any LAN9313/LAN9313i interrupts. The IRQ pin is controlled via the Interrupt Configuration Register (IRQ_CFG), which allows configuration of the IRQ buffer type, polarity, and de-assertion interval.

2.2.3 SWITCH FABRIC

The Switch Fabric consists of the following major function blocks:

- **10/100 MACs**
  There is one 10/100 Ethernet MAC per switch fabric port, which provides basic 10/100 Ethernet functionality, including transmission deferral, collision back-off/retry, TX/RX FCS checking/generation, TX/RX pause flow control, and transmit back pressure. The 10/100 MACs act as an interface between the switch engine and the 10/100 PHYs (for ports 1 and 2). The port 0 10/100 MAC interfaces the switch engine to the external MAC/PHY (see Section 2.3, "Modes of Operation"). Each 10/100 MAC includes RX and TX FIFOs and per port statistic counters.
- **Switch Engine**
  This block, consisting of a 3 port VLAN layer 2 switching engine, provides the control for all forwarding/filtering rules and supports untagged, VLAN tagged, and priority tagged frames. The switch engine provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, and port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. A 1K entry forwarding table provides ample room for MAC address forwarding tables.
- **Buffer Manager**
  This block controls the free buffer space, multi-level transmit queues, transmission scheduling, and packet dropping of the switch fabric. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed. Each port is allocated 1a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block.
- **Switch CSRs**
  This block contains all switch related control and status registers, and allows all aspects of the switch fabric to be managed. These registers are indirectly accessible via the system control and status registers

2.2.4 ETHERNET PHYS

The LAN9313/LAN9313i contains three PHYs: Port 1 PHY, Port 2 PHY and a Virtual PHY. The Port 1 & 2 PHYs are identical in functionality and each connect their corresponding Ethernet signal pins to the switch fabric MAC of their respective port. These PHYs interface with their respective MAC via an internal MII interface. The Virtual PHY provides the virtual functionality of a PHY and allows connection of an external MAC to port 0 of the switch fabric as if it was connected to a single port PHY. All PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX) or 10Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set.

2.2.5 PHY MANAGEMENT INTERFACE (PMI)

The PHY Management Interface (PMI) is used to serially access the internal PHYs as well as the external PHY on the MII pins (in MAC mode only, see Section 2.3, "Modes of Operation"). The PMI implements the IEEE 802.3 management protocol, providing read/write commands for PHY configuration.

2.2.6 SPI/I^{2}C SLAVE CONTROLLER

This module provides an SPI/I^{2}C slave interface which can be used for CPU serial management of the LAN9313/LAN9313i.

The SPI slave controller allows CPU access to all system CSRs for configuration and management. The SPI slave controller supports single register and multiple register read and write commands. Multiple read and multiple write commands support incrementing, decrementing, and static addressing.

The I^{2}C slave controller implements the low level I^{2}C slave serial interface (start and stop condition detection, data bit transmission/reception, and acknowledge generation/reception), handles the slave command protocol, and performs system register reads and writes. The I^{2}C slave controller conforms to the Philips *I^{2}C-Bus Specification*.

A list of management modes and configurations settings for these modes is discussed in Section 2.3, "Modes of Operation"

2.2.7 SMI SLAVE CONTROLLER

This module provides a SMI slave interface which can be used for CPU management of the LAN9313/LAN9313i via the MII pins, and allows CPU access to all system CSRs. SMI uses the same pins and protocol of the IEEE MII management function, and differs only in that SMI provides access to all internal registers by using a non-standard extended addressing map. The SMI protocol co-exists with the MII management protocol by using the upper half of the PHY address space (16 through 31).

A list of management modes and configurations settings for these modes is discussed in Section 2.3, "Modes of Operation"

2.2.8 EEPROM CONTROLLER/LOADER

The EEPROM Controller is an I^2C/Microwire master module which interfaces an optional external EEPROM with the system register bus and the EEPROM Loader. Multiple types (I^2C/Microwire) and sizes of external EEPROMs are supported. Configuration of the EEPROM type and size are accomplished via the eeprom_type_strap and eeprom_size_strap[1:0] configuration straps respectively. Various commands are supported for each EEPROM type, allowing for the storage and retrieval of static data. The I^2C interface conforms to the Philips *I^2C-Bus Specification*.

The EEPROM Loader module interfaces to the EEPROM Controller, Ethernet PHYs, and the system CSRs. The EEPROM Loader provides the automatic loading of configuration settings from the EEPROM into the LAN9313/LAN9313i at reset, allowing the LAN9313/LAN9313i to operate unmanaged. The EEPROM Loader runs upon a pin reset (nRST), power-on reset (POR), digital reset (DIGITAL_RST bit in the Reset Control Register (RESET_CTL)), or upon the issuance of a RELOAD command via the EEPROM Command Register (E2P_CMD).

2.2.9 1588 TIME STAMP

The IEEE 1588 Time Stamp modules provide hardware support for the IEEE 1588 Precision Time Protocol (PTP), allowing clock synchronization with remote Ethernet devices, packet time stamping, and time driven event generation. Time stamping is supported on all ports, with an individual IEEE 1588 Time Stamp module connected to each port via the MII bus. Any port may function as a master or a slave clock per the IEEE 1588 specification, and the LAN9313/LAN9313i as a whole may function as a boundary clock.

A 64-bit tunable clock is provided that is used as the time source for all IEEE 1588 time stamp related functions. The IEEE 1588 Clock/Events block provides IEEE 1588 clock comparison based interrupt generation and time stamp related GPIO event generation. Two LAN9313/LAN9313i GPIO pins (GPIO[8:9]) can be used to trigger a time stamp capture when configured as an input, or output a signal from the GPIO based on an IEEE 1588 clock target compare event when configured as an output. All features of the IEEE 1588 hardware time stamp unit can be monitored and configured via their respective IEEE 1588 configuration and status registers (CSRs).

2.2.10 GPIO/LED CONTROLLER

The LAN9313/LAN9313i provides 12 configurable general-purpose input/output pins which are controlled via this module. These pins can be individually configured via the GPIO/LED CSRs to function as inputs, push-pull outputs, or open drain outputs and each is capable of interrupt generation with configurable polarity. Two of the GPIO pins (GPIO[9:8]) can be used for IEEE 1588 timestamp functions, allowing GPIO driven 1588 time clock capture when configured as an input, or GPIO output generation based on an IEEE 1588 clock target compare event.

In addition, 8 of the GPIO pins can be alternatively configured as LED outputs. These pins, GPIO[7:0] (nP1LED[3:0] and nP2LED[3:0]), may be enabled to drive Ethernet status LEDs for external indication of various attributes of the switch ports.

2.3 Modes of Operation

The LAN9313/LAN9313i is designed to integrate into various embedded environments. To accomplish compatibility with a wide range of applications, the LAN9313/LAN9313i can operate in 2 different modes (MAC mode and PHY mode) and under various management conditions (unmanaged, SMI managed, I^2C managed, or SPI managed). The mode and management type of the LAN9313/LAN9313i is determined by the MII_mode_strap and mngt_mode_strap[1:0] configuration straps respectively. These modes and management types are detailed in the following sections. Figure 2-2 displays a typical system configuration for each mode and management type supported by the LAN9313/LAN9313i.

2.3.1 MAC MODE

The LAN9313/LAN9313i MAC mode utilizes an external PHY, which is connected to the MII pins, to provide a third Ethernet network connection. In this mode, the LAN9313/LAN9313i acts as a MAC, providing a communication path between the switch fabric and the external PHY. In MAC mode, the LAN9313/LAN9313i may be unmanaged, SMI managed, I^2C managed, or SPI managed as detailed in Section 2.3.3, "Management Modes".

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C/Microwire interface. Once operational, if managed, the CPU can use the I^2C/Microwire interface to read or write the EEPROM.

2.3.2 PHY MODE

The LAN9313/LAN9313i PHY mode utilizes an external MAC to provide a network path for the host CPU. The external MII pins of the LAN9313/LAN9313i must be connected to an external MAC, providing a communication path to the switch fabric. In PHY mode, the LAN9313/LAN9313i may be unmanaged, SMI managed, I^2C managed, or SPI managed as detailed in Section 2.3.3, "Management Modes".

When an EEPROM is connected, the EEPROM loader can be used to load the initial device configuration from the external EEPROM via the I^2C/Microwire interface. Once operational, if managed, the CPU can use the I^2C/Microwire interface to read or write the EEPROM.

2.3.3 MANAGEMENT MODES

The LAN9313/LAN9313i provides various modes of management in both MAC and PHY modes of operation. Two separate interfaces may be used to manage the LAN9313/LAN9313i: the I^2C/SPI slave interface or the SMI/MIIM(Media Independent Interface Management) slave interface.

The I^2C/SPI interface runs as either an I^2C slave or SPI slave and is used as a register access path for an external CPU.

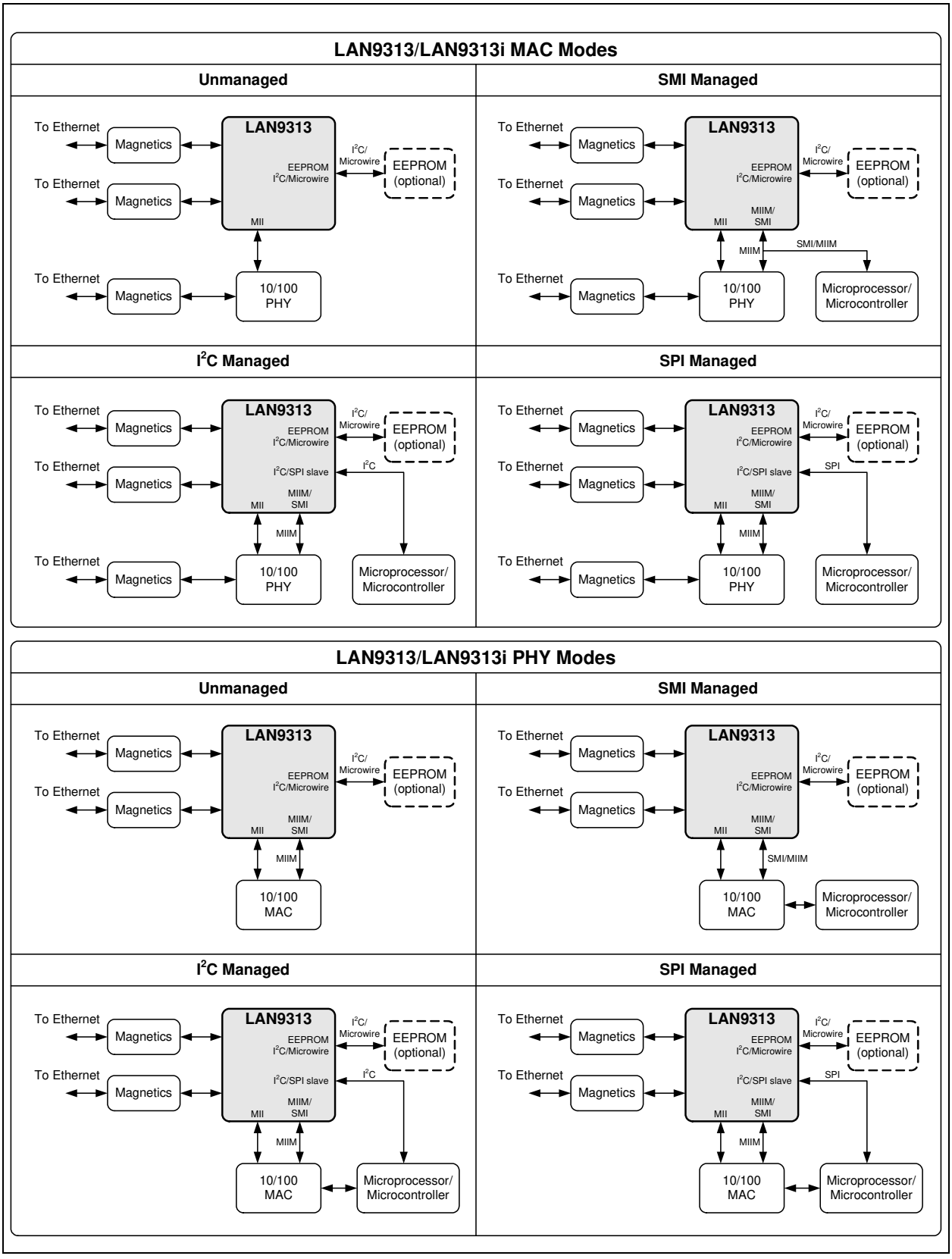
The SMI/MIIM interface runs as either an SMI/MIIM slave or MIIM master. The master mode is used to access an external PHYs registers under CPU control (assuming the CPU is using I^2C or SPI). The slave mode is used for register access by the CPU or external MAC and provides access to either the internal Port 1&2 PHY registers or to all non-PHY registers (using addresses 16-31 and a non-standard extended address map). MIIM and SMI use the same pins and protocol and differ only in that SMI provides access to all internal registers while MIIM provides access to only the Port 1&2 PHY registers. A special mode provides access to the Virtual PHY, which mimics the register operation of a single port standalone PHY. This is used for software compatibility during unmanaged operation.

The selection of LAN9313/LAN9313i modes is determined at startup via the MII_mode_strap and mngt_mode_strap[1:0] configuration straps as detailed in Table 2-1. System configuration diagrams for each mode of the LAN9313/LAN9313i are provided in Figure 2-2.

TABLE 2-1: LAN9313/LAN9313I MODES

Mode	I^2C/Microwire EEPROM Interface	I^2C/SPI Slave Interface	SMI/MIIM Interface	MII_mode_strap Value	MNGT_MODE_STRAP[1:0] Value
MAC Mode Unmanaged	Used to load initial configuration from EEPROM	Not used	Not used	0	00
MAC Mode SMI Managed	Used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	Not used	SMI/MIIM slave, used for CPU access to internal PHYs and non-PHY registers	0	01
MAC Mode I^2C Managed	Used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	I^2C slave	MIIM master, used for CPU access to external PHY registers	0	10
MAC Mode SPI Managed	Used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	SPI slave	MIIM master, used for CPU access to external PHY registers	0	11
PHY Mode Unmanaged	Used to load initial configuration from EEPROM	Not used	Virtual MIIM slave, used for external MAC access to Virtual PHY registers	1	00
PHY Mode SMI Managed	Used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	Not used	SMI/MIIM slave, used for CPU access to internal PHYs, Virtual PHY, and non-PHY registers	1	01
PHY Mode I^2C Managed	Used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	I^2C slave	Virtual MIIM slave, used for external MAC access to Virtual PHY registers	1	10
PHY Mode SPI Managed	Used to load initial configuration from EEPROM and for CPU R/W access to EEPROM	SPI slave	Virtual MIIM slave, used for external MAC access to Virtual PHY registers	1	11

FIGURE 2-2: SYSTEM BLOCK DIAGRAMS - MAC/PHY MODES OF OPERATION

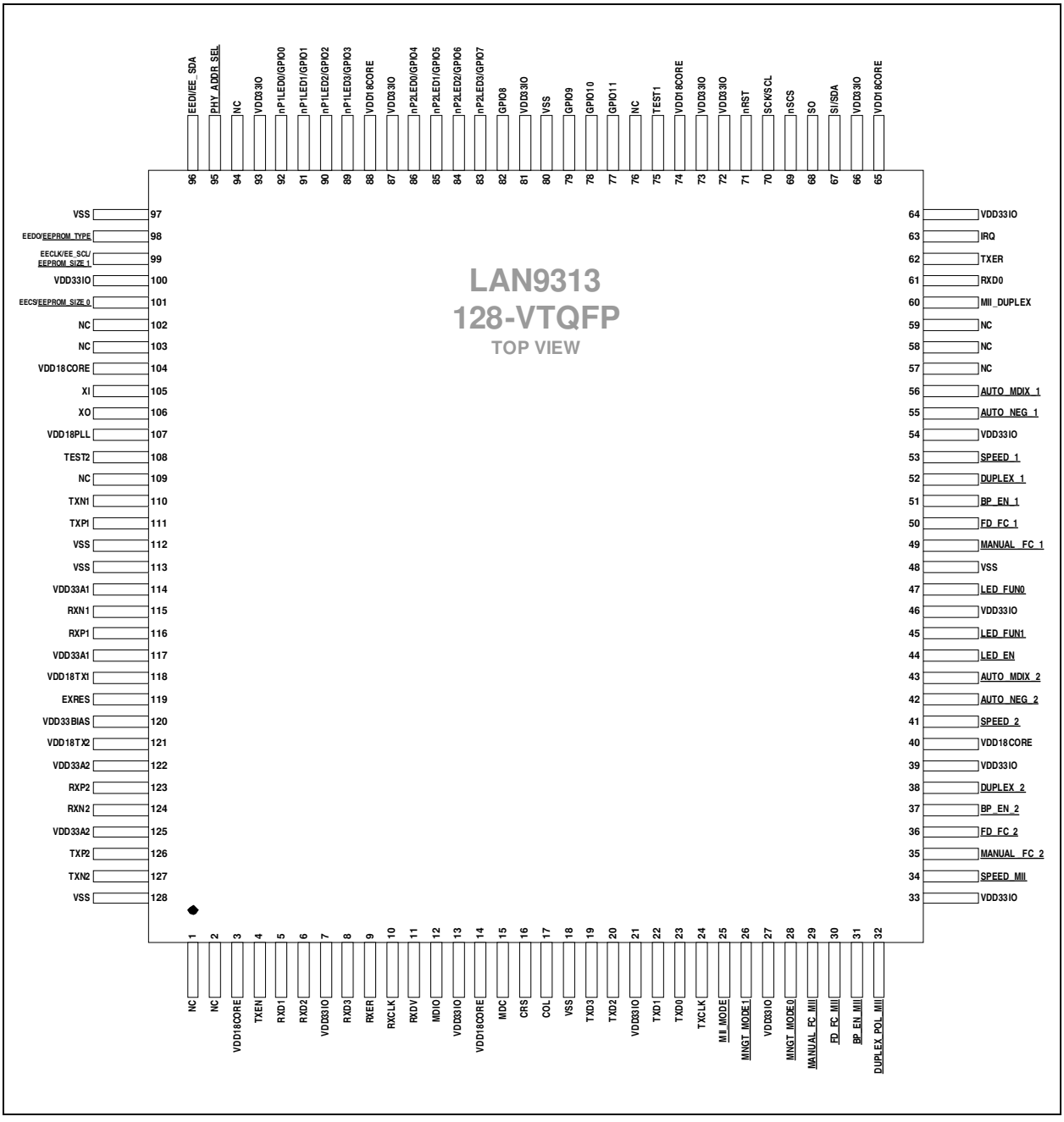


3.0 PIN DESCRIPTION AND CONFIGURATION

3.1 Pin Diagrams

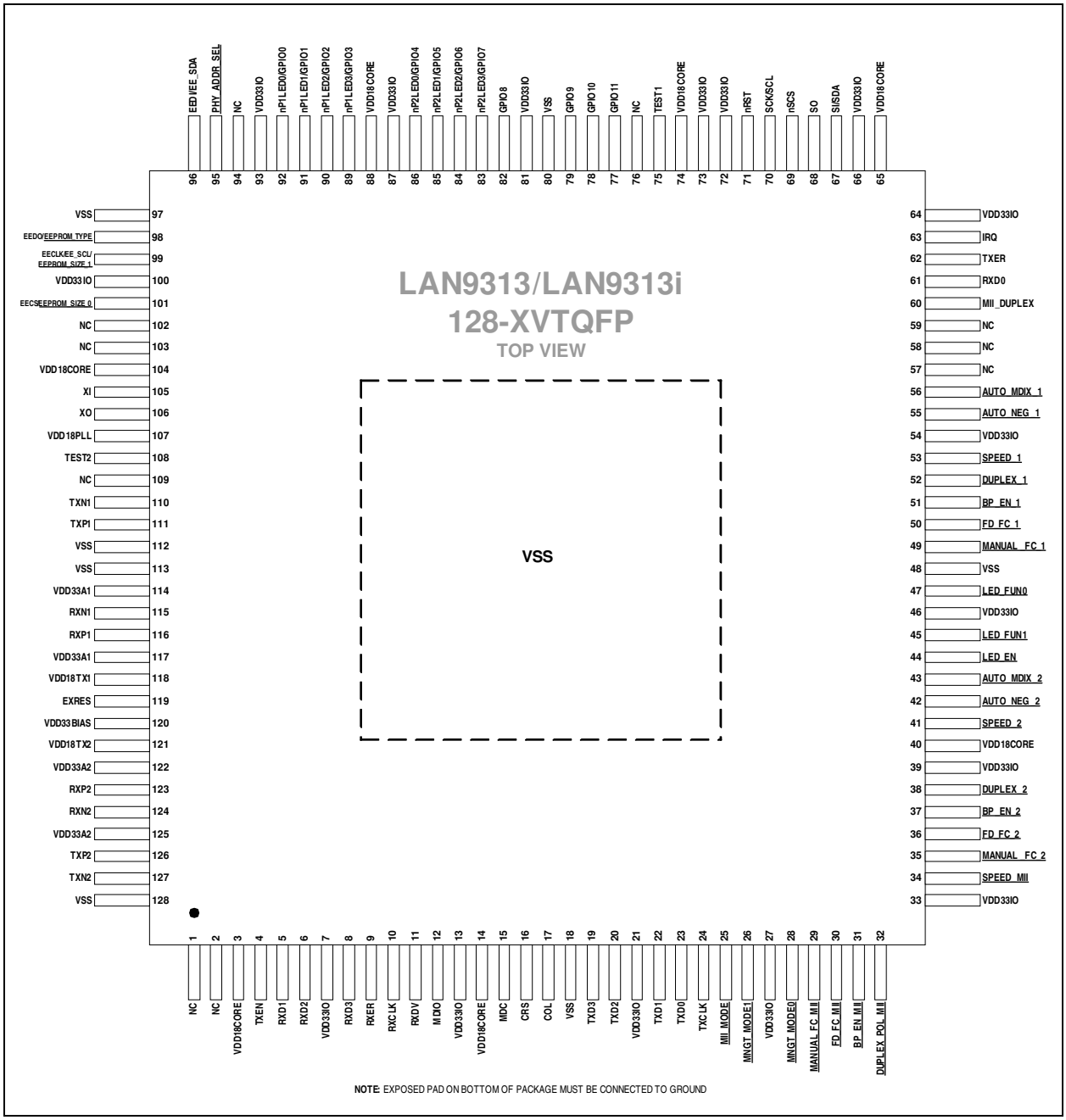
3.1.1 128-VTQFP PIN DIAGRAM

FIGURE 3-1: LAN9313 128-VTQFP PIN ASSIGNMENTS (TOP VIEW)



3.1.2 128-XVTQFP PIN DIAGRAM

FIGURE 3-2: LAN9313/LAN9313I 128-XVTQFP PIN ASSIGNMENTS (TOP VIEW)



NOTE: EXPOSED PAD ON BOTTOM OF PACKAGE MUST BE CONNECTED TO GROUND

3.2 Pin Descriptions

This section contains the descriptions of the LAN9313/LAN9313i pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port 1 Pins
- LAN Port 2 Pins
- LAN Port 1 & 2 Power and Common Pins
- LAN Port 0(External MII) Pins
- Dedicated Configuration Strap Pins
- EEPROM Pins
- Serial Management Pins
- Miscellaneous Pins
- PLL Pins
- Core and I/O Power and Ground Pins
- No-Connect Pins

Note: A list of buffer type definitions is provided in Section 1.2, "Buffer Types," on page 5.

TABLE 3-1: LAN PORT 1 PINS

Pin	Name	Symbol	Buffer Type	Description
89-92	Port 1 LED Indicators	nP1LED[3:0]	OD12	**LED Indicators:** When configured as LED outputs via the LED Configuration Register (LED_CFG), these pins are open-drain, active low outputs and the pull-ups and input buffers are disabled. The functionality of each pin is determined via the LED_CFG[9:8] bits.
	General Purpose I/O Data	GPIO[3:0]	IS/O12/OD12 (PU)	**General Purpose I/O Data:** When configured as GPIO via the LED Configuration Register (LED_CFG), these general purpose signals are fully programmable as either push-pull outputs, open-drain outputs or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The pull-ups are enabled in GPIO mode. The input buffers are disabled when set as an output. **Note:** See Section 12.0, "GPIO/LED Controller," on page 120 for additional details.
110	Port 1 Ethernet TX Negative	TXN1	AIO	**Ethernet TX Negative:** Negative output of Port 1 Ethernet transmitter. See Note 3-1 for additional information.
111	Port 1 Ethernet TX Positive	TXP1	AIO	**Ethernet TX Positive:** Positive output of Port 1 Ethernet transmitter. See Note 3-1 for additional information.
115	Port 1 Ethernet RX Negative	RXN1	AIO	**Ethernet RX Negative:** Negative input of Port 1 Ethernet receiver. See Note 3-1 for additional information.
116	Port 1 Ethernet RX Positive	RXP1	AIO	**Ethernet RX Positive:** Positive input of Port 1 Ethernet receiver. See Note 3-1 for additional information.

Note 3-1 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

TABLE 3-2: LAN PORT 2 PINS

Pin	Name	Symbol	Buffer Type	Description
83-86	Port 2 LED Indicators	nP2LED[3:0]	OD12	**LED indicators:** When configured as LED outputs via the LED Configuration Register (LED_CFG), these pins are open-drain, active low outputs and the pull-ups and input buffers are disabled. The functionality of each pin is determined via the LED_CFG[9:8] bits.
	General Purpose I/O Data	GPIO[7:4]	IS/O12/OD12 (PU)	**General Purpose I/O Data:** When configured as GPIO via the LED Configuration Register (LED_CFG), these general purpose signals are fully programmable as either push-pull outputs, open-drain outputs or Schmitt-triggered inputs by writing the General Purpose I/O Configuration Register (GPIO_CFG) and General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). The pull-ups are enabled in GPIO mode. The input buffers are disabled when set as an output. **Note:** See Section 12.0, "GPIO/LED Controller," on page 120 for additional details.
127	Port 2 Ethernet TX Negative	TXN2	AIO	**Ethernet TX Negative:** Negative output of Port 2 Ethernet transmitter. See Note 3-2 for additional information.
126	Port 2 Ethernet TX Positive	TXP2	AIO	**Ethernet TX Positive:** Positive output of Port 2 Ethernet transmitter. See Note 3-2 for additional information.
124	Port 2 Ethernet RX Negative	RXN2	AIO	**Ethernet RX Negative:** Negative input of Port 2 Ethernet receiver. See Note 3-2 for additional information.
123	Port 2 Ethernet RX Positive	RXP2	AIO	**Ethernet RX Positive:** Positive input of Port 2 Ethernet receiver. See Note 3-2 for additional information.

Note 3-2 The pin names for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

TABLE 3-3: LAN PORT 1 & 2 POWER AND COMMON PINS

Pin	Name	Symbol	Buffer Type	Description
119	Bias Reference	EXRES	AI	**Bias Reference:** Used for internal bias circuits. Connect to an external 12.4K ohm, 1% resistor to ground.
114,117	+3.3V Port 1 Analog Power Supply	VDD33A1	P	**+3.3V Port 1 Analog Power Supply** Refer to the LAN9313/LAN9313i reference schematic for additional connection information.
122,125	+3.3V Port 2 Analog Power Supply	VDD33A2	P	**+3.3V Port 2 Analog Power Supply** Refer to the LAN9313/LAN9313i reference schematic for additional connection information.
120	+3.3V Master Bias Power Supply	VDD33BIAS	P	**+3.3V Master Bias Power Supply** Refer to the LAN9313/LAN9313i reference schematic for additional connection information.

TABLE 3-3: LAN PORT 1 & 2 POWER AND COMMON PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Description
121	Port 2 Transmitter +1.8V Power Supply	VDD18TX2	P	**Port 2 Transmitter +1.8V Power Supply:** This pin is supplied from the internal PHY voltage regulator. This pin must be tied to the VDD18TX1 pin for proper operation. Refer to the LAN9313/LAN9313i reference schematic for additional connection information.
118	Port 1 Transmitter +1.8V Power Supply	VDD18TX1	P	**Port 1 Transmitter +1.8V Power Supply:** This pin must be connected directly to the VDD18TX2 pin for proper operation. Refer to the LAN9313/LAN9313i reference schematic for additional connection information.

TABLE 3-4: LAN PORT 0(EXTERNAL MII) PINS

Pin	Name	Symbol	Buffer Type	Descrption
19,20,22,23	MII Transmit Data	TXD[3:0]	IS/O8 (PD) Note 3-3	**MII Transmit Data:** The functionality of these signals is dependant on the mode of the LAN9313/LAN9313i: • In MAC mode, this is the data from the LAN9313/LAN9313i switch to an external PHY. See Note 3-3. • In PHY mode, this is the data from an external MAC to the LAN9313/LAN9313i switch.
4	MII Transmitter Enable	TXEN	IS/O8 (PD) Note 3-3	**MII Transmit Enable:** Indicates valid data on TXD[3:0]. • In MAC mode, this signal is output to an external PHY. See Note 3-3. • In PHY mode, this signal is input from an external MAC.
9	MII Receive Error	RXER	IS/O8 (PD) Note 3-3	**MII Receive Error:** Indicates a receive error in the packet. • In MAC mode, this signal is input from an external PHY. • In PHY mode, this signal is output to an external MAC. This signal is always driven low when in PHY mode. See Note 3-3.
62	MII Transmit Error	TXER	IS/O8 (PD) Note 3-3	**MII Transmit Error:** Indicates a transmit error in the packet. • In MAC mode, this signal is output to an external PHY and indicates an invalid symbol is to be transmitted. This signal is always driven low when in MAC mode. See Note 3-3. • In PHY mode, this signal is input from an external MAC and indicates the current packet should be aborted.

TABLE 3-4: LAN PORT 0(EXTERNAL MII) PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Descrption
17	MII Collision	COL	IS/O8 (PU) Note 3-4	**MII Collision:** Indicates a collision event. • In MAC mode, this signal is input from an external PHY. • In PHY mode, this signal is output to an external MAC. See Note 3-4.
16	MII carrier Sense	CRS	IS/O8 (PD) Note 3-3	**MII Carrier Sense:** Indicates a network carrier. • In MAC mode, this signal is input from an external PHY. • In PHY mode, this signal is output to an external MAC. See Note 3-3.
24	MII Transmit Clock	TXCLK	IS/O12 (PD) Note 3-3	**MII Transmit Clock:** • In MAC mode, this is the transmitter clock input from an external PHY. • In PHY mode, this is the transmitter clock output to an external MAC. See Note 3-3.
8,6,5,61	MII Receive Data	RXD[3:0]	IS/O8 (PD) Note 3-3	**MII Receive Data:** • In MAC mode, this is the data from an external PHY to the LAN9313/LAN9313i switch. • In PHY mode, this is the data from the LAN9313/LAN9313i switch to an external MAC. See Note 3-3.
11	MII Receive Data Valid	RXDV	IS/O8 (PD) Note 3-3	**MII Receive Data Valid:** Indicates valid data on RXD[3:0]. • In MAC mode, this signal is input from an external PHY. • In PHY mode, this signal is output to an external MAC. See Note 3-3.
10	MII Receive Clock	RXCLK	IS/O12 (PD) Note 3-3	**MII Receive Clock:** • In MAC mode, this is the receiver clock input from an external PHY. • In PHY mode, this is the receiver clock output to an external MAC. See Note 3-3.
12	MII Management Data	MDIO	IS/O8 Note 3-5	**MII Management Data:** • In SMI/MII slave management modes, this signal is the management data to/from an external master. • In MII master management modes, this signal is the management data to/from an external PHY. See Note 3-5

TABLE 3-4: LAN PORT 0(EXTERNAL MII) PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Descrption
15	MII Management Clock	MDC	IS/O8 Note 3-6	**MII Management Clock:** • In SMI/MII slave management modes, this is the management clock input from an external master. • In MII master management modes, this is the management clock output to an external PHY. See Note 3-6.
60	MII Port Duplex	MII_DUPLEX	IS (PU) Note 3-7	**MII Port Duplex:** This pin sets the duplex of the MII port. Its' value can be changed at any time (live value) and can be overridden by disabling the Auto-Negotiation (VPHY_AN) bit in the Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) of the Virtual PHY. In MAC mode, this signal is typically tied to the duplex indication from the external PHY. In PHY mode, this signal is typically tied high or low as needed. The polarity of this signal depends upon the duplex_pol_strap_mii strap. If duplex_pol_strap_mii is 0, a MII_DULPEX value of 0 indicates full duplex, and 1 indicates half duplex. If duplex_pol_strap_mii is 1, a MII_DULPEX value of 1 indicates full duplex, and 0 indicates half duplex.

Note 3-3 When used as an output, the pin(s) input buffer(s) and pull-down(s) are disabled.

Note 3-4 When used as an output, the pin input buffer and pull-up are disabled.

Note 3-5 An external pull-up is required when the SMI or MII management interface is used. This ensures that the IDLE state of the MDIO signal is logic 1. An external pull-up is recommended when the SMI or MII management interface is not used to avoid a floating signal.

Note 3-6 When used as an output, the pin input buffer is disabled. An external pull-down is recommended when the SMI or MII management interface is not used to avoid a floating signal.

Note 3-7 This signal is pulled high through an internal pull-up resistor at all times.

TABLE 3-5: DEDICATED CONFIGURATION STRAP PINS

Pin	Name	Symbol	Buffer Type	Description
44	LED Enable Strap	LED_EN	IS (PU) Note 3-8	**LED Enable Strap:** Configures the default value for the LED_EN bits in the LED Configuration Register (LED_CFG). When latched low, all 8 LED/GPIO pins are configured as GPIOs. When latched high, all 8 LED/GPIO pins are configured as LEDs. See Note 3-9.
45,47	LED Function Strap	LED_FUN[1:0]	IS (PU) Note 3-8	**LED Function Straps:** Configures the default value for the LED_FUN bits in the LED Configuration Register (LED_CFG). When latched low, the corresponding bit will be cleared. When latched high, the corresponding bit will be set. See Note 3-9.
56	Port 1 Auto-MDIX Enable Strap	AUTO_MDIX_1	IS (PU) Note 3-8	**Port 1 Auto-MDIX Enable Strap:** Configures the default value for the Auto-MDIX functionality on Port 1. When latched low, Auto-MDIX is disabled. When latched high, Auto-MDIX is enabled. See Note 3-9.

TABLE 3-5: DEDICATED CONFIGURATION STRAP PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Description
55	Port 1 Auto Negotiation Enable Strap	AUTO_NEG_1	IS (PU) Note 3-8	**Port 1 Auto Negotiation Enable Strap:** Configures the default value for the Auto-Negotiation (PHY_AN) enable bit in the PHY_BASIC_CTRL_1 register (See Section 13.2.2.1). When latched low, auto-negotiation is disabled. When latched high, auto-negotiation is enabled. See Note 3-9.
53	Port 1 Speed Select Strap	SPEED_1	IS (PU) Note 3-8	**Port 1 Speed Select Strap:** Configures the default value for the Speed Select LSB (PHY_SPEED_SEL_LSB) bit in the PHY_BASIC_CTRL_1 register (See Section 13.2.2.1). When latched low, 10 Mbps is selected. When latched high, 100 Mbps is selected. See Note 3-9.
52	Port 1 Duplex Select Strap	DUPLEX_1	IS (PU) Note 3-8	**Port 1 Duplex Select Strap:** Configures the default value for the Duplex Mode (PHY_DUPLEX) bit in the PHY_BASIC_CTRL_1 register (See Section 13.2.2.1). When latched low, half-duplex is selected. When latched high, full-duplex is selected. See Note 3-9.
51	Port 1 Backpressure Enable Strap	BP_EN_1	IS (PU) Note 3-8	**Port 1 Backpressure Enable Strap:** Configures the default value for the Port 1 Backpressure Enable (BP_EN_1) bit of the Port 1 Manual Flow Control Register (MANUAL_FC_1). When latched low, backpressure is disabled. When latched high, backpressure is enabled. See Note 3-9.
50	Port 1 Full-Duplex Flow Control Enable Strap	FD_FC_1	IS (PU) Note 3-8	**Port 1 Full-Duplex Flow Control Enable Strap:** Configures the default value of the Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1) and Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1) bits in the Port 1 Manual Flow Control Register (MANUAL_FC_1), which are used when manual full-duplex control is selected. When latched low, full-duplex Pause packet detection and generation are disabled. When latched high, full-duplex Pause packet detection and generation are enabled. See Note 3-9.
49	Port 1 Manual Flow Control Enable Strap	MANUAL_FC_1	IS (PU) Note 3-8	**Port 1 Manual Flow Control Enable Strap:** Configures the default value of the Port 1 Full-Duplex Manual Flow Control Select (MANUAL_FC_1) bit in the Port 1 Manual Flow Control Register (MANUAL_FC_1). When latched low, flow control is determined by auto-negotiation. When latched high, flow control is determined by the Port 1 Full-Duplex Transmit Flow Control Enable (TX_FC_1) and Port 1 Full-Duplex Receive Flow Control Enable (RX_FC_1) bits. See Note 3-9.
43	Port 2 Auto-MDIX Enable Strap	AUTO_MDIX_2	IS (PU) Note 3-8	**Port 2 Auto-MDIX Enable Strap:** Configures the default value for the Auto-MDIX functionality on Port 2. When latched low, Auto-MDIX is disabled. When latched high, Auto-MDIX is enabled. See Note 3-9.
42	Port 2 Auto Negotiation Enable Strap	AUTO_NEG_2	IS (PU) Note 3-8	**Port 2 Auto Negotiation Enable Strap:** Configures the default value for the Auto-Negotiation (PHY_AN) enable bit in the PHY_BASIC_CTRL_2 register (See Section 13.2.2.1). When latched low, auto-negotiation is disabled. When latched high, auto-negotiation is enabled. See Note 3-9.

TABLE 3-5: DEDICATED CONFIGURATION STRAP PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Description
41	Port 2 Speed Select Strap	SPEED_2	IS (PU) Note 3-8	**Port 2 Speed Select Strap:** Configures the default value for the Speed Select LSB (PHY_SPEED_SEL_LSB) bit in the PHY_BASIC_CTRL_2 register (See Section 13.2.2.1). When latched low, 10 Mbps is selected. When latched high, 100 Mbps is selected. See Note 3-9.
38	Port 2 Duplex Select Strap	DUPLEX_2	IS (PU) Note 3-8	**Port 2 Duplex Select Strap:** Configures the default value for the Duplex Mode (PHY_DUPLEX) bit in the PHY_BASIC_CTRL_2 register (See Section 13.2.2.1). When latched low, half-duplex is selected. When latched high, full-duplex is selected. See Note 3-9.
37	Port 2 Backpressure Enable Strap	BP_EN_2	IS (PU) Note 3-8	**Port 2 Backpressure Enable Strap:** Configures the default value for the Port 2 Backpressure Enable (BP_EN_2) bit of the Port 2 Manual Flow Control Register (MANUAL_FC_2). When latched low, backpressure is disabled. When latched high, backpressure is enabled. See Note 3-9.
36	Port 2 Full-Duplex Flow Control Enable Strap	FD_FC_2	IS (PU) Note 3-8	**Port 2 Full-Duplex Flow Control Enable Strap:** Configures the default value of the Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2) and Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2) bits in the Port 2 Manual Flow Control Register (MANUAL_FC_2), which are used when manual full-duplex control is selected. When latched low, full-duplex Pause packet detection and generation are disabled. When latched high, full-duplex Pause packet detection and generation are enabled. See Note 3-9.
35	Port 2 Manual Flow Control Enable Strap	MANUAL_FC_2	IS (PU) Note 3-8	**Port 2 Manual Flow Control Enable Strap:** Configures the default value of the Port 2 Full-Duplex Manual Flow Control Select (MANUAL_FC_2) bit in the Port 2 Manual Flow Control Register (MANUAL_FC_2). When latched low, flow control is determined by auto-negotiation. When latched high, flow control is determined by the Port 2 Full-Duplex Transmit Flow Control Enable (TX_FC_2) and Port 2 Full-Duplex Receive Flow Control Enable (RX_FC_2) bits. See Note 3-9.
34	Port 0 (External MII) Speed Select Strap	SPEED_MII	IS (PU) Note 3-8	**Port 0(External MII) Speed Select Strap:** Together with the DUPLEX_POL_MII and MII_DUPLEX pins, configures the base ability values in the Virtual PHY Auto-Negotiation Link Partner Base Page Ability Register (VPHY_AN_LP_BASE_ABILITY). This pin also configures the speed for Port 0 when the Virtual Auto-Negotiation fails. When latched low, 10Mbps is selected. When latched high, 100Mbps is selected. Refer to Section 13.1.7.6 and Table 13-6 for more information. See Note 3-9.

TABLE 3-5: DEDICATED CONFIGURATION STRAP PINS (CONTINUED)

Pin	Name	Symbol	Buffer Type	Description
32	Port 0 (External MII) Duplex Polarity Strap	DUPLEX_POL_MII	IS (PU) Note 3-8	**Port 0(External MII) Duplex Polarity Strap:** Configures the polarity of the MII_DUPLEX pin for Port 0. If MII_DUPLEX = DUPLEX_POL_MII, full-duplex is selected. If MII_DUPLEX != DUPLEX_POL_MII, half-duplex is selected. Refer to Section 13.1.7.6 and Table 13-6 for more information. See Note 3-9.
31	Port 0 (External MII) Backpressure Enable Strap	BP_EN_MII	IS (PU) Note 3-8	**Port 0(External MII) Backpressure Enable Strap:** Configures the default value for the Port 0 Backpressure Enable (BP_EN_MII) bit of the Port 0(External MII) Manual Flow Control Register (MANUAL_FC_MII). When latched low, backpressure is disabled. When latched high, backpressure is enabled. See Note 3-9.
30	Port 0 (External MII) Full-Duplex Flow Control Enable Strap	FD_FC_MII	IS (PU) Note 3-8	**Port 0(External MII) Full-Duplex Flow Control Enable Strap**: Configures the default of the TX_FC_MII and RX_FC_MII bits in the Port 0(External MII) Manual Flow Control Register (MANUAL_FC_MII). When latched low, flow control is disabled on RX/TX. When latched high, flow control is enabled on RX/TX. See Note 3-9.
29	Port 0 (External MII) Manual Flow Control Enable Strap	MANUAL_FC_MII	IS (PU) Note 3-8	**Port 0(External MII) Manual Flow Control Enable Strap:** Configures the default value of the MANUAL_FC_MII bit in the Port 0(External MII) Manual Flow Control Register (MANUAL_FC_MII). When latched low, flow control is determined by Virtual Auto-Negotiation. When latched high, flow control is determined by TX_FC_MII and RX_FC_MII bits in the Port 0(External MII) Manual Flow Control Register (MANUAL_FC_MII). See Note 3-9, and Note 3-10.
26,28	Serial Management Mode Strap	MNGT_MODE[1:0]	IS (PU) Note 3-8	**Serial Management Mode Strap:** Configures the serial management mode. **00 = Unmanaged mode** **01 = SMI Managed Mode** **10 = I^2C Managed Mode** **11 = SPI Managed Mode** See Note 3-9.
25	MII Mode Strap	MII_MODE	IS (PU) Note 3-8	**MII Mode Strap:** Configures the mode of the external MII port. **0 = MAC Mode** **1 = PHY Mode** See Note 3-9.

TABLE 3-5: DEDICATED CONFIGURATION STRAP PINS (CONTINUED)

<table>
<tr><th>Pin</th><th>Name</th><th>Symbol</th><th>Buffer Type</th><th>Description</th></tr>
<tr><td>95</td><td>PHY Address Strap</td><td>PHY_ADDR_SEL</td><td>IS (PU) Note 3-8</td><td>PHY Address Strap: Configures the default MII management address values for the PHYs (Virtual, Port 1, and Port 2) as detailed in Section 7.1.1, "PHY Addressing," on page 68.
<table>
<tr><th>PHY_ADDR_SEL VALUE</th><th>VIRTUAL PHY ADDRESS</th><th>PORT 1 PHY ADDRESS</th><th>PORT 2 PHY ADDRESS</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>2</td><td>3</td></tr>
</table>
See Note 3-9.</td></tr>
</table>

Note: For more information on configuration straps, refer to Section 4.2.4, "Configuration Straps," on page 33. Additional strap pins, which share functionality with the EEPROM pins, are described in Table 3-6.

Note 3-8 This signal is pulled high through an internal pull-up resistor at all times.

Note 3-9 Configuration strap values are latched on power-on reset or nRST de-assertion. Configuration strap pins are identified by an underlined symbol name. Some configuration straps can be overridden by values from the EEPROM Loader. Refer to Section 4.2.4, "Configuration Straps," on page 33 for more information.

Note 3-10 In MAC mode, this strap is not used. In this mode, the Virtual PHY is not applicable, and full-duplex flow control must be controlled manually by the host, based upon the external PHYs Auto-negotiation results.

TABLE 3-6: EEPROM PINS

Pin	Name	Symbol	Buffer Type	Description
96	EEPROM Microwire Data Input	EEDI	IS (PD)	**EEPROM Microwire Data Input (EEDI):** In Microwire EEPROM mode (EEPROM_TYPE = 0), this pin is the Microwire EEPROM serial data input.
	EEPROM I^2C Serial Data Input/Output	EE_SDA	IS/OD8	**EEPROM I^2C Serial Data Input/Output (EE_SDA):** In I^2C EEPROM mode (EEPROM_TYPE = 1), this pin is the I^2C EEPROM serial data input/output. **Note:** If I^2C is selected, an external pull-up is required when using an EEPROM and is recommended if no EEPROM is attached.