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LAN9354

3-Port 10/100 Managed Ethernet Switch with Single RMII

Highlights

- High performance 3-port switch with VLAN, QoS packet prioritization, rate limiting, IGMP monitoring and management functions
- Integrated Ethernet PHYs with HP Auto-MDIX
- Compliant with Energy Efficient Ethernet 802.3az
- Wake on LAN (WoL) support
- Integrated IEEE 1588v2 hardware time stamp unit
- Cable diagnostic support
- 1.8V to 3.3V variable voltage I/O
- Integrated 1.2V regulator for single 3.3V operation

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions & video recorders
- VoIP/Video phone systems, home gateways
- Test/Measurement equipment, industrial automation

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM, 512 entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1D spanning tree protocol support
  - 4 separate transmit queues available per port
  - Fixed or weighted egress priority servicing
  - QoS/CoS Packet prioritization
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable Traffic Class map based on input priority on per port basis
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress with coloring and random early discard, per port / priority
    - Programmable rate limiting at the egress with leaky bucket algorithm, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable broadcast storm protection with global % control and enable per port
  - Programmable buffer usage limits
  - Dynamic queues on internal memory
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any port or port pair
  - Fully compliant statistics (MIB) gathering counters
- Ports
  - Port 0: RMII PHY, RMII MAC modes
  - Port 1: Internal PHY
  - Port 2: Internal PHY
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - 100BASE-FX support via external fiber transceiver
  - Full and half duplex support, full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - Programmable interframe gap, flow control pause value
  - Auto-negotiation, polarity correction & MDI/MDI-X
- IEEE 1588v2 hardware time stamp unit
  - Global 64-bit tunable clock
  - Boundary clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Transparent Clock with Ordinary Clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Fully programmable timestamp on TX or RX, timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive power management features
  - 3 power-down levels
  - Wake on link status change (energy detect)
  - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
  - Wakeup indicator event signal
- Power and I/O
  - Integrated power-on reset circuit
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
  - Single 3.3V power supply (integrated 1.2V regulator)
- Additional Features
  - Multifunction GPIOs
  - Ability to use low cost 25MHz crystal for reduced BOM
- Packaging
  - Pb-free RoHS compliant 56-pin QFN
- Available in commercial and industrial temp. ranges

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-T	10 Mbps Ethernet, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE802.3u compliant
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
AN	Auto-Negotiation
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8 bits
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32 bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
LVDS	Low Voltage Differential Signaling
MDI	Medium Dependent Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLD	Multicast Listening Discovery
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8 mA sink and 8 mA source
VOD8	Variable voltage open-drain output with 8 mA sink
VO12	Variable voltage output with 12 mA sink and 12 mA source
VOD12	Variable voltage open-drain output with 12 mA sink
VOS12	Variable voltage open-source output with 12 mA source
VO16	Variable voltage output with 16 mA sink and 16 mA source
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
ILVPECL	Low voltage PECL input pin
OLVPECL	Low voltage PECL output pin
P	Power pin

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

2.0 GENERAL DESCRIPTION

The LAN9354 is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9354 combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and serial management. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hardware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks. The LAN9354 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications. 100BASE-FX is supported via an external fiber transceiver.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9354 provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9354 provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the RMII interface. In PHY mode, the device can be connected to an external MAC via the RMII interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The integrated I^2C and SMI slave controllers allow for full serial management of the device via the integrated I^2C or RMII interface, respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the device into various designs. It is this flexibility which allows the device to operate in 2 different modes and under various management conditions. In both MAC and PHY modes, the device can be SMI managed or I^2C managed. This flexibility in management makes the LAN9354 a candidate for virtually all switch applications.

The LAN9354 supports numerous power management and wakeup features. The LAN9354 can be placed in a reduced power mode and can be programmed to issue an external wake signal (IRQ) via several methods, including “Magic Packet”, “Wake on LAN”, wake on broadcast, wake on perfect DA, and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command or one of the wake events.

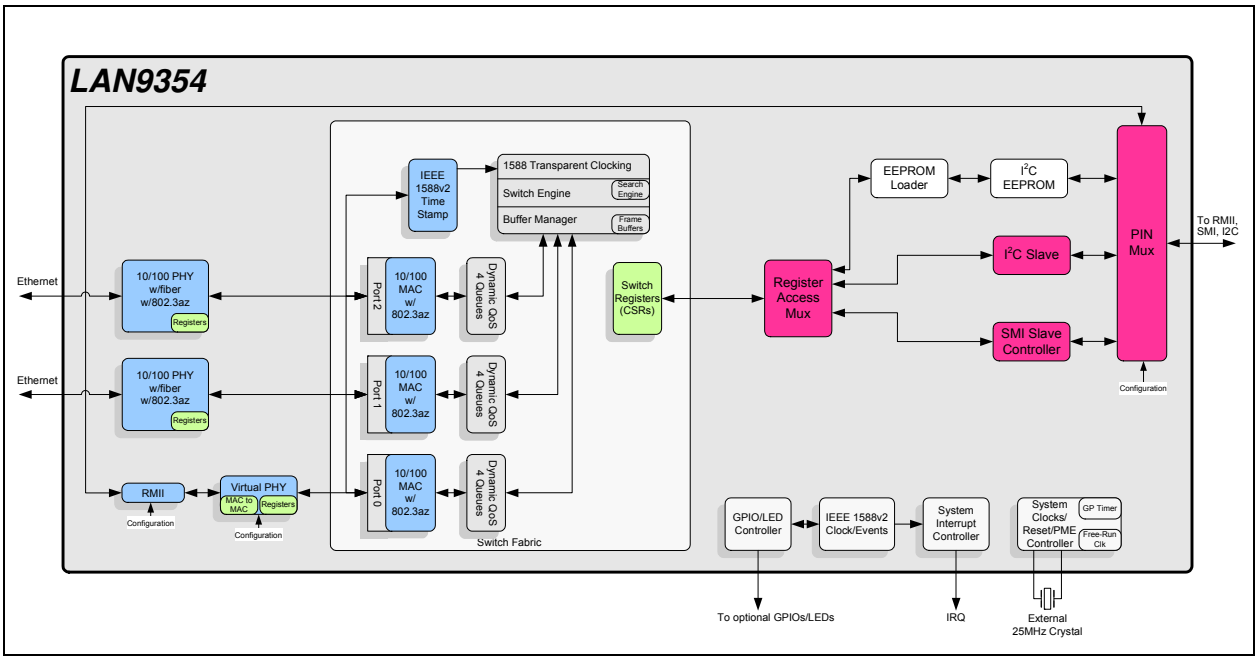
The LAN9354 contains an I^2C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset. The I^2C management slave and master EEPROM controller share common pins.

In addition to the primary functionality described above, the LAN9354 provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and all GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9354 can be configured to operate via a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN9354 is available in commercial and industrial temperature ranges. Figure 2-1 provides an internal block diagram of the LAN9354.

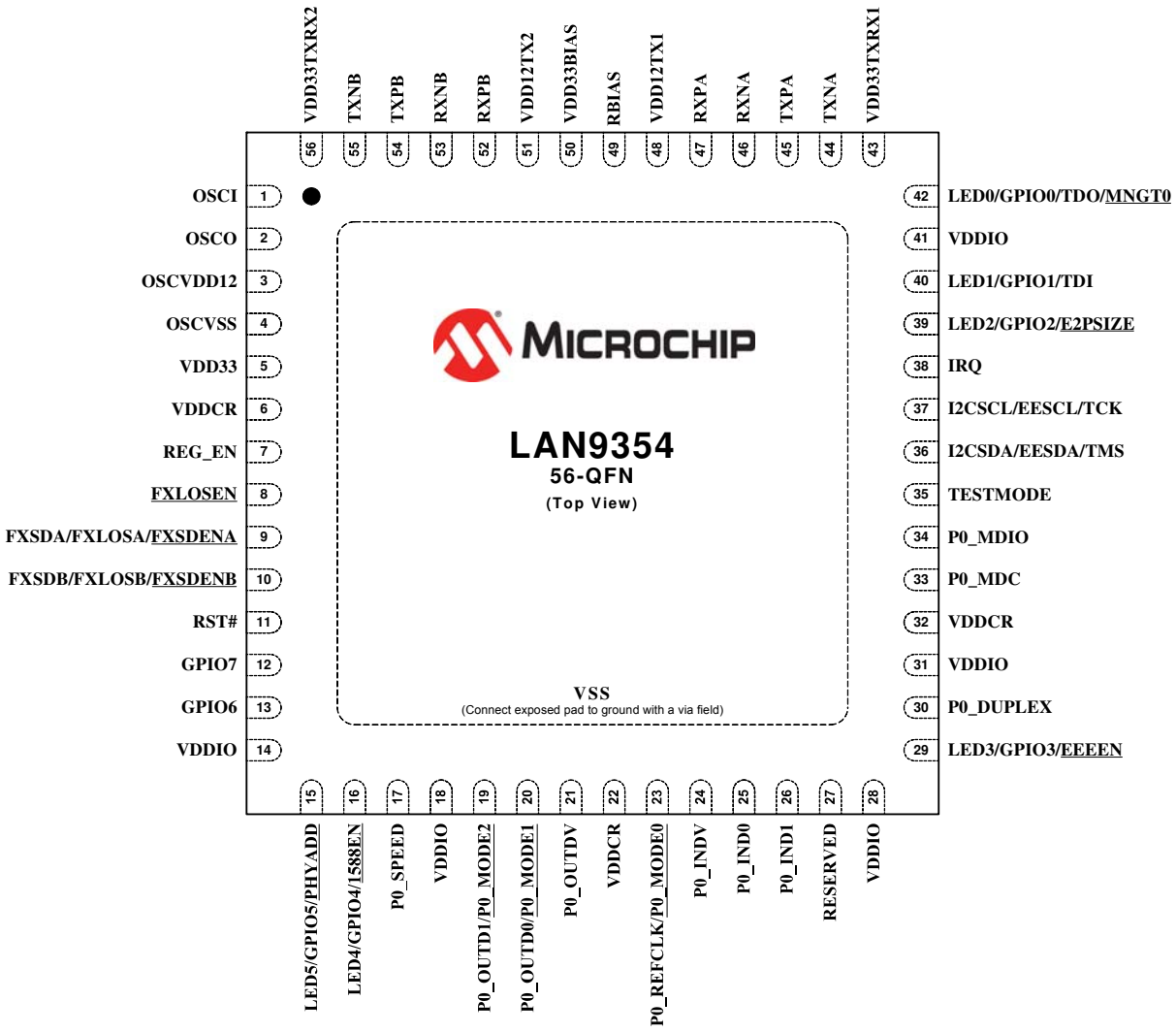
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 56-QFN Pin Assignments

FIGURE 3-1: 56-QFN PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (**VSS**) on bottom of package must be connected to ground with a via field.

Note: When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.2, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-1 details the 56-QFN package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

TABLE 3-1: 56-QFN PACKAGE PIN ASSIGNMENTS

Pin Number	Pin Name
1	OSCI
2	OSCO
3	OSCVDD12
4	OSCVSS
5	VDD33
6	VDDCR
7	REG_EN
8	FXLOSEN
9	FXSDA/FXLOSA/FXSDENA
10	FXSDB/FXLOSB/FXSDENB
11	RST#
12	GPIO7
13	GPIO6
14	VDDIO
15	LED5/GPIO5/PHYADD
16	LED4/GPIO4/1588EN
17	P0_SPEED
18	VDDIO
19	P0_OUTD1/P0_MODE2
20	P0_OUTD0/P0_MODE1
21	P0_OUTDV
22	VDDCR
23	P0_REFCLK/P0_MODE0
24	P0_INDV
25	P0_IND0
26	P0_IND1
27	RESERVED
28	VDDIO
29	LED3/GPIO3/EEEEN
30	P0_DUPLEX
31	VDDIO
32	VDDCR

TABLE 3-1: 56-QFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	Pin Name
33	**P0_MDC**
34	**P0_MDIO**
35	**TESTMODE**
36	**I2CSDA/EESDA/TMS**
37	**I2CSCL/EESCL/TCK**
38	**IRQ**
39	**LED2/GPIO2/E2PSIZE**
40	**LED1/GPIO1/TDI**
41	**VDDIO**
42	**LED0/GPIO0/TDO/MNGT0**
43	**VDD33TXRX1**
44	**TXNA**
45	**TXPA**
46	**RXNA**
47	**RXPA**
48	**VDD12TX1**
49	**RBIAS**
50	**VDD33BIAS**
51	**VDD12TX2**
52	**RXPB**
53	**RXNB**
54	**TXPB**
55	**TXNB**
56	**VDD33TXRX2**
Exposed Pad	**VSS**

3.2 Pin Descriptions

This section contains descriptions of the various LAN9354 pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port A Pin Descriptions
- LAN Port B Pin Descriptions
- LAN Port A & B Power and Common Pin Descriptions
- Switch Port 0 RMII & Configuration Strap Pin Descriptions
- I2C Management Pin Descriptions
- EEPROM Pin Descriptions
- GPIO, LED & Configuration Strap Pin Descriptions
- Miscellaneous Pin Descriptions
- JTAG Pin Descriptions
- Core and I/O Power Pin Descriptions

TABLE 3-2: LAN PORT A PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port A TP TX/RX Positive Channel 1	TXPA	AIO	Port A Twisted Pair Transmit/Receive Positive Channel 1. See Note 1
	Port A FX TX Positive		OLVPECL	Port A Fiber Transmit Positive.
1	Port A TP TX/RX Negative Channel 1	TXNA	AIO	Port A Twisted Pair Transmit/Receive Negative Channel 1. See Note 1.
	Port A FX TX Negative		OLVPECL	Port A Fiber Transmit Negative.
1	Port A TP TX/RX Positive Channel 2	RXPA	AIO	Port A Twisted Pair Transmit/Receive Positive Channel 2. See Note 1.
	Port A FX RX Positive		AI	Port A Fiber Receive Positive.
1	Port A TP TX/RX Negative Channel 2	RXNA	AIO	Port A Twisted Pair Transmit/Receive Negative Channel 2. See Note 1.
	Port A FX RX Negative		AI	Port A Fiber Receive Negative.

TABLE 3-2: LAN PORT A PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port A FX Signal Detect (SD)	**FXSDA**	ILVPECL	Port A Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
	Port A FX Loss Of Signal (LOS)	**FXLOSA**	IS (PU)	Port A Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_1), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
	Port A FX-SD Enable Strap	**FXSDENA**	AI	Port A FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD. When FX-LOS mode is selected, the input buffer is disabled. See Note 2.

Note 1: In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Note 2: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 54 for more information.

Note: Port A is connected to the Switch Fabric port 1.

TABLE 3-3: LAN PORT B PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port B TP TX/RX Positive Channel 1	**TXPB**	AIO	Port B Twisted Pair Transmit/Receive Positive Channel 1. See Note 3
	Port B FX TX Positive		OLVPECL	Port B Fiber Transmit Positive.
1	Port B TP TX/RX Negative Channel 1	**TXNB**	AIO	Port B Twisted Pair Transmit/Receive Negative Channel 1. See Note 3.
	Port B FX TX Negative		OLVPECL	Port B Fiber Transmit Negative.

TABLE 3-3: LAN PORT B PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port BTP TX/RX Positive Channel 2	**RXPB**	AIO	Port B Twisted Pair Transmit/Receive Positive Channel 2. See Note 3.
	Port B FX RX Positive		AI	Port B Fiber Receive Positive.
1	Port B TP TX/RX Negative Channel 2	**RXNB**	AIO	Port B Twisted Pair Transmit/Receive Negative Channel 2. See Note 3.
	Port B FX RX Negative		AI	Port B Fiber Receive Negative.
1	Port B FX Signal Detect (SD)	**FXSDB**	ILVPECL	Port B Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
	Port B FX Loss Of Signal (LOS)	**FXLOSB**	IS (PU)	Port B Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_2), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
	Port B FX-SD Enable Strap	**FXSDENB**	AI	Port B FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD. When FX-LOS mode is selected, the input buffer is disabled. See Note 4.

Note 3: In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Note 4: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 54 for more information.

Note: Port B is connected to Switch Fabric port 2.

TABLE 3-4: LAN PORT A & B POWER AND COMMON PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Bias Reference	**RBIAS**	AI	Used for internal bias circuits. Connect to an external 12.1 kΩ, 1% resistor to ground. Refer to the device reference schematic for connection information. **Note:** The nominal voltage is 1.2 V and the resistor will dissipate approximately 1 mW of power.
1	Port A and B FX-LOS Enable Strap	**FXLOSEN**	AI	Port A and B FX-LOS Enable. This 3 level strap input selects between FX-LOS and FX-SD / copper twisted pair mode. A level below 1 V (typ.) selects FX-SD / copper twisted pair for ports A and B, further determined by FXSDENA and FXSDENB. A level of 1.5 V selects FX-LOS for port A and FX-SD / copper twisted pair for port B, further determined by FXSDENB. A level above 2 V (typ.) selects FX-LOS for ports A and B.
1	+3.3 V Port A Analog Power Supply	**VDD33TXRX1**	P	See Note 5.
1	+3.3 V Port B Analog Power Supply	**VDD33TXRX2**	P	See Note 5.
1	+3.3 V Master Bias Power Supply	**VDD33BIAS**	P	See Note 5.
1	Port A Transmitter +1.2 V Power Supply	**VDD12TX1**	P	This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX2** pin for proper operation. See Note 5.
1	Port B Transmitter +1.2 V Power Supply	**VDD12TX2**	P	This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX1** pin for proper operation. See Note 5.

Note 5: Refer to Section 4.0, "Power Connections," on page 26, the device reference schematics, and the device LANCheck schematic checklist for additional connection information.

TABLE 3-5: SWITCH PORT 0 RMII & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 RMII Input Data 1	**P0_IND1**	VIS (PD)	**RMII MAC Mode:** This pin is the receive data 1 bit from the external PHY to the switch.
			VIS (PD)	**RMII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
1	Port 0 RMII Input Data 0	**P0_IND0**	VIS (PD)	**RMII MAC Mode:** This pin is the receive data 0 bit from the external PHY to the switch.
			VIS (PD)	**RMII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
1	Port 0 RMII Input Data Valid	**P0_INDV**	VIS (PD)	**RMII MAC Mode:** This pin is the CRS_DV signal from the external PHY.
			VIS (PD)	**RMII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on **P0_IND[1:0]**. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
1	Port 0 RMII Output Data 1	**P0_OUTD1**	VO8	**RMII MAC Mode:** This pin is the transmit data 1 bit from the switch to the external PHY.
			VO8	**RMII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
	Port 0 Mode[2] Configuration Strap	**P0_MODE2**	VIS (PU) Note 8	This strap configures the mode for Port 0. See Note 7. Refer to Table 7-3, “Port 0 Mode Strap Mapping,” on page 66 for the Port 0 strap settings.
1	Port 0 RMII Output Data 0	**P0_OUTD0**	VO8	**RMII MAC Mode:** This pin is the transmit data 0 bit from the switch to the external PHY.
			VO8	**RMII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
	Port 0 Mode[1] Configuration Strap	**P0_MODE1**	VIS (PU) Note 8	This strap configures the mode for Port 0. See Note 7. Refer to Table 7-3, “Port 0 Mode Strap Mapping,” on page 66 for the Port 0 strap settings.

TABLE 3-5: SWITCH PORT 0 RMII & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 RMII Output Data Valid	P0_OUTDV	VO8	**RMII MAC Mode:** This pin is the TX_EN signal to the external PHY.
			VO8	**RMII PHY Mode:** This pin is the CRS_DV signal to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
1	Port 0 Speed	P0_SPEED	VIS (PU)	**RMII MAC Mode:** This pin can be changed at any time (live value) and is typically tied to the speed indication from the external PHY. It can be overridden by the Speed Select LSB (VPHY_SPEED_SEL_LSB) bit in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) by clearing the Auto-Negotiation (VPHY_AN) bit in the same register. The polarity of this pin is determined by the speed_pol_strap_0.
			-	**RMII PHY Mode:** This pin is not used.
1	Port 0 RMII Duplex	P0_DUPLEX	VIS (PU)	**RMII MAC Mode:** This pin can be changed at any time (live value) and is typically tied to the duplex indication from the external PHY. It can be overridden by the Duplex Mode (VPHY_DUPLEX) bit in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL) by clearing the Auto-Negotiation (VPHY_AN) bit in the same register. The polarity of this pin is determined by the duplex_pol_strap_0.
			-	**RMII PHY Mode:** This pin is not used.

TABLE 3-5: SWITCH PORT 0 RMII & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 RMII Reference Clock	**P0_REFCLK**	VIS/ VO12/ VO16 (PD) Note 6	**RMII MAC Mode:** This pin is an input or an output running at 50 MHz and is used as the reference clock for the **P0_IND[1:0]**, **P0_INDV**, **P0_OUTD[1:0]**, and **P0_OUTDV** pins. The choice of input verses output is based on the setting of the RMII Clock Direction bit in the Port 0 Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects **P0_OUTCLK** as an input and a high selects **P0_OUTCLK** as an output. As an input, the pull-down is enabled by default. As an output, the input buffer and pull-down are disabled. The choice of drive strength is based on the MII Virtual PHY RMII Clock Strength bit. A low selects a 12 mA drive, while a high selects a 16 mA drive.
			VIS/ VO12/ VO16 (PD) Note 6	**RMII PHY Mode:** This pin is an input or an output running at 50 MHz and is used as the reference clock for the **P0_IND[1:0]**, **P0_INDV**, **P0_OUTD[1:0]**, and **P0_OUTDV** pins. The choice of input verses output is based on the setting of the RMII Clock Direction bit in the Port 0 Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS). A low selects **P0_OUTCLK** as an input and a high selects **P0_OUTCLK** as an output. As an input, the pull-down is normally enabled. The input buffer and pull-down are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL). As an output, the input buffer and pull-down are disabled. The choice of drive strength is based on the MII Virtual PHY RMII Clock Strength bit. A low selects a 12 mA drive, while a high selects a 16 mA drive. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Virtual PHY Basic Control Register (VPHY_BASIC_CTRL).
	Port 0 Mode[0] Configuration Strap	**P0_MODE0**	VIS (PU) Note 8	This strap configures the mode for Port 0. See Note 7. Refer to Table 7-3, “Port 0 Mode Strap Mapping,” on page 66 for the Port 0 strap settings.

TABLE 3-5: SWITCH PORT 0 RMII & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 SMI/MII Management Data Input/Output	**P0_MDIO**	VIS/VO8	**SMI/MII Slave Management Modes:** This is the management data to/from an external master and is used to access port 0's Virtual PHY, the two physical PHYs and internal registers. **MII Master Management Modes:** This is the management data to/from an external PHY(s). **Note:** An external pull-up is required when the SMI or MII management interface is used, to ensure that the IDLE state of the MDIO signal is a logic one. **Note:** An external pull-up is recommended when the SMI or MII management interface is not used, to avoid a floating signal.
1	Port 0 SMI/MII Management Clock	**P0_MDC**	VIS	**SMI/MII Slave Management Modes:** This is the management clock input from an external master and is used to access port 0's Virtual PHY, the two physical PHYs and internal registers. **Note:** When SMI or MII is not used, an external pull-down is recommended to avoid a floating signal.
			VO8	**MII Master Management Modes:** This is the management clock output to an external PHY(s).

Note 6: A series terminating resistor is recommended for the best PCB signal integrity.

Note 7: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 54 for more information.

Note 8: An external supplemental pull-up may be needed, depending upon the input current loading of the external MAC/PHY device.

TABLE 3-6: I^2C MANAGEMENT PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	I^2C Slave Serial Data Input/Output	**I2CSDA**	VIS/VOD8	This pin is the I^2C serial data input/output from/to the external master **Note:** This pin must be pulled-up by an external resistor at all times.
1	I^2C Slave Serial Clock	**I2CSCL**	VIS	This pin is the I^2C clock input from the external master. **Note:** These signals are not driven (high impedance) until the EEPROM is loaded.

TABLE 3-7: EEPROM PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	EEPROM I^2C Serial Data Input/Output	**EESDA**	VIS/VOD8	When the device is accessing an external EEPROM this pin is the I^2C serial data input/open-drain output. **Note:** This pin must be pulled-up by an external resistor at all times.
1	EEPROM I^2C Serial Clock	**EESCL**	VIS/VOD8	When the device is accessing an external EEPROM this pin is the I^2C clock input/open-drain output. **Note:** This pin must be pulled-up by an external resistor at all times.

TABLE 3-8: GPIO, LED & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	General Purpose I/O 7	**GPIO7**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
1	General Purpose I/O 6	**GPIO6**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
1	LED 5	**LED5**	VO12/ VOD12/ VOS12	This pin is configured to operate as an LED when the LED 5 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **PHYADD** strap value sampled at reset. **Note:** Refer to Section 17.3, "LED Operation," on page 452 to additional information.
	General Purpose I/O 5	**GPIO5**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO when the LED 5 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	PHY Address Configuration Strap	**PHYADD**	VIS (PU)	This strap configures the default value of the Switch PHY Address Select soft-strap. See Note 9.

TABLE 3-8: GPIO, LED & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	LED 4	**LED4**	VO12/ VOD12/ VOS12	This pin is configured to operate as an LED when the LED 4 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **1588EN** strap value sampled at reset. **Note:** Refer to Section 17.3, "LED Operation," on page 452 to additional information.
	General Purpose I/O 4	**GPIO4**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO when the LED 4 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	1588 Enable Configuration Strap	**1588EN**	VIS (PU)	This strap configures the default value of the 1588 Enable soft-strap. See Note 9.
1	LED 3	**LED3**	VO12/ VOD12/ VOS12	This pin is configured to operate as an LED when the LED 3 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **EEEEN** strap value sampled at reset. **Note:** Refer to Section 17.3, "LED Operation," on page 452 to additional information.
	General Purpose I/O 3	**GPIO3**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO when the LED 3 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	Energy Efficient Ethernet Enable Configuration Strap	**EEEEN**	VIS (PU)	This strap configures the default value of the EEE Enable 2-1 soft-straps. See Note 9.

TABLE 3-8: GPIO, LED & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	LED 2	**LED2**	VO12/ VOD12/ VOS12	This pin is configured to operate as an LED when the LED 2 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **E2PSIZE** strap value sampled at reset. **Note:** Refer to Section 17.3, "LED Operation," on page 452 to additional information.
	General Purpose I/O 2	**GPIO2**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO when the LED 2 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	EEPROM Size Configuration Strap	**E2PSIZE**	VIS (PU)	This strap configures the value of the EEPROM size hard-strap. See Note 9. A low selects 1K bits (128 x 8) through 16K bits (2K x 8). A high selects 32K bits (4K x 8) through 512K bits (64K x 8).
1	LED 1	**LED1**	VO12/ VOD12/ VOS12	This pin is configured to operate as an LED when the LED 1 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. **Note:** Refer to Section 17.3, "LED Operation," on page 452 to additional information.
	General Purpose I/O 1	**GPIO1**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO when the LED 1 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).

TABLE 3-8: GPIO, LED & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	LED 0	**LED0**	VO12/ VOD12/ VOS12	This pin is configured to operate as an LED when the LED 0 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **MNGT0** strap value sampled at reset. **Note:** Refer to Section 17.3, "LED Operation," on page 452 to additional information.
	General Purpose I/O 0	**GPIO0**	VIS/VO12/ VOD12 (PU)	This pin is configured to operate as a GPIO when the LED 0 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR).
	Host Interface Configuration Strap 0	**MNGT0**	VIS (PU)	This strap configures the value of the Serial Management Mode hard-strap.

Note 9: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 54 for more information.

TABLE 3-9: MISCELLANEOUS PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Interrupt Output	**IRQ**	VO8/VOD8	Interrupt request output. The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). For more information, refer to Section 8.0, "System Interrupts," on page 67.
1	System Reset Input	**RST#**	VIS (PU)	As an input, this active low signal allows external hardware to reset the device. The device also contains an internal power-on reset circuit. Thus this signal may be left unconnected if an external hardware reset is not needed. When used this signal must adhere to the reset timing requirements as detailed in the Section 20.0, "Operational Characteristics," on page 467.
1	Regulator Enable	**REG_EN**	AI	When tied to 3.3 V, the internal 1.2 V regulators are enabled.
1	Test Mode	**TESTMODE**	VIS (PD)	This pin must be tied to **VSS** for proper operation.
1	Crystal Input	**OSCI**	ICLK	External 25 MHz crystal input. This signal can also be driven by a single-ended clock oscillator. When this method is used, **OSCO** should be left unconnected.

TABLE 3-9: MISCELLANEOUS PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Crystal Output	**OSCO**	OCLK	External 25 MHz crystal output.
1	Crystal +1.2 V Power Supply	**OSCVDD12**	P	Supplied by the on-chip regulator unless configured for regulator off mode via **REG_EN**.
1	Crystal Ground	**OSCVSS**	P	Crystal ground.
1	Reserved	**RESERVED**	-	This pin is reserved and must be left unconnected for proper operation.

TABLE 3-10: JTAG PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	JTAG Test Mux Select	**TMS**	VIS	JTAG test mode select
1	JTAG Test Clock	**TCK**	VIS	JTAG test clock
1	JTAG Test Data Input	**TDI**	VIS	JTAG data input
1	JTAG Test Data Output	**TDO**	VO12	JTAG data output

TABLE 3-11: CORE AND I/O POWER PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Regulator +3.3 V Power Supply	**VDD33**	P	+3.3 V power supply for internal regulators. See Note 10. **Note:** +3.3 V must be supplied to this pin even if the internal regulators are disabled.
5	+1.8 V to +3.3 V Variable I/O Power	**VDDIO**	P	+1.8 V to +3.3 V variable I/O power. See Note 10.
3	+1.2 V Digital Core Power Supply	**VDDCR**	P	Supplied by the on-chip regulator unless configured for regulator off mode via REG_EN. 1 µF and 470 pF decoupling capacitors in parallel to ground should be used on pin 6. See Note 10.
1 pad	Ground	**VSS**	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

Note 10: Refer to Section 4.0, "Power Connections," on page 26, the device reference schematic, and the device LANCheck schematic checklist for additional connection information.