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LAN9355

3-Port 10/100 Managed Ethernet Switch with Dual MII/RMII/Turbo MII

Highlights

- High performance 3-port switch with VLAN, QoS packet prioritization, rate limiting, IGMP monitoring and management functions
- Interfaces at up to 200Mbps via Turbo MII
- Integrated Ethernet PHYs with HP Auto-MDIX
- Compliant with Energy Efficient Ethernet 802.3az
- Wake on LAN (WoL) support
- Integrated IEEE 1588v2 hardware time stamp unit
- Cable diagnostic support
- 1.8V to 3.3V variable voltage I/O
- Integrated 1.2V regulator for single 3.3V operation

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions & video recorders
- VoIP/Video phone systems, home gateways
- Test/Measurement equipment, industrial automation

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM, 512 entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1D spanning tree protocol support
  - 4 separate transmit queues available per port
  - Fixed or weighted egress priority servicing
  - QoS/CoS Packet prioritization
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable Traffic Class map based on input priority on per port basis
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress with coloring and random early discard, per port / priority
    - Programmable rate limiting at the egress with leaky bucket algorithm, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable broadcast storm protection with global % control and enable per port
  - Programmable buffer usage limits
  - Dynamic queues on internal memory
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any port or port pair
  - Fully compliant statistics (MIB) gathering counters
- Ports
  - Port 0: MII MAC, MII PHY, RMII PHY, RMII MAC modes
  - Port 1: Internal PHY, MII MAC, MII PHY, RMII MAC, RMII PHY modes
  - Port 2: Internal PHY
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - 200Mbps Turbo MII (PHY or MAC mode)
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - 100BASE-FX support via external fiber transceiver
  - Full and half duplex support, full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - Programmable interframe gap, flow control pause value
  - Auto-negotiation, polarity correction & MDI/MDI-X
- IEEE 1588v2 hardware time stamp unit
  - Global 64-bit tunable clock
  - Boundary clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Transparent Clock with Ordinary Clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Fully programmable timestamp on TX or RX, timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive power management features
  - 3 power-down levels
  - Wake on link status change (energy detect)
  - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
  - Wakeup indicator event signal
- Power and I/O
  - Integrated power-on reset circuit
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
  - Single 3.3V power supply (integrated 1.2V regulator)
- Additional Features
  - Multifunction GPIOs
  - Ability to use low cost 25MHz crystal for reduced BOM
- Packaging
  - Pb-free RoHS compliant 88-pin QFN or 80-pin TQFP-EP
- Available in commercial and industrial temp. ranges

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-T	10 Mbps Ethernet, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE802.3u compliant
ADC	Analog-to-Digital Converter
ALR	Address Logic Resolution
AN	Auto-Negotiation
BLW	Baseline Wander
BM	Buffer Manager - Part of the switch fabric
BPDU	Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information
Byte	8 bits
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32 bits
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FIFO	First In First Out buffer
FSM	Finite State Machine
GPIO	General Purpose I/O
Host	External system (Includes processor, application software, etc.)
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writing a zero.
lsb	Least Significant Bit
LSB	Least Significant Byte
LVDS	Low Voltage Differential Signaling
MDI	Medium Dependent Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLD	Multicast Listening Discovery
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PTP	Precision Time Protocol
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RTC	Real-Time Clock
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SQE	Signal Quality Error (also known as “heartbeat”)
SSD	Start of Stream Delimiter
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8 mA sink and 8 mA source
VOD8	Variable voltage open-drain output with 8 mA sink
VO12	Variable voltage output with 12 mA sink and 12 mA source
VOD12	Variable voltage open-drain output with 12 mA sink
VOS12	Variable voltage open-source output with 12 mA source
VO16	Variable voltage output with 16 mA sink and 16 mA source
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
ILVPECL	Low voltage PECL input pin
OLVPECL	Low voltage PECL output pin
P	Power pin

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Read:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

2.0 GENERAL DESCRIPTION

The LAN9355 is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9355 combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and serial management. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hardware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks. The LAN9355 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications. 100BASE-FX is supported via an external fiber transceiver.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9355 provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9355 provides 2 on-chip PHYs, 2 Virtual PHYs and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the MII/RMII/Turbo MII interface. In PHY mode, the device can be connected to an external MAC via the MII/RMII/Turbo MII interface. Optionally, the internal PHY on Port 1 can be disabled and the associated Switch Fabric port operated in the MII/Turbo MII PHY, RMII PHY, MII/Turbo MII MAC, or RMII MAC modes. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The integrated I^2C and SMI slave controllers allow for full serial management of the device via the integrated I^2C or MII interface, respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the device into various designs. It is this flexibility which allows the device to operate in 2 different modes and under various management conditions. In both MAC and PHY modes, the device can be SMI managed or I^2C managed. This flexibility in management makes the LAN9355 a candidate for virtually all switch applications.

The LAN9355 supports numerous power management and wakeup features. The LAN9355 can be placed in a reduced power mode and can be programmed to issue an external wake signal (IRQ) via several methods, including “Magic Packet”, “Wake on LAN”, wake on broadcast, wake on perfect DA, and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command or one of the wake events.

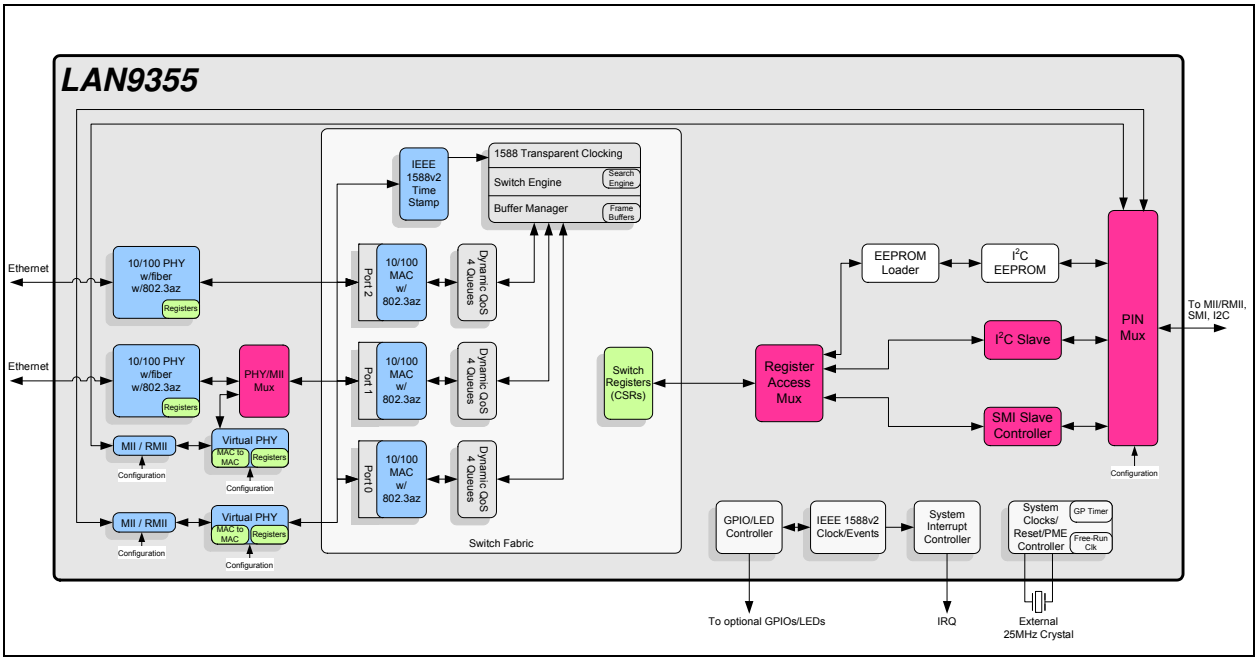
The LAN9355 contains an I^2C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset. The I^2C management slave and master EEPROM controller share common pins.

In addition to the primary functionality described above, the LAN9355 provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and all GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9355 can be configured to operate via a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN9355 is available in commercial and industrial temperature ranges. Figure 2-1 provides an internal block diagram of the LAN9355.

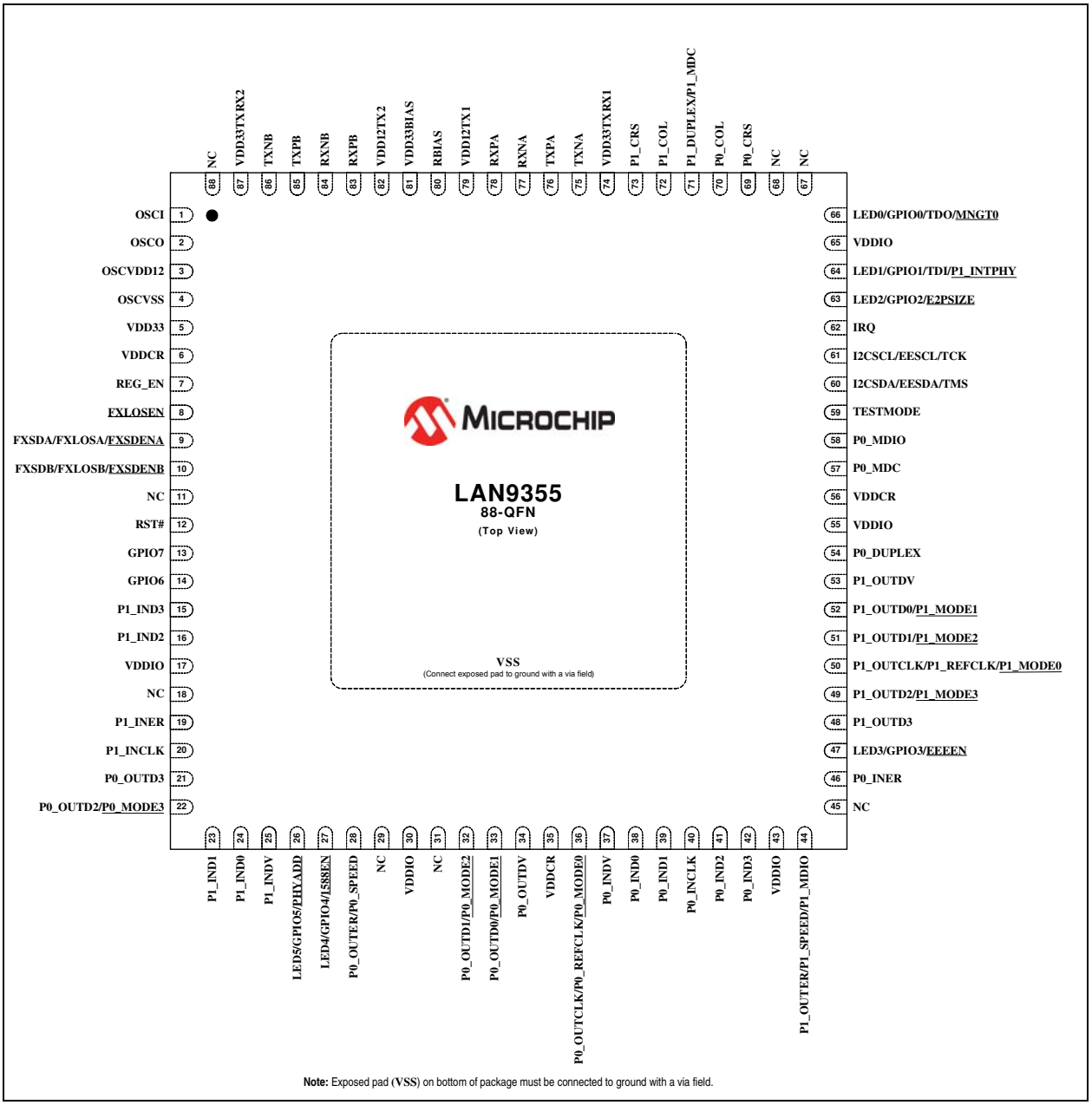
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 88-QFN Pin Assignments

FIGURE 3-1: 88-QFN PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (**VSS**) on bottom of package must be connected to ground with a via field.

Note: When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-1 details the 88-QFN package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

TABLE 3-1: 88-QFN PACKAGE PIN ASSIGNMENTS

Pin Number	Pin Name
1	OSCI
2	OSCO
3	OSCVDD12
4	OSCVSS
5	VDD33
6	VDDCR
7	REG_EN
8	FXLOSEN
9	FXSDA/FXLOSA/FXSDENA
10	FXSDB/FXLOSB/FXSDENB
11	NC
12	RST#
13	GPIO7
14	GPIO6
15	P1_IND3
16	P1_IND2
17	VDDIO
18	NC
19	P1_INER
20	P1_INCLK
21	P0_OUTD3
22	P0_OUTD2/P0_MODE3
23	P1_IND1
24	P1_IND0
25	P1_INDV
26	LED5/GPIO5/PHYADD
27	LED4/GPIO4/1588EN
28	P0_OUTER/P0_SPEED
29	NC
30	VDDIO
31	NC
32	P0_OUTD1/P0_MODE2

TABLE 3-1: 88-QFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

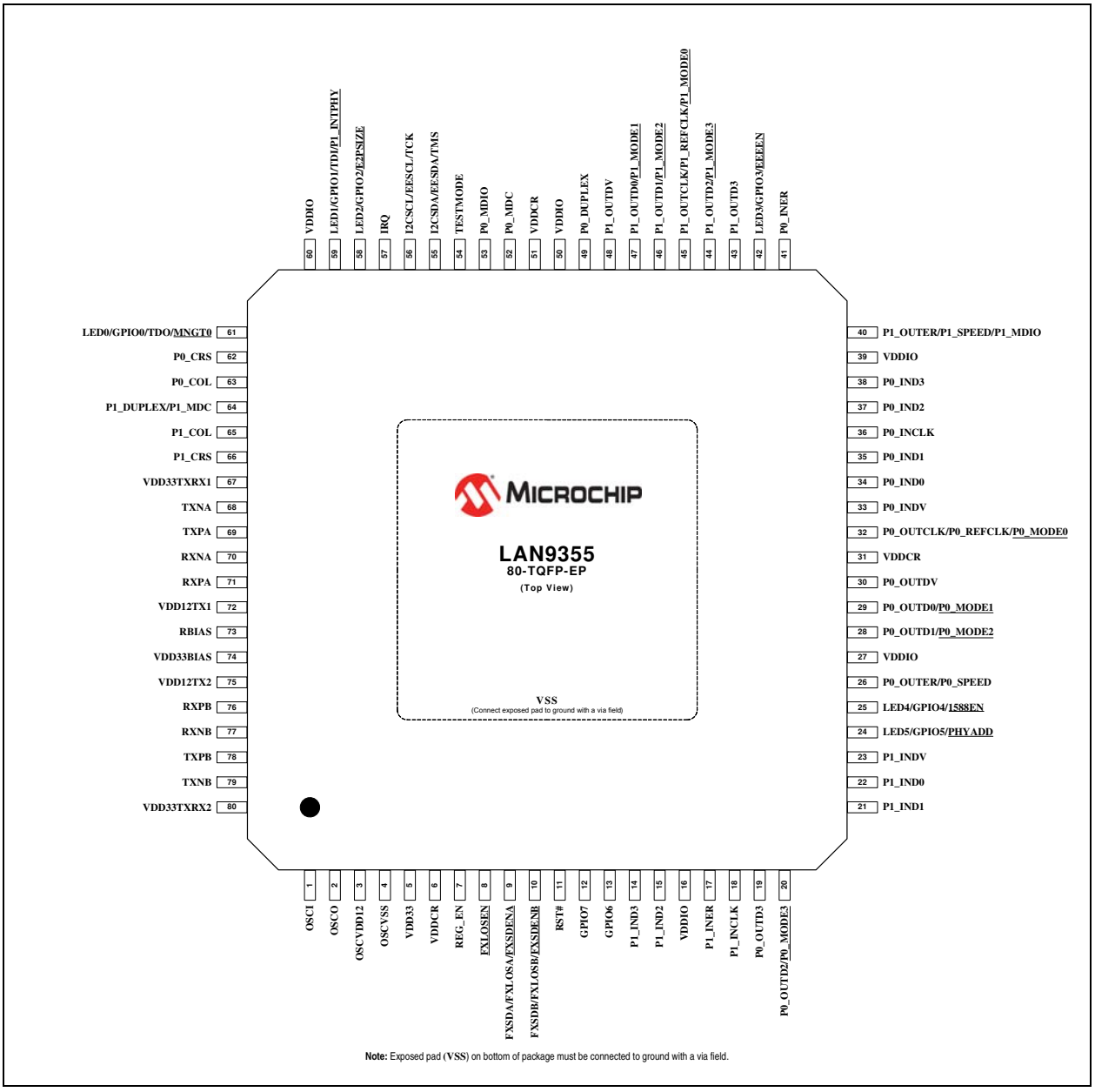
Pin Number	Pin Name
33	P0_OUTD0/P0_MODE1
34	P0_OUTDV
35	VDDCR
36	P0_OUTCLK/P0_REFCLK/P0_MODE0
37	P0_INDV
38	P0_IND0
39	P0_IND1
40	P0_INCLK
41	P0_IND2
42	P0_IND3
43	VDDIO
44	P1_OUTER/P1_SPEED/P1_MDIO
45	NC
46	P0_INER
47	LED3/GPIO3/EEEEN
48	P1_OUTD3
49	P1_OUTD2/P1_MODE3
50	P1_OUTCLK/P1_REFCLK/P1_MODE0
51	P1_OUTD1/P1_MODE2
52	P1_OUTD0/P1_MODE1
53	P1_OUTDV
54	P0_DUPLEX
55	VDDIO
56	VDDCR
57	P0_MDC
58	P0_MDIO
59	TESTMODE
60	I2CSDA/EESDA/TMS
61	I2CSCL/EESCL/TCK
62	IRQ
63	LED2/GPIO2/E2PSIZE
64	LED1/GPIO1/TDI/P1_INTPHY
65	VDDIO
66	LED0/GPIO0/TDO/MNGT0
67	NC

TABLE 3-1: 88-QFN PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	Pin Name
68	NC
69	P0_CRS
70	P0_COL
71	P1_DUPLEX/P1_MDC
72	P1_COL
73	P1_CRS
74	VDD33TXRX1
75	TXNA
76	TXPA
77	RXNA
78	RXPA
79	VDD12TX1
80	RBIAS
81	VDD33BIAS
82	VDD12TX2
83	RXPB
84	RXNB
85	TXPB
86	TXNB
87	VDD33TXRX2
88	NC
Exposed Pad	VSS

3.2 80-TQFP-EP Pin Assignments

FIGURE 3-2: 80-TQFP-EP PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Note: When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-2 details the 80-TQFP-EP package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

TABLE 3-2: 80-TQFP-EP PACKAGE PIN ASSIGNMENTS

Pin Number	Pin Name
1	OSCI
2	OSCO
3	OSCVDD12
4	OSCVSS
5	VDD33
6	VDDCR
7	REG_EN
8	FXLOSEN
9	FXSDA/FXLOSA/FXSDENA
10	FXSDB/FXLOSB/FXSDENB
11	RST#
12	GPIO7
13	GPIO6
14	P1_IND3
15	P1_IND2
16	VDDIO
17	P1_INER
18	P1_INCLK
19	P0_OUTD3
20	P0_OUTD2/P0_MODE3
21	P1_IND1
22	P1_IND0
23	P1_INDV
24	LED5/GPIO5/PHYADD
25	LED4/GPIO4/1588EN
26	P0_OUTER/P0_SPEED
27	VDDIO
28	P0_OUTD1/P0_MODE2
29	P0_OUTD0/P0_MODE1
30	P0_OUTDV
31	VDDCR
32	P0_OUTCLK/P0_REFCLK/P0_MODE0

TABLE 3-2: 80-TQFP-EP PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	Pin Name
33	P0_INDV
34	P0_IND0
35	P0_IND1
36	P0_INCLK
37	P0_IND2
38	P0_IND3
39	VDDIO
40	P1_OUTER/P1_SPEED/P1_MDIO
41	P0_INER
42	LED3/GPIO3/EEEEN
43	P1_OUTD3
44	P1_OUTD2/P1_MODE3
45	P1_OUTCLK/P1_REFCLK/P1_MODE0
46	P1_OUTD1/P1_MODE2
47	P1_OUTD0/P1_MODE1
48	P1_OUTDV
49	P0_DUPLEX
50	VDDIO
51	VDDCR
52	P0_MDC
53	P0_MDIO
54	TESTMODE
55	I2CSDA/EESDA/TMS
56	I2CSCL/EESCL/TCK
57	IRQ
58	LED2/GPIO2/E2PSIZE
59	LED1/GPIO1/TDI/P1_INTPHY
60	VDDIO
61	LED0/GPIO0/TDO/MNGT0
62	P0_CRS
63	P0_COL
64	P1_DUPLEX/P1_MDC
65	P1_COL
66	P1_CRS
67	VDD33TXRX1

TABLE 3-2: 80-TQFP-EP PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Number	Pin Name
68	TXNA
69	TXPA
70	RXNA
71	RXPA
72	VDD12TX1
73	RBIAS
74	VDD33BIAS
75	VDD12TX2
76	RXPB
77	RXNB
78	TXPB
79	TXNB
80	VDD33TXRX2
Exposed Pad	VSS

3.3 Pin Descriptions

This section contains descriptions of the various LAN9355 pins. The pin descriptions have been broken into functional groups as follows:

- LAN Port A Pin Descriptions
- LAN Port B Pin Descriptions
- LAN Port A & B Power and Common Pin Descriptions
- Switch Port 0 MII/RMII & Configuration Strap Pin Descriptions
- Switch Port 1 MII/RMII & Configuration Strap Pin Descriptions
- I2C Management Pin Descriptions
- EEPROM Pin Descriptions
- GPIO, LED & Configuration Strap Pin Descriptions
- Miscellaneous Pin Descriptions
- JTAG Pin Descriptions
- Core and I/O Power Pin Descriptions

TABLE 3-3: LAN PORT A PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port A TP TX/RX Positive Channel 1	TXPA	AIO	Port A Twisted Pair Transmit/Receive Positive Channel 1. See Note 1
	Port A FX TX Positive		OLVPECL	Port A Fiber Transmit Positive.
1	Port A TP TX/RX Negative Channel 1	TXNA	AIO	Port A Twisted Pair Transmit/Receive Negative Channel 1. See Note 1.
	Port A FX TX Negative		OLVPECL	Port A Fiber Transmit Negative.
1	Port A TP TX/RX Positive Channel 2	RXPA	AIO	Port A Twisted Pair Transmit/Receive Positive Channel 2. See Note 1.
	Port A FX RX Positive		AI	Port A Fiber Receive Positive.
1	Port A TP TX/RX Negative Channel 2	RXNA	AIO	Port A Twisted Pair Transmit/Receive Negative Channel 2. See Note 1.
	Port A FX RX Negative		AI	Port A Fiber Receive Negative.

TABLE 3-3: LAN PORT A PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port A FX Signal Detect (SD)	**FXSDA**	ILVPECL	Port A Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
	Port A FX Loss Of Signal (LOS)	**FXLOSA**	IS (PU)	Port A Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_1), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
	Port A FX-SD Enable Strap	**FXSDENA**	AI	Port A FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD. When FX-LOS mode is selected, the input buffer is disabled. See Note 2.

Note 1: In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Note 2: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 72 for more information.

Note: Port A is connected to the Switch Fabric port 1.

TABLE 3-4: LAN PORT B PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port B TP TX/RX Positive Channel 1	**TXPB**	AIO	Port B Twisted Pair Transmit/Receive Positive Channel 1. See Note 3
	Port B FX TX Positive		OLVPECL	Port B Fiber Transmit Positive.
1	Port B TP TX/RX Negative Channel 1	**TXNB**	AIO	Port B Twisted Pair Transmit/Receive Negative Channel 1. See Note 3.
	Port B FX TX Negative		OLVPECL	Port B Fiber Transmit Negative.

TABLE 3-4: LAN PORT B PIN DESCRIPTIONS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Port BTP TX/RX Positive Channel 2	**RXPB**	AIO	Port B Twisted Pair Transmit/Receive Positive Channel 2. See Note 3.
	Port B FX RX Positive		AI	Port B Fiber Receive Positive.
1	Port B TP TX/RX Negative Channel 2	**RXNB**	AIO	Port B Twisted Pair Transmit/Receive Negative Channel 2. See Note 3.
	Port B FX RX Negative		AI	Port B Fiber Receive Negative.
1	Port B FX Signal Detect (SD)	**FXSDB**	ILVPECL	Port B Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal. When FX-LOS mode is selected, the input buffer is disabled.
	Port B FX Loss Of Signal (LOS)	**FXLOSB**	IS (PU)	Port B Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_2), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal. When FX-LOS mode is not selected, the input buffer and pull-up are disabled.
	Port B FX-SD Enable Strap	**FXSDENB**	AI	Port B FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD. When FX-LOS mode is selected, the input buffer is disabled. See Note 4.

Note 3: In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

Note 4: Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 72 for more information.

Note: Port B is connected to Switch Fabric port 2.

TABLE 3-5: LAN PORT A & B POWER AND COMMON PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Bias Reference	**RBIAS**	AI	Used for internal bias circuits. Connect to an external 12.1 kΩ, 1% resistor to ground. Refer to the device reference schematic for connection information. **Note:** The nominal voltage is 1.2 V and the resistor will dissipate approximately 1 mW of power.
1	Port A and B FX-LOS Enable Strap	**FXLOSEN**	AI	Port A and B FX-LOS Enable. This 3 level strap input selects between FX-LOS and FX-SD / copper twisted pair mode. A level below 1 V (typ.) selects FX-SD / copper twisted pair for ports A and B, further determined by FXSDENA and FXSDENB. A level of 1.5 V selects FX-LOS for port A and FX-SD / copper twisted pair for port B, further determined by FXSDENB. A level above 2 V (typ.) selects FX-LOS for ports A and B.
1	+3.3 V Port A Analog Power Supply	**VDD33TXRX1**	P	See Note 5.
1	+3.3 V Port B Analog Power Supply	**VDD33TXRX2**	P	See Note 5.
1	+3.3 V Master Bias Power Supply	**VDD33BIAS**	P	See Note 5.
1	Port A Transmitter +1.2 V Power Supply	**VDD12TX1**	P	This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX2** pin for proper operation. See Note 5.
1	Port B Transmitter +1.2 V Power Supply	**VDD12TX2**	P	This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX1** pin for proper operation. See Note 5.

Note 5: Refer to Section 4.0, "Power Connections," on page 43, the device reference schematics, and the device LANCheck schematic checklist for additional connection information.

TABLE 3-6: SWITCH PORT 0 MII/RMII & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 MII Input Data 3	**P0_IND3**	VIS (PD)	**MII MAC Mode:** This pin is the receive data 3 bit from the external PHY to the switch.
			VIS (PD)	**MII PHY Mode:** This pin is the transmit data 3 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			-	**RMII MAC and RMII PHY Modes:** This pin is not used.
1	Port 0 MII Input Data 2	**P0_IND2**	VIS (PD)	**MII MAC Mode:** This pin is the receive data 2 bit from the external PHY to the switch.
			VIS (PD)	**MII PHY Mode:** This pin is the transmit data 2 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			-	**RMII MAC and RMII PHY Modes:** This pin is not used.
1	Port 0 MII/RMII Input Data 1	**P0_IND1**	VIS (PD)	**MII MAC Mode:** This pin is the receive data 1 bit from the external PHY to the switch.
			VIS (PD)	**MII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			VIS (PD)	**RMII MAC Mode:** This pin is the receive data 1 bit from the external PHY to the switch.
			VIS (PD)	**RMII PHY Mode:** This pin is the transmit data 1 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).

TABLE 3-6: SWITCH PORT 0 MII/RMII & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 MII/RMII Input Data 0	**P0_IND0**	VIS (PD)	**MII MAC Mode:** This pin is the receive data 0 bit from the external PHY to the switch.
			VIS (PD)	**MII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			VIS (PD)	**RMII MAC Mode:** This pin is the receive data 0 bit from the external PHY to the switch.
			VIS (PD)	**RMII PHY Mode:** This pin is the transmit data 0 bit from the external MAC to the switch. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
1	Port 0 MII/RMII Input Data Valid	**P0_INDV**	VIS (PD)	**MII MAC Mode:** This pin is the RX_DV signal from the external PHY and indicates valid data on **P0_IND[3:0]** and **P0_INER**.
			VIS (PD)	**MII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on **P0_IND[3:0]** and **P0_INER**. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			VIS (PD)	**RMII MAC Mode:** This pin is the CRS_DV signal from the external PHY.
			VIS (PD)	**RMII PHY Mode:** This pin is the TX_EN signal from the external MAC and indicates valid data on **P0_IND[1:0]**. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
1	Port 0 MII/RMII Input Error	**P0_INER**	VIS (PD)	**MII MAC Mode:** This pin is the RX_ER signal from the external PHY and indicates a receive error in the packet or that Lower Power Idle is being received.
			VIS (PD)	**MII PHY Mode:** This pin is the TX_ER signal from the external MAC and indicates that the current packet should be aborted. The pull-down and input buffer are disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			VIS (PD)	**RMII MAC Mode:** This pin is the RX_ER signal from the external PHY and indicates a receive error in the packet.
			-	**RMII PHY Mode:** This pin is not used.

TABLE 3-6: SWITCH PORT 0 MII/RMII & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 MII Input Clock	**P0_INCLK**	VIS (PD)	**MII MAC Mode:** This pin is an input and is used as the reference clock for the **P0_IND[3:0]**, **P0_INER** and **P0_INDV** pins. It is connected to the receive clock of the external PHY.
			VO12/ VO16 Note 6	**MII PHY Mode:** This pin is an output and is used as the reference clock for the **P0_IND[3:0]**, **P0_INER** and **P0_INDV** pins. It is connected to the transmit clock of the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x). When operating at 200 Mbps, the choice of drive strength is based on the setting of the RMII/Turbo MII Clock Strength bit in the Port 0 Port x Virtual PHY Special Control/Status Register (VPHY_SPECIAL_CONTROL_STATUS_x). A low selects a 12 mA drive, while a high selects a 16 mA drive.
			-	**RMII MAC and RMII PHY Modes:** This pin is not used.
1	Port 0 MII Output Data 3	**P0_OUTD3**	VO8	**MII MAC Mode:** This pin is the transmit data 3 bit from the switch to the external PHY.
			VO8	**MII PHY Mode:** This pin is the receive data 3 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			-	**RMII MAC and RMII PHY Modes:** This pin is not used.
1	Port 0 MII Output Data 2	**P0_OUTD2**	VO8	**MII MAC Mode:** This pin is the transmit data 2 bit from the switch to the external PHY.
			VO8	**MII PHY Mode:** This pin is the receive data 2 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			-	**RMII MAC and RMII PHY Modes:** This pin is not used.
	Port 0 Mode[3] Configuration Strap	**P0_MODE3**	VIS (PU) Note 8	This strap configures the mode for Port 0. See Note 7. Refer to Table 7-3, “Port 0 Mode Strap Mapping,” on page 87 for the Port 0 strap settings.

TABLE 3-6: SWITCH PORT 0 MII/RMII & CONFIGURATION STRAP PIN DESCRIPTIONS

Num Pins	Name	Symbol	Buffer Type	Description
1	Port 0 MII/RMII Output Data 1	**P0_OUTD1**	VO8	**MII MAC Mode:** This pin is the transmit data 1 bit from the switch to the external PHY.
			VO8	**MII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			VO8	**RMII MAC Mode:** This pin is the transmit data 1 bit from the switch to the external PHY.
			VO8	**RMII PHY Mode:** This pin is the receive data 1 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
	Port 0 Mode[2] Configuration Strap	**P0_MODE2**	VIS (PU) Note 8	This strap configures the mode for Port 0. See Note 7. Refer to Table 7-3, "Port 0 Mode Strap Mapping," on page 87 for the Port 0 strap settings.
1	Port 0 MII/RMII Output Data 0	**P0_OUTD0**	VO8	**MII MAC Mode:** This pin is the transmit data 0 bit from the switch to the external PHY.
			VO8	**MII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
			VO8	**RMII MAC Mode:** This pin is the transmit data 0 bit from the switch to the external PHY.
			VO8	**RMII PHY Mode:** This pin is the receive data 0 bit from the switch to the external MAC. The output driver is disabled when the Isolate (VPHY_ISO) bit is set in the Port 0 Port x Virtual PHY Basic Control Register (VPHY_BASIC_CTRL_x).
	Port 0 Mode[1] Configuration Strap	**P0_MODE1**	VIS (PU) Note 8	This strap configures the mode for Port 0. See Note 7. Refer to Table 7-3, "Port 0 Mode Strap Mapping," on page 87 for the Port 0 strap settings.