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LAN9420/LAN9420i

Single-Chip Ethernet Controller with HP Auto-MDIX Support and PCI Interface

PRODUCT FEATURES

Datasheet

Highlights

- Optimized for embedded applications with 32-bit RISC CPUs
- Integrated descriptor based scatter-gather DMA and IRQ deassertion timer effectively increase network throughput and reduce CPU loading
- Integrated Ethernet MAC with full-duplex support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX support
- 32-bit, 33MHz, PCI 3.0 compliant interface
- Reduced power operating modes with PCI Power Management Specification 1.1 compliance
- Supports multiple audio & video streams over Ethernet

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- Home gateways
- Digital media clients/servers
- Industrial automation systems
- Industrial/single board PC
- Kiosk/POS enterprise equipment

Key Benefits

- Integrated High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated 10/100 Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - Supports HP Auto-MDIX
    - Supports energy-detect power down
  - Support for 3 status LEDs
  - Receive and transmit TCP checksum offload
- PCI Interface
  - PCI Local Bus Specification Revision 3.0 compliant
  - 32-bit/33-MHz PCI bus
  - Descriptor based scatter-gather DMA enables zero-copy drivers
- Comprehensive Power Management Features
  - Supports PCI Bus Power Management Interface Specification, Revision 1.1
  - Supports optional wake from D3cold (via configuration strap option when Vaux is available)
  - Wake on LAN
  - Wake on link status change (energy detect)
  - Magic packet wakeup
- General Purpose I/O
  - 3 programmable GPIO pins
  - 2 GPO pins
- Support for Optional EEPROM
  - Serial interface provided for EEPROM
  - Used to store PCI and MAC address configuration values
- Miscellaneous Features
  - Big/Little/Mixed endian support for registers, descriptors, and buffers
  - IRQ deassertion timer
  - General purpose timer
- Single 3.3V Power Supply
  - Integrated 1.8V regulator
- Packaging
  - Available in 128-pin VTQFP Lead-free RoHS Compliant package
- Environmental
  - Available in commercial & industrial temperature ranges

Order Numbers:

LAN9420-NU For 128-PIN VTQFP, Lead-Free RoHS Compliant Package (0 to 70^{o}C)

LAN9420i-NU For 128-PIN VTQFP, Lead-Free RoHS Compliant Package (-40^{o} to 85^{o}C)

This product meets the halogen maximum concentration values per IEC61249-2-21

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Chapter 1 Introduction

1.1 Block Diagrams

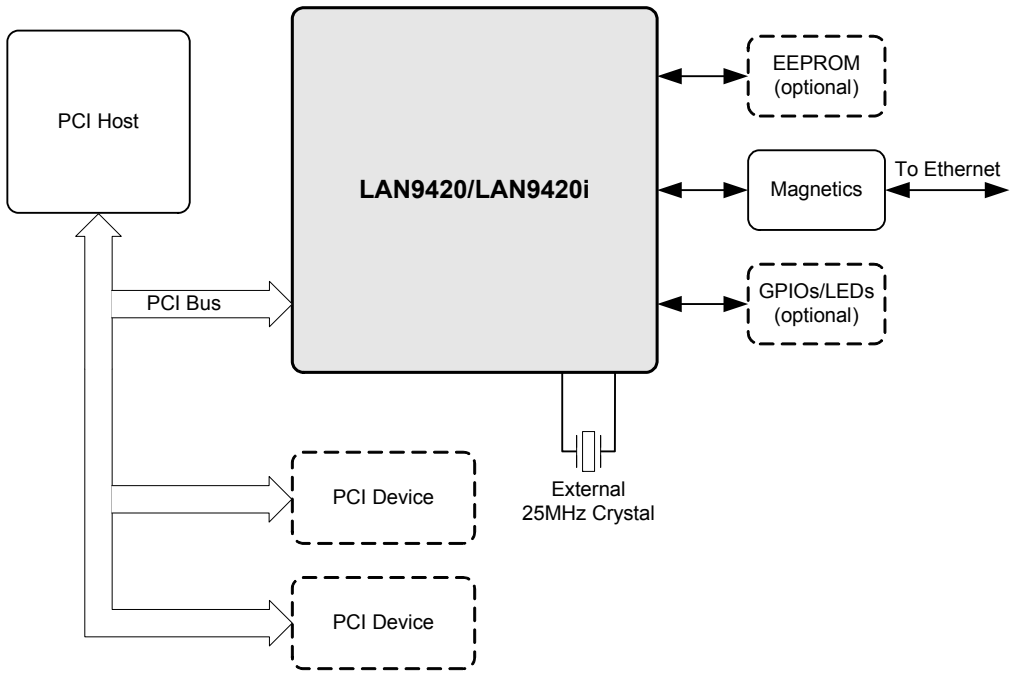


Figure 1.1 System Level Block Diagram

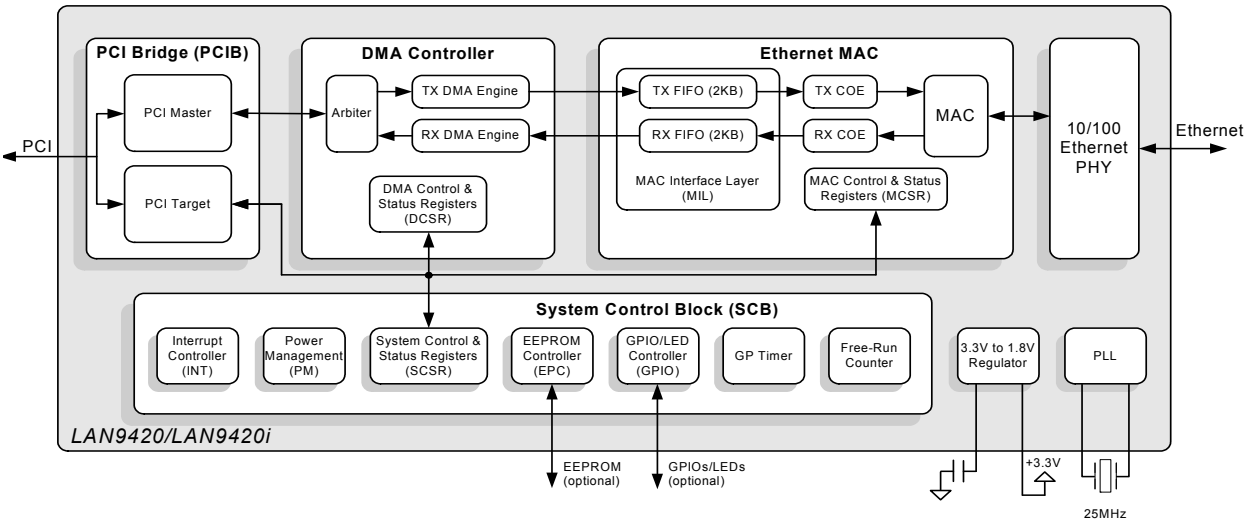


Figure 1.2 LAN9420/LAN9420i Internal Block Diagram

1.2 General Description

LAN9420/LAN9420i is a full-featured, Fast Ethernet controller which allows for the easy and cost-effective integration of Fast Ethernet into a PCI-based system. A system configuration diagram of LAN9420/LAN9420i in a typical embedded environment can be seen in Figure 1.1, followed by an internal block diagram of LAN9420/LAN9420i in Figure 1.2. LAN9420/LAN9420i consists of a PCI Local Bus Specification Revision 3.0 compliant interface, DMA Controller, Ethernet MAC, and 10/100 Ethernet PHY.

LAN9420/LAN9420i provides full IEEE 802.3 compliance and all internal components support full/half-duplex 10BASE-T, 100BASE-TX, and manual full-duplex flow control. The descriptor based scatter-gather DMA supports usage of zero-copy drivers, effectively increasing throughput while decreasing Host load. The integrated IRQ deassertion timer allows a minimum IRQ deassertion time to be set, providing reduced Host load and greater control over service routines. Automatic 32-bit CRC generation/checking, automatic payload padding, and 2K jumbo packets (2048 byte) are supported.

Big, little, and mixed endian support provides independent control over register, descriptor, and buffer endianess. This feature enables easy integration into various ARM/MIPS/PowerPC designs.

LAN9420/LAN9420i supports the PCI Bus Power Management Interface Specification Revision 1.1 and provides the optional ability to generate wake events in the D3cold state when Vaux is available. Wake on LAN, wake on link status change (energy detect), and magic packet wakeup detection are also supported, allowing for a range of power management options.

LAN9420/LAN9420i contains an EEPROM controller for connection to an optional EEPROM. This allows for the automatic loading of static configuration data upon power-up or reset. When connected, the EEPROM can be configured to load a predetermined MAC address, the PCI SSID, and the PCI SSVID of LAN9420/LAN9420i.

In addition to the primary functionality described above, LAN9420/LAN9420i provides additional features designed for extended functionality. These include a multipurpose 16-bit configurable General Purpose Timer (GPT), a Free-Run Counter, a 3-pin configurable GPIO/LED interface, and 2 GPO pins. All aspects of LAN9420/LAN9420i are managed via a set of memory mapped control and status registers.

LAN9420/LAN9420i's performance and features make it an ideal solution for many applications in the consumer electronics, enterprise, and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, home gateways, digital media clients/servers, industrial automation systems, industrial single board PCs, and kiosk/POS enterprise equipment.

1.3 PCI Bridge

LAN9420/LAN9420i implements a PCI Local Bus Specification Revision 3.0 compliant interface, supporting the PCI Bus Power Management Interface Specification Revision 1.1. It provides the PCI Configuration Space Control and Status registers used to configure LAN9420/LAN9420i for PCI device operation. Please refer to Section 3.2, "PCI Bridge (PCIB)," on page 23 for more information.

1.4 DMA Controller

The DMA controller consists of independent Transmit and Receive engines and a control and status register (CSR) space. The Transmit Engine transfers data from Host memory to the MAC Interface Layer (MIL) while the Receive Engine transfers data from the MIL to Host memory. The controller utilizes descriptors to efficiently move data from source to destination with minimal processor intervention. Descriptors are DWORD aligned data structures in system memory that inform the DMA controller of the location of data buffers in Host memory and also provide a mechanism for communicating the status to the Host CPU. The DMA controller has been designed for packet-oriented data transfer, such as frames in Ethernet. Zero copy DMA transfer is supported. Copy operations for the purpose of data re-alignment are not required in the case where buffers are fragmented or not aligned to a DWORD boundary. The controller can be programmed to interrupt the Host on the occurrence of particular events, such as frame transmit or receive transfer completed, and other normal, as well as error, conditions. Please refer to Section 3.4, "DMA Controller (DMAC)," on page 38 for more information.

1.5 Ethernet MAC

The transmit and receive data paths are separate within the 10/100 Ethernet MAC, allowing the highest performance, especially in full duplex mode. The data paths connect to the PCI Bridge via a DMA engine. The MAC also implements a CSR space used by the Host to obtain status and control its operation. The MAC Interface Layer (MIL), within the MAC, contains a 2K Byte transmit and receive FIFO. The MIL supports store and forward and operate on second frame mode for minimum inter-packet gap. Please refer to Section 3.5, "10/100 Ethernet MAC," on page 53 for more information.

1.6 Ethernet PHY

The PHY implements an IEEE 802.3 physical layer for twisted pair Ethernet applications. It can be configured for either 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) Ethernet operation in either full or half duplex configurations. The PHY block includes support for auto-negotiation, auto-polarity correction and Auto-MDIX. Minimal external components are required for the utilization of the integrated PHY. Please refer to Section 3.6, "10/100 Ethernet PHY," on page 64 for more information.

1.7 System Control Block

The System Control Block provides the following additional elements for system operation. These elements are controlled via its System Control and Status Registers (SCSR). Please refer to Section 3.3, "System Control Block (SCB)," on page 28 for more information.

1.7.1 Interrupt Controller

The Interrupt Controller (INT) can be programmed to issue a PCI interrupt to the Host on the occurrence of various events. Please refer to Section 3.3.1, "Interrupt Controller," on page 28 for more information.

1.7.2 PLL and Power Management

LAN9420/LAN9420i interfaces with a 25MHz crystal oscillator from which all internal clocks, with the exception of PCI clock, are generated. The internal clocks are all generated by the PLL and Power Management blocks. Various power savings modes exists that allow for the clocks to be shut down. These modes are defined by the power state of the PCI function. Please refer to Section 3.7, "Power Management," on page 74 for more information.

1.7.3 EEPROM Controller

LAN9420/LAN9420i provides support for an optional EEPROM via the EEPROM Controller. Please refer to Section 3.3.5, "EEPROM Controller (EPC)," on page 31 for more information.

1.7.4 GPIO/LED Controller

The 3-bit GPIO and 2-bit GPO (Multiplexed on the LED and EEPROM Pins) interface is managed by the GPIO/LED Controller. It is accessible via the System Control and Status Registers (SCSR). The GPIO signals can function as inputs, push-pull outputs and open drain outputs. The GPIOs can also be configured to trigger interrupts with programmable polarity. The GPOs are outputs only and have no means of generating interrupts.

Please refer to Section 4.2.5, "General Purpose Input/Output Configuration Register (GPIO_CFG)," on page 93 for more information.

1.7.5 General Purpose Timer

The General Purpose Timer has no dedicated function within LAN9420/LAN9420i and may be programmed to issue a timed interrupt. Please refer to Section 3.3.3, "General Purpose Timer (GPT)," on page 30 for more information.

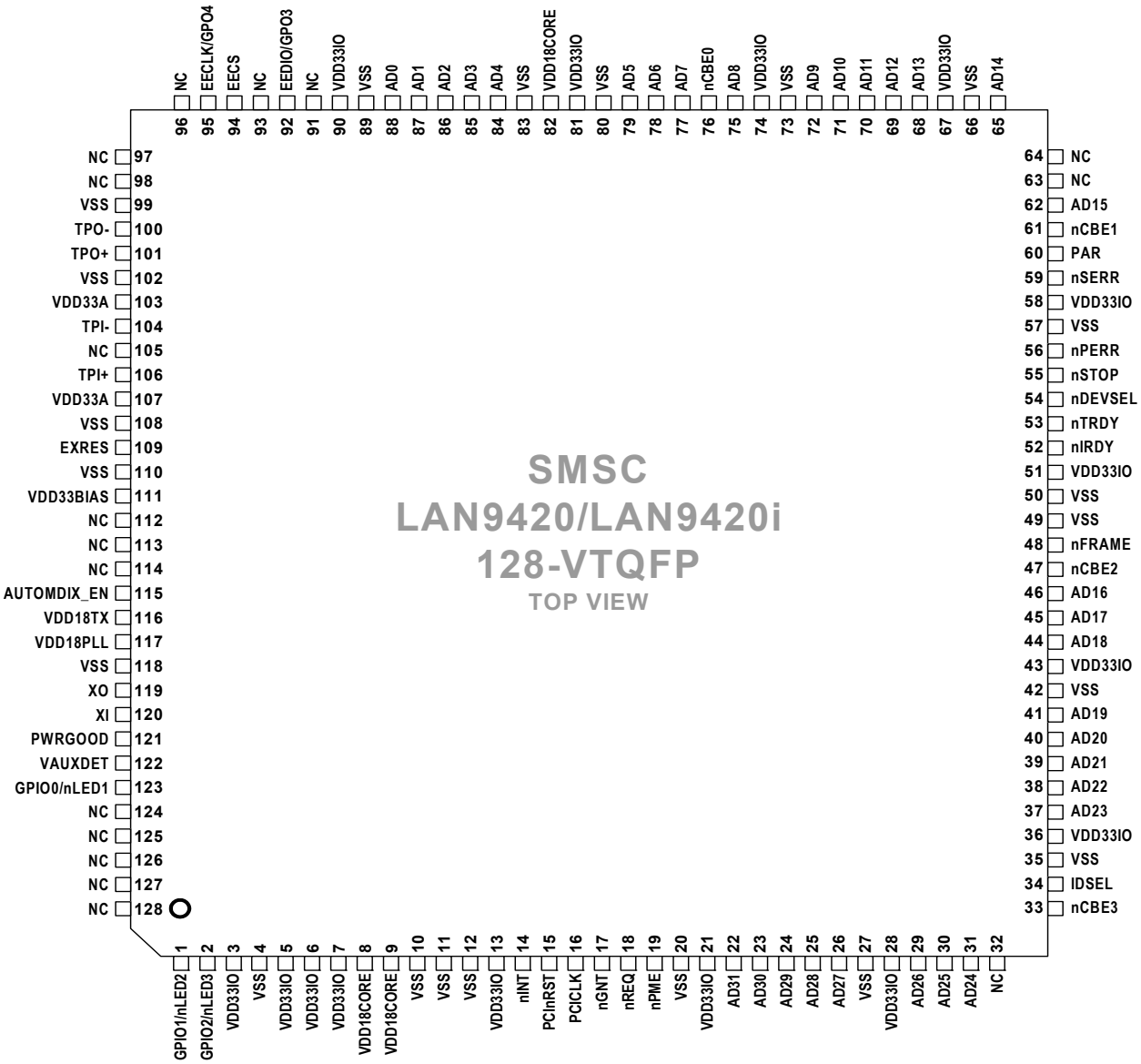
1.7.6 Free Run Counter

The Free Run Counter has no dedicated function within LAN9420/LAN9420i and may be used by the software drivers as a timebase. Please refer to Section 3.3.4, "Free-Run Counter (FRC)," on page 31 for more information.

1.8 Control and Status Registers (CSR)

LAN9420/LAN9420i's functions are controlled and monitored by the Host via the Control and Status Registers (CSR). This register space includes registers that control and monitor the DMA controller (DMA Control and Status Registers - DCSR), the MAC (MAC Control and Status Registers - MCSR), the PHY (accessed indirectly through the MAC via the MII_ACCESS and MII_DATA registers), and the elements of the System Control Block via the System Control and Status Registers (SCSR). The CSR may be accessed be via I/O or memory operations. Big or Little Endian access is also configurable.

Chapter 2 Pin Description and Configuration



NOTE: When HP Auto-MDIX is activated, the TPO+/- pins function as TPI+/- and vice-versa.

Figure 2.1 LAN9420/LAN9420i 128-VTQFP (Top View)

2.1 Pin List

Table 2.1 PCI Bus Interface Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	PCI Clock In	PCICLK	IS	**PCI Clock In:** 0 to 33MHz PCI Clock Input.
1	PCI Frame	nFRAME	IPCI/ OPCI	**PCI Cycle Frame**
32	PCI Address and Data Bus	AD[31:0]	IPCI/ OPCI	**PCI Address and Data Bus**
1	PCI Reset	PCInRST	IS	**PCI Reset**
4	PCI Bus Command and Byte Enables	nCBE[3:0]	IPCI/ OPCI	**PCI Bus Command and Byte Enables**
1	PCI Initiator Ready	nIRDY	IPCI/ OPCI	**PCI Initiator Ready**
1	PCI Target Ready	nTRDY	IPCI/ OPCI	**PCI Target Ready**
1	PCI Stop	nSTOP	IPCI/ OPCI	**PCI Stop**
1	PCI Device Select	nDEVSEL	IPCI/ OPCI	**PCI Device Select**
1	PCI Parity	PAR	IPCI/ OPCI	**PCI Parity**
1	PCI Parity Error	nPERR	IPCI/ OPCI	**PCI Parity Error**
1	PCI System Error	nSERR	IPCI/ OPCI	**PCI System Error**
1	PCI Interrupt	nINT	OPCI	**PCI Interrupt** **Note:** This pin is an open drain output.
1	PCI IDSEL	IDSEL	IPCI	**PCI IDSEL**
1	PCI Request	nREQ	OPCI	**PCI Request** **Note:** This pin is a tri-state output.
1	PCI Grant	nGNT	IPCI	**PCI Grant**
1	PCI Power Management Event	nPME	OPCI	**PCI Power Management Event** **Note:** This pin is an open drain output.
1	Power Good	PWRGOOD	IS (PD)	**PCI Bus Power Good:** This pin is used to sense the presence of PCI bus power during the D3 power management state. **Note:** This pin is pulled low through an internal pull-down resistor
1	V_{AUX} Detection	VAUXDET	IS (PD)	**PCI Auxiliary Voltage Sense:** This pin is used to sense the presence of a 3.3V auxiliary supply in order to define the PME support available. **Note:** This pin is pulled low through an internal pull-down resistor

Table 2.2 EEPROM

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	EEPROM Data	EEDIO	IS/O8	**EEPROM Data:** This bi-directional pin can be connected to an optional serial EEPROM DIO.
	GPO3	GPO3	O8	**General Purpose Output 3:** This pin can also function as a general purpose output. The EECS pin is deasserted so as to never unintentionally access the serial EEPROM.
	TX_EN	TX_EN	O8	**TX_EN Signal Monitor:** This pin can also be configured to monitor the TX_EN signal on the internal MII port. The EECS pin is deasserted so as to never unintentionally access the serial EEPROM.
	TX_CLK	TX_CLK	O8	**TX_CLK Signal Monitor:** This pin can also be configured to monitor the TX_CLK signal on the internal MII port. The EECS pin is deasserted so as to never unintentionally access the serial EEPROM.
1	EEPROM Chip Select	EECS	O8	**Serial EEPROM Chip Select**.
1	EEPROM Clock	EECLK	IS/O8 (PU) Note 2.1	**EEPROM Clock:** Serial EEPROM Clock pin
	GPO4	GPO4	O8	**General Purpose Output 4:** This pin can also function as a general purpose output. The EECS pin is deasserted so as to never unintentionally access the serial EEPROM.
	RX_DV	RX_DV	O8	**RX_DV Signal Monitor:** This pin can also be configured to monitor the RX_DV signal on the internal MII port. The EECS pin is deasserted so as to never unintentionally access the serial EEPROM.
	RX_CLK	RX_CLK	O8	**RX_CLK Signal Monitor:** This pin can also be configured to monitor the RX_CLK signal on the internal MII port. The EECS pin is deasserted so as to never unintentionally access the serial EEPROM.

Note 2.1 This pin is used for factory testing and is latched on power up. This pin is pulled high through an internal resistor and must not be pulled low externally. This pin must be augmented with an external resistor when connected to a load. The value of the resistor must be such that the pin reaches its valid level before de-assertion of PCInRST following power up. The “IS” input buffer type is enabled only during power up. The “IS” input buffer type is disabled at all other times.

Table 2.3 GPIO and LED Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	General Purpose I/O data 0	GPIO0	IS/O12/ OD12	**General Purpose I/O data 0:** This general-purpose pin is fully programmable as either push-pull output, open-drain output or input by writing the GPIO_CFG configuration register in the SCSR. GPIO pins are Schmitt-triggered inputs.
	nLED1 (Speed Indicator)	nLED1	OD12	**nLED1 (Speed Indicator):** This pin can also function as the Ethernet speed indicator LED and is driven low when the operating speed is 100Mbs, during auto-negotiation, and when the cable is disconnected. This pin is driven high only during 10Mbs operation.
1	General Purpose I/O data 1	GPIO1	IS/O12/ OD12	**General Purpose I/O data 1:** This general-purpose pin is fully programmable as either push-pull output, open-drain output or input by writing the GPIO_CFG configuration register in the SCSR. GPIO pins are Schmitt-triggered inputs.
	nLED2 (Link & Activity Indicator)	nLED2	OD12	**nLED2 (Link & Activity Indicator):** This pin can also function as the Ethernet Link and Activity Indicator LED and is driven low (LED on) when LAN9420/LAN9420i detects a valid link. This pin is pulsed high (LED off) for 80mS whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will flash as an activity indicator.
1	General Purpose I/O data 2	GPIO2	IS/O12/ OD12	**General Purpose I/O data 2:** This general-purpose pin is fully programmable as either push-pull output, open-drain output or input by writing the GPIO_CFG configuration register in the SCSR. GPIO pins are Schmitt-triggered inputs.
	nLED3 (Full-Duplex Indicator)	nLED3	OD12	**nLED3 (Full-Duplex Indicator):** This pin can also function as the Ethernet Full-Duplex Indicator LED and is driven low when the link is operating in full-duplex mode.

Table 2.4 Configuration Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	AutoMDIX Enable	AUTOMDIX_EN	IS (PU)	**AutoMDIX Enable:** Enables Auto-MDIX. Pull high or leave unconnected to enable Auto-MDIX, pull low to disable Auto-MDIX.

Table 2.5 PLL and Ethernet PHY Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Crystal Input	XI	ICLK	**Crystal Input:** External 25MHz crystal input. This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
1	Crystal Output	XO	OCLK	**Crystal Output:** External 25MHz crystal output.
1	Ethernet TX Data Out Negative	TPO-	AIO	**Ethernet Transmit Data Out Negative:** The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet TX Data Out Positive	TPO+	AIO	**Ethernet Transmit Data Out Positive:** The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Negative	TPI-	AIO	**Ethernet Receive Data In Negative:** The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Positive	TPI+	AIO	**Ethernet Receive Data In Positive:** The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	External PHY Bias Resistor	EXRES	AI	**External PHY Bias Resistor:** Used for the internal PHY bias circuits. Connect to an external 12.4K 1.0% resistor to ground.

Table 2.6 Power and Ground Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
2	+3.3V Analog Power Supply	VDD33A	P	**+3.3V Analog Power Supply** Refer to the LAN9420/LAN9420i application note for connection information.
1	+1.8V PLL Power Supply	VDD18PLL	P	**+1.8V PLL Power Supply:** This pin must be connected to VDD18CORE for proper operation. Refer to the LAN9420/LAN9420i application note for additional connection information.
1	+1.8V TX Power Supply	VDD18TX	P	**+1.8V Transmitter Power Supply:** This pin must be connected to VDD18CORE for proper operation. Refer to the LAN9420/LAN9420i application note for additional connection information.
1	+3.3V Master Bias Power Supply	VDD33BIAS	P	**+3.3V Master Bias Power Supply** Refer to the LAN9420/LAN9420i application note for additional connection information.
15	+3.3V I/O Power	VDD33IO	P	**+3.3V Power Supply for I/O Pins and Internal Regulator** Refer to the LAN9420/LAN9420i application note for additional connection information.
21	Ground	VSS	P	**Common Ground for I/O Pins, Core, and Analog Circuitry**
3	+1.8V Core Power	VDD18CORE	P	**Digital Core +1.8V Power Supply Output from Internal Regulator** Refer to the LAN9420/LAN9420i application note for additional connection information.

Table 2.7 No-Connect Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
17	No Connect	NC	-	**No Connect:** These pins must be left floating for normal device operation.

Table 2.8 128-VTQFP Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	GPIO1/nLED2	33	nCBE3	65	AD14	97	NC
2	GPIO2/nLED3	34	IDSEL	66	VSS	98	NC
3	VDD33IO	35	VSS	67	VDD33IO	99	VSS
4	VSS	36	VDD33IO	68	AD13	100	TPO-
5	VDD33IO	37	AD23	69	AD12	101	TPO+
6	VDD33IO	38	AD22	70	AD11	102	VSS
7	VDD33IO	39	AD21	71	AD10	103	VDD33A
8	VDD18CORE	40	AD20	72	AD9	104	TPI-
9	VDD18CORE	41	AD19	73	VSS	105	NC
10	VSS	42	VSS	74	VDD33IO	106	TPI+
11	VSS	43	VDD33IO	75	AD8	107	VDD33A
12	VSS	44	AD18	76	nCBE0	108	VSS
13	VDD33IO	45	AD17	77	AD7	109	EXRES
14	nINT	46	AD16	78	AD6	110	VSS
15	PCInRST	47	nCBE2	79	AD5	111	VDD33BIAS
16	PCICLK	48	nFRAME	80	VSS	112	NC
17	nGNT	49	VSS	81	VDD33IO	113	NC
18	nREQ	50	VSS	82	VDD18CORE	114	NC
19	nPME	51	VDD33IO	83	VSS	115	AUTOMDIX_EN
20	VSS	52	nIRDY	84	AD4	116	VDD18TX
21	VDD33IO	53	nTRDY	85	AD3	117	VDD18PLL
22	AD31	54	nDEVSEL	86	AD2	118	VSS
23	AD30	55	nSTOP	87	AD1	119	XO
24	AD29	56	nPERR	88	AD0	120	XI
25	AD28	57	VSS	89	VSS	121	PWRGOOD
26	AD27	58	VDD33IO	90	VDD33IO	122	VAUXDET
27	VSS	59	nSERR	91	NC	123	GPIO0/nLED1
28	VDD33IO	60	PAR	92	EEDIO/GPO3	124	NC
29	AD26	61	nCBE1	93	NC	125	NC
30	AD25	62	AD15	94	EECS	126	NC
31	AD24	63	NC	95	EECLK/GPO4	127	NC
32	NC	64	NC	96	NC	128	NC

2.2 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered Input
O8	Output with 8mA sink and 8mA source current
O12	Output with 12mA sink and 12mA source current
OD12	Open-drain output with 12mA sink current
IPCI	PCI compliant Input
OPCI	PCI compliant Output
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to LAN9420/LAN9420i. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to LAN9420/LAN9420i. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog Input
AIO	Analog bi-directional
ICLK	Crystal oscillator input
OCLK	Crystal oscillator output
P	Power and Ground pin

Chapter 3 Functional Description

3.1 Functional Overview

The LAN9420/LAN9420i Ethernet Controller consists of five major functional blocks. These blocks are:

- PCI Bridge (PCIB)
- System Control Block (SCB)
- DMA Controller (DMAC)
- 10/100 Ethernet MAC
- 10/100 Ethernet PHY

The following sections discuss the features of each block. A block diagram of LAN9420/LAN9420i is shown in Figure 1.2 LAN9420/LAN9420i Internal Block Diagram on page 11.

3.2 PCI Bridge (PCIB)

The PCI Bridge (PCIB) facilitates LAN9420/LAN9420i's operation on a PCI bus as a device. It has the following features:

PCI Master Interface: This interface connects LAN9420/LAN9420i to the PCI bus when it is functioning as a PCI Master. It is used by the DMA engines to directly access the PCI Host's memory.

PCI Target Interface: This interface connects LAN9420/LAN9420i to the PCI bus when it is functioning as a PCI Target. It provides access to PCI Configuration Space Control and Status Register (CONFIG CSR), and access to the Control and Status Registers (CSR) via I/O or Non-Prefetchable (NP) memory accesses. In addition, Big/Little Endian support for the registers may be selected.

PCI Power Management Support: LAN9420/LAN9420i supports PCI Bus Power Management Interface Specification Rev. 1.1. Refer to Section 3.7, "Power Management," on page 74 for more information.

Interrupt Gating Logic: This logic controls assertion of the nINT signal to the Host system.

PCI Configuration Space Control and Status Registers (CONFIG CSR): The Host system controls and monitors the LAN9420/LAN9420i device using registers in this space.

3.2.1 PCI Bridge (PCIB) Block Diagram

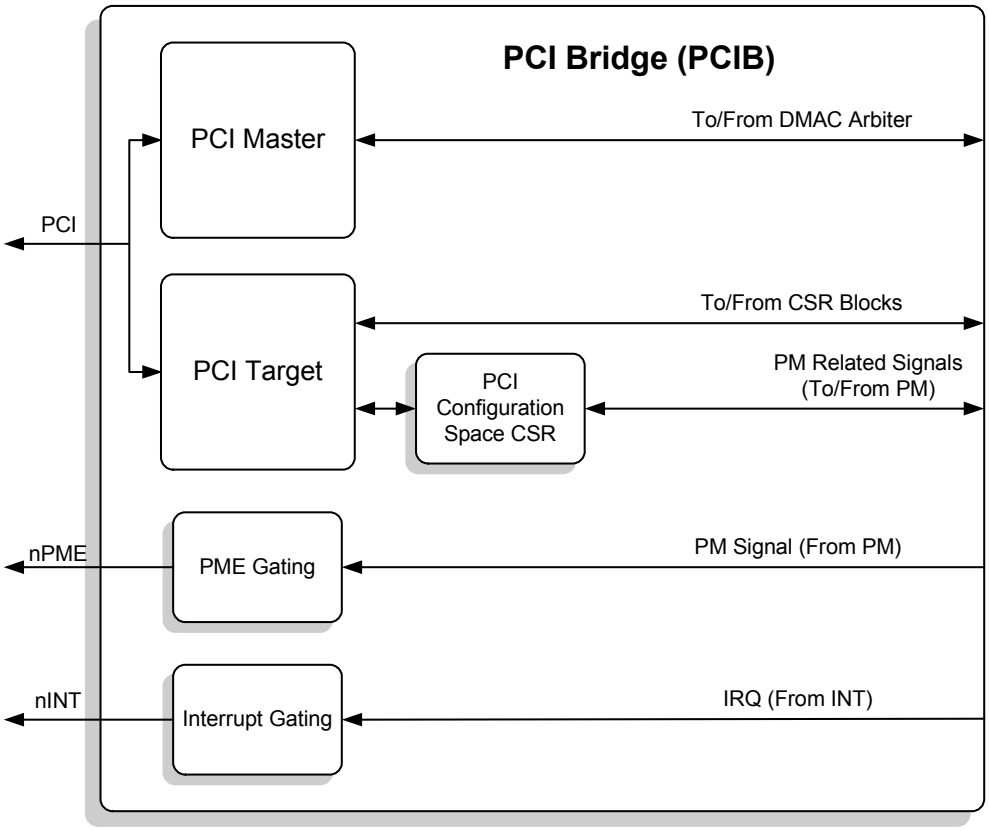


Figure 3.1 PCI Bridge Block Diagram

3.2.2 PCI Interface Environments

The PCIB supports only Device operation. It functions as a simple bridge, permitting LAN9420/LAN9420i to act as a master/target PCI device on the PCI bus. The Host performs PCI arbitration and is responsible for initializing configuration space for all devices on the bus. Figure 3.2 illustrates Device operation.

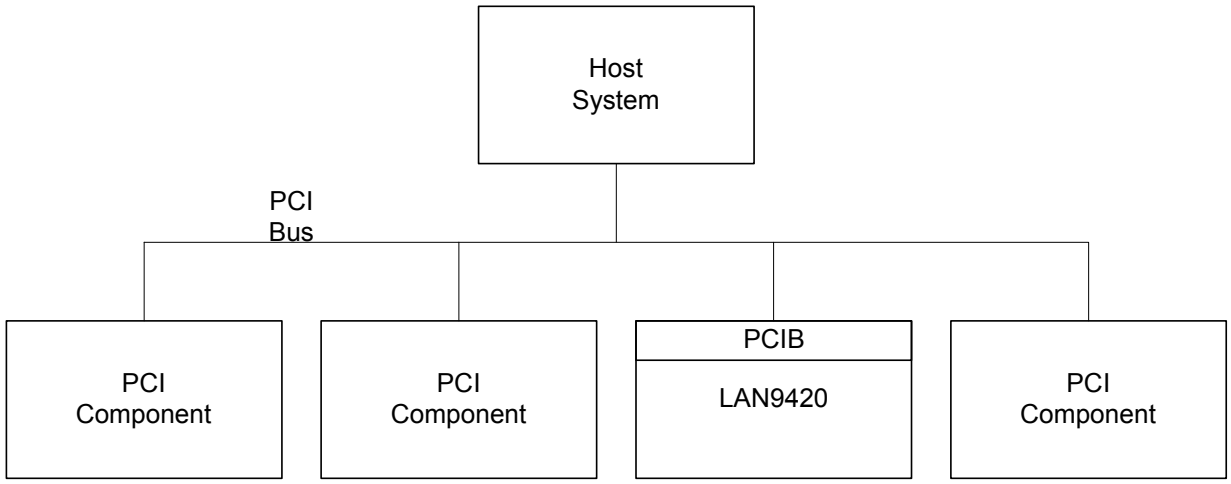


Figure 3.2 Device Operation

3.2.3 PCI Master Interface

The PCI Master Interface is used by the DMA engines to directly access the PCI Host's memory. It is used by the TX and RX DMA Controllers to access Host descriptor ring elements and Host DMA buffers. No address translation occurs, as these entities are contained within the Host, which allocates them within the flat PCI address space.

3.2.3.1 PCI Master Transaction Errors

In the event of an error during a descriptor read or during a transmit data read, the DMA controller will generate a Master Bus Error Interrupt (MBERR_INT).

When an MBERR_INT is asserted, all subsequent transactions from the DMAC will be aborted. In order to cleanly recover from this condition, a software reset or H/W reset must be performed. A software reset is accomplished by setting the SRST bit of the BUS_MODE register.

Note: It is guaranteed that the MBERR_INT will be reported on the frame upon which the error occurred as follows:
- Errors on descriptor reads will be aborted immediately.
- Errors on TX data will be reported either upon the data or the close descriptor (if the error occurs on the last data transfer).
- DMA RX data and descriptor write operations are posted and will therefore not generate the MBERR_INT.