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LAN950x USB 2.0 to 10/100 Ethernet Controller

Highlights

- Single Chip Hi-Speed USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated USB 2.0 Hi-Speed PHY
- Implements Reduced Power Operating Modes

Target Applications

- Embedded Systems
- Set-Top Boxes
- PVRs
- CE Devices
- Networked Printers
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Test Instrumentation
- Industrial

Key Features

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification Revision 2.0
  - Supports HS (480 Mbps) and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Integrated USB 2.0 PHY
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible address filtering modes
    - –One 48-bit perfect address
    - –64 hash-filtered multicast addresses
    - –Pass all multicast
    - –Promiscuous mode
    - –Inverse filtering
    - –Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - –Auto-negotiation
    - –Automatic polarity detection and correction
    - –HP Auto-MDIX support
    - –Link status change wake-up detection
  - Support for 3 status LEDs
  - External MII and Turbo MII support HomePNA™ and HomePlug® PHY
- Power and I/Os
  - Various low power modes
  - NetDetach feature increases battery life[1]
  - Supports PCI-like PME wake[1]
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - Single external 3.3v I/O supply
    - –Internal core regulator
- Miscellaneous Features
  - EEPROM Controller
  - Supports custom operation without EEPROM[1]
  - IEEE 1149.1 (JTAG) Boundary Scan
  - Requires single 25 MHz crystal
- Software
  - Windows XP/Vista Driver
  - Linux Driver
  - Win CE Driver
  - MAC OS Driver
  - EEPROM Utility
- Packaging
  - 56-pin QFN (8x8 mm) RoHS Compliant

Environmental

- Commercial Temperature Range (0°C to +70°C)
- Industrial Temperature Range (-40°C to +85°C)

[1] = LAN9500A/LAN9500Ai ONLY

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1.0 LAN950X FAMILY DIFFERENCES OVERVIEW

The Microchip LAN950x is a family of high performance Hi-Speed USB 2.0 to 10/100 Ethernet controllers. The “x” in the part number is a generic term referring to the entire family, which includes the following devices:

- LAN9500
- LAN9500i
- LAN9500A
- LAN9500Ai

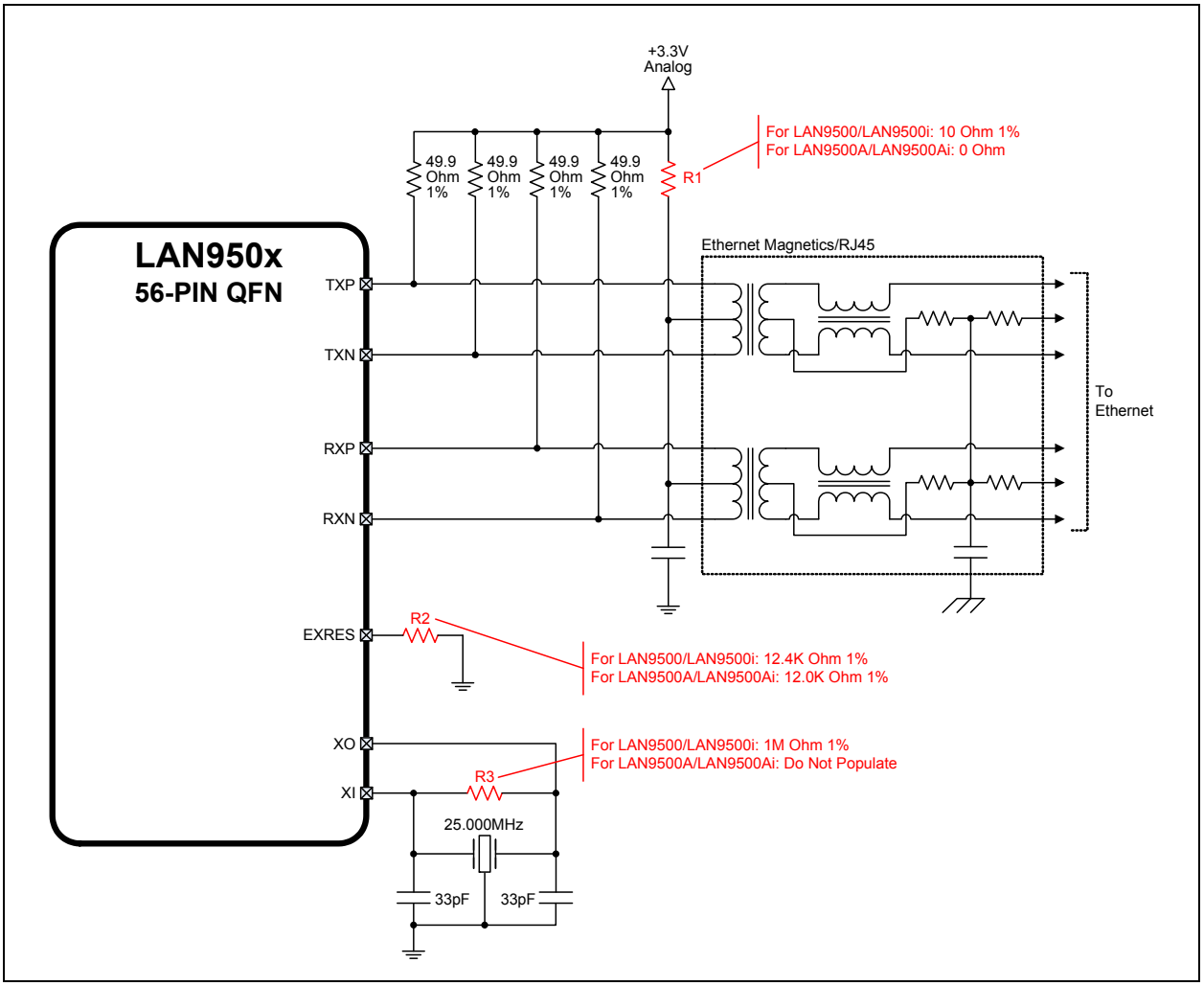
Device specific features that do no pertain to the entire LAN950x family are called out independently throughout this document. Table 1-1 provides a summary of the feature differences between family members.

TABLE 1-1: LAN950X FAMILY DIFFERENCES

Part Number	PME Wake	Net Detach	Suspend3 State	Good Packet Wakeup	PHY Boost	Custom Operation without EEPROM	Increased Wakeup Frame Filter	Low Power 100 mW Crystal Support	0° To 70°C	-40° to 85°c
LAN9500									X	
LAN9500i										X
LAN9500A	X	X	X	X	X	X	X	X	X	
LAN9500Ai	X	X	X	X	X	X	X	X		X

The LAN9500/LAN9500i and LAN9500A/LAN9500Ai are pin compatible. However, the value of the required EXRES resistor and other system components differ between devices. Refer to Figure 1-1 and the LAN950x reference schematics for additional information.

FIGURE 1-1: SYSTEM COMPONENT DIFFERENCES



2.0 INTRODUCTION

2.1 General Terms and Conventions

The following is a list of the general terms used in this document:

BYTE	8-bits
CSR	Control and Status Registers
DWORD	32-bits
FIFO	First In First Out buffer
Frame	In the context of this document, a frame refers to transfers on the Ethernet interface.
FSM	Finite State Machine
GPIO	General Purpose I/O
HOST	External system (Includes processor, application software, etc.)
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true, and the status bit is cleared by writing a zero.
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller
MII	Media Independent Interface
N/A	Not Applicable
Packet	In the context of this document, a packet refers to transfers on the USB interface.
POR	Power on Reset.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SCSR	System Control and Status Registers
SMI	Serial Management Interface
TLI	Transaction Layer Interface
URX	USB Bulk Out Packet Receiver
UTX	USB Bulk In Packet Transmitter
WORD	16-bits
ZLP	Zero Length USB Packet

2.2 Block Diagram

FIGURE 2-1: LAN950X BLOCK DIAGRAM

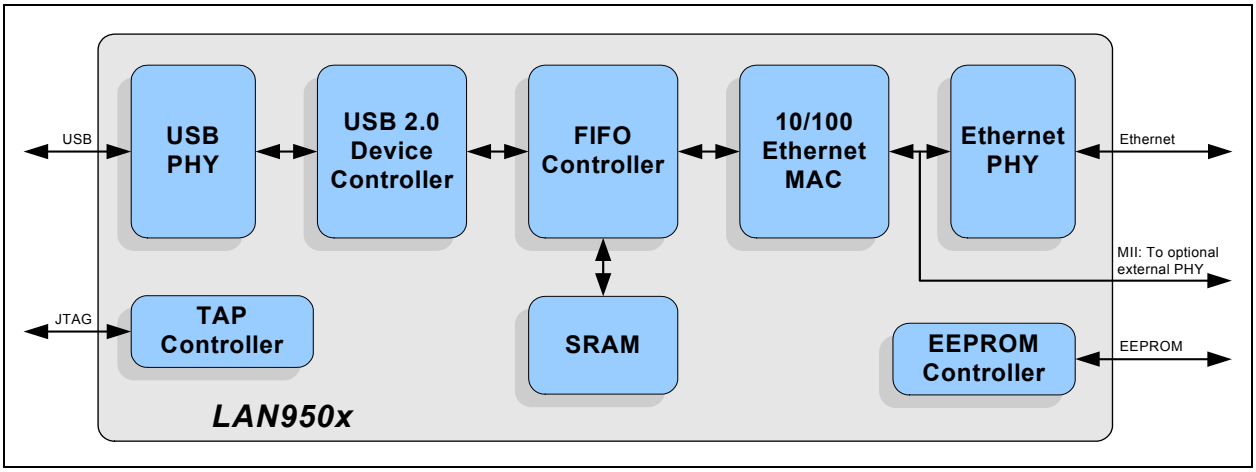
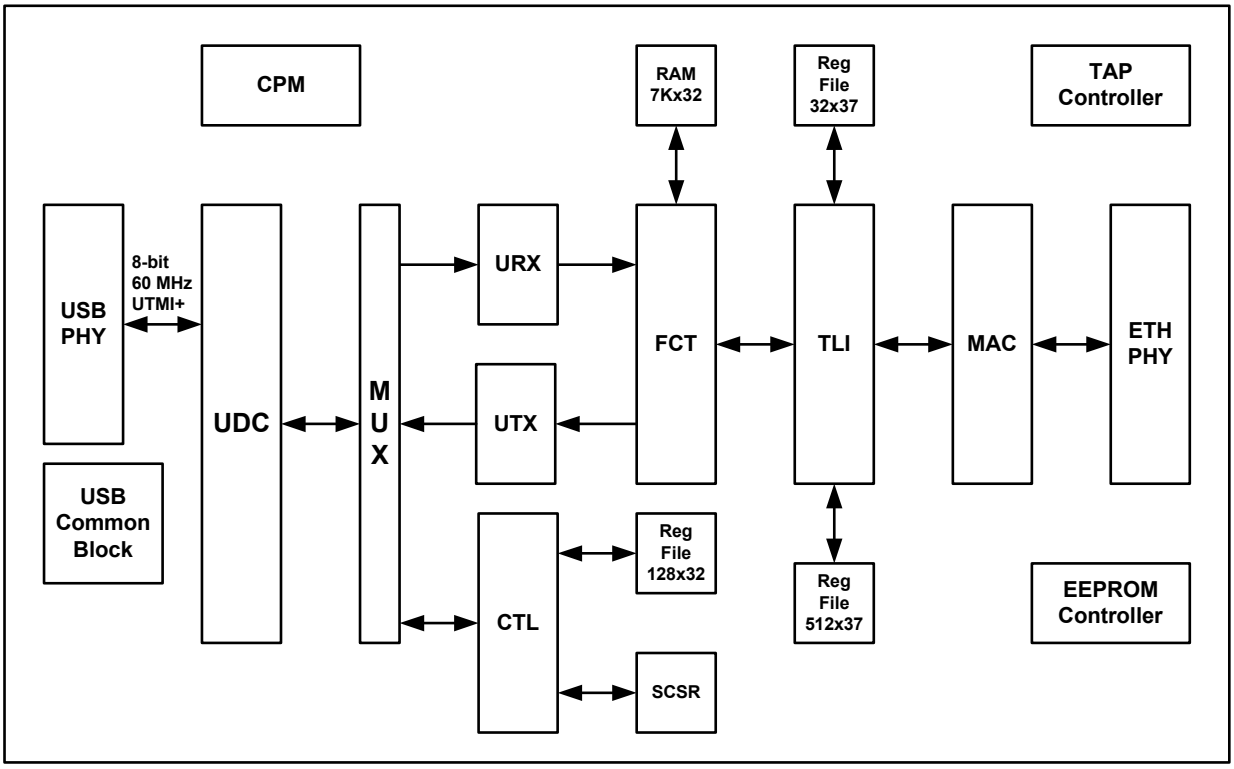


FIGURE 2-2: LAN950X SYSTEM DIAGRAM



2.2.1 OVERVIEW

The LAN950x is a high performance solution for USB to 10/100 Ethernet port bridging. With applications ranging from embedded systems, set-top boxes, and PVRs, to USB port replicators, USB to Ethernet dongles, and test instrumentation, the device is targeted as a high performance, low cost USB/Ethernet connectivity solution.

The LAN950x contains an integrated 10/100 Ethernet PHY, USB PHY, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 KB of internal packet buffering. Two KB of buffer memory are allocated to the Transaction Layer Interface (TLI), while 28 KB are allocated to the FIFO Controller (FCT).

The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The device implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and IEEE 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low power modes and “Magic Packet”, “Wake On LAN”, and “Link Status Change” wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

2.2.2 USB

The USB portion of LAN950x consists of the USB Device Controller (UDC), USB Bulk Out Packet Receiver (URX), USB Bulk In Packet Transmitter (UTX), Control Block (CTL), System Control and Status Registers (SCSR), and USB PHY.

The USB device controller (UDC) contains a USB low-level protocol interpreter that controls the USB bus protocol, packet generation/extraction, PID/Device ID parsing, and CRC coding/decoding with autonomous error handling. It is capable of operating either in USB 1.1 or 2.0 compliant modes. It has autonomous protocol handling functions like stall condition clearing on setup packets, suspend/resume/reset conditions, and remote wakeup. It also autonomously handles contingency operations for error conditions such as retry for CRC errors, Data toggle errors, and generation of NYET, STALL, ACK and NACK depending on the endpoint buffer status. The UDC implements four USB endpoints: Control, Interrupt, Bulk-In, and Bulk-Out.

The Control block (CTL) manages traffic to/from the control endpoint that is not handled by the UDC and constructs the packets used by the interrupt endpoint. The CTL is responsible for handling some USB standard commands and all vendor specific commands. The vendor specific commands allow for efficient statistics collection and access to the SCSR.

The URX and UTX implement the bulk-out and bulk-in pipes, respectively, which connect the USB Host and the UDC. They perform the following functions:

The URX passes USB Bulk-Out packets to the FIFO Controller (FCT). It tracks whether or not a USB packet is erroneous. It instructs the FCT to flush erroneous packets by rewinding its write pointer.

The UTX retrieves Ethernet frames from the FCT and constructs USB Bulk-In packets from them. If the handshake for a transmitted Bulk-In packet does not complete, the UTX is capable of retransmitting the packet. The UTX will not instruct the FCT to advance its read head pointer until the current USB packet has been successfully transmitted to the USB Host.

Both the URX and UTX are responsible for handling Ethernet frames encapsulated over USB by one of the following methods.

- Multiple Ethernet frames per USB Bulk packet
- Single Ethernet frame per USB Bulk packet

The UDC also implements the System Control and Status Register (SCSR) space used by the Host to obtain status and control overall system operation.

The integrated USB 2.0 compliant device PHY supports high speed and full speed modes.

2.2.3 FIFO CONTROLLER (FCT)

The FIFO controller uses a 28 KB internal SRAM to buffer RX and TX traffic. 20 KB is allocated for received Ethernet-USB traffic (RX buffer), while 8 KB is allocated for USB-Ethernet traffic (TX buffer). Bulk-Out packets from the USB controller are directly stored into the TX buffer. The FCT is responsible for extracting Ethernet frames from the USB packet data and passing the frames to the MAC.Ethernet Frames are directly stored into the RX buffer and become the basis for bulk-in packets. The FCT passes the stored data to the UTX in blocks typically 512 or 64 bytes in size, depending on the current HS/FS USB operating speed.

2.2.4 ETHERNET

LAN950x integrates an IEEE 802.3 PHY for twisted pair Ethernet applications and a 10/100 Ethernet Media Access Controller (MAC).

The PHY can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation in either Full or Half Duplex configurations. The PHY block includes auto-negotiation, auto-polarity correction, and Auto-MDIX. Minimal external components are required for the utilization of the Integrated PHY.

Optionally, an external PHY may be used via the MII (Media Independent Interface) port, effectively bypassing the internal PHY. This option allows support for HomePNA and HomePlug applications.

The transmit and receive data paths within the 10/100 Ethernet MAC are independent, allowing for the highest performance possible, particularly in full-duplex mode. The Ethernet MAC operates in store and forward mode, utilizing an independent 2KB buffer for transmitted frames, and a smaller 128 byte buffer for received frames. The Ethernet MAC data paths connect to the FIFO controller. The MAC also implements a Control and Status Register (CSR) space used by the Host to obtain status and control its operation.

The Ethernet MAC/PHY supports numerous power management wakeup features, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. Eight wakeup frame filters are provided by LAN9500A/LAN9500Ai, while four are provided by LAN9500/LAN9500i.

2.2.5 TRANSACTION LAYER INTERFACE (TLI)

The TLI interfaces the MAC with the FCT. It is a conduit between these two modules through which all transmitted and received data, along with status information, is passed. It has separate receive and transmit data paths. The TLI contains a 2KB transmit FIFO and a 128-byte receive FIFO. The transmit FIFO operates in store and forward mode and is capable of storing up to two Ethernet frames.

2.2.6 POWER MANAGEMENT

The LAN950x features four (Note 2-1) variations of USB suspend: SUSPEND0, SUSPEND1, SUSPEND2, and SUSPEND3. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, “Wake On LAN”, and “Magic Packet” remote wakeup events. This suspend state reduces power by stopping the clocks of the MAC and other internal modules.
- **SUSPEND1:** Supports GPIO and “Link Status Change” for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the device.
- **SUSPEND3:** (Note 2-1) Supports GPIO and “Good Packet” remote wakeup event. A “Good Packet” is a received frame passing certain filtering constraints independent of those imposed on “Wake On LAN” and “Magic Packet” frames. This suspend state consumes power at a level similar to the NORMAL state, however, it allows for power savings in the Host CPU.

Note 2-1 All four SUSPEND states are supported by LAN9500A/LAN9500Ai. SUSPEND3 is not supported by LAN9500/LAN9500i.

Please refer to Section 5.12, "Wake Events," on page 100 for more information on the USB suspend states and the wake events supported in each state.

2.2.7 EEPROM CONTROLLER (EPC)

LAN950x contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon power-on reset, pin reset, or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration, and MAC address.

(LAN9500A/LAN9500Ai ONLY)

2.2.8 GENERAL PURPOSE I/O

When configured for internal PHY mode, up to eleven GPIOs are supported. All GPIOs can serve as remote wakeup events when the LAN950x is in a suspended state.

2.2.9 TAP CONTROLLER

IEEE 1149.1 compliant TAP Controller supports boundary scan and various test modes.

2.2.10 CONTROL AND STATUS REGISTERS (CSR)

LAN950x's functions are controlled and monitored by the Host via the Control and Status Registers (CSR). This register space includes registers that control and monitor the USB controller, as well as elements of overall system operation (System Control and Status Registers - SCSR), the MAC (MAC Control and Status Registers - MCSR), and the PHY (accessed indirectly through the MAC via the MII_ACCESS and MII_DATA registers). The CSR may be accessed via the USB Vendor Commands (REGISTER READ/REGISTER WRITE). Please refer to Section 5.3.3, "USB Vendor Commands," on page 41 for more information.

2.2.11 RESETS

LAN950x supports the following system reset events:

- Power on Reset (POR)
- Hardware Reset Input Pin Reset (nRESET)
- Lite Reset (LRST)
- Software Reset (SRST)
- USB Reset
- VBUS Reset

The device supports the following module level reset events:

- Ethernet PHY Software Reset (PHY_RST)
- nTRST Pin Reset for Tap Controller

2.2.12 TEST FEATURES

Read/Write access to internal SRAMs is provided via the CSRs. JTAG based USB BIST is available. Full internal scan and At Speed scan are supported.

2.2.13 SYSTEM SOFTWARE

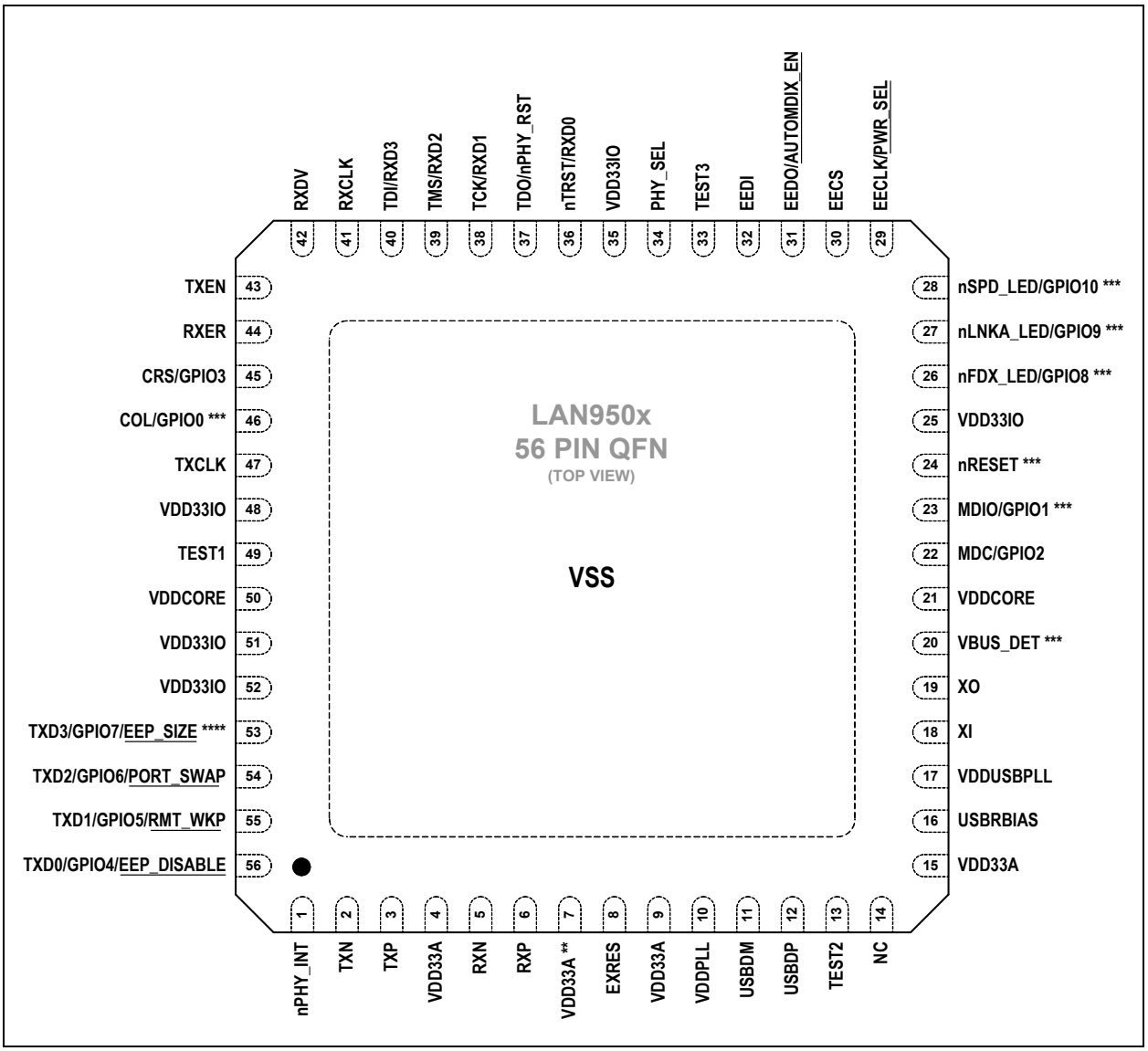
LAN950x software drivers are available for the following operating systems:

- Windows XP
- Windows Vista
- Linux
- Win CE
- MAC OS

In addition, an EEPROM programming utility is available for configuring the external EEPROM.

3.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note 1: ** This pin is a no-connect (NC) for LAN9500A/LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500/LAN9500i.

2: *** For LAN9500A/LAN9500Ai this pin provides additional PME related functionality. Refer to the respective pin descriptions and Section 6.0, "PME Operation," on page 112 for additional information.

3: **** For LAN9500A/LAN9500Ai GPIO7 may provide additional PHY Link Up related functionality. Refer to Section 5.12.2.4, "Enabling PHY Link Up Wake Events (LAN9500A/LAN9500Ai ONLY)," on page 108 for additional information.

4: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa.

5: Exposed pad (VSS) on bottom of package must be connected to ground.

TABLE 3-1: MII INTERFACE PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	Receive Error (Internal PHY Mode)	RXER	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Receive Error (External PHY Mode)	RXER	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates a receive error in the packet.
1	Transmit Enable (Internal PHY Mode)	TXEN	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Transmit Enable (External PHY Mode)	TXEN	O8 (PD)	In external PHY mode, this pin functions as an output to the external PHY and indicates valid data on TXD[3:0].
1	Receive Data Valid (Internal PHY Mode)	RXDV	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Receive Data Valid (External PHY Mode)	RXDV	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates valid data on RXD[3:0].
1	Receive Clock (Internal PHY Mode)	RXCLK	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Receive Clock (External PHY Mode)	RXCLK	IS (PD)	In external PHY mode, this pin is the receiver clock input from the external PHY.
1	Carrier Sense (Internal PHY Mode)	CRS	IS/O8 (PU)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Carrier Sense (External PHY Mode)	CRS	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates a network carrier.
	General Purpose I/O 3 (Internal PHY Mode Only)	GPIO3	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.

TABLE 3-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	MII Collision Detect (Internal PHY Mode)	COL	IS/O8 (PU)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	MII Collision Detect (External PHY Mode)	COL	IS (PD)	In external PHY mode, the signal on this pin is input from the external PHY and indicates a collision event.
	General Purpose I/O 0 (Internal PHY Mode Only)	**GPIO0**	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note: (LAN9500A/LAN9500Ai ONLY):** This pin may be used to signal PME when Internal PHY and PME modes of operation are in effect. Refer to Section 6.0, "PME Operation," on page 112 for additional information.
1	Management Data (Internal PHY Mode)	MDIO	IS/O8 (PU)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Management Data (External PHY Mode)	MDIO	IS/O8 (PD)	In external PHY mode, this pin provides the management data to/from the external PHY.
	General Purpose I/O 1 (Internal PHY Mode Only)	**GPIO1**	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note: (LAN9500A/LAN9500Ai ONLY):** This pin may serve as the PME_MODE_SEL input when Internal PHY and PME modes of operation are in effect. Refer to Section 6.0, "PME Operation," on page 112 for additional information.
1	Management Clock (Internal PHY Mode)	MDC	IS/O8 (PU)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Management Clock (External PHY Mode)	MDC	O8 (PD)	In external PHY mode, this pin outputs the management clock to the external PHY.
	General Purpose I/O 2 (Internal PHY Mode Only)	GPIO2	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.

TABLE 3-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Transmit Data 3 (Internal PHY Mode)	TXD3	IS/O8 (PU)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Transmit Data 3 (External PHY Mode)	TXD3	O8 (PU)	In external PHY mode, this pin functions as the transmit data 3 output to the external PHY.
	General Purpose I/O 7 (Internal PHY Mode Only)	GPIO7	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note: (LAN9500A/LAN9500Ai ONLY):** GPIO7 may provide additional PHY Link Up related functionality. Refer to Section 5.12.2.4, "Enabling PHY Link Up Wake Events (LAN9500A/LAN9500Ai ONLY)," on page 108 for additional information.
	EEPROM Size Configuration Strap	**EEP_SIZE**	IS (PU)	The EEP_SIZE strap selects the size of the EEPROM attached to the device. 0 = 128 byte EEPROM is attached and a total of seven address bits are used. 1 = 256/512 byte EEPROM is attached and a total of nine address bits are used. **Note:** A 3-wire style 1K/2K/4K EEPROM that is organized for 128 x 8-bit or 256/512 x 8-bit operation must be used. See Note 3-1 for more information on configuration straps.
1	Transmit Data 2 (Internal PHY Mode)	TXD2	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Transmit Data 2 (External PHY Mode)	TXD2	O8 (PD)	In external PHY mode, this pin functions as the transmit data 2 output to the external PHY.
	General Purpose I/O 6 (Internal PHY Mode Only)	GPIO6	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	USB Port Swap Configuration Strap	**PORT_SWAP**	IS (PD)	Swaps the mapping of USBDP and USBDM. 0 = USBDP maps to the USB D+ line and USBDM maps to the USB D- line. 1 = USBDP maps to the USB D- line. USBDM maps to the USB D+ line. See Note 3-1 for more information on configuration straps.

TABLE 3-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Transmit Data 1 (Internal PHY Mode)	TXD1	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Transmit Data 1 (External PHY Mode)	TXD1	O8 (PD)	In external PHY mode, this pin functions as the transmit data 1 output to the external PHY.
	General Purpose I/O 5 (Internal PHY Mode Only)	GPIO5	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	Remote Wakeup Configuration Strap	**RMT_WKP**	IS (PD)	This strap configures the default descriptor values to support remote wakeup. This strap is overridden by the EEPROM. 0 = Remote wakeup is not supported. 1 = Remote wakeup is supported. See Note 3-1 for more information on configuration straps.
1	Transmit Data 0 (Internal PHY Mode)	TXD0	IS/O8 (PD)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Transmit Data 0 (External PHY Mode)	TXD0	O8 (PD)	In external PHY mode, this pin functions as the transmit data 0 output to the external PHY.
	General Purpose I/O 4 (Internal PHY Mode Only)	GPIO4	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	EEPROM Disable Configuration Strap	**EEP_DISABLE**	IS (PD)	This strap disables the autoloading of the EEPROM contents. The assertion of this strap does not prevent register access to the EEPROM. 0 = EEPROM is recognized if present. 1 = EEPROM is not recognized even if it is present. See Note 3-1 for more information on configuration straps.
1	Transmit Clock (Internal PHY Mode)	TXCLK	IS/O8 (PU)	In internal PHY mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 122 for additional information.
	Transmit Clock (External PHY Mode)	TXCLK	IS (PU)	In external PHY mode, this pin is the transmitter clock input from the external PHY.

Note 3-1 Configuration strap values are latched on Power-On Reset (POR) or External Chip Reset (nRESET). Configuration straps are identified by an underlined symbol name. Pins that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 5.14, "Configuration Straps," on page 111 for additional information.

TABLE 3-2: EEPROM PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	EEPROM Data In	EEDI	IS (PD)	This pin is driven by the EEDO output of the external EEPROM.
1	EEPROM Data Out	EEDO	O8 (PU)	This pin drives the EEDI input of the external EEPROM.
1	Auto-MDIX Enable Configuration Strap	**AUTOMDIX_EN**	IS (PU)	Determines the default Auto-MDIX setting. 0 = Auto-MDIX is disabled. 1 = Auto-MDIX is enabled. See Note 3-2 for more information on configuration straps.
1	EEPROM Chip Select	EECS	O8	This pin drives the chip select output of the external EEPROM. **Note:** The EECS output may tri-state briefly during power-up. Some EEPROM devices may be prone to false selection during this time. When an EEPROM is used, an external pull-down resistor is recommended on this signal to prevent false selection. Refer to your EEPROM manufacturer's data sheet for additional information.
1	EEPROM Clock	EECLK	O8 (PD)	This pin drives the EEPROM clock of the external EEPROM.
1	Power Select Configuration Strap	**PWR_SEL**	IS (PD)	Determines the default power setting when no EEPROM is present. This strap is overridden by the EEPROM. 0 = The device is bus powered. 1 = The device is self powered. See Note 3-2 for more information on configuration straps.

Note 3-2 Configuration strap values are latched on Power-On Reset (POR) or External Chip Reset (nRESET). Configuration straps are identified by an underlined symbol name. Pins that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 5.14, "Configuration Straps," on page 111 for additional information.

TABLE 3-3: JTAG PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	JTAG Test Port Reset (Internal PHY Mode)	nTRST	IS (PU)	In internal PHY mode, this active-low pin functions as the JTAG test port reset input.
	Receive Data 0 (External PHY Mode)	RXD0	IS (PD)	In external PHY mode, this pin functions as the receive data 0 input from the external PHY.
1	JTAG Test Data Out (Internal PHY Mode)	TDO	O8	In internal PHY mode, this pin functions as the JTAG data output.
	PHY Reset (External PHY Mode)	nPHY_RST	O8	In external PHY mode, this active-low pin functions as the PHY reset output.
1	JTAG Test Clock (Internal PHY Mode)	TCK	IS (PU)	In internal PHY mode, this pin functions as the JTAG test clock. The maximum operating frequency of this clock is 25MHz.
	Receive Data 1 (External PHY Mode)	RXD1	IS (PD)	In external PHY mode, this pin functions as the receive data 1 input from the external PHY.
1	JTAG Test Mode Select (Internal PHY Mode)	TMS	IS (PU)	In internal PHY mode, this pin functions as the JTAG test mode select.
	Receive Data 2 (External PHY Mode)	RXD2	IS (PD)	In external PHY mode, this pin functions as the receive data 2 input from the external PHY.
1	JTAG Test Data Input (Internal PHY Mode)	TDI	IS (PU)	In internal PHY mode, this pin functions as the JTAG data input.
	Receive Data 3 (External PHY Mode)	RXD3	IS (PD)	In external PHY mode, this pin functions as the receive data 3 input from the external PHY.

TABLE 3-4: MISCELLANEOUS PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	PHY Select	**PHY_SEL**	IS (PD)	Selects whether to use the internal Ethernet PHY or the external PHY connected to the MII port. 0 = Internal PHY is used. 1 = External PHY is used. **Note:** When in external PHY mode, the internal PHY is placed into general power down after a POR. Please Refer to Section 5.6, "10/100 Internal Ethernet PHY," on page 69 for details.
1	System Reset	nRESET	IS (PU)	This active-low pin allows external hardware to reset the device. **Note: (LAN9500A/LAN9500Ai ONLY):** This pin may be used to signal PME_CLEAR when PME mode of operation is in effect. Refer to Section 6.0, "PME Operation," on page 112 for additional information.
1	Ethernet Full-Duplex Indicator LED	nFDX_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet link is operating in full-duplex mode.
	General Purpose I/O 8	**GPIO8**	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note 1: (LAN9500A/LAN9500Ai ONLY):** This pin may be used to signal PME when External PHY and PME modes of operation are in effect. Refer to **Section 6.0 "PME Operation"** for additional information. **2:** By default this pin is configured as a GPIO.
1	Ethernet Link Activity Indicator LED	nLNKA_LED	OD12 (PU)	This pin is driven low (LED on) when a valid link is detected. This pin is pulsed high (LED off) for 80 mS whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80 mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will function as an activity indicator.
	General Purpose I/O 9	**GPIO9**	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note 1: (LAN9500A/LAN9500Ai ONLY):** This pin may serve as the PME_MODE_SEL input when External PHY and PME modes of operation are in effect. Refer to **Section 6.0 "PME Operation"** for additional information. **2:** By default this pin is configured as a GPIO.

TABLE 3-4: MISCELLANEOUS PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Ethernet Speed Indicator LED	nSPD_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet operating speed is 100 Mbs, or during auto-negotiation. This pin is driven high during 10 Mbs operation, or during line isolation.
	General Purpose I/O 10	**GPIO10**	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note 1: (LAN9500A/LAN9500Ai ONLY):** This pin may serve as a wakeup pin whose detection mode is selectable when External PHY and PME modes of operation are in effect. Refer to **Section 6.0 "PME Operation"** for additional information. **2:** By default this pin is configured as a GPIO.
1	Detect Upstream VBUS Power	VBUS_DET	IS_5V (PD)	Detects state of upstream bus power. For bus powered applications, this pin must be tied to VDD33IO. For self-powered applications where the device is permanently attached to a host, VBUS_DET should be pulled to VDD33IO. For other self-powered applications, refer to the device reference schematic for additional connection information. **Note: (LAN9500A/LAN9500Ai ONLY):** This pin may be used to signal bus power availability when PME mode of operation is in effect. Refer to **Section 6.0 "PME Operation"** for additional information.
1	Test 1	TEST1	-	This pin must always be connected to VDD33IO for proper operation.
1	Test 2	TEST2	-	This pin must always be connected to VSS for proper operation.
1	Test 3	TEST3	-	This pin must always be connected to VSS for proper operation.

TABLE 3-5: USB PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	USB DMINUS	USBDM	AIO	**Note:** The functionality of this pin may be swapped to USB DPLUS via the PORT_SWAP configuration strap.
1	USB DPLUS	USBDP	AIO	**Note:** The functionality of this pin may be swapped to USB DMINUS via the PORT_SWAP configuration strap.
1	External USB Bias Resistor.	USBRBIAS	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12K 1.0% resistor to ground.
1	USB PLL Supply	VDDUSBPLL	P	This pin must be connected to VDDCORE for proper operation. Refer to Section 4.0, "Power Connections," on page 24 and the device reference schematics for additional connection information.
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.

TABLE 3-6: ETHERNET PHY PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	Ethernet TX Data Out Negative	TXN	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet TX Data Out Positive	TXP	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Negative	RXN	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Positive	RXP	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	PHY Interrupt (Internal PHY Mode)	nPHY_INT	O8	In internal PHY mode, this pin can be configured to output the internal PHY interrupt signal. **Note:** The internal PHY interrupt signal is active-high.
	PHY Interrupt (External PHY Mode)	nPHY_INT	IS (PU)	In external PHY mode, the active-low signal on this pin is input from the external PHY and indicates a PHY interrupt has occurred.

TABLE 3-6: ETHERNET PHY PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
4	+3.3V Analog Power Supply	VDD33A	P	Refer to the device reference schematics for connection information. **Note:** Pin 7 is a no-connect (NC) for LAN9500A/LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500/LAN9500i.
1	External PHY Bias Resistor	EXRES	AI	Used for the internal bias circuits. Connect to an external resistor to ground. For LAN9500A/LAN9500Ai use 12.0K 1.0% For LAN9500/LAN9500i use 12.4K 1.0%.
1	Ethernet PLL Power Supply	VDDPLL	P	This pin must be connected to VDDCORE for proper operation. Refer to **Section 4.0 "Power Connections"** and the device reference schematics for additional connection information.

TABLE 3-7: I/O POWER PINS, CORE POWER PINS, AND GROUND PAD

Num Pins	Name	Symbol	Buffer Type	Description
5	+3.3V I/O Power	VDD33IO	P	Refer to the device reference schematics for connection information.
2	Digital Core Power Supply Output	VDDCORE	P	Refer to Section 4.0, "Power Connections" and the device reference schematics for connection information.
Exposed pad on package bottom (Figure 3-1)	Ground	VSS	P	Common Ground

TABLE 3-8: NO-CONNECT PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	No Connect	NC	—	These pins must be left floating for normal device operation.

3.1 Pin Assignments

TABLE 3-9: 56-QFN PACKAGE PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	nPHY_INT	15	VDD33A	29	EECLK/ PWR_SEL	43	TXEN
2	TXN	16	USBRBIAS	30	EECS	44	RXER
3	TXP	17	VDDUSBPLL	31	EEDO/ AUTOMDIX_EN	45	CRS/GPIO3
4	VDD33A	18	XI	32	EEDI	46	COL/GPIO0 Note 3-4
5	RXN	19	XO	33	TEST3	47	TXCLK
6	RXP	20	VBUS_DET Note 3-4	34	PHY_SEL	48	VDD33IO
7	NC Note 3-3	21	VDDCORE	35	VDD33IO	49	TEST1
8	EXRES	22	MDC/GPIO2	36	nTRST/RXD0	50	VDDCORE
9	VDD33A	23	MDIO/GPIO1 Note 3-4	37	TDO/nPHY_RST	51	VDD33IO
10	VDDPLL	24	nRESET Note 3-4	38	TCK/RXD1	52	VDD33IO
11	USBDM	25	VDD33IO	39	TMS/RXD2	53	TXD3/GPIO7/ EEP_SIZE
12	USBDP	26	nFDX_LED/ GPIO8	40	TDI/RXD3	54	TXD2/GPIO6/ PORT_SWAP
13	TEST2	27	nLNKA_LED/ GPIO9 Note 3-4	41	RXCLK	55	TXD1/GPIO5/ RMT_WKP
14	NC	28	nSPD_LED/ GPIO10 Note 3-4	42	RXDV	56	TXD0/GPIO4/ EEP_DISABLE
EXPOSED PAD MUST BE CONNECTED TO VSS							

Note 3-3 This pin is a no-connect (NC) for LAN9500A/LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500/LAN9500i.

Note 3-4 For LAN9500A/LAN9500Ai this pin provides additional PME related functionality. Refer to the respective pin descriptions and Section 6.0, "PME Operation," on page 112 for additional information.

3.2 Buffer Types

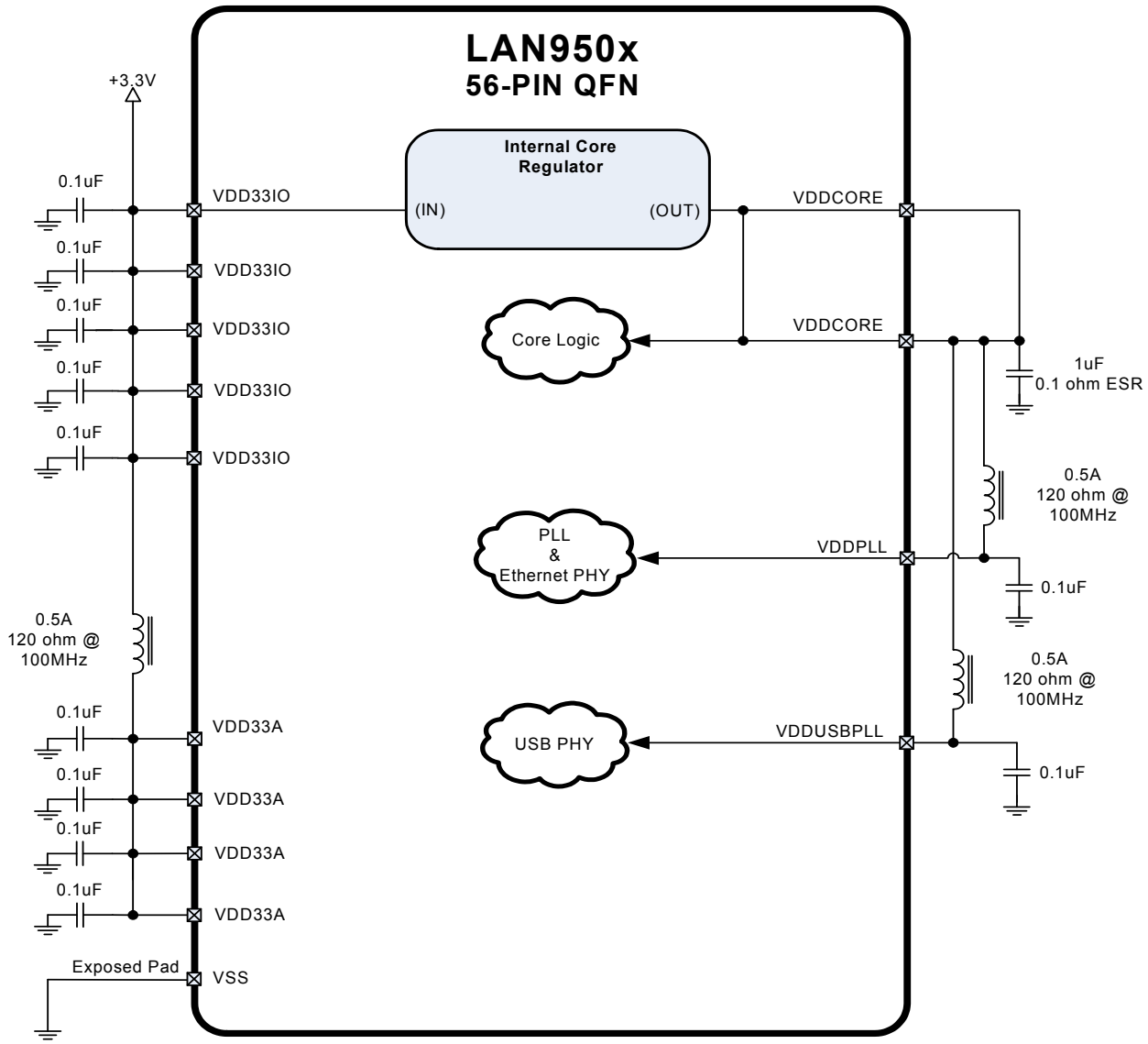
TABLE 3-10: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered Input
IS_5V	5V Tolerant Schmitt-triggered Input
O8	Output with 8 mA sink and 8mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12mA source
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

4.0 POWER CONNECTIONS

Figure 4-1 illustrates the power connections for LAN950x.

FIGURE 4-1: POWER CONNECTIONS



5.0 FUNCTIONAL DESCRIPTION

5.1 Functional Overview

The LAN950x USB 2.0 to 10/100 Ethernet Controller consists of the following major functional blocks:

- USB PHY
- USB 2.0 Device Controller (UDC)
- FIFO Controller (FCT) and Associated SRAM
- 10/100 Ethernet MAC
- 10/100 Internal Ethernet PHY
- IEEE 1149.1 Tap Controller
- EEPROM Controller (EPC)

The following sections discuss the features of each block. A block diagram of the device is shown in Figure 2-1.

5.2 USB PHY

The USB PHY has the USB interface on one end, and connects to the USB 2.0 Device Controller on the other. The Parallel-to-serial/serial-to-parallel conversion, bit stuffing, and NRZI coding / decoding are handled in the PHY block. The PHY is capable of operating in the USB 1.1 and 2.0 modes.

5.3 USB 2.0 Device Controller (UDC)

The USB functionality in the device consists of five major parts. The USB PHY (discussed in Section 5.2), UCB (USB Common Block), UDC (USB Device Controller), URX (USB Bulk Out Receiver), UTX (USB Bulk In Receiver), and CTL (USB Control Block). They are represented as the USB PHY and UDC, collectively, in Figure 2-1.

The UCB generates various clocks, including the system clocks of the device. The URX and UTX implement the Bulk Out and Bulk In endpoints respectively. The CTL manages control and interrupt endpoints.

The UDC is a USB low-level protocol interpreter. The UDC controls the USB bus protocol, packet generation/extraction, PID/Device ID parsing, and CRC coding/decoding with autonomous error handling. It is capable of operating either in USB 1.1 or 2.0 compliant modes. It has autonomous protocol handling functions like stall condition clearing on setup packets, suspend/resume/reset conditions, and remote wakeup. It also autonomously handles error conditions such as retry for CRC errors, Data toggle errors, and generation of NYET, STALL, ACK and NACK, depending on the endpoint buffer status.

The UDC is configured to support one configuration, one interface, one alternate setting, and four endpoints.

5.3.1 SUPPORTED ENDPOINTS

Table 5-1lists the supported endpoints. The following subsections discuss these endpoints in detail.

TABLE 5-1: SUPPORTED ENDPOINTS

Endpoint Number	Description
0	Control Endpoint
1	Bulk In Endpoint
2	Bulk Out Endpoint
3	Interrupt Endpoint

The URX and UTX implement the Bulk Out and Bulk In endpoints, respectively. The CTL manages the Control and Interrupt endpoints.

5.3.1.1 Endpoint 1 (Bulk In)

The Bulk In Endpoint is controlled by the UTX (USB Bulk In Transmitter). The UTX is responsible for encapsulating Ethernet data into a USB Bulk In packet. Ethernet frames are retrieved from the FCT's RX FIFO.

The UTX supports the following two modes of operation: MEF and SEF, selected via the Multiple Ethernet Frames per USB Packet (MEF) bit of the Hardware Configuration Register (HW_CFG).