Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LAN9512/LAN9512i

USB 2.0 Hub and 10/100 Ethernet Controller

Highlights

- Two downstream ports, one upstream port
  - Two integrated downstream USB 2.0 PHYs
  - One integrated upstream USB 2.0 PHY
- Integrated 10/100 Ethernet MAC with full-duplex support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX
- Implements Reduced Power Operating Modes
- Minimized BOM Cost
  - Single 25 MHz crystal (Eliminates cost of separate crystals for USB and Ethernet)
  - Built-in Power-On-Reset (POR) circuit (Eliminates requirement for external passive or active reset)

Target Applications

- Desktop PCs
- Notebook PCs
- Printers
- Game Consoles
- Embedded Systems
- Docking Stations

Key Features

- USB Hub
  - Fully compliant with Universal Serial Bus Specification Revision 2.0
  - HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) compatible
  - Two downstream ports, one upstream port
  - Port mapping and disable support
  - Port Swap: Programmable USB diff-pair pin location
  - PHY Boost: Programmable USB signal drive strength
  - Select presence of a permanently hardwired USB peripheral device on a port by port basis
  - Advanced power saving features
  - Downstream PHY goes into low power mode when port power to the port is disabled
  - Full Power Management with individual or ganged power control of each downstream port.
  - Integrated USB termination Pull-up/Pull-down resistors
  - Internal short circuit protection of USB differential signal pins

Key Features (continued)

- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support with flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP checksum offload support
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - Auto-negotiation, HP Auto-MDIX
    - Automatic polarity detection and correction
    - Energy Detect
- Power and I/Os
  - Three PHY LEDs
  - Eight GPIOs
  - Supports bus-powered and self-powered operation
  - Internal 1.8v core supply regulator
  - External 3.3v I/O supply
- Miscellaneous features
  - Optional EEPROM
  - Optional 24MHz reference clock output for partner hub
  - IEEE 1149.1 (JTAG) Boundary Scan
- Software
  - Windows 2000/XP/Vista Driver
  - Linux Driver
  - Win CE Driver
  - MAC OS Driver
  - EEPROM Utility
- Packaging
  - 64-pin QFN, lead-free RoHS compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)
  - ±8 kV HBM without External Protection Devices
  - ±8 kV contact mode (IEC61000-4-2)
  - ±15 kV air-gap discharge mode (IEC61000-4-2)

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

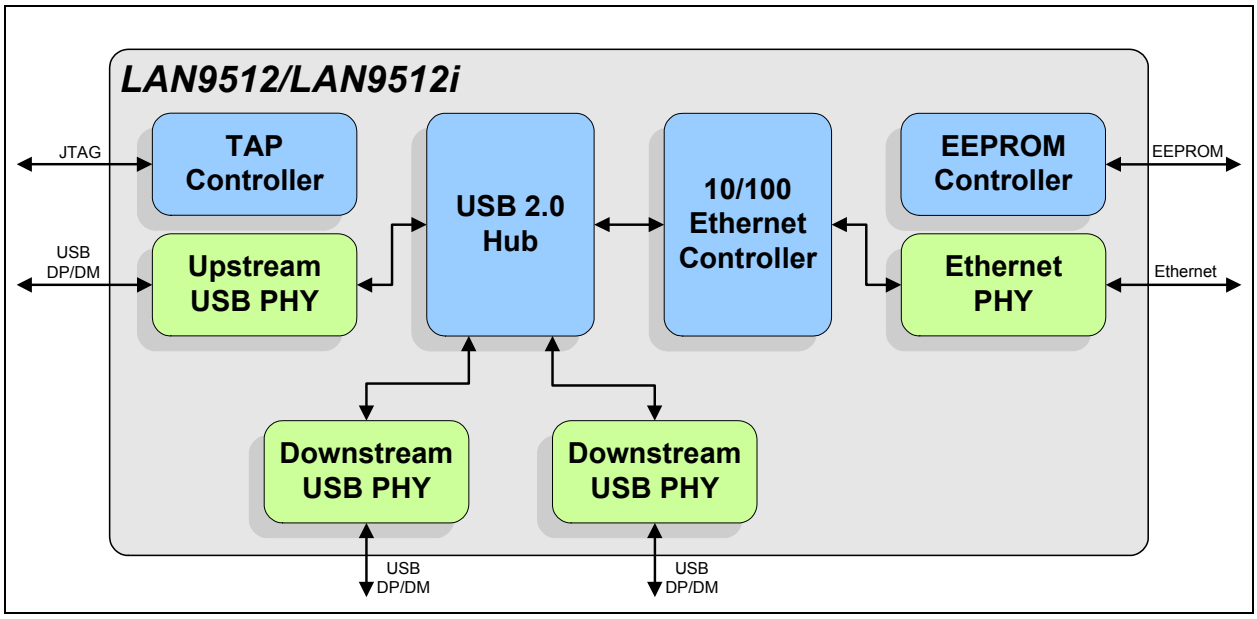
Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 INTRODUCTION

1.1 Block Diagram

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



1.1.1 OVERVIEW

The LAN9512/LAN9512i is a high performance Hi-Speed USB 2.0 hub with a 10/100 Ethernet controller. With applications ranging from embedded systems, desktop PCs, notebook PCs, printers, game consoles, and docking stations, the LAN9512/LAN9512i is targeted as a high performance, low cost USB/Ethernet and USB/USB connectivity solution.

The LAN9512/LAN9512i contains an integrated USB 2.0 hub, two integrated downstream USB 2.0 PHYs, an integrated upstream USB 2.0 PHY, a 10/100 Ethernet PHY, a 10/100 Ethernet Controller, a TAP controller, and a EEPROM controller. A block diagram of the LAN9512/LAN9512i is provided in Figure 1-1.

The LAN9512/LAN9512i hub provides over 30 programmable features, including:

- **PortMap** (also referred to as port remap) which provides flexible port mapping and disabling sequences. The downstream ports of the LAN9512/LAN9512i hub can be reordered or disabled in any sequence to support multiple platform designs' with minimum effort. For any port that is disabled, the LAN9512/LAN9512i automatically reorders the remaining ports to match the USB host controller's port numbering scheme.
- **PortSwap** which adds per-port programmability to USB differential pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost** which enables four programmable levels of USB signal drive strength in USB port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, long cables, etc.

1.1.2 USB HUB

The integrated USB hub is fully compliant with the USB 2.0 Specification and will attach to a USB host as a Full-Speed Hub or as a Full-/High-Speed Hub. The hub supports Low-Speed, Full-Speed, and High-Speed (if operating as a High-Speed hub) downstream devices on all of the enabled downstream ports.

A dedicated Transaction Translator (TT) is available for each downstream facing port. This architecture ensures maximum USB throughput for each connected device when operating with mixed-speed peripherals.

The hub works with an external USB power distributed switch device to control V_{BUS} switching to downstream ports, and to limit current and sense over-current conditions.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Two external ports are available for general USB device connectivity.

1.1.3 ETHERNET CONTROLLER

The 10/100 Ethernet controller provides an integrated Ethernet MAC and PHY which are fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant. The 10/100 Ethernet controller also supports numerous power management wakeup features, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. These wakeup events can be programmed to initiate a USB remote wakeup.

The 10/100 Ethernet PHY integrates an IEEE 802.3 physical layer for twisted pair Ethernet applications. The PHY block includes support for auto-negotiation, full or half-duplex configuration, auto-polarity correction and Auto-MDIX. Minimal external components are required for the utilization of the integrated PHY.

The Ethernet controller implements four USB endpoints: Control, Interrupt, Bulk-in, and Bulk-out. The Bulk-in and Bulk-out Endpoints allow for Ethernet reception and transmission respectively. Implementation of vendor-specific commands allows for efficient statistics gathering and access to the Ethernet controller’s system control and status registers.

1.1.4 EEPROM CONTROLLER

The LAN9512/LAN9512i contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon power-on reset, pin reset, or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration, and the MAC address.

1.1.5 PERIPHERALS

The LAN9512/LAN9512i also contains a TAP controller, and provides three PHY LED indicators, as well as eight general purpose I/O pins. All GPIOs can serve as remote wakeup events when LAN9512/LAN9512i is in a suspended state.

The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

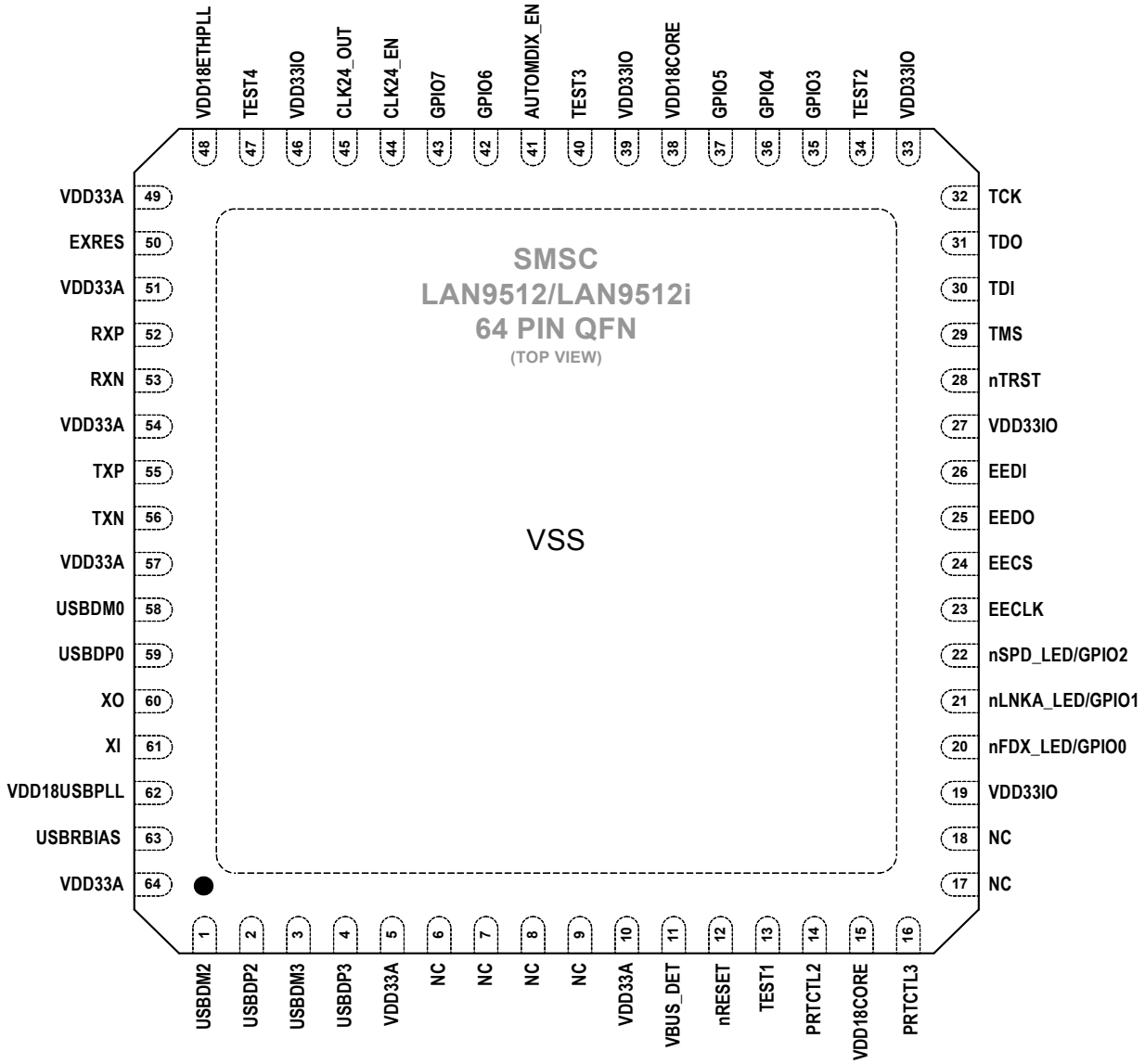
1.1.6 POWER MANAGEMENT

The LAN9512/LAN9512i features three variations of USB suspend: SUSPEND0, SUSPEND1, and SUSPEND2. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, “Wake On LAN”, and “Magic Packet” remote wakeup events. This suspend state reduces power by stopping the clocks of the MAC and other internal modules.
- **SUSPEND1:** Supports GPIO and “Link Status Change” for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the LAN9512/LAN9512i.

2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: LAN9512/LAN9512I 64-QFN PIN ASSIGNMENTS (TOP VIEW)



NOTE: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa

NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

TABLE 2-1: EEPROM PINS

Num PINs	Name	Symbol	Buffer Type	Description
1	EEPROM Data In	EEDI	IS (PD)	This pin is driven by the EEDO output of the external EEPROM.
1	EEPROM Data Out	EEDO	O8	This pin drives the EEDI input of the external EEPROM.
1	EEPROM Chip Select	EECS	O8	This pin drives the chip select output of the external EEPROM.
1	EEPROM Clock	EECLK	O8	This pin drives the EEPROM clock of the external EEPROM.

TABLE 2-2: JTAG PINS

Num PINs	Name	Symbol	Buffer Type	Description
1	JTAG Test Port Reset	nTRST	IS	This active low pin functions as the JTAG test port reset input. **Note:** This pin should be tied high if it is not used.
1	JTAG Test Mode Select	TMS	IS	This pin functions as the JTAG test mode select.
1	JTAG Test Data Input	TDI	IS	This pin functions as the JTAG data input.
1	JTAG Test Data Out	TDO	O12	This pin functions as the JTAG data output.
1	JTAG Test Clock	TCK	IS	This pin functions as the JTAG test clock. This pin should be tied high through a 10 kΩ resistor.

TABLE 2-3: MISCELLANEOUS PINS

Num PINs	Name	Symbol	Buffer Type	Description
1	System Reset	nRESET	IS	This active low pin allows external hardware to reset the device. **Note:** This pin should be tied high if it is not used.
1	Ethernet Full-Duplex Indicator LED	nFDX_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet link is operating in full-duplex mode.
	General Purpose I/O 0	GPIO0	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	Ethernet Link Activity Indicator LED	nLNKA_LED	OD12 (PU)	This pin is driven low (LED on) when a valid link is detected. This pin is pulsed high (LED off) for 80 mS whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80 mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will function as an activity indicator.
	General Purpose I/O 1	GPIO1	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	Ethernet Speed Indicator LED	nSPD_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet operating speed is 100 Mbs, or during auto-negotiation. This pin is driven high during 10Mbs operation, or during line isolation.
	General Purpose I/O 2	GPIO2	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 3	GPIO3	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 4	GPIO4	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 5	GPIO5	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 6	GPIO6	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 7	GPIO7	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.

TABLE 2-3: MISCELLANEOUS PINS (CONTINUED)

Num PINs	Name	Symbol	Buffer Type	Description
1	Detect Upstream VBUS Power	VBUS_DET	IS_5V	This pin detects the state of the upstream bus power. The Hub monitors VBUS_DET to determine when to assert the USBDP0 pin's internal pull-up resistor (signaling a connect event). For bus-powered hubs, this pin must be tied to VDD33IO. For self-powered hubs where the device is permanently attached to a host, VBUS_DET should be pulled to VDD33IO. For other self-powered applications, refer to the device reference schematic for additional connection information.
1	Auto-MDIX Enable	**AUTOMDIX_EN**	IS	Determines the default Auto-MDIX setting. 0 = Auto-MDIX is disabled. 1 = Auto-MDIX is enabled.
1	Test 1	TEST1	—	Used for factory testing, this pin must always be left unconnected.
1	Test 2	TEST2	—	Used for factory testing, this pin must always be connected to VSS for proper operation.
1	Test 3	TEST3	—	Used for factory testing, this pin must always be connected to VDD33IO for proper operation.
1	24 MHz Clock Enable	CLK24_EN	IS	This pin enables the generation of the 24 MHz clock on the CLK_24_OUT pin.
1	24 MHz Clock	CLK24_OUT	08	This pin outputs a 24 MHz clock that can be used a reference clock for a partner hub.
1	Test 4	TEST4	—	Used for factory testing, this pin must always be left unconnected.

TABLE 2-4: USB PINS

Num PINs	Name	Symbol	Buffer Type	Description
1	Upstream USB DMINUS 0	USBDM0	AIO	Upstream USB DMINUS signal.
1	Upstream USB DPLUS 0	USBDP0	AIO	Upstream USB DPLUS signal.
1	Downstream USB DMINUS 2	USBDM2	AIO	Downstream USB peripheral 2 DMINUS signal.
1	Downstream USB DPLUS 2	USBDP2	AIO	Downstream USB peripheral 2 DPLUS signal.

TABLE 2-4: USB PINS (CONTINUED)

Num PINs	Name	Symbol	Buffer Type	Description
1	Downstream USB DMINUS 3	USBDM3	AIO	Downstream USB peripheral 3 DMINUS signal.
1	Downstream USB DPLUS 3	USBDP3	AIO	Downstream USB peripheral 3 DPLUS signal.
1	USB Port Power Control 2	PRTCTL2	IS/OD12 (PU)	When used as an output, this pin enables power to downstream USB peripheral 2. When used as an input, this pin is used to sample the output signal from an external current monitor for downstream USB peripheral 2. An overcurrent condition is indicated when the signal is low. Refer to Section 2.2 for additional information.
1	USB Port Power Control 3	PRTCTL3	IS/OD12 (PU)	When used as an output, this pin enables power to downstream USB peripheral 3. When used as an input, this pin is used to sample the output signal from an external current monitor for downstream USB peripheral 3. An overcurrent condition is indicated when the signal is low. Refer to Section 2.2 for additional information.
1	External USB Bias Resistor	USBRBIAS	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12K 1.0% resistor to ground.
1	USB PLL +1.8V Power Supply	VDD18USBPLL	P	Refer to the LAN9512/LAN9512i reference schematics for additional connection information.
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.

TABLE 2-5: ETHERNET PHY PINS

Num PINs	Name	Symbol	Buffer Type	Description
1	Ethernet TX Data Out Negative	TXN	AIO	Negative output of the Ethernet transmitter. The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet TX Data Out Positive	TXP	AIO	Positive output of the Ethernet transmitter. The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.

TABLE 2-5: ETHERNET PHY PINS (CONTINUED)

Num PINs	Name	Symbol	Buffer Type	Description
1	Ethernet RX Data In Negative	RXN	AIO	Negative input of the Ethernet receiver. The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Positive	RXP	AIO	Positive input of the Ethernet receiver. The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
7	+3.3V Analog Power Supply	VDD33A	P	Refer to the LAN9512/LAN9512i reference schematics for connection information.
1	External PHY Bias Resistor	EXRES	AI	Used for the internal bias circuits. Connect to an external 12.4K 1.0% resistor to ground.
1	Ethernet PLL +1.8V Power Supply	VDD18ETHPLL	P	Refer to the LAN9512/LAN9512i reference schematics for additional connection information.

TABLE 2-6: I/O POWER PINS, CORE POWER PINS, AND GROUND PAD

Num PINs	Name	Symbol	Buffer Type	Description
5	+3.3V I/O Power	VDD33IO	P	+3.3V Power Supply for I/O Pins. Refer to the LAN9512/LAN9512i reference schematics for connection information.
2	Digital Core +1.8V Power Supply Output	VDD18CORE	P	+1.8V power from the internal core voltage regulator. All VDD18CORE pins must be tied together for proper operation. Refer to the LAN9512/LAN9512i reference schematics for connection information.
1 Note 2-1	Ground	VSS	P	Ground

Note 2-1 Exposed pad on package bottom (Figure 2-1).

TABLE 2-7: NO-CONNECT PINS

Num PINs	Name	Symbol	Buffer Type	Description
6	No Connect	NC	—	These pins must be left floating for normal device operation

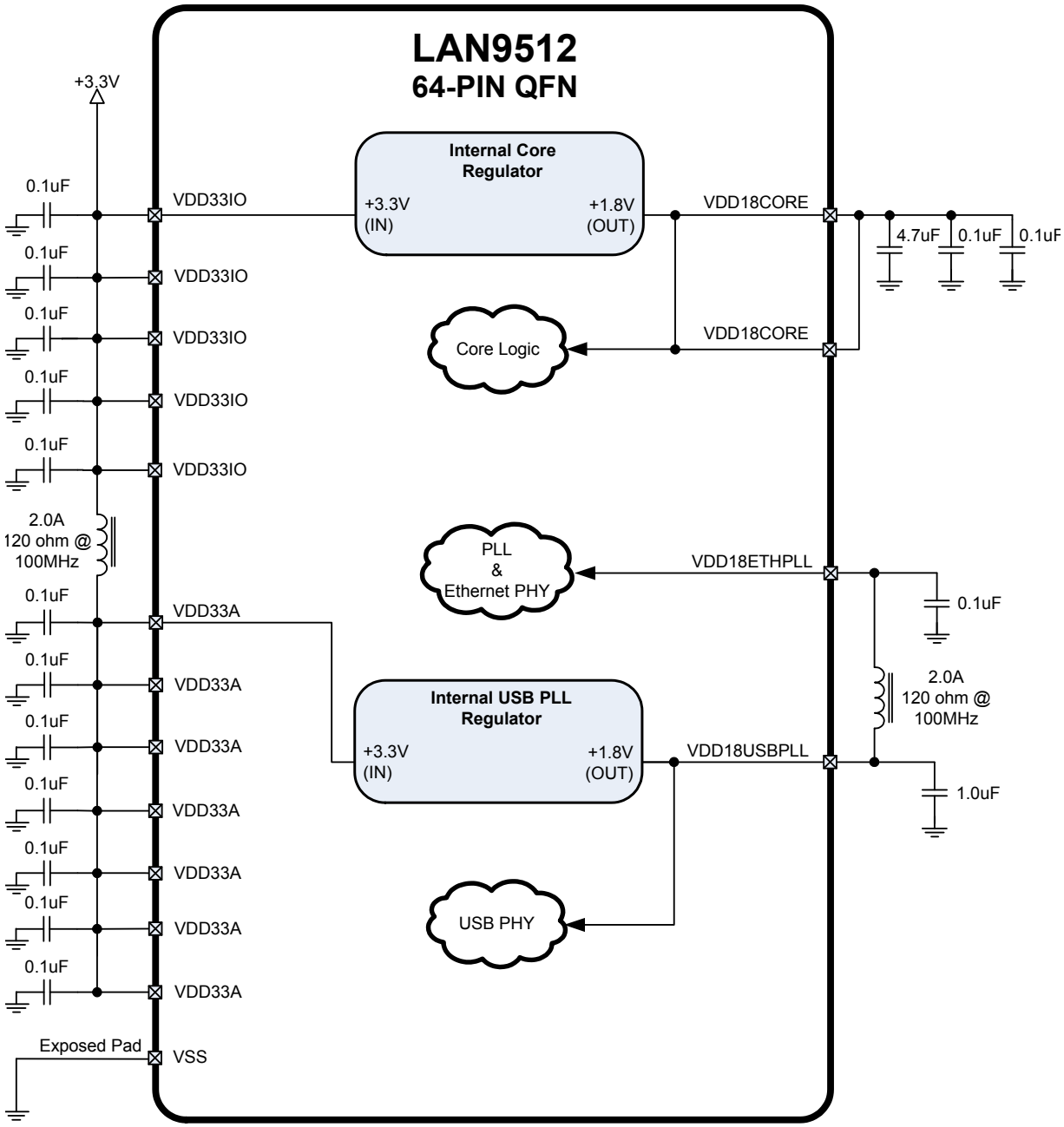
TABLE 2-8: 64-QFN PACKAGE PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	USBDM2	17	NC	33	VDD33IO	49	VDD33A
2	USBDP2	18	NC	34	TEST2	50	EXRES
3	USBDM3	19	VDD33IO	35	GPIO3	51	VDD33A
4	USBDP3	20	nFDX_LED/ GPIO0	36	GPIO4	52	RXP
5	VDD33A	21	nLNKA_LED/ GPIO1	37	GPIO5	53	RXN
6	NC	22	nSPD_LED/ GPIO2	38	VDD18CORE	54	VDD33A
7	NC	23	EECLK	39	VDD33IO	55	TXP
8	NC	24	EECS	40	TEST3	56	TXN
9	NC	25	EEDO	41	AUTOMDIX_EN	57	VDD33A
10	VDD33A	26	EEDI	42	GPIO6	58	USBDM0
11	VBUS_DET	27	VDD33IO	43	GPIO7	59	USBDP0
12	nRESET	28	nTRST	44	CLK24_EN	60	XO
13	TEST1	29	TMS	45	CLK24_OUT	61	XI
14	PRTCTL2	30	TDI	46	VDD33IO	62	VDD18USBPLL
15	VDD18CORE	31	TDO	47	TEST4	63	USBRBIAS
16	PRTCTL3	32	TCK	48	VDD18ETHPLL	64	VDD33A
EXPOSED PAD MUST BE CONNECTED TO VSS							

2.1 Power Connections

Figure 2-2 illustrates the power connections for LAN9512/LAN9512i.

FIGURE 2-2: POWER CONNECTIONS



2.2 Port Power Control

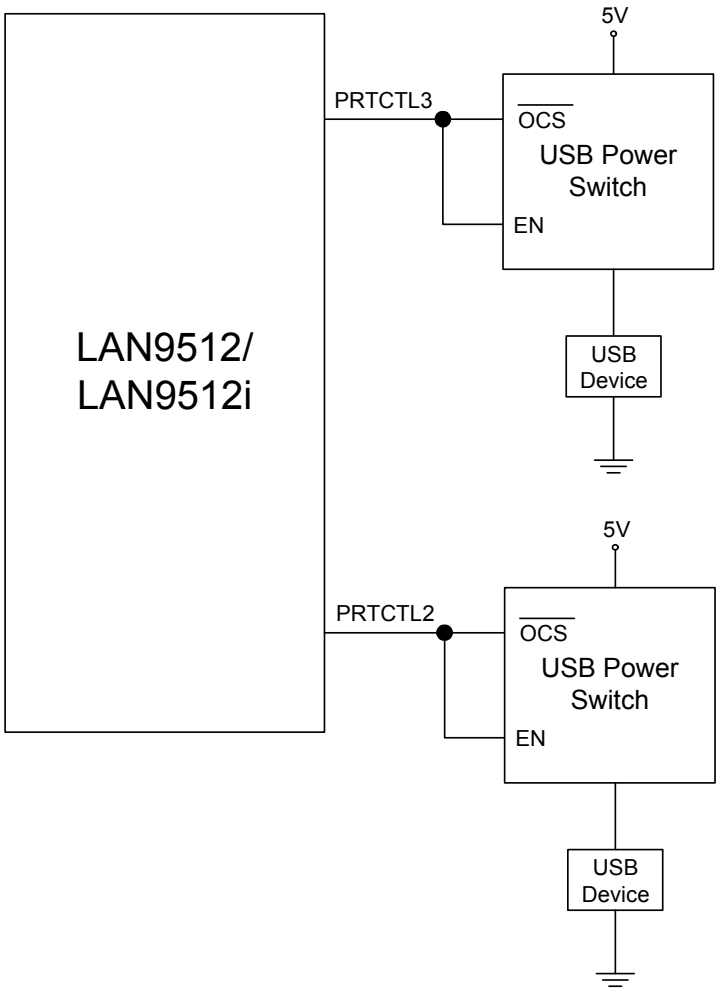
This section details the usage of the port power control pins PRTCTL[3:2].

2.2.1 PORT POWER CONTROL USING A USB POWER SWITCH

The LAN9512/LAN9512i has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a ‘0’. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled and the pull-up resistor is

enabled, creating an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will recognize this situation as a low. The open drain output does not interfere. The overcurrent sense filter handles the transient conditions, such as low voltage, while the device is powering up.

FIGURE 2-3: PORT POWER CONTROL WITH USB POWER SWITCH

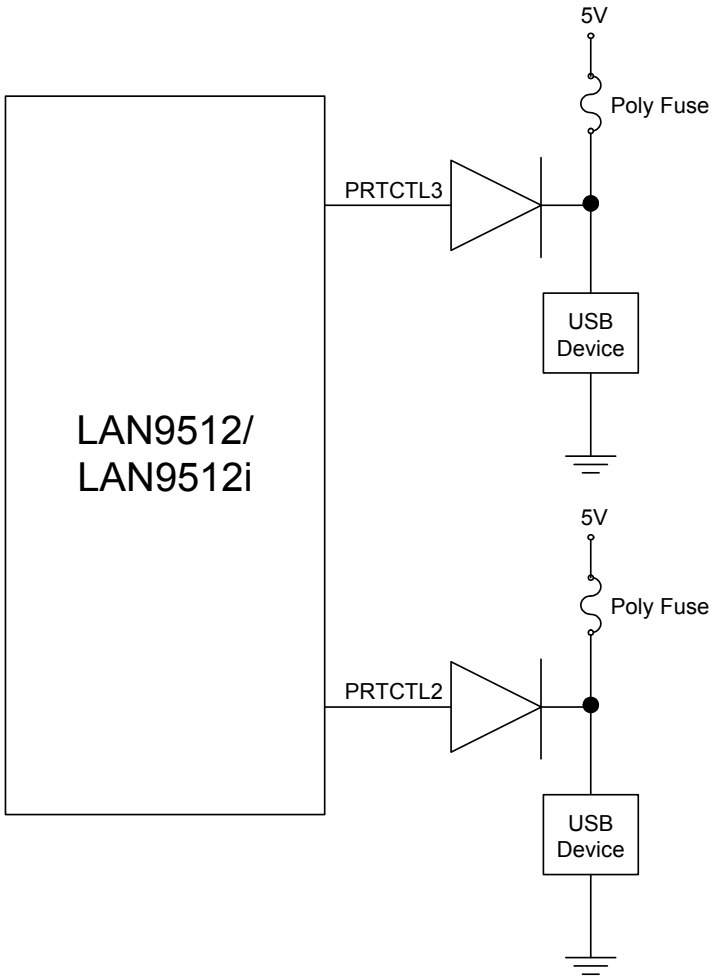


2.2.2 PORT POWER CONTROL USING A POLY FUSE

When using the LAN9512/LAN9512i with a poly fuse, an external diode must be used (See Figure 2-4). When disabling port power, the driver will drive a '0'. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the output driver is disabled and the pull-up resistor is enabled, which creates an open drain output. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-

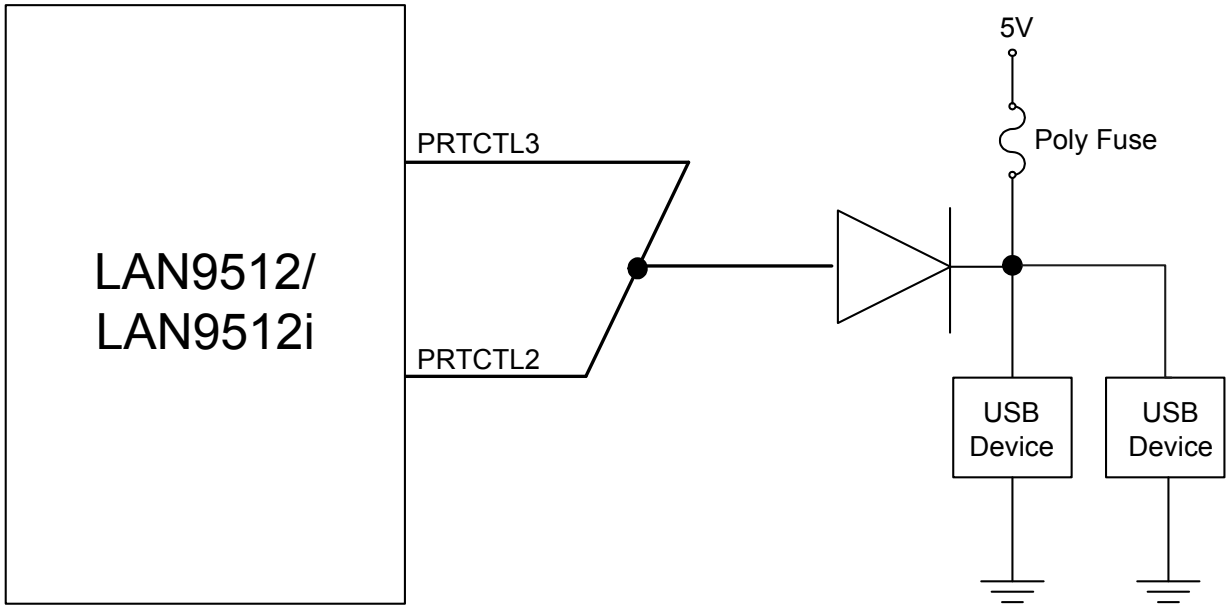
current situation, the poly fuse will open. This will cause the cathode of the diode to go to 0_volts. The anode of the diode will be at 0.7_volts, and the Schmidt trigger input will register this as a low, resulting in an overcurrent detection. The open drain output does not interfere.

FIGURE 2-4: PORT POWER CONTROL WITH POLY FUSE



Many customers use a single poly fuse to power all their devices. For the ganged situation, all power control pins must be tied together.

FIGURE 2-5: PORT POWER WITH GANGED CONTROL WITH POLY FUSE



2.3 Buffer Types

TABLE 2-9: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered Input
IS_5V	5V Tolerant Schmitt-triggered Input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to LAN9512/LAN9512i. When connected to a load that must be pulled high, an external resistor must be added.

TABLE 2-9: BUFFER TYPES (CONTINUED)

Buffer Type	Description
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to LAN9512/LAN9512i. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

3.0 EEPROM CONTROLLER (EPC)

LAN9512/LAN9512i may use an external EEPROM to store the default values for the USB descriptors and the MAC address. The EEPROM controller supports most “93C46” type EEPROMs. A total of nine address bits are used to support 256/512 byte EEPROMs.

A 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation must be used.

The MAC address is used as the default Ethernet MAC address and is loaded into the MAC’s ADDRH and ADDRL registers. If a properly configured EEPROM is not detected, it is the responsibility of the Host LAN Driver to set the IEEE addresses.

After a system-level reset occurs, the device will load the default values from a properly configured EEPROM. The device will not accept USB transactions from the Host until this process is completed.

The EEPROM controller also allows the Host system to read, write and erase the contents of the Serial EEPROM.

3.1 EEPROM Format

Table 3-1 illustrates the format in which data is stored inside of the EEPROM.

Note the EEPROM offsets are given in units of 16-bit word offsets. A length field with a value of zero indicates that the field does not exist in the EEPROM. The device will use the field’s HW default value in this case.

Note: For Device Descriptors, the only valid values for the length are 0 and 18.

Note: For Configuration and Interface Descriptors, the only valid values for the length are 0 and 18.

Note: The EEPROM programmer must ensure that if a String Descriptor does not exist in the EEPROM, the referencing descriptor must contain 00h for the respective string index field.

Note: If no Configuration Descriptor is present in the EEPROM, then the Configuration Flags affect the values of bmAttributes and bMaxPower in the Ethernet Controller Configuration Descriptor.

Note: If all String Descriptor lengths are zero, then a Language ID will not be supported.

TABLE 3-1: EEPROM FORMAT

EEPROM Address	EEPROM Contents
00h	0xA5
01h	MAC Address [7:0]
02h	MAC Address [15:8]
03h	MAC Address [23:16]
04h	MAC Address [31:24]
05h	MAC Address [39:32]
06h	MAC Address [47:40]
07h	Full-Speed Polling Interval for Interrupt Endpoint
08h	Hi-Speed Polling Interval for Interrupt Endpoint
09h	Configuration Flags
0Ah	Language ID Descriptor [7:0]
0Bh	Language ID Descriptor [15:8]
0Ch	Manufacturer ID String Descriptor Length (bytes)
0Dh	Manufacturer ID String Descriptor EEPROM Word Offset

TABLE 3-1: EEPROM FORMAT (CONTINUED)

EEPROM Address	EEPROM Contents
0Eh	Product Name String Descriptor Length (bytes)
0Fh	Product Name String Descriptor EEPROM Word Offset
10h	Serial Number String Descriptor Length (bytes)
11h	Serial Number String Descriptor EEPROM Word Offset
12h	Configuration String Descriptor Length (bytes)
13h	Configuration String Descriptor Word Offset
14h	Interface String Descriptor Length (bytes)
15h	Interface String Descriptor Word Offset
16h	Hi-Speed Device Descriptor Length (bytes)
17h	Hi-Speed Device Descriptor Word Offset
18h	Hi-Speed Configuration and Interface Descriptor Length (bytes)
19h	Hi-Speed Configuration and Interface Descriptor Word Offset
1Ah	Full-Speed Device Descriptor Length (bytes)
1Bh	Full-Speed Device Descriptor Word Offset
1Ch	Full-Speed Configuration and Interface Descriptor Length (bytes)
1Dh	Full-Speed Configuration and Interface Descriptor Word Offset
1Eh-1Fh	RESERVED
20h	Vendor ID LSB Register (VIDL)
21h	Vendor ID MSB Register (VIDM)
22h	Product ID LSB Register (PIDL)
23h	Product ID MSB Register (PIDM)
24h	Device ID LSB Register (DIDL)
25h	Device ID MSB Register (DIDM)
26h	Config Data Byte 1 Register (CFG1)
27h	Config Data Byte 2 Register (CFG2)
28h	Config Data Byte 3 Register (CFG3)
29h	Non-Removable Devices Register (NRD)
2Ah	Port Disable (Self) Register (PDS)
2Bh	Port Disable (Bus) Register (PDB)
2Ch	Max Power (Self) Register (MAXPS)
2Dh	Max Power (Bus) Register (MAXPB)
2Eh	Hub Controller Max Current (Self) Register (HCMCS)

TABLE 3-1: EEPROM FORMAT (CONTINUED)

EEPROM Address	EEPROM Contents
2Fh	Hub Controller Max Current (Bus) Register (HCMCB)
30h	Power-on Time Register (PWRT)
31h	Boost_Up Register (BOOSTUP)
32h	RESERVED
33h	Boost_3:2 Register (BOOST32)
34h	RESERVED
35h	Port Swap Register (PRTSP)
36h	Port Remap 12 Register (PRTR12)
37h	Port Remap 3 Register (PRTR3)
38h	RESERVED
39h	Status/Command Register (STCD)

Note: EEPROM byte addresses past 39h can be used to store data for any purpose.

Table 3-2 describes the Configuration Flags

TABLE 3-2: CONFIGURATION FLAGS DESCRIPTION

Bit	Name	Description
7:3	**RESERVED**	00000b
2	Remote Wakeup Support	0 = The device does not support remote wakeup. 1 = The device supports remote wakeup.
1	**RESERVED**	0b
0	Power Method	0 = The device Controller is bus-powered. 1 = The device Controller is self-powered.

3.1.1 HUB CONFIGURATION

EEPROM offsets 20h through 39h comprise the Hub Configuration parameters. Table 3-3 describes these parameters and their default ROM values (Values assumed if no valid EEPROM present).

TABLE 3-3: HUB CONFIGURATION

EEPROM Offset	Description	Default
20h	**Vendor ID LSB Register (VIDL)** Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum).	24h

TABLE 3-3: HUB CONFIGURATION (CONTINUED)

EEPROM Offset	Description	Default
21h	**Vendor ID MSB (VIDM)** Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum).	04h
22h	**Product ID LSB Register (PIDL)** Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by the OEM).	12h
23h	**Product ID MSB Register (PIDM)** Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by the OEM).	95h
24h	**Device ID LSB Register (DIDL)** Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by the OEM).	00h
25h	**Device ID MSB Register (DIDM)** Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by the OEM).	Note 3-1
26h	**Config Data Byte 1 Register (CFG1)** Refer to Table 3-4, “Config Data Byte 1 Register (CFG1) Format,” on page 26 for details.	9Bh
27h	**Config Data Byte 2 Register (CFG2)** Refer to Table 3-5, “Config Data Byte 2 Register (CFG2) Format,” on page 27 for details.	18h
28h	**Config Data Byte 3 Register (CFG3)** Refer to Table 3-6, “Config Data Byte 3 Register (CFG3) Format,” on page 27 for details.	00h
29h	**Non-Removable Devices Register (NRD)** Indicates which port(s) include non-removable devices. 0 = Port is removable 1 = Port is non-removable Informs the host if one of the active ports has a permanent device that is not detachable from the Hub. **Note:** The device must provide its own descriptor data. Bit 7 = RESERVED Bit 6 = RESERVED Bit 5 = RESERVED Bit 4 = RESERVED Bit 3 = 1; Port 3 non-removable Bit 2 = 1; Port 2 non-removable Bit 1 = 1; Port 1 non-removable Bit 0 is RESERVED, always = 0b **Note:** Bit 1 must be set to 1 by firmware for proper identification of the Ethernet Controller as a non-removable device.	02h

TABLE 3-3: HUB CONFIGURATION (CONTINUED)

EEPROM Offset	Description	Default
2Ah	**Port Disable (Self) Register (PDS)** Disables 1 or more ports. 0 = Port is available 1 = Port is disabled During Self-Powered operation, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function. Bit 7 = RESERVED Bit 6 = RESERVED Bit 5 = RESERVED Bit 4 = RESERVED Bit 3 = 1; Port 3 disabled Bit 2 = 1; Port 2 disabled Bit 1 = 1; Port 1 disabled Bit 0 is RESERVED, always = 0b	30h
2Bh	**Port Disable (Bus) Register (PDB)** Disables 1 or more ports. 0 = Port is available 1 = Port is disabled During Bus-Powered operation, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function. Bit 7 = RESERVED Bit 6 = RESERVED Bit 5 = RESERVED Bit 4 = RESERVED Bit 3 = 1; Port 3 disabled Bit 2 = 1; Port 2 disabled Bit 1 = 1; Port 1 disabled Bit 0 is RESERVED, always = 0b	30h
2Ch	**Max Power (Self) Register (MAXPS)** Value in 2 mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA.	01h
2Dh	**Max Power (Bus) Register (MAXPB)** Value in 2 mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.	00h

TABLE 3-3: HUB CONFIGURATION (CONTINUED)

EEPROM Offset	Description	Default
2Eh	**Hub Controller Max Current (Self) Register (HCMCS)** Value in 2 mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB 2.0 Specification does not permit this value to exceed 100mA.	01h
2Fh	**Hub Controller Max Current (Bus) Register (HCMCB)** Value in 2 mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.	00h
30h	**Power-on Time Register (PWRT)** The length of time that it takes (in 2 mS intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. System software uses this value to determine how long to wait before accessing a powered-on port.	32h
31h	**Boost_Up Register (BOOSTUP)** Refer to Table 3-7, “Boost_Up Register (BOOSTUP) Format,” on page 28 for details.	00h
32h	**RESERVED**	00h
33h	**Boost_3:2 Register (BOOST32)** Refer to Table 3-8, “Boost_4:2 Register (BOOST42) Format,” on page 28 for details.	00h
34h	**RESERVED**	00h
35h	**Port Swap Register (PRTSP)** Swaps the Upstream and Downstream USB DP and DM pins for ease of board routing to devices and connectors. 0 = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. 1 = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 = RESERVED Bit 6 = RESERVED Bit 5 = RESERVED Bit 4 = RESERVED Bit 3 = 1; Port 3 DP/DM is swapped Bit 2 = 1; Port 2 DP/DM is swapped Bit 1 = RESERVED Bit 0 = 1; Upstream Port DP/DM is swapped	00h

TABLE 3-3: HUB CONFIGURATION (CONTINUED)

<table>
<tr><th>EEPROM Offset</th><th>Description</th><th>Default</th></tr>
<tr><td>36h</td><td>
Port Remap 12 Register (PRTR12)
When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has. The hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.

The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the "Physical Port Number". When remapping mode is enabled, (see Port Re-Mapping Enable (PRTMAP_EN) bit in Config Data Byte 3 Register (CFG3) Format) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: The OEM must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports. This ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.
<table>
<tr><td>Bit [7:4] =</td><td>0000</td><td>Physical Port 2 is Disabled</td></tr>
<tr><td></td><td>0001</td><td>Physical Port 2 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>0010</td><td>Physical Port 2 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>0011</td><td>Physical Port 2 is mapped to Logical Port 3</td></tr>
<tr><td></td><td></td><td>All others RESERVED</td></tr>
<tr><td>Bit [3:0] =</td><td>0000</td><td>Physical Port 1 is Disabled</td></tr>
<tr><td></td><td>0001</td><td>Physical Port 1 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>0010</td><td>Physical Port 1 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>0011</td><td>Physical Port 1 is mapped to Logical Port 3</td></tr>
<tr><td></td><td></td><td>All others RESERVED</td></tr>
</table>
</td><td>21h</td></tr>
</table>

TABLE 3-3: HUB CONFIGURATION (CONTINUED)

<table>
<tr><th>EEPROM Offset</th><th>Description</th><th>Default</th></tr>
<tr><td>37h</td><td>Port Remap 3 Register (PRTR3)
When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has. The hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.

The host's port number is referred to as "Logical Port Number" and the physical port on the hub is the "Physical Port Number". When remapping mode is enabled (see Port Re-Mapping Enable (PRTMAP_EN) bit in Config Data Byte 3 Register (CFG3) Format), the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: The OEM must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports, this ensures that the hub's ports are numbered in accordance with the way a Host will communicate with the ports.

<table>
<tr><td>Bit [7:4] =</td><td>—</td><td>RESERVED</td></tr>
<tr><td>Bit [3:0] =</td><td>0000</td><td>Physical Port 3 is Disabled</td></tr>
<tr><td></td><td>0001</td><td>Physical Port 3 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>0010</td><td>Physical Port 3 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>0011</td><td>Physical Port 3 is mapped to Logical Port 3</td></tr>
<tr><td></td><td></td><td>All others RESERVED</td></tr>
</table>
</td><td>03h</td></tr>
<tr><td>38h</td><td>RESERVED</td><td>00h</td></tr>
<tr><td>39h</td><td>Status/Command Register (STCD)
Refer to Table 3-9, "Status/Command Register (STCD) Format," on page 29 for details.</td><td>01h</td></tr>
</table>

Note 3-1 Default value is dependent on device revision.