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# LAN9730/LAN9730i

# High-Speed Inter-Chip (HSIC) USB 2.0 to 10/100 Ethernet Controller

## PRODUCT FEATURES

**Datasheet**

### Highlights

- Single Chip HSIC USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX Support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated HSIC Interface
- Implements Reduced Power Operating Modes

### Target Applications

- Embedded Systems
- Set-Top Boxes
- PVRs
- CE Devices
- Networked Printers
- USB Port Replicators
- Test Instrumentation
- Industrial

### Key Features

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification, revision 2.0
  - Supports HS (480 Mbps) mode
  - Four Endpoints supported
  - Supports vendor specific commands
  - Integrated HSIC Interface
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE 802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for three status LEDs
  - External MII and Turbo MII support HomePNA® and HomePlug® PHY
- Power and I/Os
  - Various low power modes
  - Supports PCI-like PME wake when USB Host disabled
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - Single external 3.3 V I/O supply
    - Optional internal core regulator
- Miscellaneous Features
  - EEPROM controller
  - Supports custom operation without EEPROM
  - IEEE 1149.1 (JTAG) boundary scan
  - Requires single 25 MHz crystal
- Software
  - Windows® 7/XP/Vista driver
  - Linux® driver
  - Win CE driver
  - MAC® OS driver
  - EEPROM utility
- Packaging
  - 56-pin QFN (8x8 mm) lead-free, RoHS compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

**Order Numbers:**

**LAN9730-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp)**

**LAN9730i-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp)**

**LAN9730-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp)**

**LAN9730i-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp)**

**This product meets the halogen maximum concentration values per IEC61249-2-21**

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# Chapter 1 Introduction

## 1.1 Block Diagram

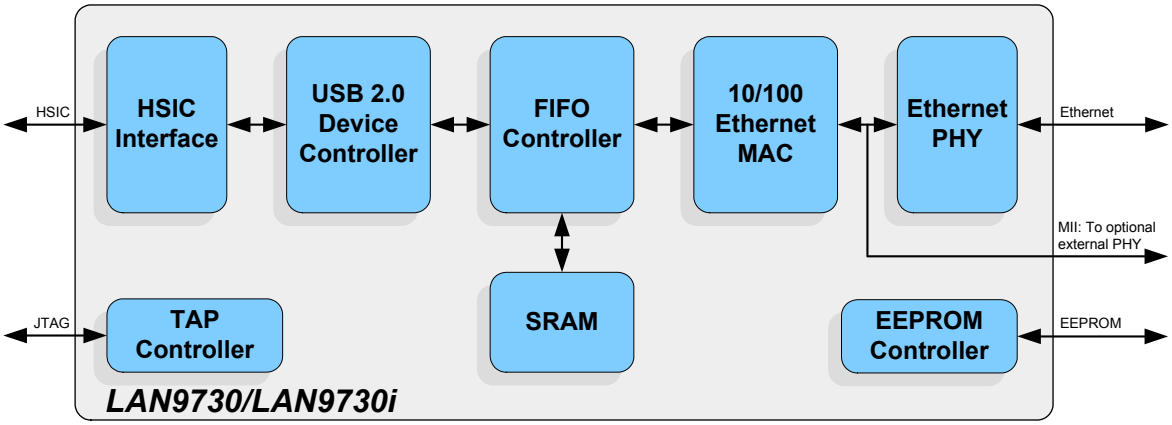


**Figure 1.1 LAN9730/LAN9730i Block Diagram**

## 1.2 Overview

The LAN9730/LAN9730i is a high performance solution for USB to 10/100 Ethernet port bridging. With applications ranging from embedded systems, set-top boxes, and PVRs, to USB port replicators, and test instrumentation, the device is targeted as a high-performance, low-cost USB/Ethernet connectivity solution.

The LAN9730/LAN9730i contains an integrated 10/100 Ethernet PHY, HSIC interface, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 kB of internal packet buffering.

The internal USB 2.0 device controller is compliant with the USB 2.0 Hi-Speed standard. The HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0. High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. The device implements Control, Interrupt, Bulk-in and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low-power modes, and Magic Packet, Wake On LAN and Link Status Change wake events. These wake events can be programmed to initiate a USB remote wakeup. A PCI-like PME wake is also supported when the Host controller is disabled.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

### 1.2.1 USB

The USB portion of the LAN9730/LAN9730i integrates a Hi-Speed USB 2.0 device controller and HSIC interface.

The USB device controller (UDC) contains a USB low-level protocol interpreter which implements the USB bus protocol, packet generation/extraction, PID/Device ID parsing and CRC coding/decoding, with autonomous error handling. The USB device controller is capable of operating in USB 2.0 Hi-Speed mode and contains autonomous protocol handling functions such as handling of suspend/resume/reset conditions, remote wakeup, and stall condition clearing on Setup packets. The USB device controller also autonomously handles error conditions such as retry for CRC and data toggle errors, and generates NYET, STALL, ACK and NACK handshake responses, depending on the Endpoint buffer status.

The LAN9730/LAN9730i implements four USB Endpoints: Control, Interrupt, Bulk-in, and Bulk-out. The Bulk-in and Bulk-out Endpoints allow for Ethernet reception and transmission respectively. Implementation of vendor-specific commands allows for efficient statistics gathering and access to the device's system control and status registers.

The integrated HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0 (09-23-07) and supports the Hi-Speed mode of operation.

### 1.2.2 FIFO Controller

The FIFO controller uses an internal SRAM to buffer RX and TX traffic. Bulk-out packets from the USB controller are directly stored into the TX buffer. Ethernet frames are directly stored into the RX buffer and become the basis for bulk-in packets.

### 1.2.3 Ethernet

LAN9730/LAN9730i integrates an IEEE 802.3 PHY for twisted pair Ethernet applications and a 10/100 Ethernet Media Access Controller (MAC).

The PHY can be configured for either 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) Ethernet operation in either Full or Half Duplex configurations. The PHY block includes auto-negotiation, auto-polarity correction, and Auto-MDIX. Minimal external components are required for the utilization of the Integrated PHY.

Optionally, an external PHY may be used via the MII (Media Independent Interface) port, effectively bypassing the internal PHY. This option allows support for HomePNA and HomePlug applications.

The Ethernet MAC/PHY supports numerous power management wakeup features, including Magic Packet, Wake on LAN and Link Status Change. Eight wakeup frame filters are provided by the device.

### 1.2.4 Power Management

The LAN9730/LAN9730i features four variations of USB suspend: SUSPEND0, SUSPEND1, SUSPEND2 and SUSPEND3. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, Wake On LAN and Magic Packet events. This state reduces power by stopping the clocks of the MAC and other internal modules.
- **SUSPEND1:** Supports GPIO and Link Status Change for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the device.
- **SUSPEND3:** Supports GPIO and Good Packet events. A Good Packet is a received frame passing certain filtering constraints independent of those imposed on Wake On LAN and Magic Packet frames. This suspend state consumes power at a level similar to the full operational state, however, it allows for power savings in the Host CPU.

### 1.2.5 EEPROM Controller (EPC)

LAN9730/LAN9730i contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon power-on reset, pin reset or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration and MAC address.

### 1.2.6 General Purpose I/O

When configured for Internal PHY Mode, up to eleven GPIOs are supported. All GPIOs can serve as remote wakeup events when the LAN9730/LAN9730i is suspended.

### 1.2.7 System Software

LAN9730/LAN9730i software drivers are available for the following operating systems:

- Windows 7
- Windows Vista
- Windows XP
- Linux
- Win CE
- MAC OS

In addition, an EEPROM programming utility is available for configuring the external EEPROM.

# Chapter 2 Pin Description and Configuration

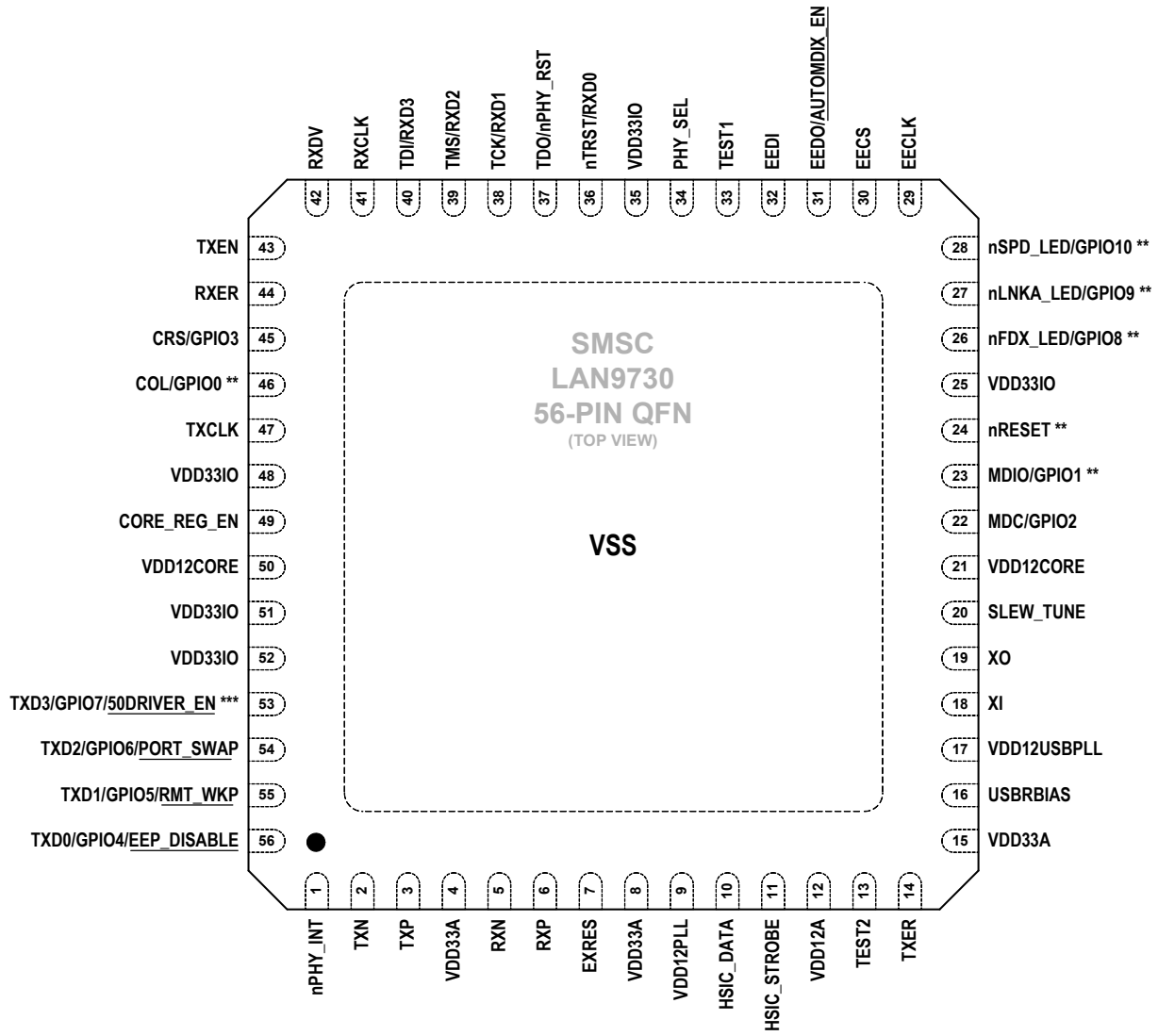


**Figure 2.1 Pin Assignments (TOP VIEW)**

**Note:** ** This pin provides additional PME related functionality. Refer to the respective pin descriptions and Chapter 5, "PME Operation," on page 37 for additional information.

**Note:** *** GPIO7 may provide additional PHY Link Up related functionality.

**Note:** When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa.

**Note:** Exposed pad (VSS) on bottom of package must be connected to ground.

**Table 2.1 MII Interface Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Receive Error (Internal PHY Mode) | RXER | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Receive Error (External PHY Mode) | RXER | IS (PD) | In External PHY Mode, the signal on this pin is input from the external PHY and indicates a receive error in the packet. |
| 1 | Transmit Error (Internal PHY Mode) | TXER | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Error (External PHY Mode) | TXER | O8 (PD) | In External PHY Mode, this pin functions as an output to the external PHY and indicates a transmit error. |
| 1 | Transmit Enable (Internal PHY Mode) | TXEN | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Enable (External PHY Mode) | TXEN | O8 (PD) | In External PHY Mode, this pin functions as an output to the external PHY and indicates valid data on TXD[3:0]. |
| 1 | Receive Data Valid (Internal PHY Mode) | RXDV | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Receive Data Valid (External PHY Mode) | RXDV | IS (PD) | In External PHY Mode, the signal on this pin is input from the external PHY and indicates valid data on RXD[3:0]. |
| 1 | Receive Clock (Internal PHY Mode) | RXCLK | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Receive Clock (External PHY Mode) | RXCLK | IS (PD) | In External PHY Mode, this pin is the receiver clock input from the external PHY. |
| 1 | Transmit Clock (Internal PHY Mode) | TXCLK | IS/O8 (PU) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Clock (External PHY Mode) | TXCLK | IS (PU) | In External PHY Mode, this pin is the transmitter clock input from the external PHY. |

**Table 2.1 MII Interface Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Carrier Sense (Internal PHY Mode) | CRS | IS/O8 (PU) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Carrier Sense (External PHY Mode) | CRS | IS (PD) | In External PHY Mode, the signal on this pin is input from the external PHY and indicates a network carrier. |
| | General Purpose I/O 3 (Internal PHY Mode Only) | GPIO3 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. |
| 1 | MII Collision Detect (Internal PHY Mode) | COL | IS/O8 (PU) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | MII Collision Detect (External PHY Mode) | COL | IS (PD) | In External PHY Mode, the signal on this pin is input from the external PHY and indicates a collision event. |
| | General Purpose I/O 0 (Internal PHY Mode Only) | GPIO0 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.<br>**Note:** This pin may be used to signal PME when Internal PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information. |
| 1 | Management Data (Internal PHY Mode) | MDIO | IS/O8 (PU) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Management Data (External PHY Mode) | MDIO | IS/O8 (PD) | In External PHY Mode, this pin provides the management data to/from the external PHY. |
| | General Purpose I/O 1 (Internal PHY Mode Only) | GPIO1 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.<br>**Note:** This pin may serve as the PME_MODE_SEL input when Internal PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information. |

**Table 2.1 MII Interface Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Management Clock (Internal PHY Mode) | MDC | IS/O8 (PU) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Management Clock (External PHY Mode) | MDC | O8 (PD) | In External PHY Mode, this pin outputs the management clock to the external PHY. |
| | General Purpose I/O 2 (Internal PHY Mode Only) | GPIO2 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. |
| 1 | Transmit Data 3 (Internal PHY Mode) | TXD3 | IS/O8 (PU) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Data 3 (External PHY Mode) | TXD3 | O8 (PU) | In External PHY Mode, this pin functions as the transmit data 3 output to the external PHY. |
| | General Purpose I/O 7 (Internal PHY Mode Only) | GPIO7 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.<br>**Note:** GPIO7 may provide additional external PHY Link Up related functionality. |
| | HSIC Output Impedance Configuration Strap | 50DRIVER_EN | IS (PU) | The 50DRIVER_EN strap selects the driver output impedance for the HSIC_DATA and HSIC_STROBE pins.<br>0 = 40 Ω output impedance<br>1 = 50 Ω output impedance<br>See Note 2.1 for more information on configuration straps. |

**Table 2.1 MII Interface Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Transmit Data 2 (Internal PHY Mode) | TXD2 | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Data 2 (External PHY Mode) | TXD2 | O8 (PD) | In External PHY Mode, this pin functions as the transmit data 2 output to the external PHY. |
| | General Purpose I/O 6 (Internal PHY Mode Only) | GPIO6 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. |
| | HSIC Port Swap Configuration Strap | PORT_SWAP | IS (PD) | Swaps the mapping of HSIC_DATA and HSIC_STROBE.<br><br>0 = The HSIC_DATA and HSIC_STROBE pin functionality is not swapped.<br><br>1 = The HSIC_DATA and HSIC_STROBE pin functionality is swapped.<br><br>See Note 2.1 for more information on configuration straps. |
| 1 | Transmit Data 1 (Internal PHY Mode) | TXD1 | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Data 1 (External PHY Mode) | TXD1 | O8 (PD) | In External PHY Mode, this pin functions as the transmit data 1 output to the external PHY. |
| | General Purpose I/O 5 (Internal PHY Mode Only) | GPIO5 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. |
| | Remote Wakeup Configuration Strap | RMT_WKP | IS (PD) | This strap configures the default descriptor values to support remote wakeup. This strap is overridden by the EEPROM.<br><br>0 = Remote wakeup is not supported.<br>1 = Remote wakeup is supported.<br><br>See Note 2.1 for more information on configuration straps. |

**Table 2.1 MII Interface Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Transmit Data 0 (Internal PHY Mode) | TXD0 | IS/O8 (PD) | In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. |
| | Transmit Data 0 (External PHY Mode) | TXD0 | O8 (PD) | In External PHY Mode, this pin functions as the transmit data 0 output to the external PHY. |
| | General Purpose I/O 4 (Internal PHY Mode Only) | GPIO4 | IS/O8/ OD8 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. |
| | EEPROM Disable Configuration Strap | EEP_DISABLE | IS (PD) | This strap disables the autoloading of the EEPROM contents. The assertion of this strap does not prevent register access to the EEPROM.<br><br>0 = EEPROM is recognized if present.<br>1 = EEPROM is not recognized even if it is present.<br><br>See Note 2.1 for more information on configuration straps. |

**Table 2.2 EEPROM Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | EEPROM Data In | EEDI | IS (PD) | This pin is driven by the EEDO output of the external EEPROM. |
| 1 | EEPROM Data Out | EEDO | O8 (PU) | This pin drives the EEDI input of the external EEPROM. |
| 1 | Auto-MDIX Enable Configuration Strap | AUTOMDIX_EN | IS (PU) | Determines the default Auto-MDIX setting.<br>0 = Auto-MDIX is disabled.<br>1 = Auto-MDIX is enabled.<br>See Note 2.1 for more information on configuration straps. |
| 1 | EEPROM Chip Select | EECS | O8 | This pin drives the chip select output of the external EEPROM.<br>**Note:** The EECS output may tri-state briefly during power-up. Some EEPROM devices may be prone to false selection during this time. When an EEPROM is used, an external pull-down resistor is recommended on this signal to prevent false selection. Refer to your EEPROM manufacturer's datasheet for additional information. |
| 1 | EEPROM Clock | EECLK | O8 (PD) | This pin drives the EEPROM clock of the external EEPROM.<br>**Note:** This pin must be pulled-up externally for proper operation. |

**Note 2.1** Configuration strap values are latched on Power-On Reset (POR) or External Chip Reset (nRESET). Configuration straps are identified by an underlined symbol name. Pins that function as configuration straps must be augmented with an external resistor when connected to a load.

**Table 2.3 JTAG Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | JTAG Test Port Reset (Internal PHY Mode) | nTRST | IS (PU) | In Internal PHY Mode, this active-low pin functions as the JTAG test port reset input. |
| | Receive Data 0 (External PHY Mode) | RXD0 | IS (PD) | In External PHY Mode, this pin functions as the receive data 0 input from the external PHY. |
| 1 | JTAG Test Data Out (Internal PHY Mode) | TDO | O8 | In Internal PHY Mode, this pin functions as the JTAG data output. |
| | PHY Reset (External PHY Mode) | nPHY_RST | O8 | In External PHY Mode, this active-low pin functions as the PHY reset output. |
| 1 | JTAG Test Clock (Internal PHY Mode) | TCK | IS (PU) | In Internal PHY Mode, this pin functions as the JTAG test clock. The maximum operating frequency of this clock is 25 MHz. |
| | Receive Data 1 (External PHY Mode) | RXD1 | IS (PD) | In External PHY Mode, this pin functions as the receive data 1 input from the external PHY. |
| 1 | JTAG Test Mode Select (Internal PHY Mode) | TMS | IS (PU) | In Internal PHY Mode, this pin functions as the JTAG test mode select. |
| | Receive Data 2 (External PHY Mode) | RXD2 | IS (PD) | In External PHY Mode, this pin functions as the receive data 2 input from the external PHY. |
| 1 | JTAG Test Data Input (Internal PHY Mode) | TDI | IS (PU) | In Internal PHY Mode, this pin functions as the JTAG data input. |
| | Receive Data 3 (External PHY Mode) | RXD3 | IS (PD) | In External PHY Mode, this pin functions as the receive data 3 input from the external PHY. |

**Table 2.4 Miscellaneous Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | PHY Select | PHY_SEL | IS (PD) | Selects whether to use the internal Ethernet PHY or the external PHY connected to the MII port.<br>0 = Internal PHY is used.<br>1 = External PHY is used.<br>**Note:** When in External PHY Mode, the internal PHY is placed into general power down after a POR. |
| 1 | System Reset | nRESET | IS (PU) | This active-low pin allows external hardware to reset the device.<br>**Note:** This pin may be used to signal PME_CLEAR when PME Mode of operation is in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information. |
| 1 | Ethernet Full-Duplex Indicator LED | nFDX_LED | OD12 (PU) | This pin is driven low (LED on) when the Ethernet link is operating in Full-Duplex mode. |
| | General Purpose I/O 8 | GPIO8 | IS/O12/ OD12 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.<br>**Note:** This pin may be used to signal PME when External PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information.<br>**Note:** By default this pin is configured as a GPIO. |
| 1 | Ethernet Link Activity Indicator LED | nLNKA_LED | OD12 (PU) | This pin is driven low (LED on) when a valid link is detected. This pin is pulsed high (LED off) for 80 ms whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80 ms, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will function as an activity indicator. |
| | General Purpose I/O 9 | GPIO9 | IS/O12/ OD12 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.<br>**Note:** This pin may serve as the PME_MODE_SEL input when External PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information.<br>**Note:** By default this pin is configured as a GPIO. |

**Table 2.4 Miscellaneous Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Ethernet Speed Indicator LED | nSPD_LED | OD12 (PU) | This pin is driven low (LED on) when the Ethernet operating speed is 100 Mbs, or during auto-negotiation. This pin is driven high during 10 Mbs operation or during line isolation. |
| | General Purpose I/O 10 | GPIO10 | IS/O12/ OD12 (PU) | This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.<br>**Note:** This pin may serve as a wakeup pin whose detection mode is selectable when External PHY and PME Modes of operation are in effect. Refer to Chapter 5, "PME Operation," on page 37 for additional information.<br>**Note:** By default this pin is configured as a GPIO. |
| 1 | Core Regulator Enable | CORE_REG_EN | AI | This pin enables/disables the internal core logic voltage regulator.<br>When tied low to VSS, the internal core regulator is disabled and +1.2 V must be supplied to the device by an external source.<br>When tied high to +3.3 V, the internal core regulator is enabled.<br>Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information. |
| 1 | Test 1 | TEST1 | - | This pin must always be connected to VSS for proper operation. |
| 1 | Test 2 | TEST2 | - | This pin must always be connected to +3.3 V for proper operation. |
| 1 | Crystal Input | XI | ICLK | External 25 MHz crystal input.<br>**Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected |
| 1 | Crystal Output | XO | OCLK | External 25 MHz crystal output. |

**Table 2.5 USB Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | HSIC Data | HSIC_DATA | HSIC | Bi-directional Double Data Rate (DDR) data signal that is synchronous to the HSIC_STROBE signal as defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*. |
| 1 | HSIC Strobe | HSIC_STROBE | HSIC | Bi-directional data strobe signal as defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*. |
| 1 | HSIC Slew Tune | SLEW_TUNE | IS (PD) | Applies a slew rate boost to the HSIC_DATA and HSIC_STROBE pins when driven high. |
| 1 | External USB Bias Resistor | USBRBIAS | AI | Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12.0 kΩ 1.0% resistor to ground. |

**Table 2.6 Ethernet PHY Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Ethernet TX Data Out Negative | TXN | AIO | The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled. |
| 1 | Ethernet TX Data Out Positive | TXP | AIO | The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled. |
| 1 | Ethernet RX Data In Negative | RXN | AIO | The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled. |
| 1 | Ethernet RX Data In Positive | RXP | AIO | The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled. |
| 1 | PHY Interrupt (Internal PHY Mode) | nPHY_INT | O8 | In Internal PHY Mode, this pin can be configured to output the internal PHY interrupt signal.<br>**Note:** The internal PHY interrupt signal is active-high. |
| | PHY Interrupt (External PHY Mode) | nPHY_INT | IS (PU) | In External PHY Mode, the active-low signal on this pin is input from the external PHY and indicates a PHY interrupt has occurred. |
| 1 | External PHY Bias Resistor | EXRES | AI | Used for the internal bias circuits. Connect to an external 12.0 kΩ 1.0% resistor to ground. |

**Table 2.7 Power Pins and Ground Pad**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 5 | +3.3 V I/O Power | VDD33IO | P | Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information. |
| 3 | +3.3 V Analog Power | VDD33A | P | Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information. |
| 2 | +1.2 V Digital Core Power | VDD12CORE | P | Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information. |
| 1 | +1.2 V USB PLL Power | VDD12USBPLL | P | This pin must be connected to VDD12CORE for proper operation.<br><br>Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for additional connection information. |
| 1 | +1.2 V HSIC Power | VDD12A | P | This pin must be connected to VDD12CORE for proper operation.<br><br>Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for connection information. |
| 1 | +1.2 V Ethernet PLL Power | VDD12PLL | P | This pin must be connected to VDD12CORE for proper operation.<br><br>Refer to Chapter 3, "Power Connections," on page 24 and the device reference schematics for additional connection information. |
| Exposed pad on package bottom (Figure 2.1) | Ground | VSS | P | Common Ground |

## 2.1 Pin Assignments

**Table 2.8 56-QFN Package Pin Assignments**

| PIN NUM | PIN NAME | PIN NUM | PIN NAME | PIN NUM | PIN NAME | PIN NUM | PIN NAME |
|---|---|---|---|---|---|---|---|
| 1 | nPHY_INT | 15 | VDD33A | 29 | EECLK | 43 | TXEN |
| 2 | TXN | 16 | USBRBIAS | 30 | EECS | 44 | RXER |
| 3 | TXP | 17 | VDD12USBPLL | 31 | EEDO/ AUTOMDIX_EN | 45 | CRS/GPIO3 |
| 4 | VDD33A | 18 | XI | 32 | EEDI | 46 | COL/GPIO0 Note 2.2 |
| 5 | RXN | 19 | XO | 33 | TEST1 | 47 | TXCLK |
| 6 | RXP | 20 | SLEW_TUNE | 34 | PHY_SEL | 48 | VDD33IO |
| 7 | EXRES | 21 | VDD12CORE | 35 | VDD33IO | 49 | CORE_REG_EN |
| 8 | VDD33A | 22 | MDC/GPIO2 | 36 | nTRST/RXD0 | 50 | VDD12CORE |
| 9 | VDD12PLL | 23 | MDIO/GPIO1 Note 2.2 | 37 | TDO/nPHY_RST | 51 | VDD33IO |
| 10 | HSIC_DATA | 24 | nRESET Note 2.2 | 38 | TCK/RXD1 | 52 | VDD33IO |
| 11 | HSIC_STROBE | 25 | VDD33IO | 39 | TMS/RXD2 | 53 | TXD3/GPIO7/ 50DRIVER_EN |
| 12 | VDD12A | 26 | nFDX_LED/ GPIO8 | 40 | TDI/RXD3 | 54 | TXD2/GPIO6/ PORT_SWAP |
| 13 | TEST2 | 27 | nLNKA_LED/ GPIO9 Note 2.2 | 41 | RXCLK | 55 | TXD1/GPIO5/ RMT_WKP |
| 14 | TXER | 28 | nSPD_LED/ GPIO10 Note 2.2 | 42 | RXDV | 56 | TXD0/GPIO4/ EEP_DISABLE |
| EXPOSED PAD MUST BE CONNECTED TO VSS | | | | | | | |

**Note 2.2** This pin provides additional PME-related functionality. Refer to the respective pin descriptions and Section Chapter 5, "PME Operation," on page 37 for additional information.

## 2.2 Buffer Types

**Table 2.9 Buffer Types**

| BUFFER TYPE | DESCRIPTION |
|---|---|
| IS | Schmitt-triggered input |
| O8 | Output with 8 mA sink and 8 mA source |
| OD8 | Open-drain output with 8 mA sink |
| O12 | Output with 12 mA sink and 12 mA source |
| OD12 | Open-drain output with 12 mA sink |
| HSIC | *High-Speed Inter-Chip (HSIC) USB Specification, Version 1.0* compliant input/output |
| PU | 50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled.<br>**Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| PD | 50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled.<br>**Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added. |
| AI | Analog input |
| AIO | Analog bi-directional |
| ICLK | Crystal oscillator input pin |
| OCLK | Crystal oscillator output pin |
| P | Power pin |

# Chapter 3 Power Connections

The LAN9730/LAN9730i can be operated with the internal core regulator enabled or disabled. Figure 3.1 illustrates the power connections for operating the device with the internal regulator enabled. Figure 3.2 illustrates the power connections for operating the device with the internal regulator disabled. In this mode, +1.2 V must be supplied to the device by an external source.

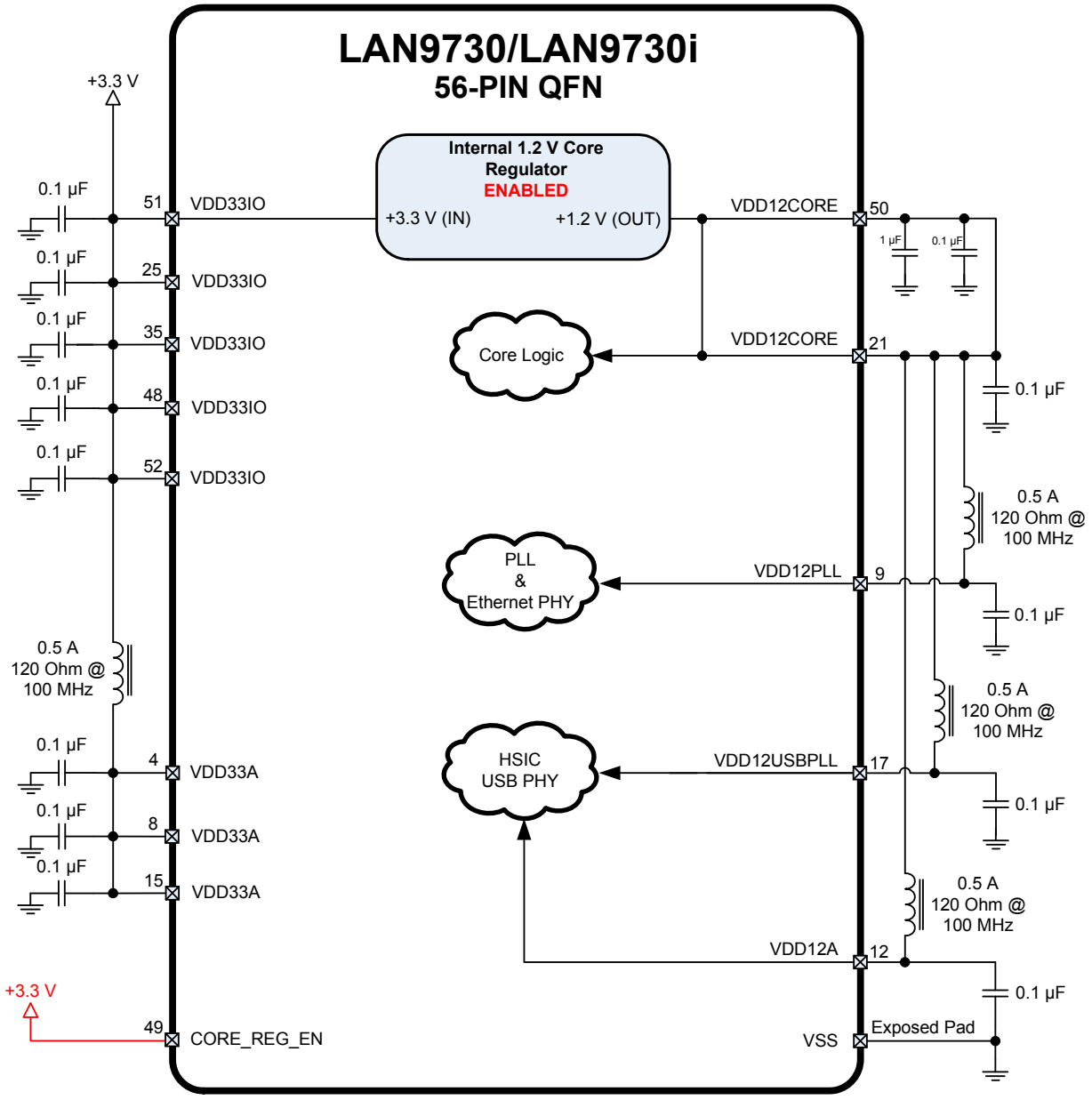


**Figure 3.1 Power Connections - Internal Regulator Enabled**

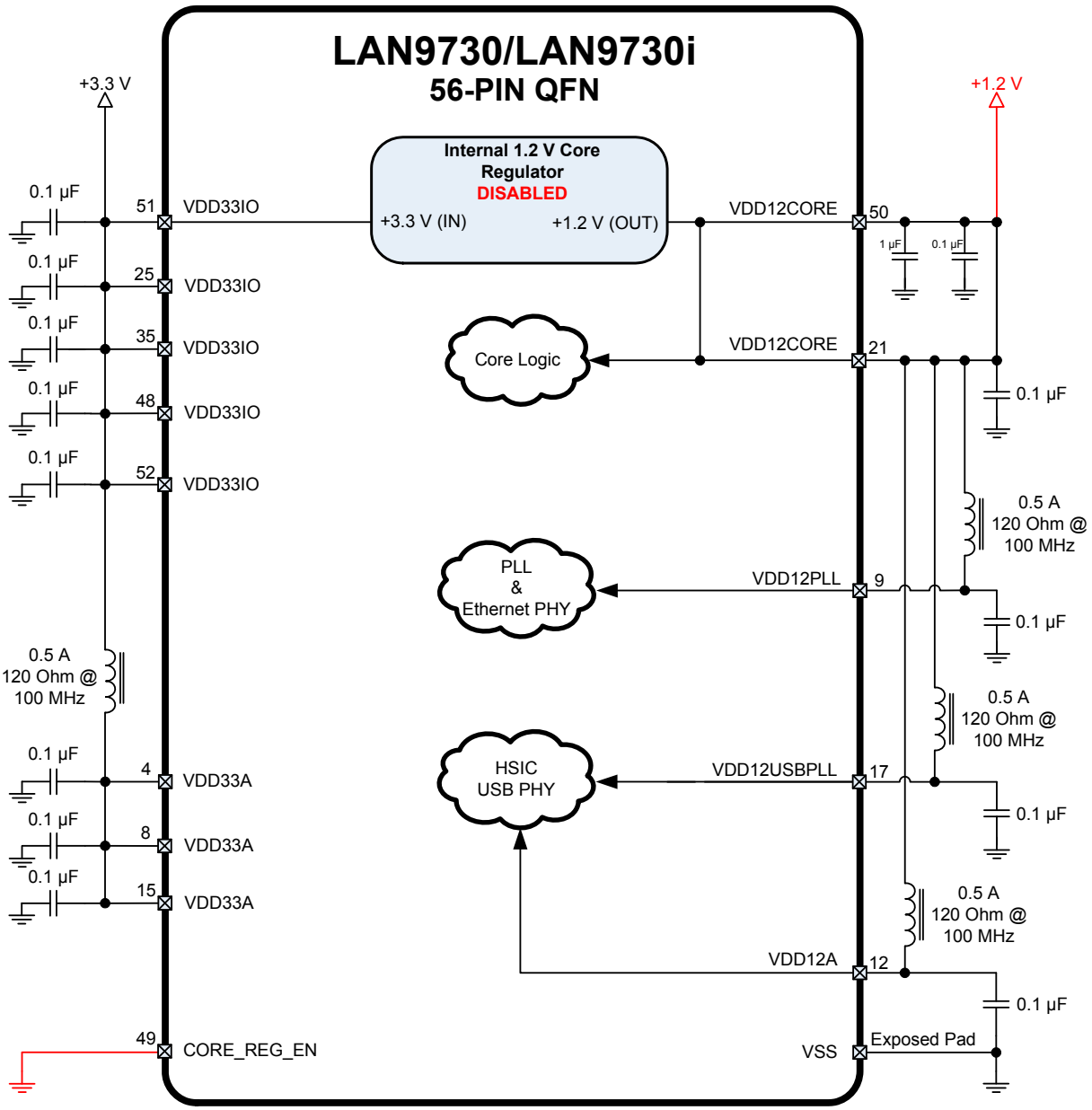


**Figure 3.2 Power Connections - Internal Regulator Disabled**