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LB11693H

Monolithic Digital IC

3-Phase Brushless Motor Driver for 24V Fan Motors

ON Semiconductor®

http://onsemi.com

Overview

The LB11693H reduces motor noise by imparting a slope to the output current when switching the phase to which power
is applied. This motor driver includes an automatic recovery constraint protection circuit and is optimal for driving 24V fan motors.

Functions

- Soft phase switching + direct PWM drive
- PWM control based on both a DC voltage input (the CTL voltage) and a pulse input
- Provides a 5 V regulator output
- One Hall-effect sensor FG output
- Integrating amplifier
- Automatic recovery constraint protection circuit (on/off = 1/14), RD output
- Current limiter circuit
- LVSD circuit
- Thermal protection circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC} max		30	V
Output current	I_O max	T ≤ 500mS	1.8	A
Allowable power dissipation 1	Pd max1	Independent IC	0.9	W
Allowable power dissipation 2	Pd max2	When mounted on a circuit board *	2.1	W
Operating temperature	Topr		-30 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

*: On the specified circuit board (114.3mm×76.1mm×1.6mm, glass epoxy)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage rang	V_{CC}		9.5 to 28	V
Constant voltage output current	I_{REG}		0 to -30	mA
RD output current	I_{RD}		0 to 10	mA
FG output current	I_{FG}		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	$I_{CC}1$			10	13.5	mA
Current drain 2	$I_{CC}2$	When STOP		4.0	5.5	mA
Output Block						
Output saturation voltage 1	$V_O$sat1	I_O = 0.7A, V_O (SINK) + V_O (SOURCE)		1.5	2.05	V
Output saturation voltage 2	$V_O$sat2	I_O = 1.5A, V_O (SINK) + V_O (SOURCE)		2.2	2.9	V
Output leakage current	$I_O$leak				100	μA
High side diode forward voltage 1	VD1	ID = 0.7A		1.25	1.65	V
High side diode forward voltage 2	VD2	ID = 1.5A		1.9	2.5	V
5V Constant Voltage Output						
Output voltage	VREG	I_O = -5mA	4.7	5.0	5.3	V
Voltage regulation	ΔVREG1	V_{CC} = 9.5 to 28V		30	100	mV
Load regulation	ΔVREG2	I_O = -5 to -20mA		20	100	mV
Hall amplifier						
Input bias current	I_B(HA)			2	10	μA
Differential input voltage range	VHIN	Sine wave input	50		350	mVp-p
Common-mode input voltage range	VICM	Differential input 50mVp-p	1.5		VREG-1.0	V
Input offset voltage	VIOH	Design target value	-20		20	mV
CSD Pin						
High-level output voltage	V_{OH}(CSD)		2.75	3.0	3.25	V
Low-level output voltage	V_{OL}(CSD)		0.85	1.0	1.15	V
External capacitor charge current	$I_{CSD}1$		-3.3	-2.4	-1.4	μA
External capacitor charge current	$I_{CSD}2$		0.09	0.17	0.23	μA
Charge/discharge current ratio	R_{CSD}	Charge current/discharge current		14		Times
Undervoltage Protection Circuit (LVS pin)						
Operating voltage	$V_{SD}L$		3.6	3.8	4.0	V
Release voltage	$V_{SD}H$		4.1	4.3	4.5	V
Hysteresis	ΔV_{SD}		0.35	0.5	0.65	V
Current Limiter Circuit (RF pin)						
Limiter voltage	V_{RF}	V_{CC}-VM	0.45	0.5	0.55	V
Thermal Shutdown Operation						
Thermal shutdown operating voltage	TSD	Design target value (junction temperature)	150	170		°C
Hysteresis	ΔTSD	Design target value (junction temperature)		40		°C
CTL Amplifier						
Input offset voltage	V_{IO}(CTL)		-10		10	mV
Input bias current	I_B(CTL)		-1		1	μA
Common-mode input voltage range	VICM		0		VREG-1.7	V
High-level output voltage	V_{OH}(CTL)	I_{TOC} = -0.2mA	VREG-1.2	VREG-0.8		V
Low-level output voltage	V_{OL}(CTL)	I_{TOC} = 0.2mA		0.8	1.05	V
Open-loop gain	G(CTL)	f(CTL) = 1kHz	45	51		dB

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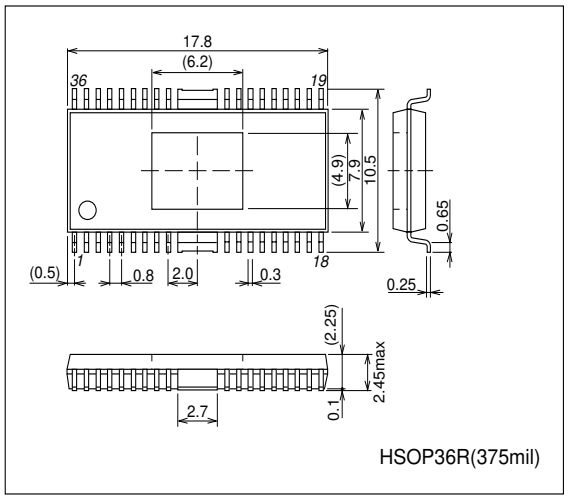
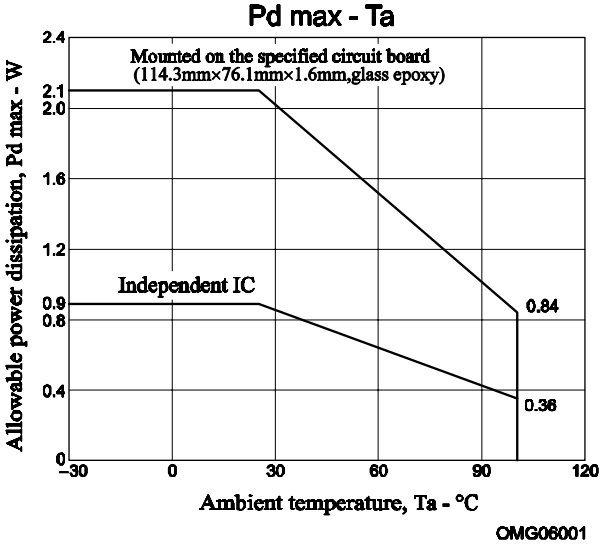
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
PWM Oscillator Circuit						
High-level output voltage	V_{OH}(PWM)		2.75	3.0	3.25	V
Low-level output voltage	V_{OL}(PWM)		1.1	1.3	1.4	V
Amplitude	V(PWM)		1.5	1.7	2.0	Vp-p
External capacitor charge current	I_{CHG}	VPWM = 2.1V	-125	-90	-70	µA
Oscillator frequency	f(PWM)	C = 2200pF	15.5	19.5	27.0	kHz
TOC pin						
Input voltage 1	$V_{TOC}1$	Output duty: 100%	2.72	3.0	3.30	V
Input voltage 2	$V_{TOC}2$	Output duty: 0%	1.07	1.3	1.45	V
Input voltage 1L	$V_{TOC}1L$	Design target value. 100% when VREG = 4.7V	2.72	2.80	2.90	V
Input voltage 2L	$V_{TOC}2L$	Design target value. 0% when VREG = 4.7V	1.07	1.17	1.27	V
Input voltage 1H	$V_{TOC}1H$	Design target value. 100% when VREG = 5.3V	3.08	3.20	3.30	V
Input voltage 2H	$V_{TOC}2H$	Design target value. 0% when VREG = 5.3V	1.21	1.33	1.45	V
RD pin						
Low-level output voltage	V_{OL}(RD)	I_{RD} = 5mA		0.1	0.3	V
Output leakage current	I_L(RD)	V_{RD} = 28V			10	µA
FG pin						
Low-level output voltage	V_{OL}(FG)	I_{FG} = 5mA		0.1	0.3	V
Output leakage current	I_L(FG)	V_{FG} = 28V			10	µA
FGFIL Pin						
Charge current	$I_{FGFIL}1$		-7	-5	-3	µA
Discharge current	$I_{FGFIL}2$		3	5	7	µA
FG Amplifier Schmitt Block (IN1)						
Amplifier gain	G(FG)	Design target value.		7		Times
Hysteresis	V_{IS}(FG)	Design target value. Input equivalent		8		mV
S/S Pin						
High-level input voltage	V_{IH}(SS)		2.0		VREG	V
Low-level input voltage	V_{IL}(SS)		0		1.0	V
Input open voltage	V_{IO}(SS)		2.6	2.9	3.2	V
Hysteresis	V_{IS}(SS)		0.16	0.25	0.34	V
High-level input current	I_{IH}(SS)	VS/S = VREG		100	130	µA
Low-level input current	I_{IL}(SS)	VS/S = 0V	-170	-130		µA
PWMIN Pin						
Input frequency range	f(PI)				50	kHz
High-level input voltage range	V_{IH}(PI)		2.0		VREG	V
Low-level input voltage range	V_{IL}(PI)		0		1.0	V
Input open voltage	V_{IO}(PI)		2.6	2.9	3.2	V
Hysteresis	V_{IS}(PI)		0.16	0.25	0.34	V
High-level input current	I_{IH}(PI)	VPWMIN = VREG		100	130	µA
Low-level input current	I_{IL}(PI)	VPWMIN = 0V	-170	-130		µA
F/R Pin						
High-level input voltage	V_{IH}(FR)		2.0		VREG	V
Low-level input voltage	V_{IL}(FR)		0		1.0	V
Input open voltage	V_{IO}(FR)		VREG-0.5		VREG	V
Hysteresis	V_{IS}(FR)		0.16	0.25	0.34	V
High-level input current	I_{IH}(FR)	V_{FR} = VREG	-10	0	10	µA
Low-level input current	I_{IL}(FR)	V_{FR} = 0V	-165	-115		µA

Package Dimensions

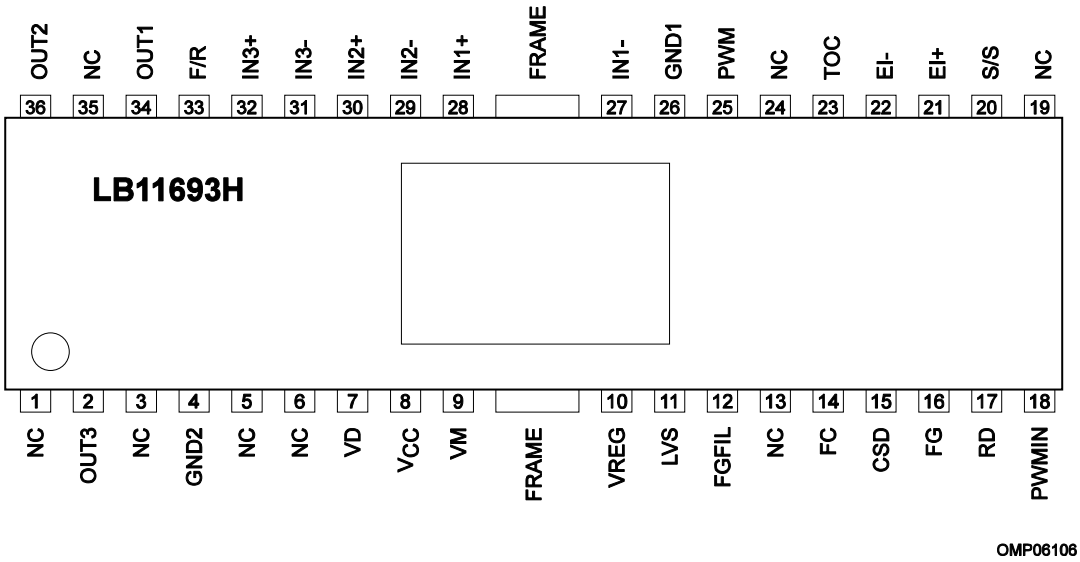
unit : mm

3251





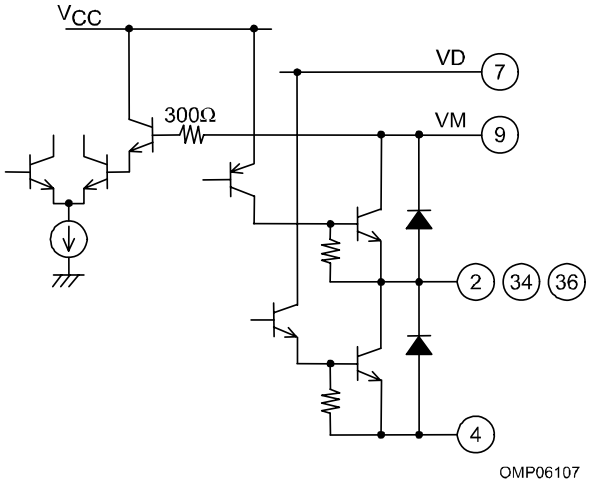
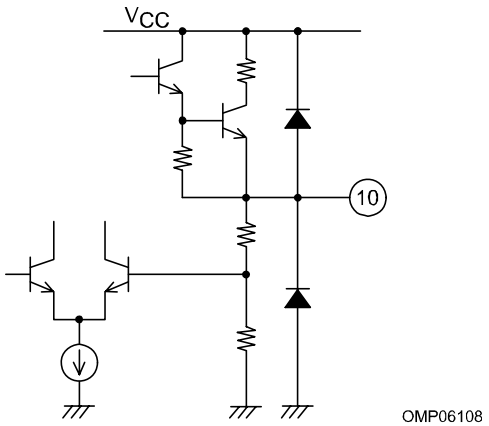
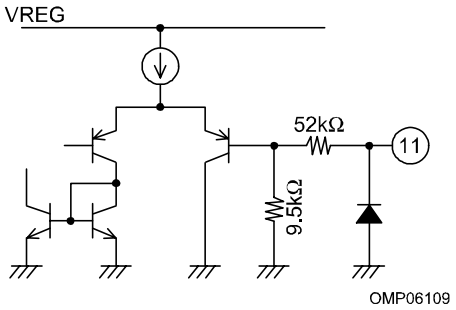
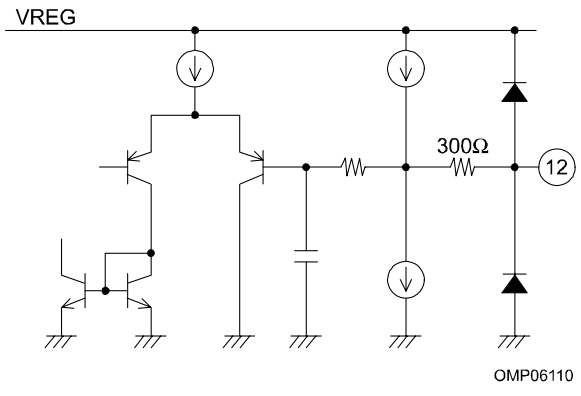
Pin Assignment



Truth Table

	Source → Sink	F/R = 'L'			F/R = 'H'		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2 → OUT1	H	L	H	L	H	L
2	OUT3 → OUT1	H	L	L	L	H	H
3	OUT3 → OUT2	H	H	L	L	L	H
4	OUT1 → OUT2	L	H	L	H	L	H
5	OUT1 → OUT3	L	H	H	H	L	L
6	OUT2 → OUT3	L	L	H	H	H	L

Pin Function

Pin No.	Symbol	Description	Equivalent circuit
34 36 2	OUT1 OUT2 OUT3	Motor drive output	
4	GND2	Motor drive output system ground	
7	VD	Low side output transistor drive current supply	
9	VM	Motor drive output power supply and output current detection. Connect a resistor (Rf) between this pin and V_{CC}. The output current is limited to a value determined by the equation $I_{OUT} = V_{RF}/Rf$.	
8	V_{CC}	Power supply (Systems other than the motor drive output)	
10	VREG	5V regulator output (control circuit power supply). Connect a capacitor (about 0.1μF) between this pin and ground for stabilization.	
11	LVS	Undervoltage protection voltage detection. Connect this pin to VREG if the VREG level is to be detected. If the V_{CC} level is to be detected, insert a zener diode in series to set the detection level.	
12	FGFIL	FG filter. Normally, this IC will be used with this pin open. Connect a capacitor between this pin and ground if noise on the FG signal becomes a problem.	

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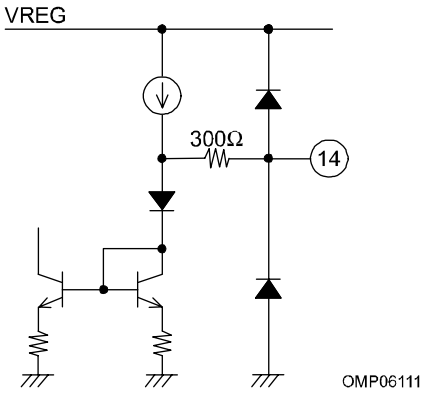
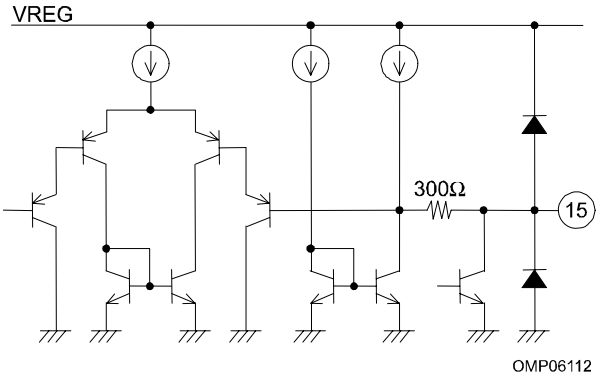
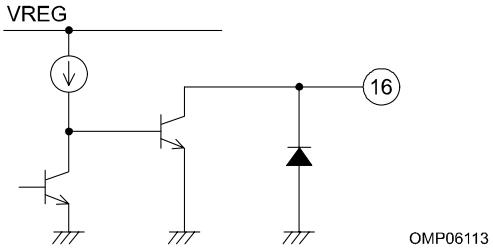
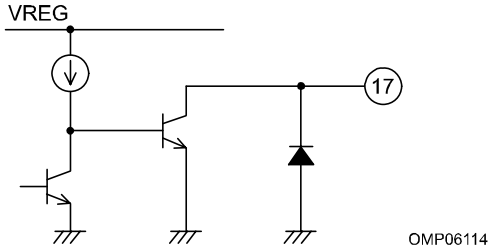
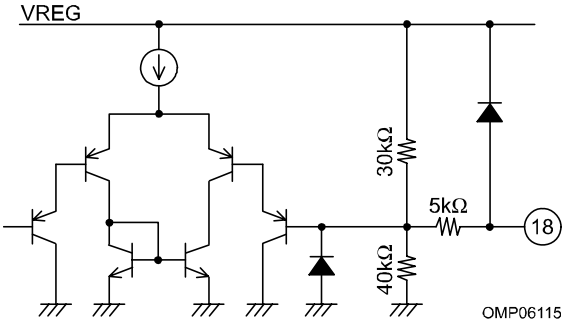
Pin No.	Symbol	Description	Equivalent circuit
14	FC	Control loop frequency characteristics correction. Connect a capacitor between this pin and ground.	
15	CSD	Constraint protection circuit operating time setting.	
16	FG	Hall input 1FG output. (This is an open-collector output.)	
17	RD	Motor constrained state detection output (This is an open-collector output.) When the motor is constrained: high, when the motor is turning: low.	
18	PWMIN	PWM pulse input. When low the output will be on and when high the outputs will be off. If this pin is used to control this IC, connect EI^- to ground and connect EI^+ to TOC.	

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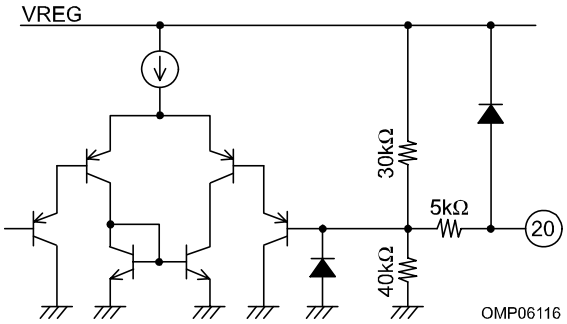
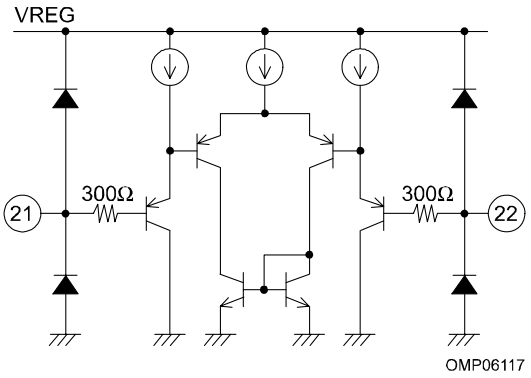
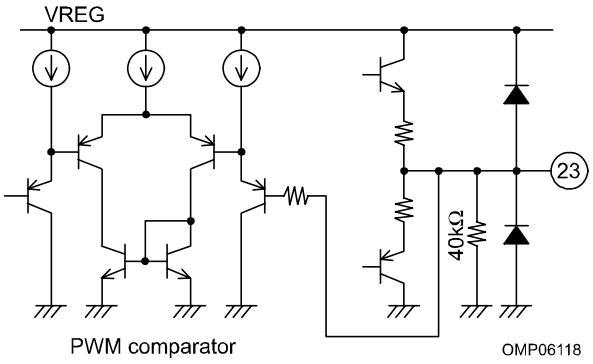
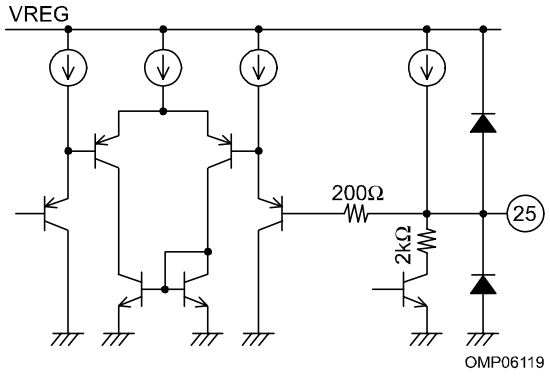
Pin No.	Symbol	Description	Equivalent circuit
20	S/S	Start/stop control. Low: start, high or open: stop.	
21 22	EI+ EI-	CTL amplifier noninverting input CTL amplifier inverting input	
23	TOC	PWM waveform comparator (CTL amplifier output)	
25	PWM	PWM oscillator frequency setting. Connect a capacitor between this pin and ground. A frequency of about 20kHz can be set by using a 2200pF capacitor.	

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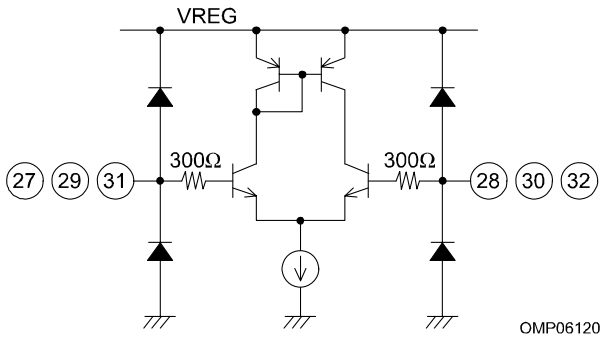
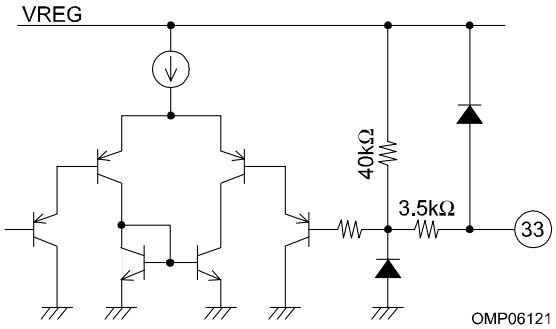
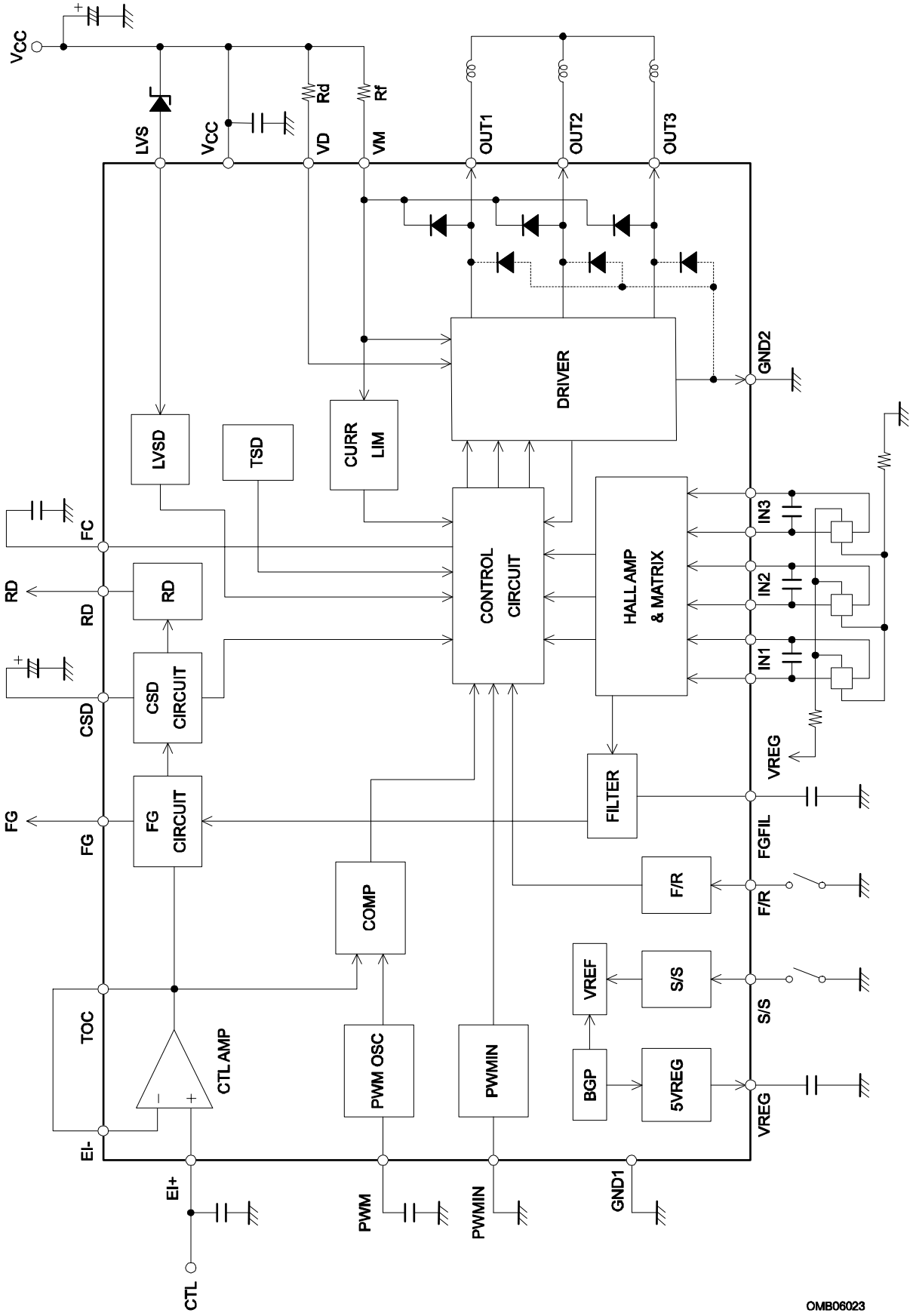
Pin No.	Symbol	Description	Equivalent circuit
26	GND1	Ground (For circuits other than the motor drive output system)	
28 27 30 29 32 31	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall effect sensor inputs High when $IN^+ > IN^-$, low for the reverse state. Signal inputs with an amplitude (differential) of at least 50mVp-p are desirable for the Hall inputs. If noise is a problem, connect capacitors between the IN^+ and IN^- inputs.	
33	F/R	Forward/reverse control Low: forward, high or open: reverse.	
1,3 5,6 13,1 9 24,3 5	NC	No connection. The NC pins may be used for wiring connections.	
	FRAME	Frame connection The FRAME pin is connected internally to the IC surface metal parts. Both must be used in the electrically open state.	

Block Diagram



LB11693H Overview

1. Output Drive Circuit

The LB11693H reduces motor vibration and noise by switching the output current smoothly when switching phases. Since the Hall input waveform is used for the change in (slope of) the output current during phase switching, if the slope of the Hall input waveform is too steep, the change in the output current during phase switching will also be too steep and the effectiveness of this technique at lowering vibration and noise effect will be reduced. Thus the slope of the Hall input waveform requires attention during application design.

Low side output transistor PWM switching is used for motor speed control. The drive output is adjusted by changing the duty. The diodes between the outputs and VM used for the regenerative current when the PWM signal is in the off state are built in.

If the slope (amplitude) of the Hall input waveform is large, and if used with a high current, the parasitic diodes between the outputs and ground will operate due to the low side kickback during phase switching. If problems such as disruption of the waveforms occur, connect either rectifying diodes or Schottky diodes between the outputs and ground.

2. Power Supply Stabilization

Since the LB11693H uses a control method based on PWM switching, the power supply lines are susceptible to disruption. Electrolytic capacitors with an adequate capacitance for stabilization must be connected between V_{CC} and ground. If diodes are inserted in the power supply lines to prevent destruction of the equipment if the power supply is connected in reverse, the power supply lines will be particularly susceptible to disruption. In this case, even larger capacitors must be used. The connected electrolytic capacitors must be located as close as possible to the IC pins (V_{CC}, VM, and GND2). If the electrolytic capacitors cannot be attached close to the pins due to problems with the heat sink or other issues, ceramic capacitors of about 0.1μF must be attached close to the pins.

3. VREG Pin

At the same time as being the 5V regulator output, the VREG pin is also the power supply for the IC internal control circuits. Therefore, a capacitor of at least 0.1μF must be connected between the VREG pin and ground to stabilize the control circuit power supply. The ground side of the connected capacitor must be connected to the GND1 pin with as short a line as possible.

4. FC Pin

The capacitor connected to the FC pin is required to correct the control loop's frequency characteristics. (It should be about 0.1μF.)

5. VD Pin

The VD pin supplies the low side output transistor drive current (a maximum of about 0.1A).

The IC internal power consumption is suppressed by connecting a resistor between the V_{CC} and VD pins and dividing power consumption due to the low side output transistor drive current with that resistor. Although the IC internal power consumption due to the drive current can be reduced by lowering the VD pin voltage, a voltage of at least 4 V must be assured at the VD pin. Use a resistor in the range from about 50Ω (0.5W) to about 100Ω (1W) between the V_{CC} and VD pins when the LB11693H is used with V_{CC} = 24V.

6. Hall Input Signals

Signal inputs with an amplitude (differential) of at least 50mVp-p are required for the Hall inputs. If the output waveforms are disrupted by noise, capacitors must be connected between the Hall input pins (the + and - sides).

7. Current Limiter Circuit

The current limiter circuit limits the peak value of the output current to a current determined by the equation I = V_{RF}/Rf (where V_{RF} = 0.5V (typical), Rf = current detection resistor value). When the limiter operates, it suppresses the current by PWM control of the low side output transistor at the PWM frequency determined by the external capacitor connected to the PWM pin, in particular, by reducing the on duty.

8. Forward/Reverse Switching

The LB11693H was designed assuming that forward/reverse switching would not be performed while the motor is operating. We recommend that the F/R pin be held fixed at either the low (forward) or high (reverse) level when the motor is turning. Although it will be pulled up to the high level by an internal pull-up resistor (about 40kΩ) when left open, this must be strengthened by an external resistor if fluctuations are large.

If the direction is switched while the motor is turning, large currents will flow due to the braking operation. The LB11693H's current limiter circuit, however, cannot limit this braking current. Therefore, forward/reverse switching during motor rotation is only possible if the braking current is limited to a value under $I_O$max (1.8A) by the motor coil resistance or other circuit or phenomenon. Furthermore, since through current will flow in the high and low side transistors at the instant the switch occurs with switching that only uses the F/R pin, applications must provide a drive off period for switching directions. A drive off period must be provided by either setting the IC to the stopped state with the S/S pin or setting the PWM signal to the 0% duty state with the TOC and PWMIN pins, and the F/R pin must only be switched during that period to prevent through current.

9. Power Saving Circuit

This IC can be set to a power saving state in which current consumption is reduced by setting it to the stopped state with the S/S pin. The bias current to most of the circuits in the IC is cut off in this power saving state. Note, however, that the 5V regulator output is still provided in the power saving state.

10. Notes on the PWM Frequency

The PWM frequency is determined by the capacitance (F) of the capacitor connected to the PWM pin.

$fPWM \approx 1/(23400 \times C)$

A frequency in the range 15 to 25kHz is desirable for the PWM frequency. The ground side of the connected capacitor must be connected to the GND1 pin by as short a line as possible.

11. Control Methods

The output duty can be controlled by either of the following methods.

- Comparison of the TOC pin voltage with the PWM oscillator waveform

  This method determines the low side output transistor duty according to the result of comparing the TOC pin voltage with the PWM oscillator waveform. The PWM duty will be 0% when the TOC pin voltage is under about 1.3 V and will be 100% when that voltage is over about 3.0V.

  Since the TOC pin is the output of the CTL amplifier, a control voltage cannot be directly input to the TOC pin. Accordingly, the CTL amplifier is normally used as a full feedback amplifier (by connecting the EI^- pin to the TOC pin) and inputting a DC voltage to the EI pin (here the TOC voltage will be equal to the EI^+ pin voltage). When the EI^+ pin voltage increases, the output duty will increase as well. Since the motor will be driven if the EI^+ pin is in the open state, a pull-down resistor should be connected to the EI^+ pin in applications where this is not desirable.

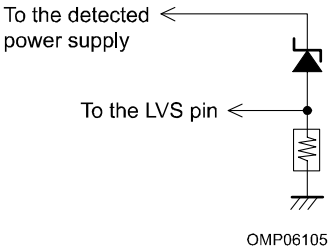
  A low level must be input to the PWMIN pin (or it must be connected to ground) if the TOC pin voltage control system is used.

- PWMIN pulse input

  A 15 to 25kHz frequency pulse signal can be input to the PWMIN pin and the low side output transistor duty can be controlled based on the duty of that input signal. When the PWMIN pin is low, the output will be on, and when high, the output will be off. When the PWMIN pin is open, the input will go to the high level and the output will be off.

  If PWMIN pin control is used, the EI^- pin must be connected to ground and the EI^+ pin must be connected to the TOC pin.

12. Undervoltage Protection Circuit



The undervoltage protection circuit turns off the low side output transistor if the LVS pin voltage falls below the circuit's operating voltage (about 3.8V). This operating voltage is the detection level for a 5V system. The detection level can be increased by connecting a zener diode in series with the LVS pin to apply a level shift to the detection level. The current flowing into the LVS pin during detection is about 65µA. To suppress variations in the zener voltage, it is necessary to stabilize the rise of the zener diode voltage by increasing the current that flows in the zener diode. If this is necessary, insert a resistor between the LVS pin and ground.

When the LCS pin is open, it will be pulled to the ground level by the built-in pull-down resistor and the output will be turned off. Thus if the undervoltage protection circuit is not used, a voltage in excess of the release voltage (about 4.3V) must be applied to the LVS pin. Note that the maximum rating for the LVS pin voltage is 30V.

13. Motor Constraint Protection Circuit

When motor motion is constrained, the external capacitor connected to the CSD pin will be alternately charged (up to about 3.0V) with a constant current of about 2.4µA and discharged with a constant current of about 0.17µA (to about 1.0V). Thus the CSD pin voltage will have a sawtooth waveform. The motor constraint protection circuit turns the motor (the low side output transistor) on or off repeatedly based on this sawtooth waveform. Motor drive will be on during the period the CSD pin external capacitor is being charged from about 1.0V to about 3.0V and will be off when it is being discharged from about 3.0V to about 1.0V. The drive on/off operation protects the IC and the motor when the motor is physically constrained from moving. If a 0.47µF capacitor is connected to the CSD pin, the IC will iterate an on/off cycle in which drive is on for about 0.4 seconds and off for about 5.5 seconds.

While the motor is turning, the CSD pin voltage will be held at a certain voltage (that depends on the motor speed) by (a) a CSD pin external capacitor discharge operation based on about 10µs discharge pulses generated internally in the IC when the Hall input IN1 switches (that is, on rising and falling edges on the FG output) and (b) a charge operation on that capacitor by a constant current of about 2.4µA.

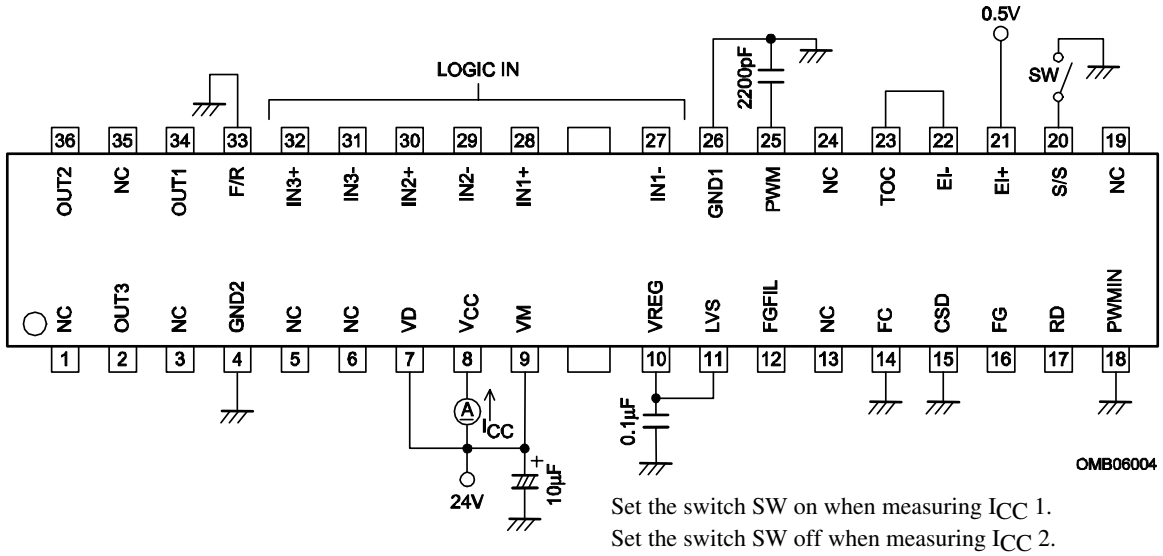
Since the Hall input IN1 does not switch when the motor is physically constrained, the discharge pulses are not generated and the CSD pin external capacitor will be charged to about 3.0V by the constant current of about 2.4µA. The motor constraint protection circuit operates when the capacitor reaches about 3.0V. The constraint protection operation will be released when the motor constraint is released.

If the motor speed is extremely low, the CSD pin voltage during that motor rotation will be held at a comparatively high voltage, and if that voltage reaches about 3.0V, the constraint protection function will operate. Since the constraint protection function will operate if the Hall input IN1 frequency falls below about 10Hz, caution is required when using the motor constraint protection circuit with motors that will operate at low speeds.

Connect the CSD pin to ground if the motor constraint protection circuit is not used.

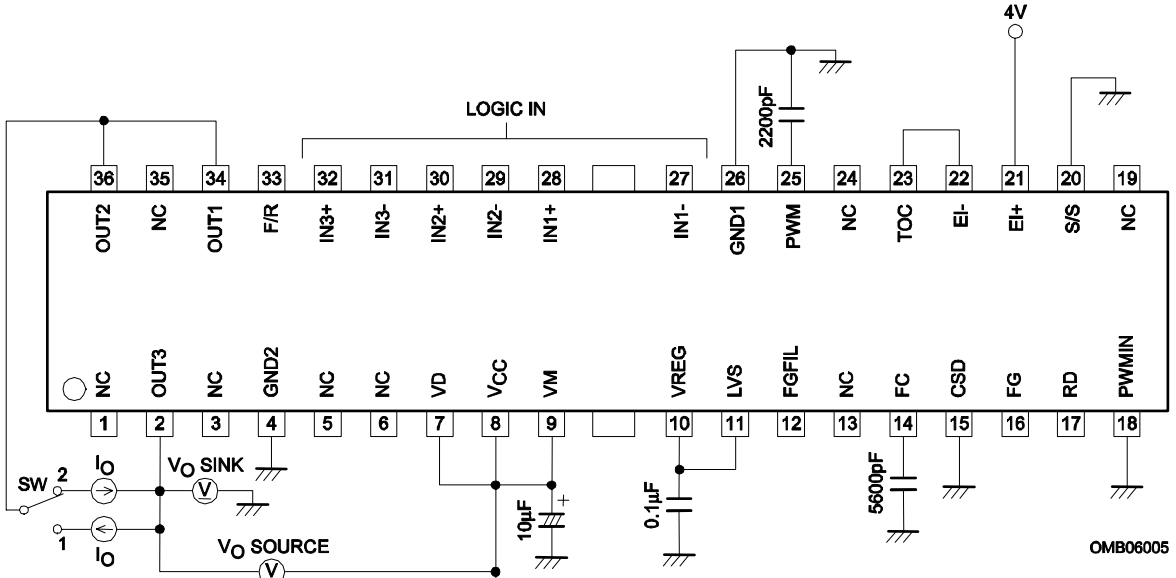
Test Circuits

$I_{CC}1$, $I_{CC}2$



Set the switch SW on when measuring I_{CC} 1.
Set the switch SW off when measuring I_{CC} 2.

$V_O$sat1 , $V_O$sat2

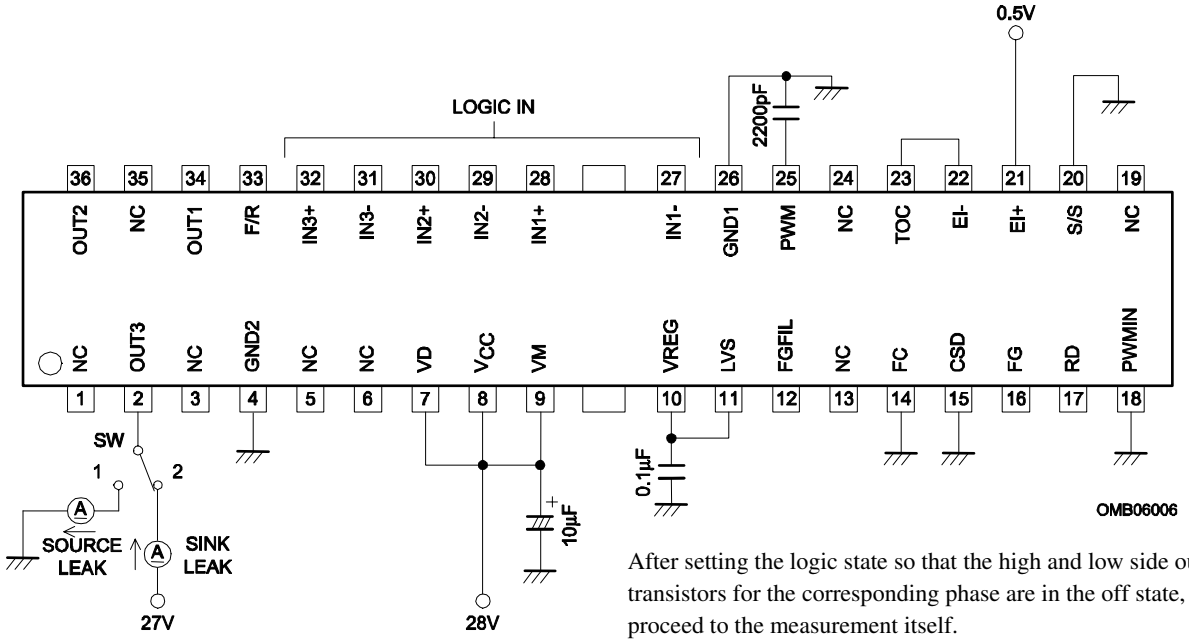


Logic table

	IN1	IN2	IN3
OUT1 Source	H	L	M
OUT1 Sink	L	H	M
OUT2 Source	M	H	L
OUT2 Sink	M	L	H
OUT3 Source	L	M	H
OUT3 Sink	H	M	L

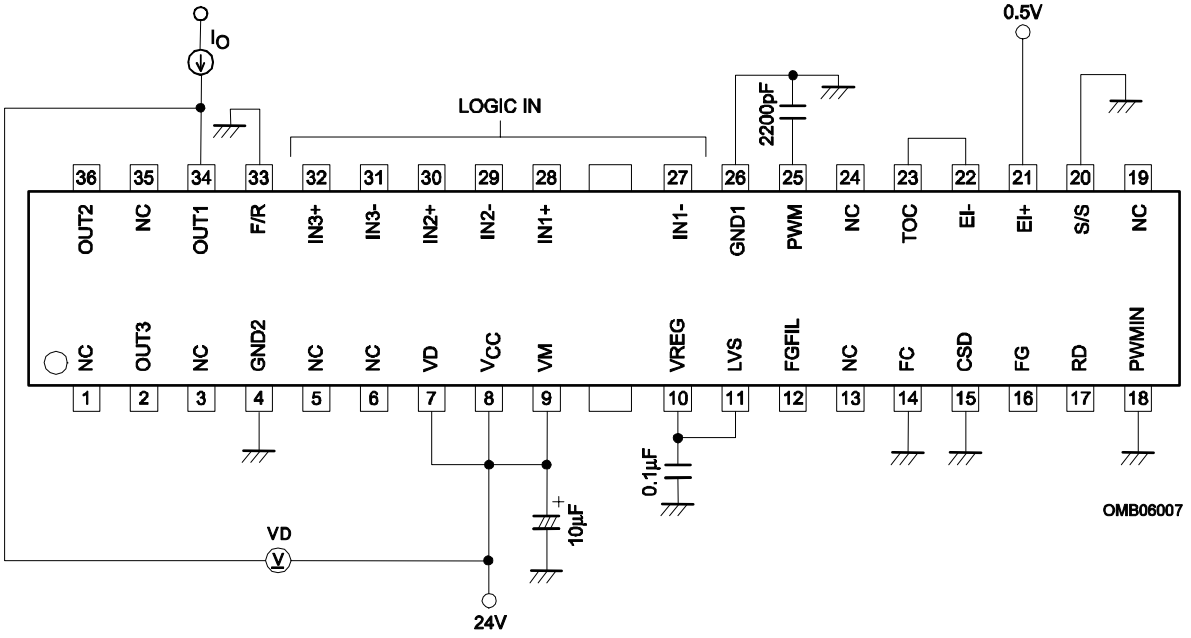
Input the logic states shown in the table so that the output transistor for the corresponding phase is on. After setting the switch SW to position 1 for source transistor measurement or to position 2 for sink transistor measurement, proceed to the measurement itself.
$V_O$sat = V_O SOURCE + V_O SINK
The figure shows the circuit used for measuring OUT3. Use similar circuits for measurement of the other phases.

$I_O$leak



After setting the logic state so that the high and low side output transistors for the corresponding phase are in the off state, proceed to the measurement itself.
Set the switch SW to position 1 for source transistor leakage measurement, and to position for sink transistor leakage measurement.
The figure shows the circuit used for measuring OUT3. Use similar circuits for measurement of the other phases.

VD1, VD2(EX, OUT1)

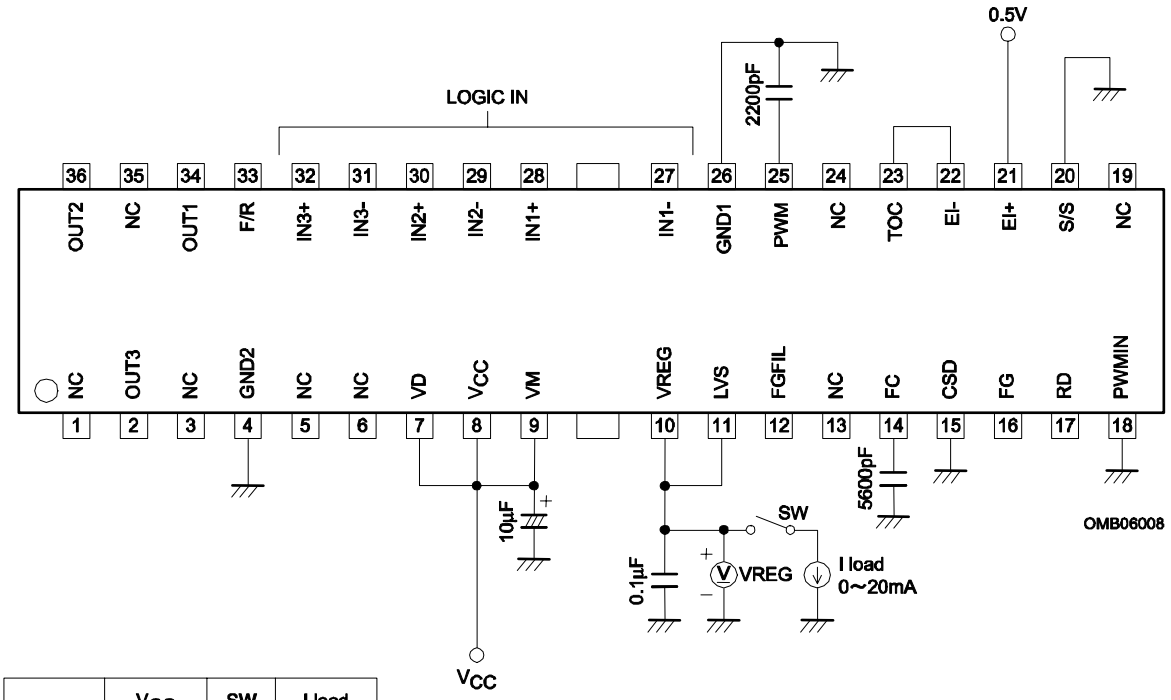


Logic table

	IN1	IN2	IN3
OUT1	H	H	L
OUT2	H	L	L
OUT3	L	H	L

Input the logic states shown in the table so that the output transistor for the corresponding phase is off.
Set I_O to 0.7A when measuring VD1.
Set I_O to 1.5A when measuring VD2.
The figure shows the circuit used for measuring OUT1. Use similar circuits for measurement of the other phases.

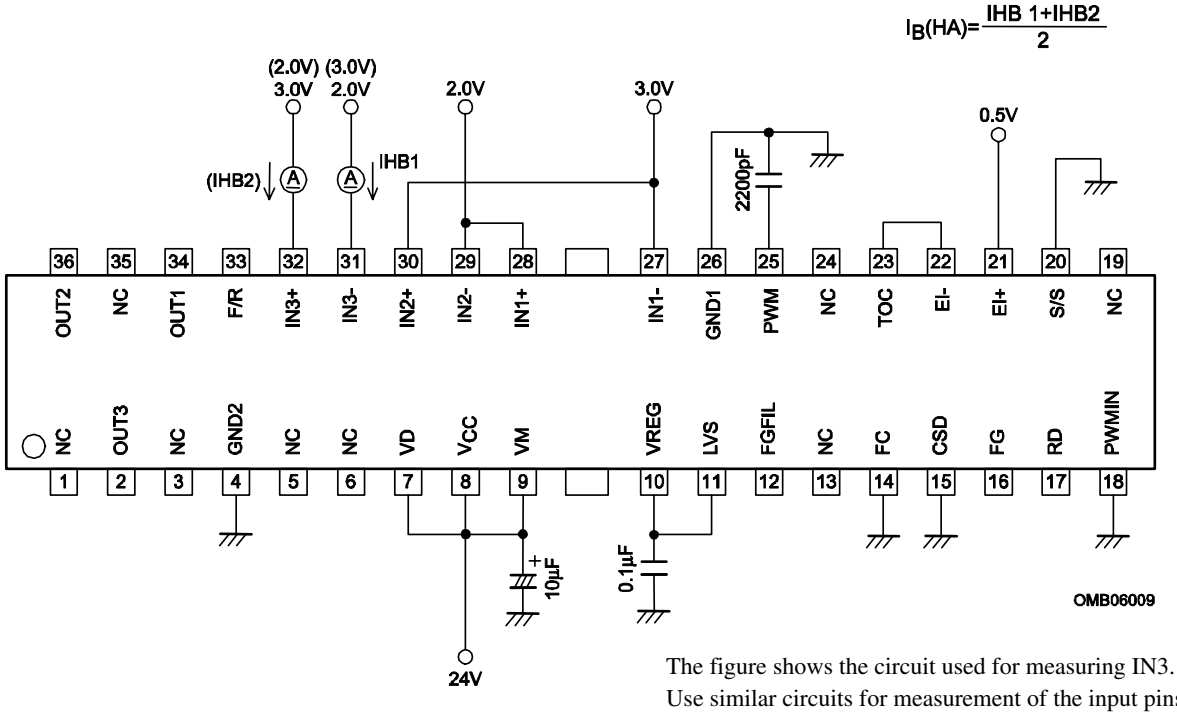
VREG, ΔVREG1, ΔVREG2



	V_{CC}	SW	I load
VREG	24V	ON	5mA
ΔVREG1	9.5~28V	ON	5mA
ΔVREG2	24V	ON	5~20mA

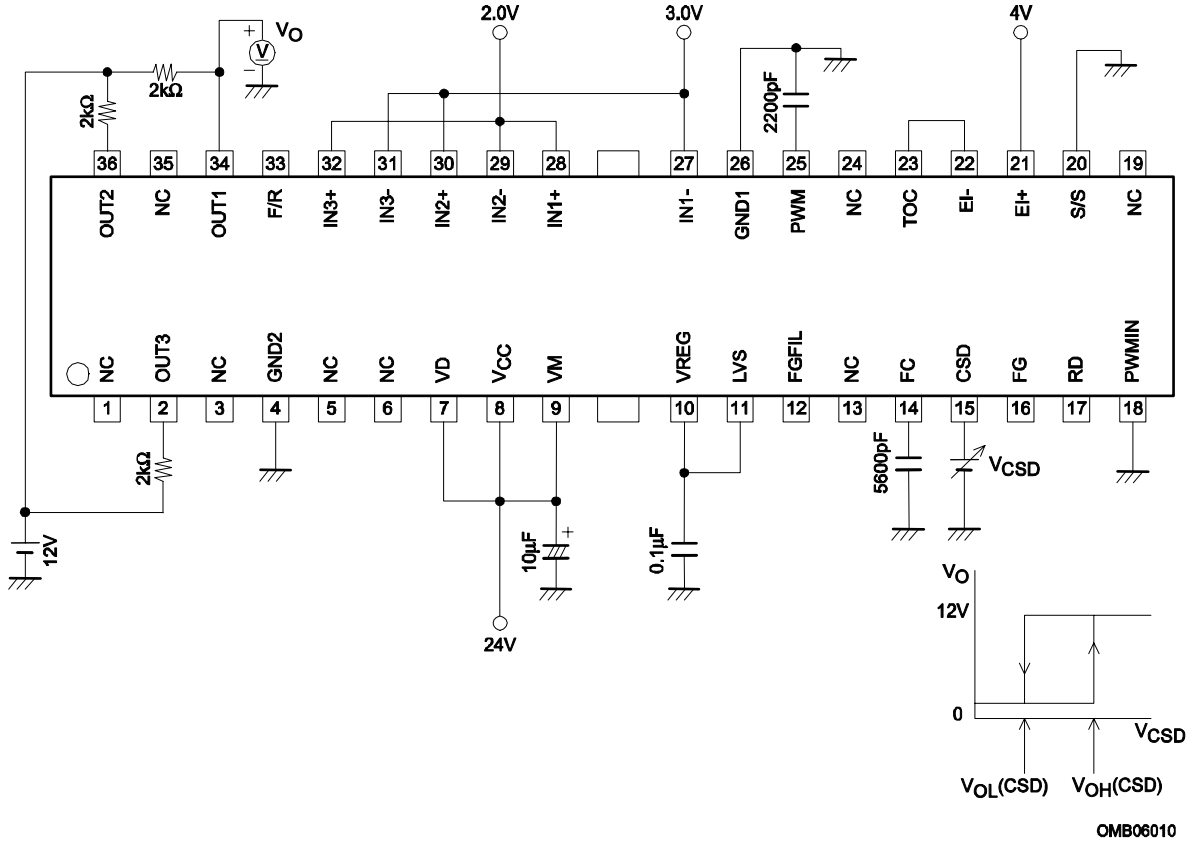
ΔVREG1=VREG28V - VREG9.5V
ΔVREG2=VREG5mA - VREG20mA

I_B(HA)

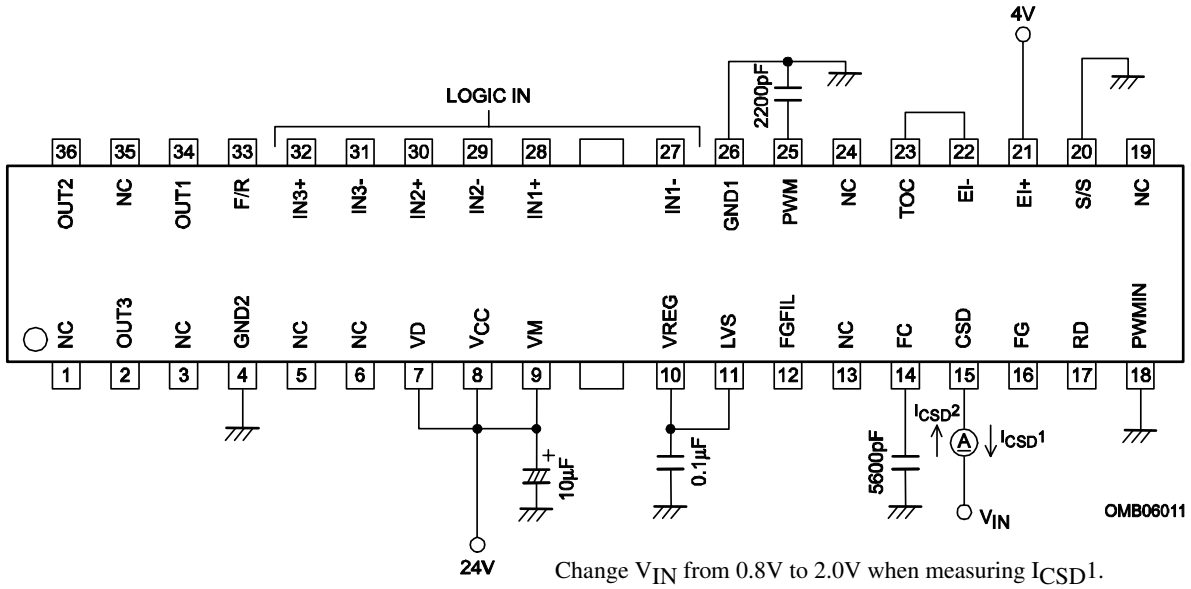


The figure shows the circuit used for measuring IN3. Use similar circuits for measurement of the input pins for the other phases.

$V_{OH(CSD)}$, $V_{OL(CSD)}$

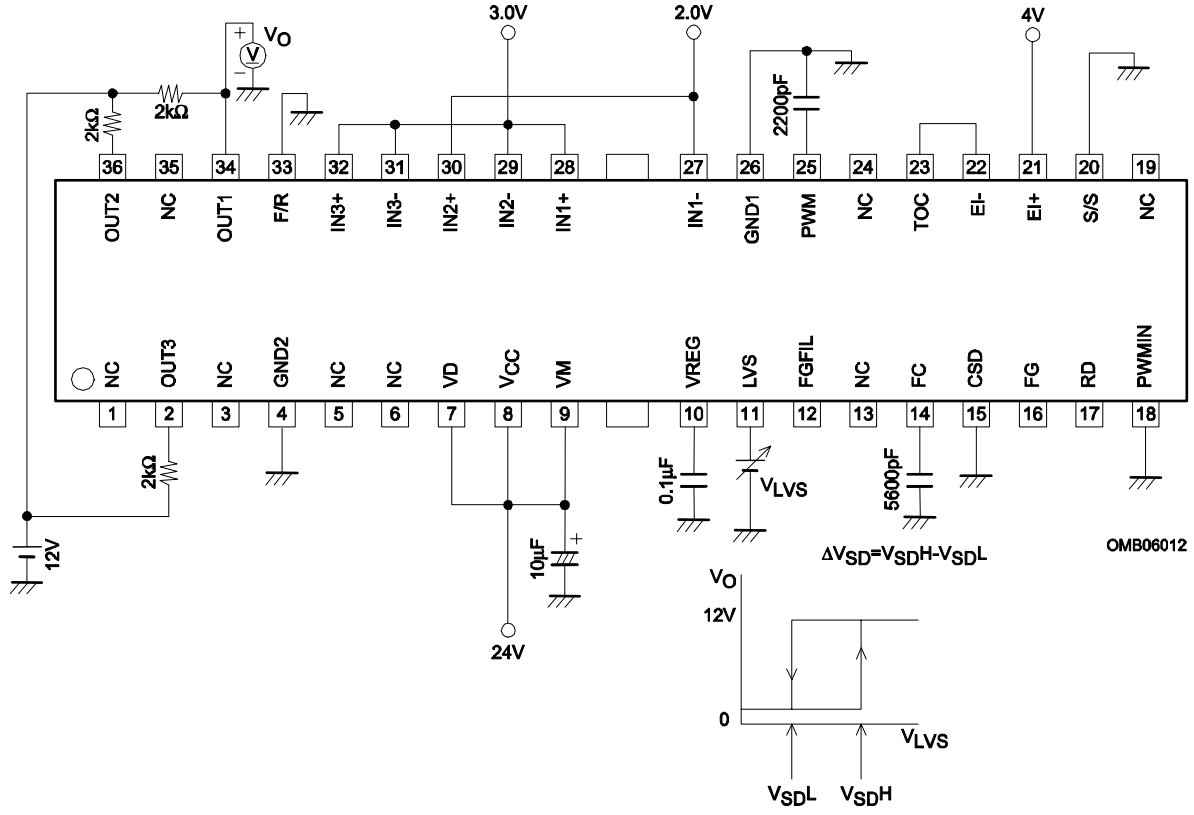


$I_{CSD}1$, $I_{CSD}2$

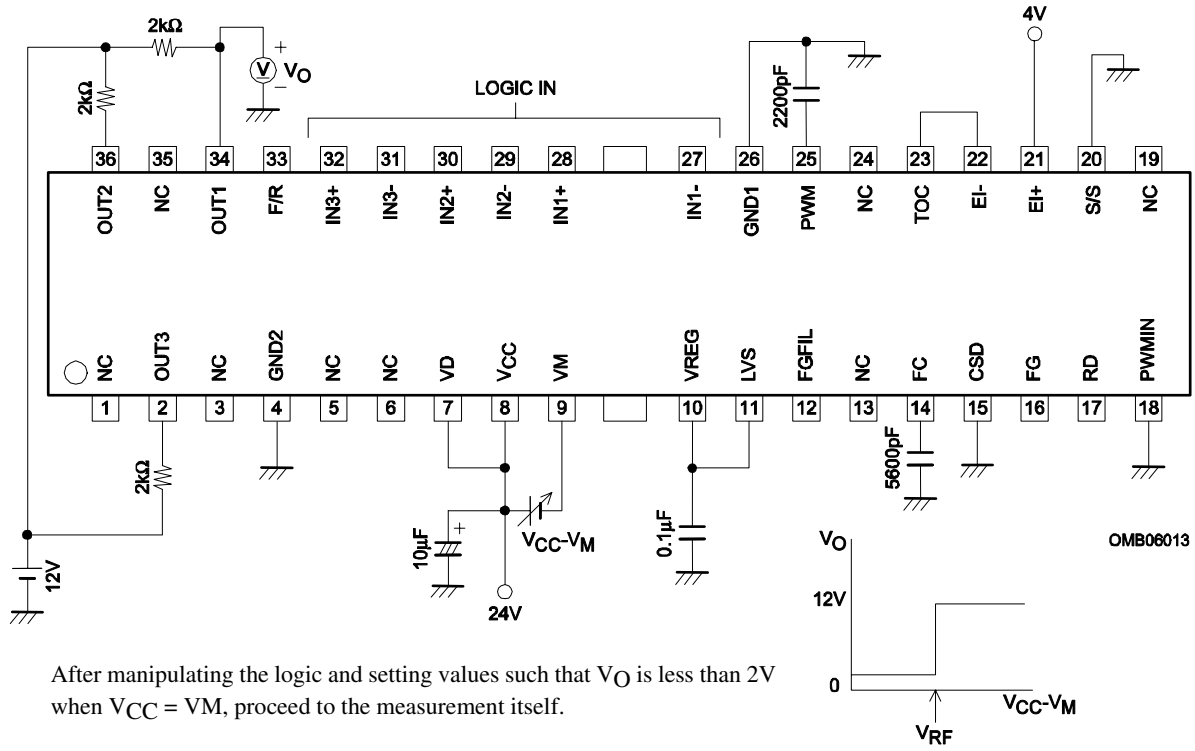


Change V_{IN} from 0.8V to 2.0V when measuring $I_{CSD}1$.
Change V_{IN} from 3.3V to 2.0V when measuring $I_{CSD}2$.

$V_{SD}L$, $V_{SD}H$, ΔV_{SD}

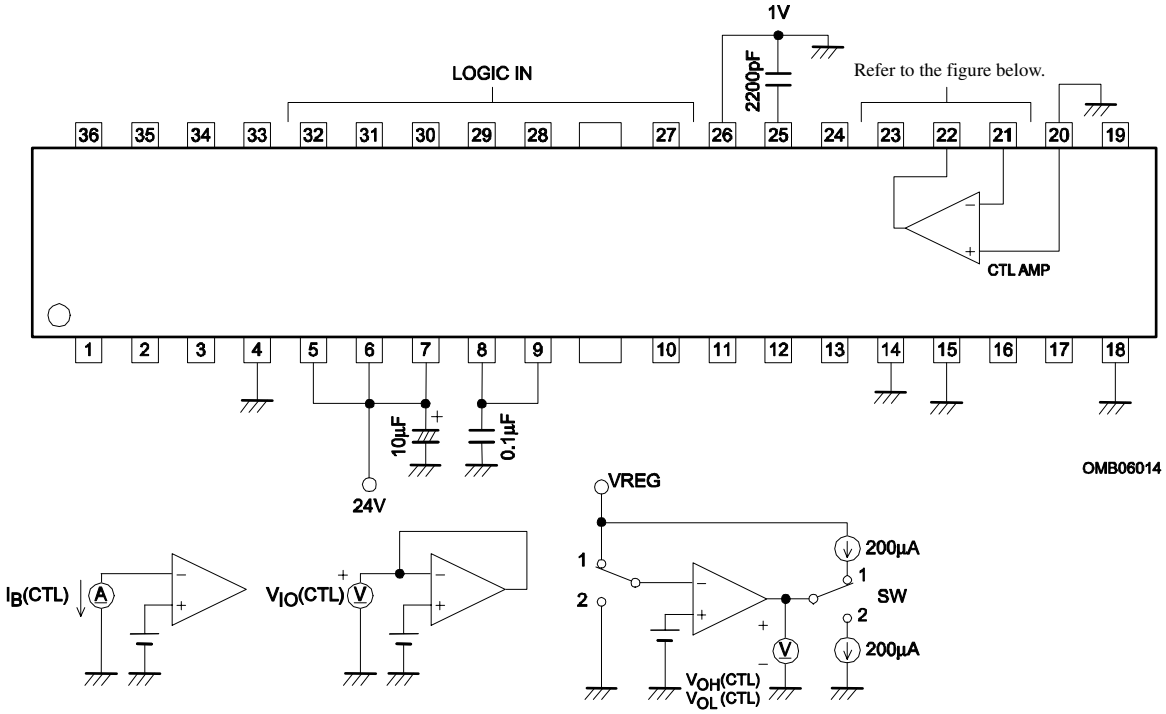


V_{RF}



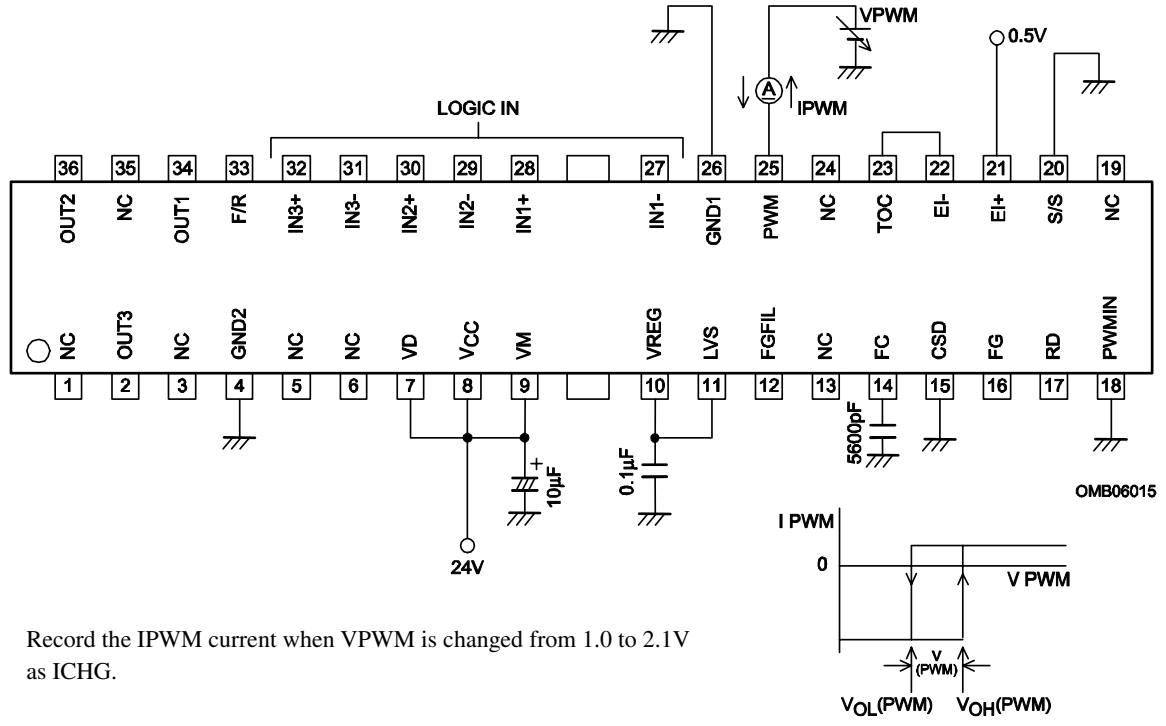
After manipulating the logic and setting values such that V_O is less than 2V when V_{CC} = VM, proceed to the measurement itself.

V_{IO}(CTL), I_B(CTL), V_{OH}(CTL), V_{OL}(CTL)



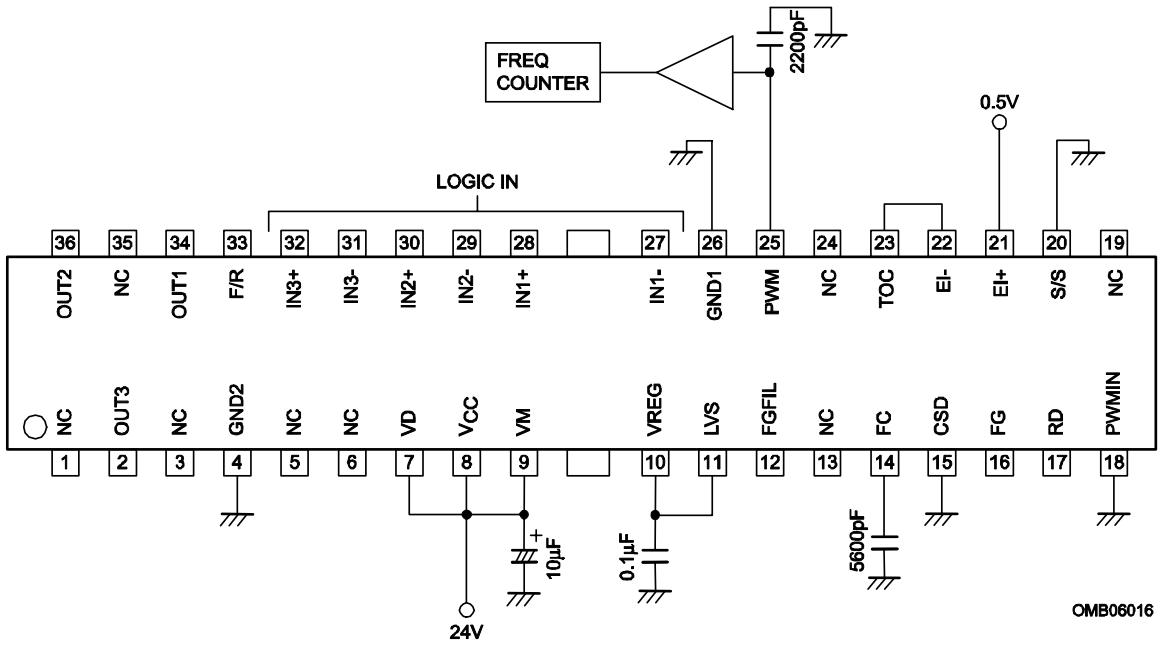
Set the switch SW to the 2 position when measuring V_{OH}(CTL).
Set the switch SW to the 1 position when measuring V_{OL}(CTL).

V_{OH}(PWM), V_{OL}(PWM), V(PWM), I_{CHG}(PWM)

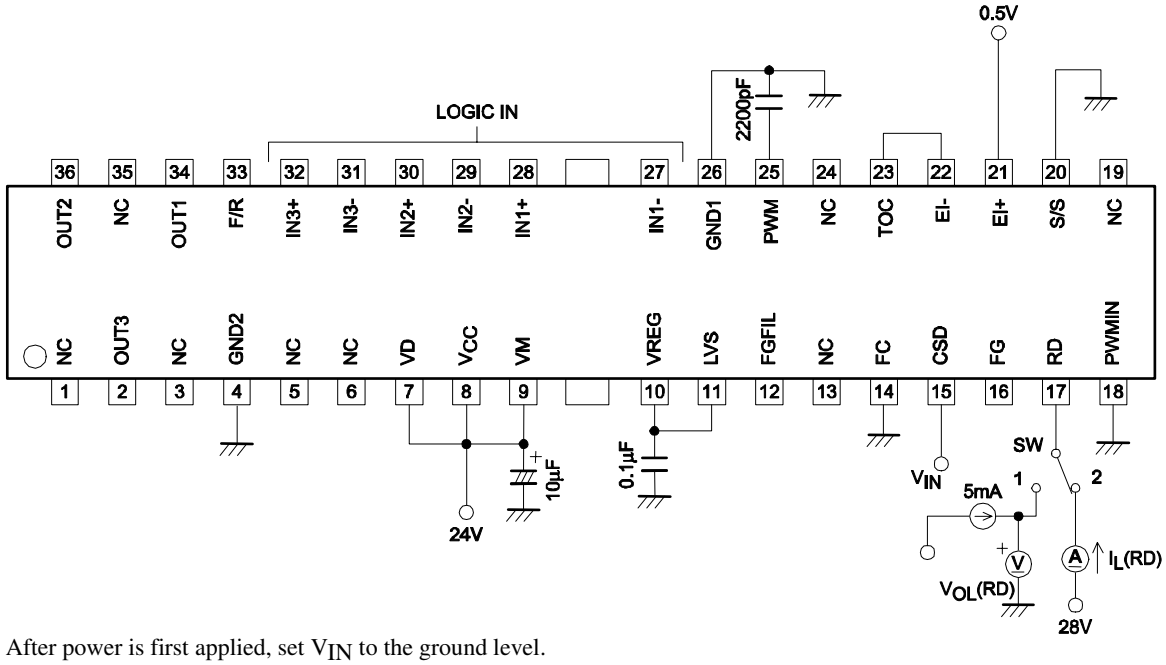


Record the IPWM current when VPWM is changed from 1.0 to 2.1V as ICHG.

f(PWM)

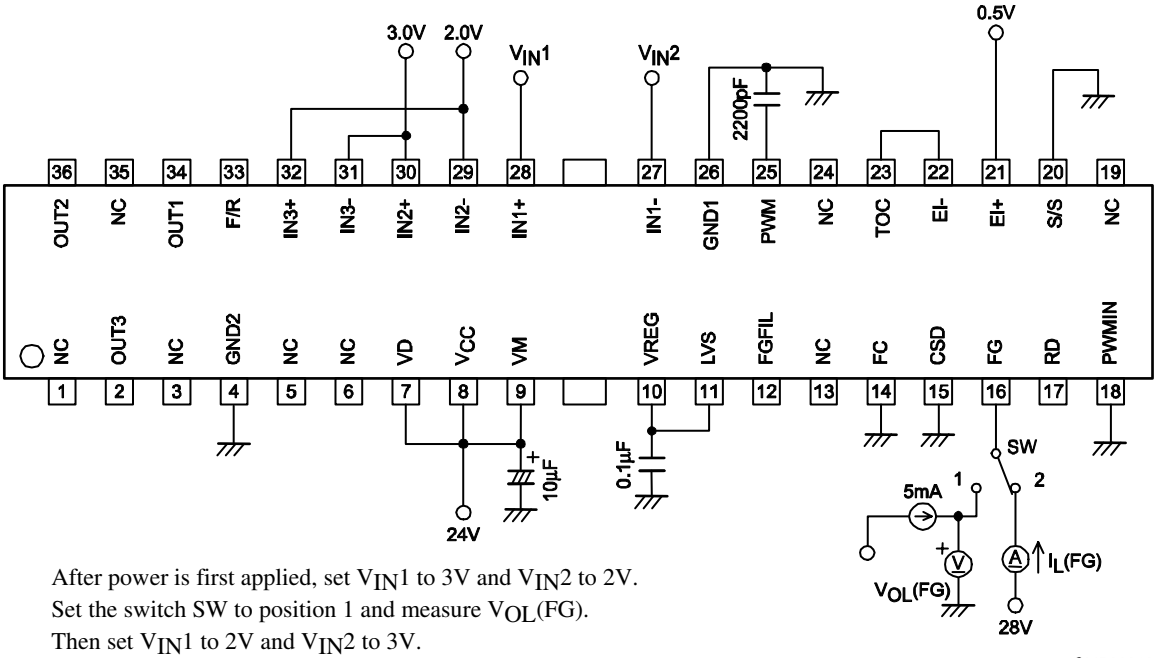


V_{OL}(RD), I_L(RD)



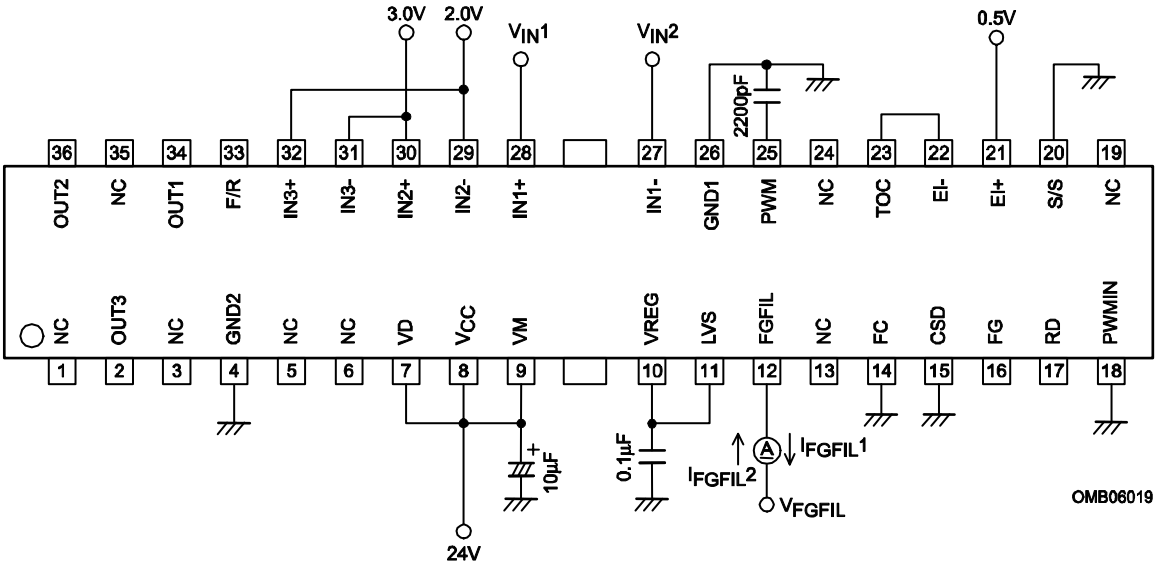
After power is first applied, set V_{IN} to the ground level.
Set the switch SW to position 1 and measure V_{OL} (RD).
Then set V_{IN} to 3.3V.
Set the switch SW to position 2 and measure I_L(RD).

$V_{OL}(FG)$, $I_L(FG)$



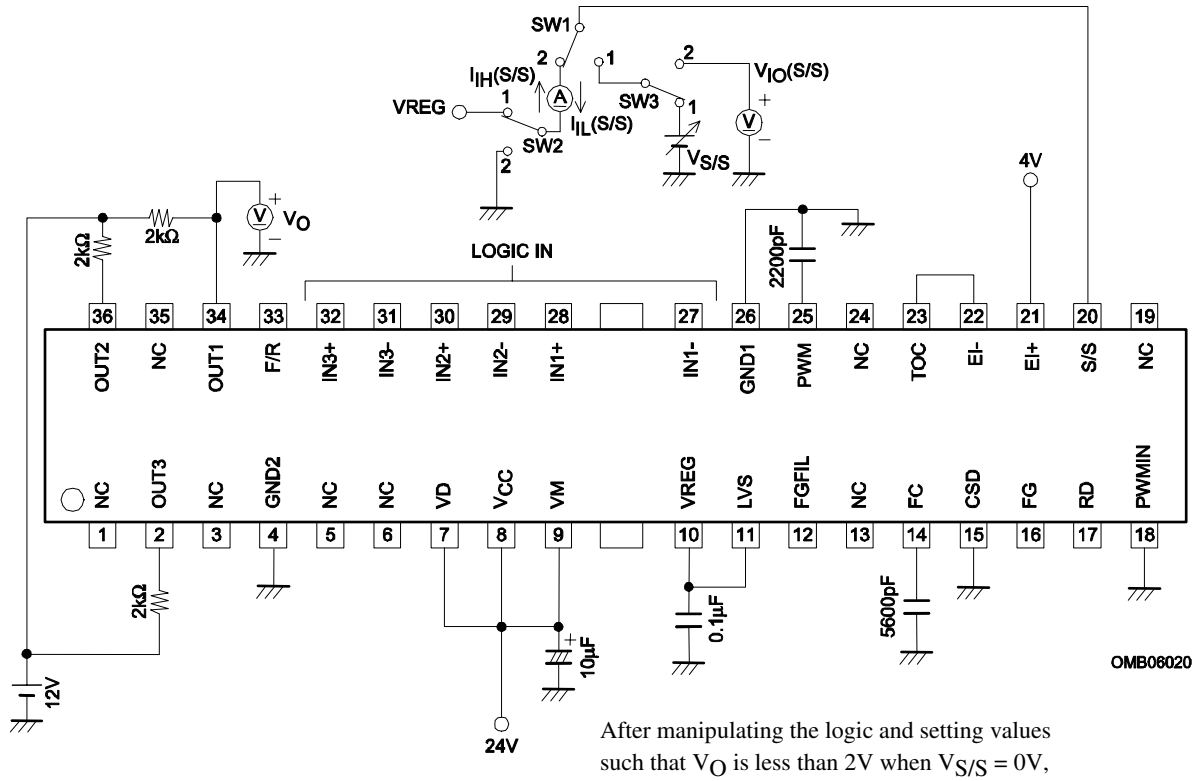
After power is first applied, set $V_{IN}1$ to 3V and $V_{IN}2$ to 2V.
Set the switch SW to position 1 and measure $V_{OL}(FG)$.
Then set $V_{IN}1$ to 2V and $V_{IN}2$ to 3V.
Set the switch SW to position 2 and measure $I_L(FG)$.

$I_{FGFIL}1$, $I_{FGFIL}2$



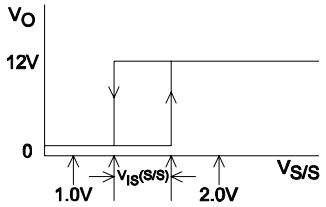
When measuring IFGFIL1, set $V_{IN}1$ = 3V, $V_{IN}2$ = 2V, and VFGIL from 0.5 to 2.0V.
When measuring IFGFIL2, set $V_{IN}1$ = 2V, $V_{IN}2$ = 3V, and VFGIL from 3.5 to 2.0V.

$V_{IH}(S/S)$, $V_{IL}(S/S)$, $V_{IO}(S/S)$, $V_{IS}(S/S)$, $I_{IH}(S/S)$, $I_{IL}(S/S)$



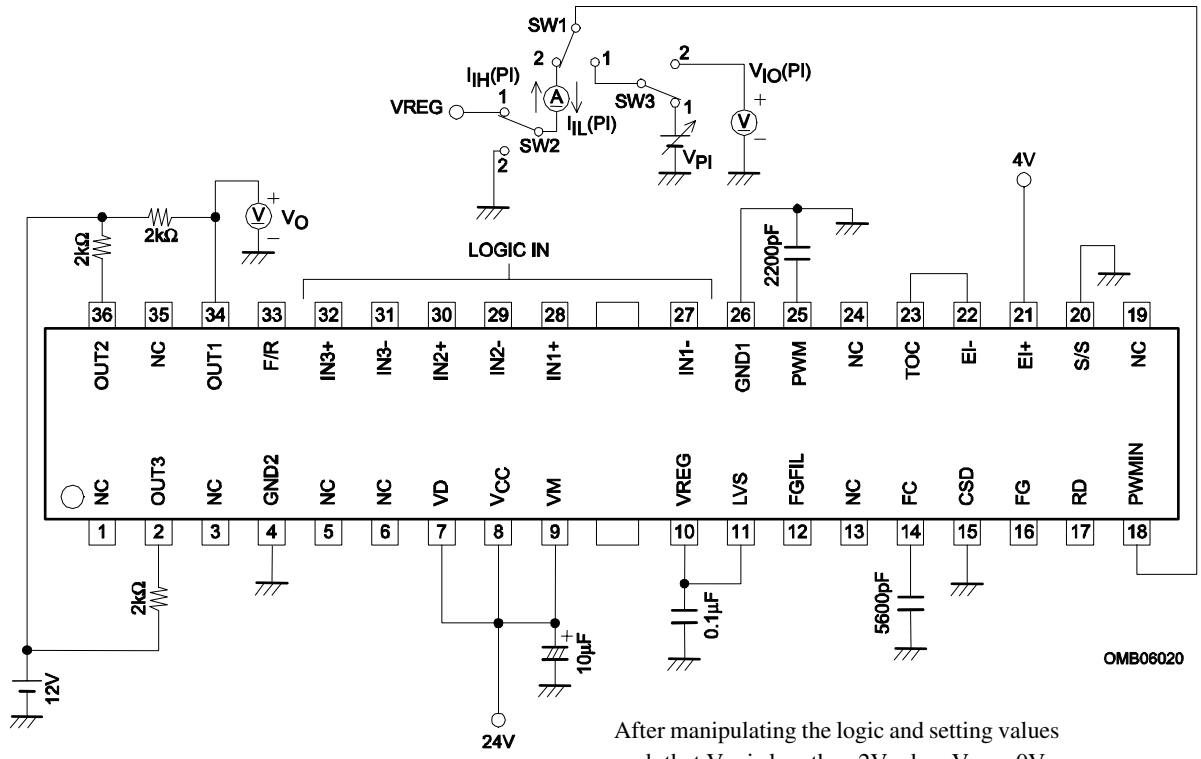
After manipulating the logic and setting values such that V_O is less than 2V when $V_{S/S}$ = 0V, proceed to the measurement itself.

	SW1	SW2	SW3
$V_{IH}(S/S)$	1	-	1
$V_{IL}(S/S)$	1	-	1
$V_{IO}(S/S)$	1	-	2
$I_{IH}(S/S)$	2	1	-
$I_{IL}(S/S)$	2	2	-



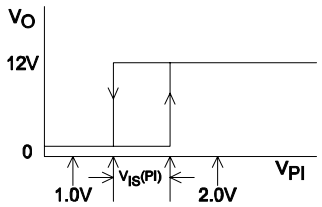
$V_{IH}(S/S)$, $V_{IL}(S/S)$: IC operation is OK as long as the output voltage changes when $V_{S/S}$ is between 1.0 and 2.0V.

$V_{IH(PI)}$, $V_{IL(PI)}$, $V_{IO(PI)}$, $V_{IS(PI)}$, $I_{IH(PI)}$, $I_{IL(PI)}$



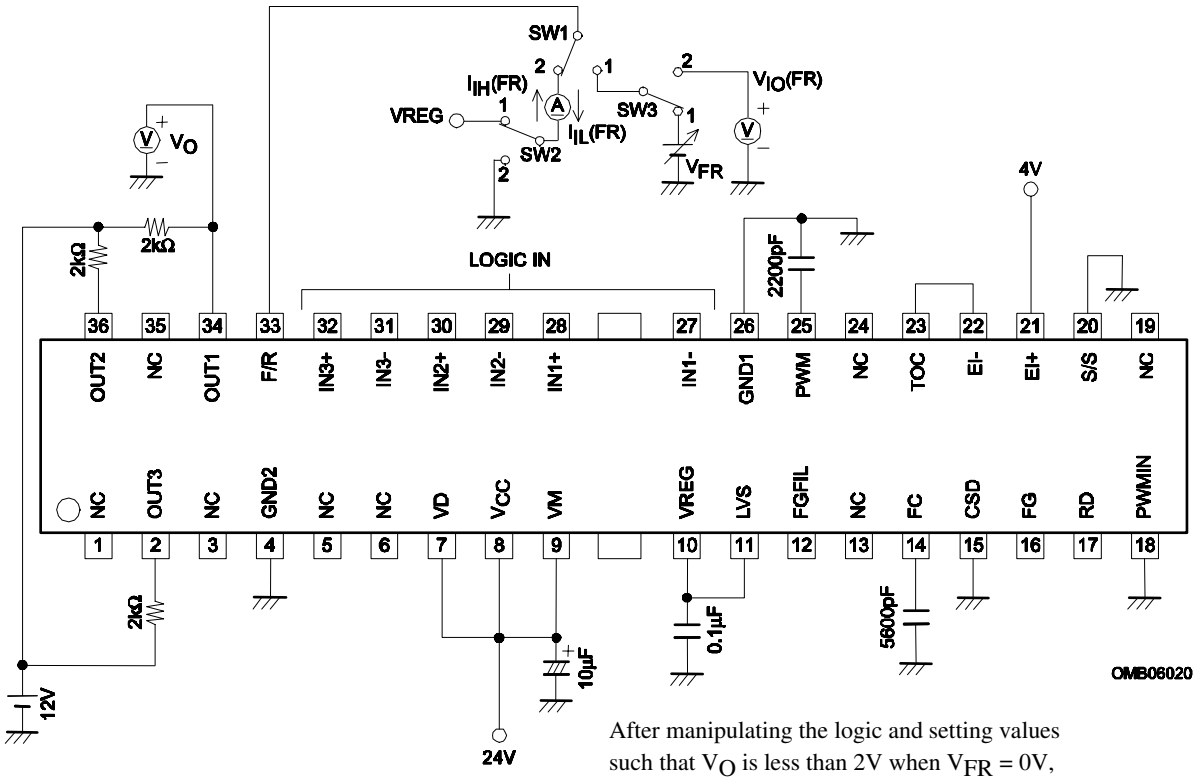
After manipulating the logic and setting values such that V_O is less than 2V when V_{PI} = 0V, proceed to the measurement itself.

	SW1	SW2	SW3
$V_{IH(PI)}$	1	-	1
$V_{IL(PI)}$	1	-	1
$V_{IO(PI)}$	1	-	2
$I_{IH(PI)}$	2	1	-
$I_{IL(PI)}$	2	2	-



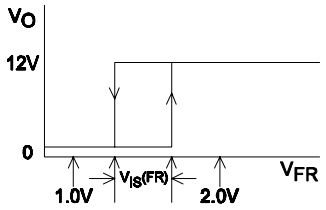
$V_{IH}(PI)$, $V_{IL}(PI)$: IC operation is OK as long as the output voltage changes when V_{PI} is between 1.0 and 2.0V.

$V_{IH}(FR)$, $V_{IL}(FR)$, $V_{IO}(FR)$, $V_{IS}(FR)$, $I_{IH}(FR)$, $I_{IL}(FR)$



After manipulating the logic and setting values such that V_O is less than 2V when V_{FR} = 0V, proceed to the measurement itself.

	SW1	SW2	SW3
$V_{IH}(FR)$	1	-	1
$V_{IL}(FR)$	1	-	1
$V_{IO}(FR)$	1	-	2
$I_{IH}(FR)$	2	1	-
$I_{IL}(FR)$	2	2	-



$V_{IH}(FR)$, $V_{IL}(FR)$: IC operation is OK as long as the output voltage changes when V_{FR} is between 1.0 and 2.0V.