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W-LAN / LAN Module Data Sheet

Cypress WLAN / LAN Chipset CYW43907

Electric Imp P/N : imp005
MURATA P/N : LBWA1UZ1GC-901

This Datasheet is a preliminary version, and subject to change without notice.

The revision history of the product specification

Issued Date	Revision Code	Revision Page	Changed Items	Change Reason
Dec. 25. 2015			First Issue	
Mar. 18. 2016	A	P5 P6 P11 P13 P14 P21	Adding Structure Adding Pin Layout Revised 6. Operating Condition Adding 9. Digital I/O Requirements Revised 10. RF Characteristics Adding 12. Reference Circuit	Update
Dec. 30. 2016	B	P3 P4 P7 P11 P12 P13 P16 P17 P18 P19 -	Modifying Scope and Part Number Changing Block diagram. Updated 4.2. Terminal configurations Adding 5. LED Drive Adding 6. Phototransistor Adding 7. SPI Flash Requirements Updated 12. Pin characteristics Updated 13. Land pattern Updated 14. Reference circuits Updated 15. Recommended component Erased RF Characteristics	Update

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Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

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1. Scope

This specification is for the LBWA1UZ1GC (imp005) module that provides connectivity to the internet via WiFi or Ethernet.

The device is pre-provisioned with keys to boot impOS – a fully maintained, secure OS that is part of the Electric Imp cloud service.

- 802.11 a/b/g/n 1x1 WiFi (dual band 2.4GHz & 5GHz)
  - 802.11a 13.0dBm +/-2.0dBm
  - 802.11b 17.0dBm +/-2.0dBm
  - 802.11g 13.0dBm +/-2.0dBm
  - 802.11n(5GHz) 12.0dBm +/-2.0dBm (20/40MHz channels)
  - 802.11n(2.4GHz) 12.0dBm +/-2.0dBm (20MHz channels)
  - RX Sensitivity -97dBm typical (@1Mbps)
  - Diversity antenna switch outputs
  - Supports WPA, WPA2, WPS
- 10/100MHz Ethernet MAC
  - Connects to external RMII Ethernet PHY & magnetics
- 32-bit Cortex R4 application processor
  - Secure boot from external QSPI
  - 32kB instruction & data caches
  - Over 1.2MB RAM for application use
  - 256kB of secure application storage on external QSPI
  - Secure credential storage on external QSPI
- Electric Imp OS & service
  - Robust embedded operating system with fail-safe & secure OS & application updates
  - Pre-provisioned MAC addresses (per interfdace) & per device secrets
  - TLS1.2-RSA-ECDHE (forward secrecy) cloud connection
  - Elliptic curve challenge-response to prevent device impersonation
  - Fully featured cloud VM for every device for easy integration with cloud services
  - Open source integrations with AWS, Azure, IBM Watson, etc
- LED drive for red/green status LEDs
- Phototransistor input for Electric imp's patented BlinkUp™ technology
  - Provides secure, replay-proof provisioning from a mobile app or webpage
- Flexible I/O
  - 28x GPIO, configurable to support 1x SPI, 1x I2C and 6xPWM
  - Dedicated interfaces: 1x SPI, 1x I2C, 3x UART, 1x USB host
- Compliant with the RoHS directive

2. Part Number

Sample Part Number
LBWA1UZ1GC-TEMP-IMP

Production Part Number
LBWA1UZ1GC-901

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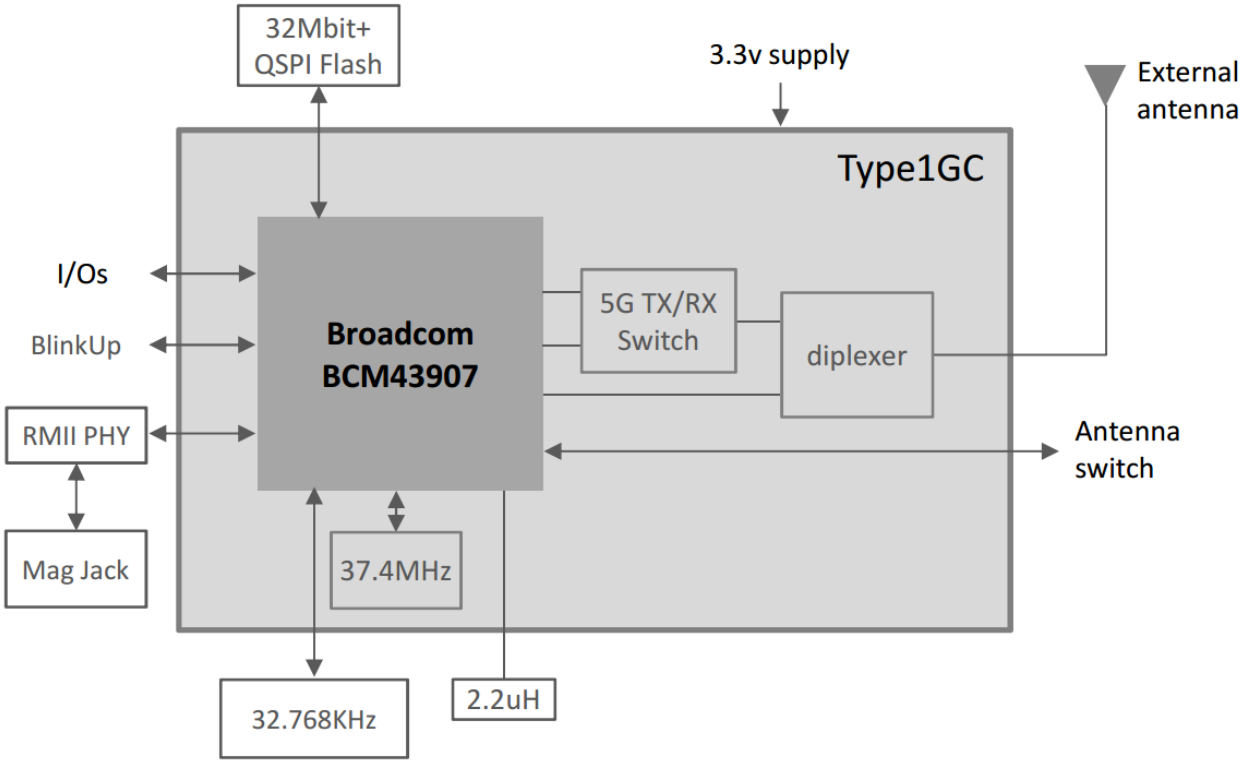
3. Block Diagram



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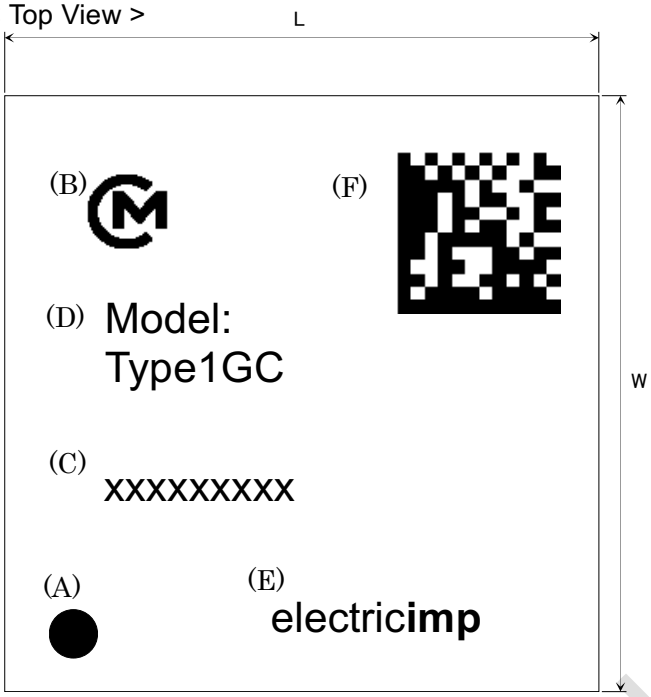
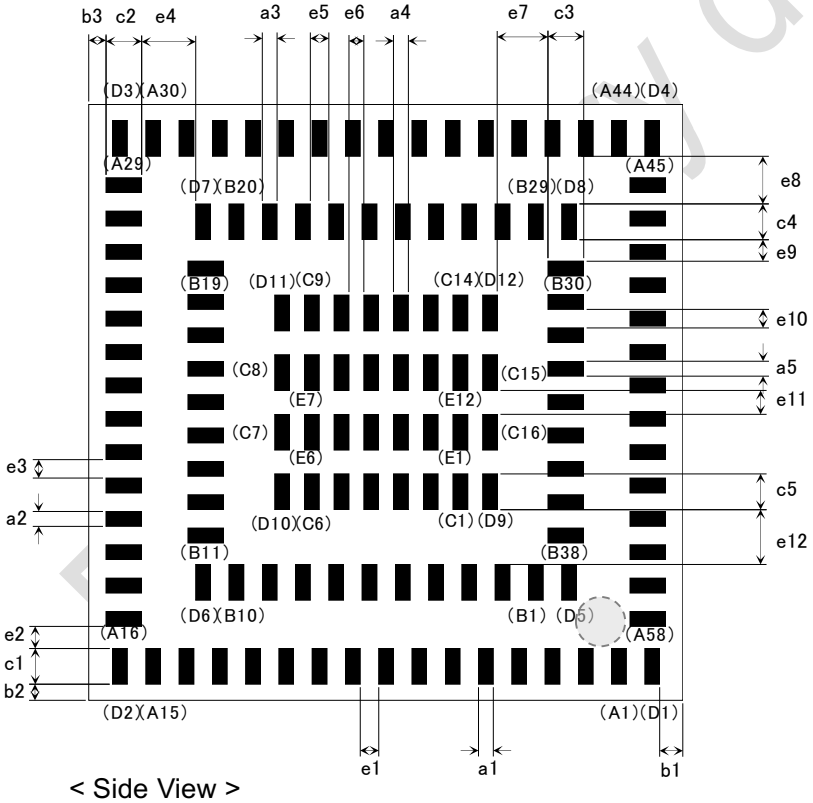
4. Dimensions, Marking and Terminal Configurations

4.1. Dimensions

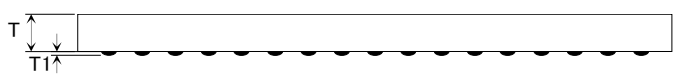
< Top View >



< Bottom View: **NOTE THIS IS BOTTOM VIEW** >



< Side View >



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Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	10.0 +/- 0.2	W	10.0 +/- 0.2		
T	1.20 max.	T1	0.07 typ.		
a1	0.25 +/- 0.1	a2	0.25 +/- 0.1	a3	0.25 +/- 0.1
a4	0.25 +/- 0.1	a5	0.25 +/- 0.1		
b1	0.395 +/- 0.2	b2	0.293 +/- 0.2	b3	0.313 +/- 0.2
c1	0.55+/- 0.1	c2	0.55+/- 0.1	c3	0.55+/- 0.1
c4	0.55+/- 0.1	c5	0.55+/- 0.1		
e1	0.31 +/- 0.1	e2	0.392 +/- 0.1	e3	0.31 +/- 0.1
e4	0.932 +/- 0.1	e5	0.31 +/- 0.1	e6	0.25 +/- 0.1
e7	0.882 +/- 0.1	e8	0.858 +/- 0.1	e9	0.384 +/- 0.1
e10	0.31 +/- 0.1	e11	0.45 +/- 0.1	e12	0.974+/- 0.1

(unit : mm)

Marking

Marking	Meaning
(A)	Pin 1 Marking
(B)	Murata Logo
(C)	Inspection Number
(D)	Module Type
(E)	Electric Imp Logo
(F)	2D code

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4.2. Terminal Configurations

Pin#	Name	Type	Description
D1	SFLASH_MISO_3	I/O	Flash data bit 4
A1	SFLASH_CLK	O	Flash clock
A2	SFLASH_MOSI_0	I/O	Flash data bit 1
A3	SFLASH_MISO_2	I/O	Flash data bit 3
A4	SFLASH_CS_L	O	Flash slave select
A5	GND	GND	
A6	RF_ANT0	I/O	Antenna port 0
A7	GND	GND	
A8	TEST_3V3	I	Tie high
A9	pinB	I/O	GPIO/SPI MOSI (default driven high)
A10	pinD	I/O	GPIO/SPI nCS (default driven high)
A11	pinA	I/O	GPIO/SPI CLK (default driven low)
A12	pinC	I/O	GPIO/SPI MISO
A13	RMII_TXEN	O	RMII Transmit Enable
A14	RMII_CRS_DV	I	Receive Data Valid
A15	RMII_MDC	O	RMII Management Data Clock
D2	RMII_TXD0	O	RMII Transmit Data Output
A16	RMII_RXD0	I	RMII Receive Data Input
A17	RMII_REF_CLK	I	Transmit Clock
A18	RMII_RXD1	I	RMII Receive Data Input
A19	RMII_TXD1	O	RMII Transmit Data Output
A20	RMII_MDIO	I/O	RMII Management Data I/O
A21	ANT1_DIV	O	ANT1 Diversity RF switch control
A22	VDD_3V0_IN	PWR	3.0V input: see design guide, sensitive trace. Connected to VDD_3V0_OUT.
A23	XTAL32K_IN	I	XTAL input
A24	XTAL32K_OUT	O	XTAL output
A25	ANT0_DIV	O	ANT0 Diversity RF switch control
A26	pinE	I/O	GPIO/PWM (default driven low)
A27	pinF	O	GPIO/PWM (default driven low)
A28	USB2_DN	I/O	USB Host Data Minus
A29	USB2_DP	I/O	USB Host Data Plus
D3	GND	GND	
A30	n/c	n/c	
A31	pinG	O	GPIO/PWM (default driven low)
A32	TEST_GND	I	Tie low
A33	GND	GND	
A34	USB_VDD_3V3	PWR	3.3V supply for USB
A35	VDD_3V3_IN_2	PWR	3.3V input
A36	GND	GND	
A37	VDDIO	PWR	I/O supply

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A38	GND	GND	
A39	VDD_3V0_OUT	PWR	3.0V output of internal LDO
A40	GND	GND	
A41	DCDC_IN	PWR	Input to internal PMU LDO
A42	GND	GND	
A43	VDD	PWR	Main power input (VBAT)
A44	DCDC_OUT	PWR	PMU CBUCK Switching Regulator Out
D4	GND	GND	
A45	pinH	I/O	GPIO
A46	pinK	I/O	GPIO/i2cJK SDA (default driven high)
A47	pinJ	I/O	GPIO/i2cJK SCL (default driven low)
A48	n/c	n/c	
A49	pinM	I/O	GPIO
A50	BLINKUP_DIN	I	Blinkup data input
A51	BLINKUP_EN_L	O	Blinkup power enable (high = on)
A52	UART0_RXD	I	uart0 serial input
A53	UART0_RTS	O	uart0 request-to-send
A54	UART0_CTS	I	uart0 clear-to-send
A55	UART0_TXD	O	uart0 serial output
A56	VDDIO_3V3	PWR	I/O supply
A57	VDDIO_3V3	PWR	I/O supply for RMII
A58	SFLASH_MISO_1	I/O	Flash data bit 2
D5	n/c	n/c	
B1	pinL	I/O	GPIO
B2	I2C0_SCL	I/O	i2c0 SCL
B3	GND	GND	
B4	pinXA	I/O	GPIO/WAKE
B5	n/c	n/c	
B6	n/c	n/c	
B7	n/c	n/c	
B8	n/c	n/c	
B9	n/c	n/c	
B10	n/c	n/c	
D6	n/c	n/c	
B11	GND	GND	
B12	RESET_L	I	Reset (not recommended for chip reset, see PWR_DWN_L)
B13	HIB_WAKE_L	I	Pull-up to 3v3
B14	UART1_RXD	I	uart1 RXD (default driven low: note, use series resistor to limit current at boot)
B15	UART1_TXD	O	uart1 RXD
B16	n/c	n/c	
B17	TEST_GND	I	Tie low

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B18	UART2_RXD	I	uart2 RXD (default driven low: note, use series resistor to limit current at boot)
B19	pinR	I/O	GPIO/USB_PWR_EN
D7	pinS	I/O	GPIO/PWM (default driven low)
B20	pinXB	I/O	GPIO/WAKE
B21	n/c	I/O	n/c
B22	n/c	I/O	n/c
B23	n/c	I/O	n/c
B24	n/c	I/O	n/c
B25	n/c	I/O	n/c
B26	n/c	I/O	n/c
B27	n/c	I/O	n/c
B28	GND	GND	
B29	GND	GND	
D8	pinT	I/O	GPIO
B30	SPI0_MOSI	O	spi0 SPI data master out
B31	SPI0_MISO	I	spi0 SPI data master in
B32	SPI0_CLK	O	spi0 SPI clock
B33	SPI0_CS_L	O	spi0 SPI slave select
B34	GND	GND	
B35	Red LED	O	Red LED drive (CA/CC – fit 10k resistor across red LED for CA/CC detect)
B36	Green LED	O	Green LED drive (CA/CC)
B37	pinQ	I/O	GPIO (default driven low)
B38	pinP	I/O	GPIO
D9	GND	GND	
C1	I2C0_SDA	I/O	i2c0 SDA
C2	pinXC	I/O	GPIO/WAKE
C3	pinXD	I/O	GPIO/WAKE
C4	n/c	n/c	
C5	PWR_DWN_L	I	Pull low to power chip down. Pull high to wake chip up. Use in preference to RESET_L if chip reset is desired
C6	TEST_GND	I	Tie low
D10	GND	GND	
C7	UART2_TXD	O	uart2 TXD
C8	GND	GND	
D11	GND	GND	
C9	pinU	I/O	GPIO/PWM (default driven low)
C10	pinV	I/O	GPIO/PWM (default driven low)
C11	pinW	I/O	GPIO/USB fault indication
C12	VDDIO_3V3	PWR	I/O supply
C13	pinXE	I/O	GPIO/WAKE
C14	pinY	I/O	GPIO

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D12	GND	GND	
C15	TEST_3V3	I	Tie high
C16	pinN	I/O	GPIO
E1	GND	GND	
E2	GND	GND	
E3	GND	GND	
E4	GND	GND	
E5	GND	GND	
E6	GND	GND	
E7	GND	GND	
E8	GND	GND	
E9	GND	GND	
E10	GND	GND	
E11	GND	GND	
E12	GND	GND	

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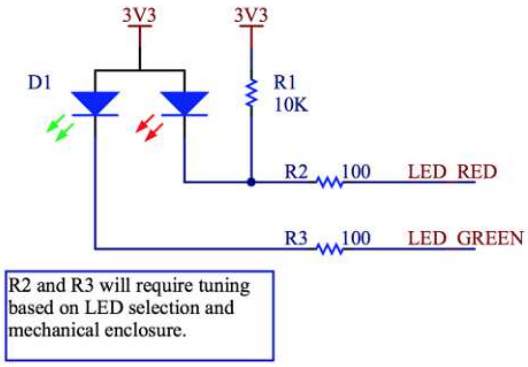
5. LED Drive

The indicator LED should be bicolor, because red, green and amber (red+green) are used to indicate status.

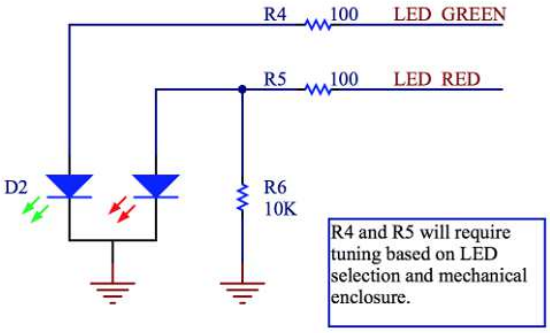
The LED drive pins will auto-detect common anode or common cathode parts. The detection is done by looking to see which way up the LED_RED pin is idling at boot; to ensure this works correctly, please place a 10k resistor in parallel with the red LED.

The current drive on these pins is 8mA maximum.
Please refer to section 15 for the recommended LEDs.

<Common anode diagram>



<Common cathode diagram>



Two specific LED codes indicate errors when talking to the SPI flash:

SPI flash not found	amber	red	off
SPI flash error	red	amber	off

If you encounter either of these codes, then this indicates an electrical connection issue or an incompatible flash part.

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6. Phototransistor

The phototransistor is used to receive BlinkUp configuration data. Unlike other imps, the imp005 does not have an on-board ADC, so an external ramp ADC circuit is used to capture the light levels. This circuit feeds a pulse train into the imp where it is interpreted by software.

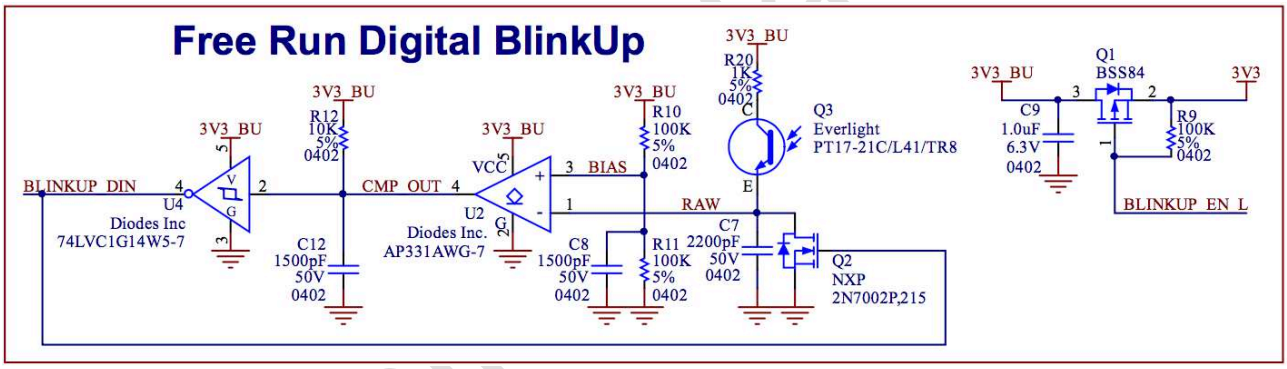
Sensitivity is tuned by adjusting C7 – a smaller capacitor increases sensitivity. Typically, the value used will range between 470pF and 4700pF, and the value should only be picked when the final optical path is available for testing. Please see the section on tuning blinkup on www.electricimp.com. Note that a C0G capacitor with 5% or better tolerance is recommended to reduce unit to unit variation.

The components used here have been chosen to be easily available and low cost. U2 is a simple comparator which triggers when the voltage on C7 rises to above 0.5xVDD, and R12/C12 and U4 give a fixed length pulse at the start of every slot, turning on Q2 to drain C7.

If the application is not power sensitive, Q1/R9 can be removed, connecting 3V3_BU directly to the main 3V3 rail.

End-user BlinkUp sends data at between 30 and 60 bits per second, depending on the user's device. For factory configuration, data is typically sent at 142 bits per second using red LED(s) in a test fixture. If your application does not require optical configuration, config can be sent electrically at 142 bits per second from another micro using the OPTO_IN pin. Please contact us for more details.

Please refer to section 15 for recommended phototransistors.



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7. SPI Flash Requirements

An external SPI Flash part is required for operation.

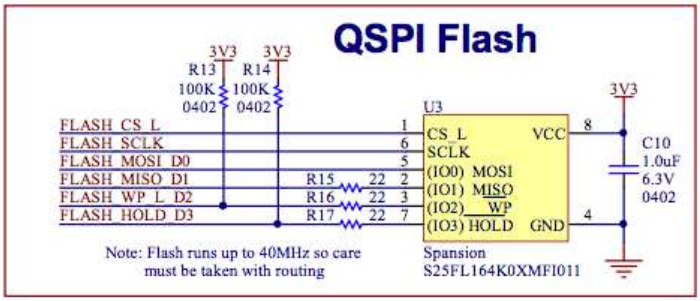
Minimum Size	32 Mbit (4 MByte)
Reserved for OS (must be pre-programmed)	0x000000 to 0x35E000 (3448 kByte)

The minimum size of the SPI Flash is 32Mbit (4MB), and the maximum size is 128Mbit (16MB). The area below address 0x35E000 (3448kB) is reserved for use by the OS. The remainder of the flash device is made available to user code programmatically, and may optionally be pre-programmed for user applications before assembly.

The imp005's SPI flash chip **must** support both 4KB and 64KB erases (command 0x20 and 0xD8) and Page Program (command 0x02).

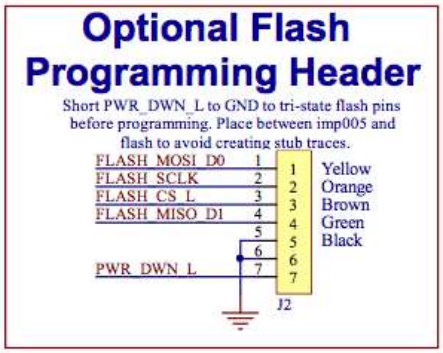
Though the imp005 always boots in single bit mode, it will move to QSPI if this is enabled via the device configuration page within flash. See the imp005 hardware design guide for more information on the device configuration page.

We recommend fitting 22R source termination resistors near the imp005 (for SCLK & MOSI/IO0) and the flash (for MISO/IO1, nWP/IO2 and HOLD/IO3).



The OS image must be loaded onto the flash before the device will operate

This can be done before SMT, or in-circuit by asserting the PWR_DWM_L signal and driving the SPI bus directly; the imp005 breakout board exposes the necessary pins for this on a 0.1" header. The public cloud OS image is available for download from the imp005 design section of www.electricimp.com



Note that the imp005, unlike the Murata 1GC, is pre-loaded with AES & RSA keys that will only accept firmware images signed by Electric Imp's FIPS140-2 HSM. It is not possible to run generic WICED software on this part.

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8. Absolute Maximum Rating

		min.	max.	unit
Storage Temperature		-40	85	deg.C
Supply Voltage	VDD_VBAT	-0.5	5.5	V
	VDD1_35	-0.5	1.5	V
	USB_VDD_3V3	-0.5	3.9	V
	VDDIO	-0.5	3.9	V
	VDDIO_AUDIO	-0.5	3.9	V
	VDDIO_RMII	-0.5	3.9	V
	VDDIO_SD	-0.5	3.9	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters is set within operating condition.

9. Operating Condition

		min.	typ.	max.	unit
Operating Temperature Range(*1)		-30		70	deg.C
Specification Temperature Range		-20		70	deg.C
Supply Voltage	VDD_VBAT	3.13		4.8	V
	VDD1_35	1.3	1.35	1.5	V
	USB_VDD_3V3	2.97	3.3	3.63	V
	VDDIO	2.97	3.3	3.63	V
	VDDIO_AUDIO	1.71		3.63	V
	VDDIO_RMII	1.71		3.63	V
	VDDIO_SD	1.71		3.63	V

[Note] All RF characteristics in this datasheet are defined by Specification Temperature Range. Default configuration of VDD_3V3_IN and VDD_3V3_IN2 is to connect with VDD_3V3_LDO. Specifications require derating at extreme temperatures.

10. External 32.768 kHz Low-Power Oscillator

This module uses a secondary low frequency clock for low-power mode timing.

Parameter	***LPO Clock***	***unit***
Normal Input Frequency	32.768	kHz
Frequency Accuracy	+/-200	ppm
Duty Cycle	30 – 70	%
Input Signal Amplitude	200 – 3300	mVp-p
Signal Type	Square-wave, or Sine-wave	-
Input Impedance[1)]	>100k <5	Ohm pF
Clock Jitter (During Initial Start-up)	< 10,000	ppm

1) When power is applied or switched off.

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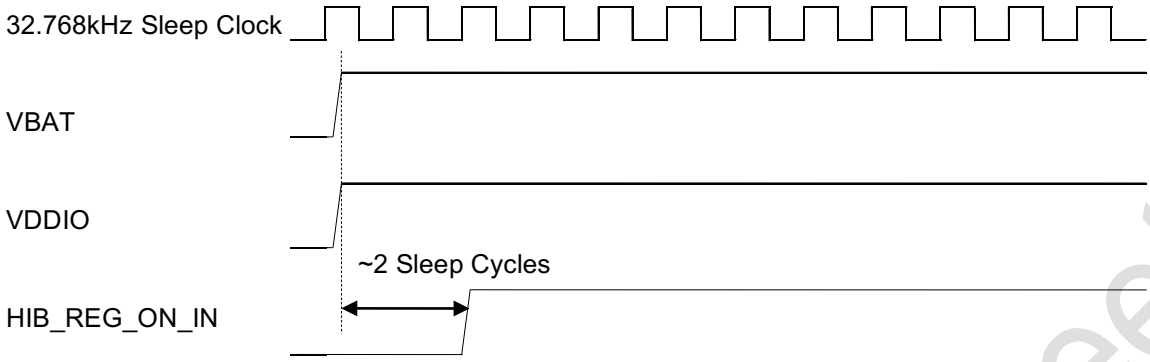
11. Power Up Sequence

Following timing diagram explain module power up sequence.



*Power down sequence is opposite sequence of power up.

Note: The CYW43907 has an internal power-on-reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC (internal LDO output) and VDDIO have both passed the POR threshold.

Note: The 10% - 90% VBAT rise time should not be faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

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12. Digital I/O Specifications

All specifications are at 3.3v.

Digital I/O Pins	Sym	min.	typ.	max.	unit
Input high voltage	VIH	2.00	-	-	V
Input low voltage	VIL	-	-	0.80	V
Output high voltage@2mA	VOH	VDDIO-0.4	-	-	V
Output low voltage@2mA	VOL	-	-	0.40	V

RF Switch control Output Pins	Sym	min.	typ.	max.	unit
Output high voltage@2mA	VOH	VDDIO-0.4	-	-	V
Output low voltage@2mA	VOL	-	-	0.4	V
Input capacitance	CIN	-	-	5	pF

GPIO, SPI, UART interfaces	Sym	min.	typ.	max.	unit
Input high voltage	VIH	2.0	-	VDDIO+0.5	V
Input low voltage	VIL	-0.5	-	0.8	V
Output high voltage@2mA	VOH	2.4	-	-	V
Output low voltage@2mA	VOL	-	-	0.4	V

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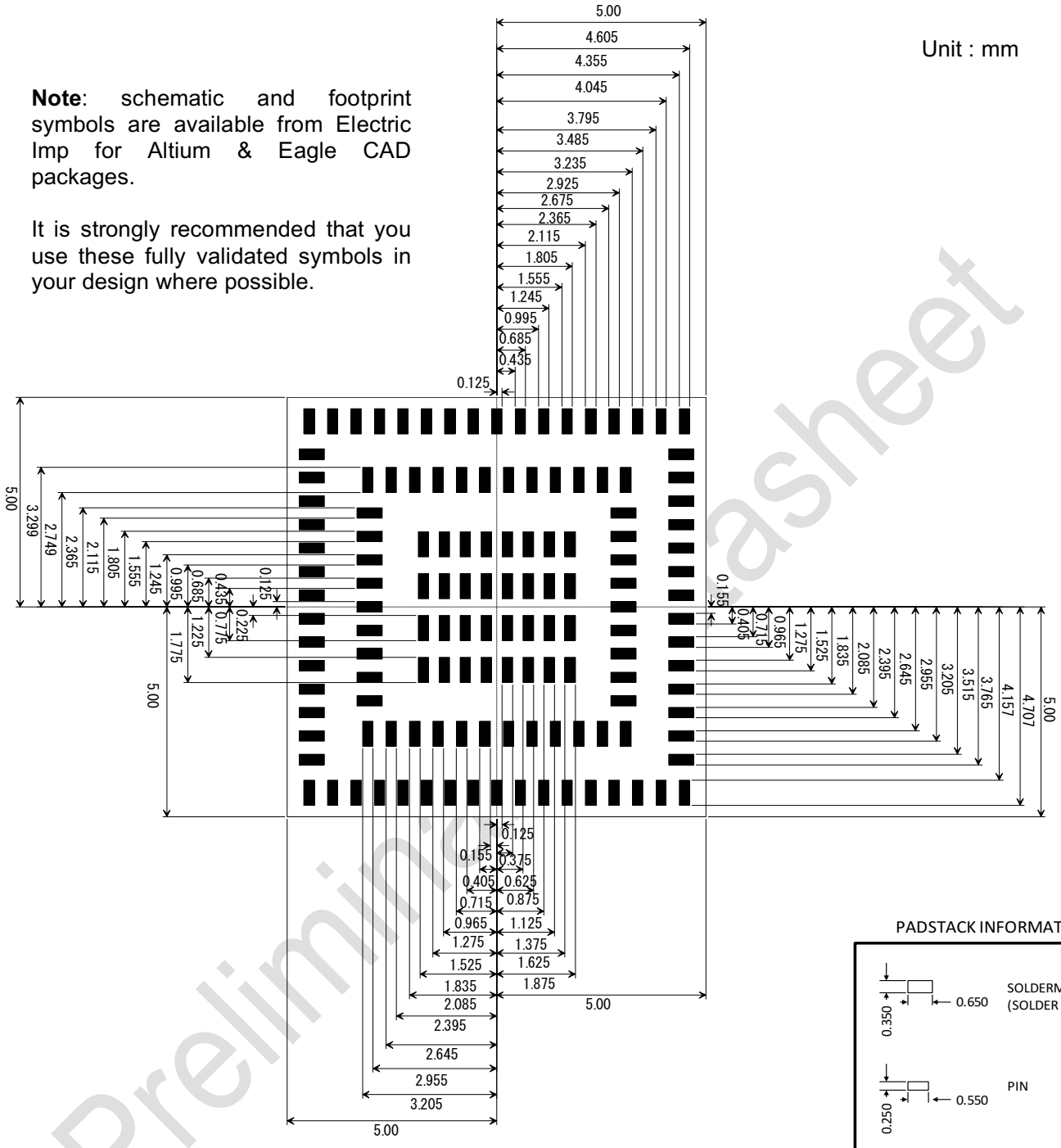
13. Land pattern (Top View)

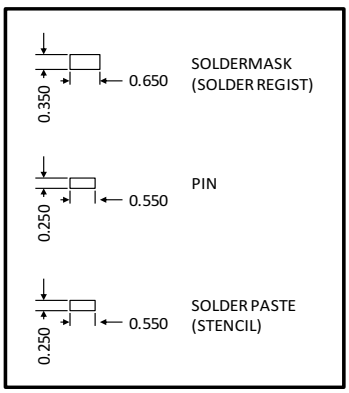
Unit : mm

Note: schematic and footprint symbols are available from Electric Imp for Altium & Eagle CAD packages.

It is strongly recommended that you use these fully validated symbols in your design where possible.



PADSTACK INFORMATION



Note: For PINs on the board that have a copper pour (flood) associated with it, usually the case with Ground PINs, please assure that the Land Pattern (PCB Footprint) for these PINs becomes Solder Mask Defined (SMD). In other words, the SOLDERMASK (SOLDER RESIST) for these Ground (GND) pins should be 0.550 mm x 0.250 mm (basically SODLERMASK (SOLDER RESIST) becomes same size as the PIN).

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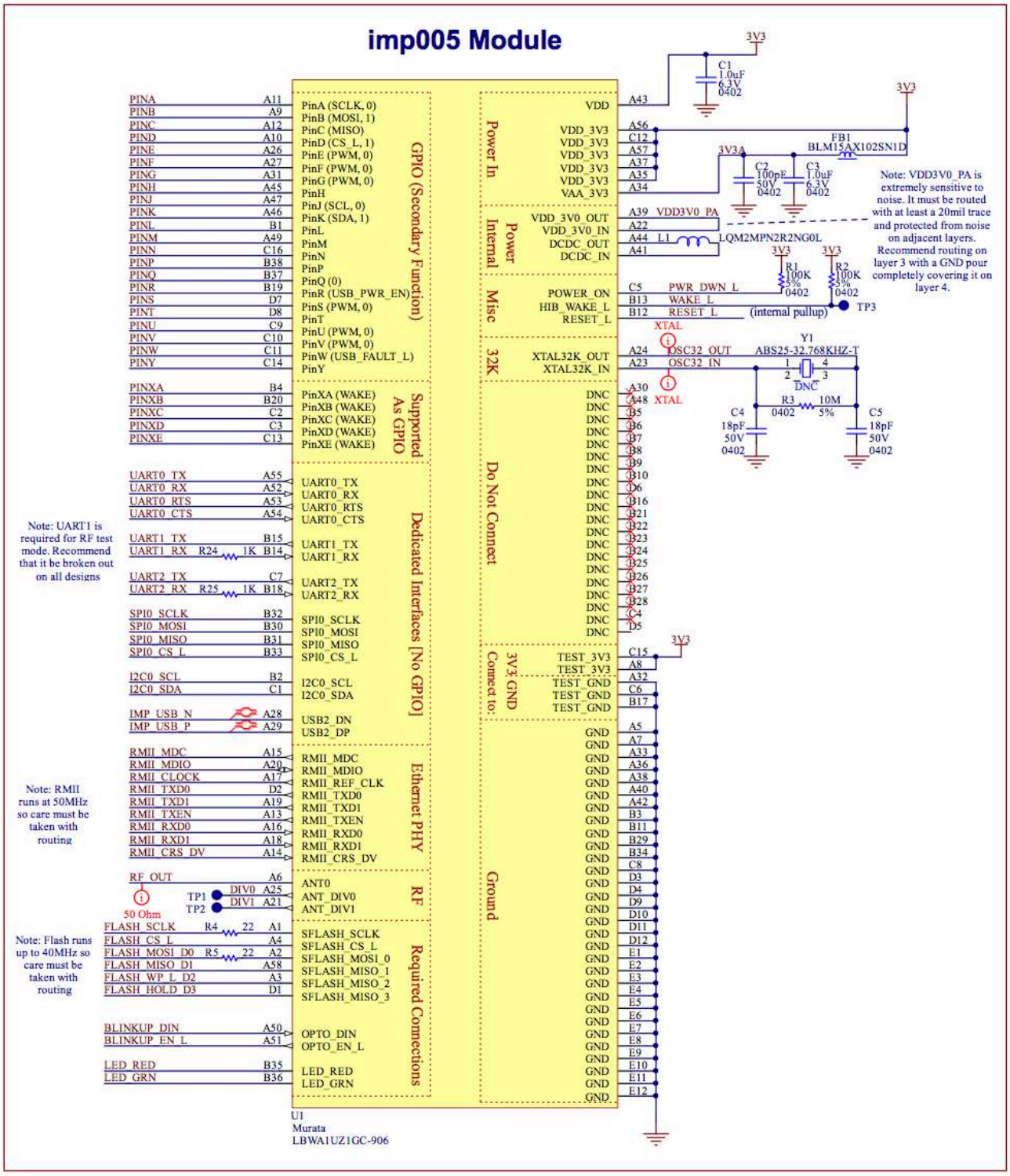
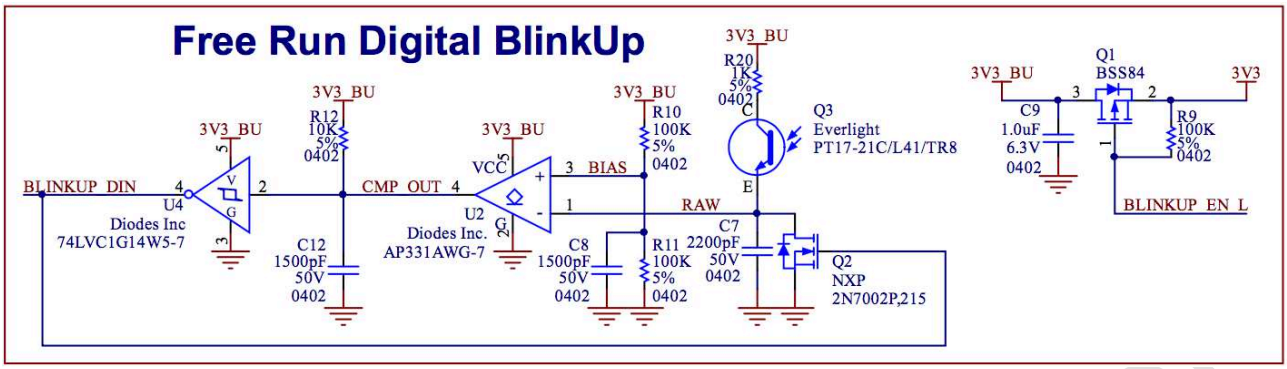
14. Reference Circuits

The Altium source files for many imp005-based designs are freely downloadable from www.electricimp.com in the imp005 design section. It's strongly recommended that new designs copy as much as possible from these reference designs.

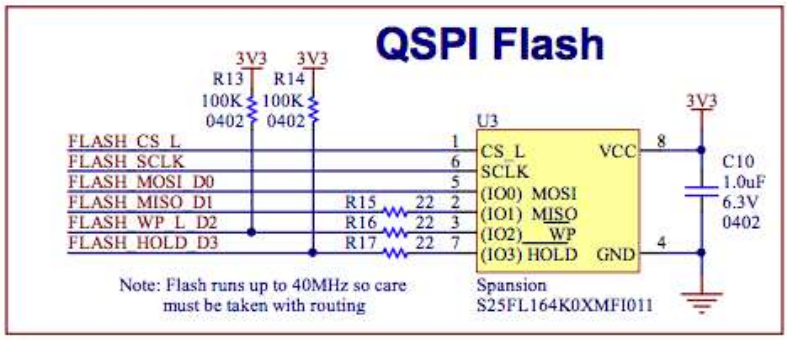
14.1. Module connections

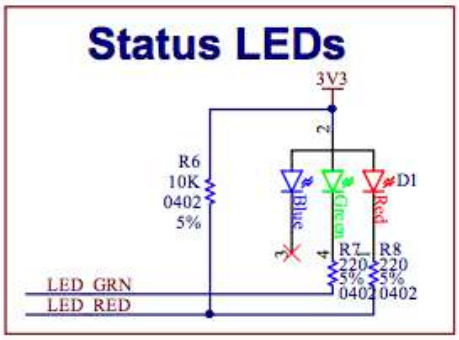


14.2. Blinkup circuit



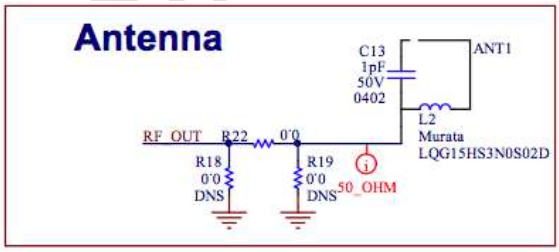
14.3. Boot flash & status indication





14.4. Antenna

When the Murata reference PCB antenna is used appropriately in your application, you may be able to reuse the FCC/IC modular approval of the type 1GC/imp005 module. Please contact Electric Imp for more details.



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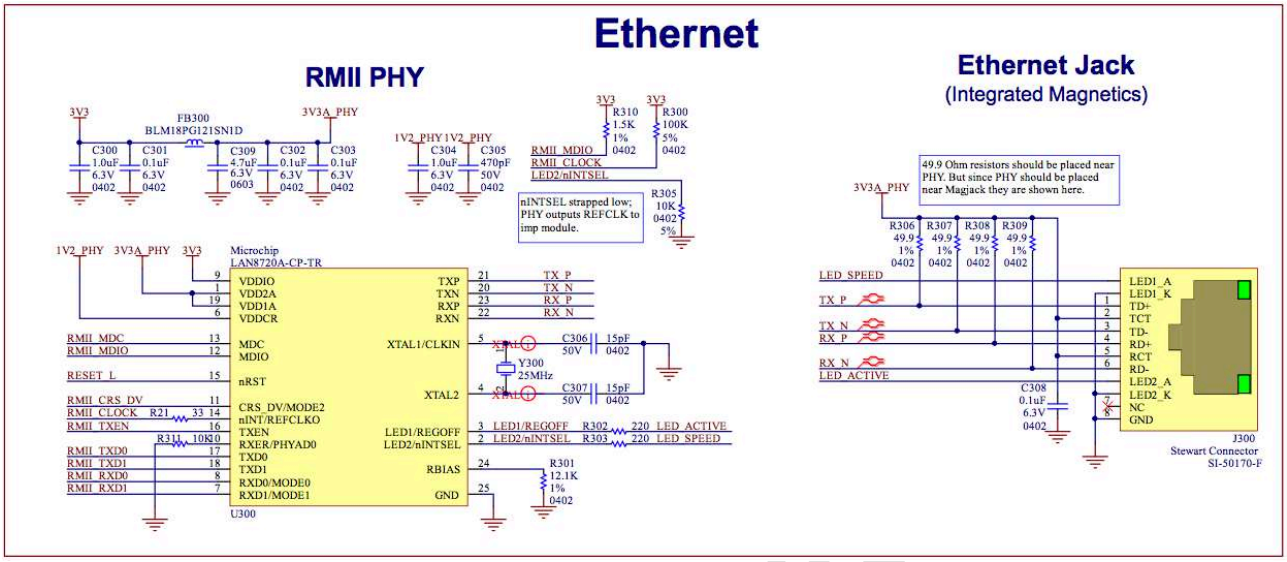
Murata Manufacturing Co., Ltd.

14.5. Ethernet 10/100Mbps

Take care when routing the RMII bus as it runs at 50MHz. See the imp005 breakout reference design for more information.

Example designs including PoE receivers are also available from Electric Imp.



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15. Recommended Components

15.1. Bi-color LED

	Manufacturer	Manufacturer's part number
Surface mount		
top-view	SunLED	XZMDKVG59W-1
	Liteon	LTST-C195KGJRKT
side-view	SunLED	XZMDKVG88W
	Bivar	SM1204BC
Through-hole		
3mm	SunLED	XLMDKVG34M
	Liteon	LTL1BEKVJNN

15.2. Phototransistor

	Manufacturer	Manufacturer's part number
Surface mount		
top-view	Everlight	PT17-21C/L41/TR8
	Fairchild	KDT00030TR
side-view	SunLED	XZRNI56W-1
	Everlight	PT12-21C/TR8
Through-hole		
3mm	SunLED	XRNI30W-1
	LiteOn	LTR-4206

15.3. SPI Flash

Size	Manufacturer	Manufacturer's part number
32 Mbit	Cypress	S25FL132K
64 Mbit	Cypress	S25FL164K
128 Mbit	Winbond	W25Q128JV

Note: Cypress 128Mbit S25FL127/128 parts are not compatible because they do not offer a uniform 4k erase size across the flash area.

15.4. Blinkup circuit

Part	Manufacturer	Manufacturer's part number
Comparator, open-drain	Diodes Inc	AP331AWG-7
Schmitt inverter	Diodes Inc	74LVC1G14W5-7

15.5. Ethernet PHY & magnetics

Part	Manufacturer	Manufacturer's part number
10/100 Ethernet PHY	Microchip	LAN8720A-CP-TR
RJ45 Magjack with LEDs	Stewart Connector	SI-50170-F

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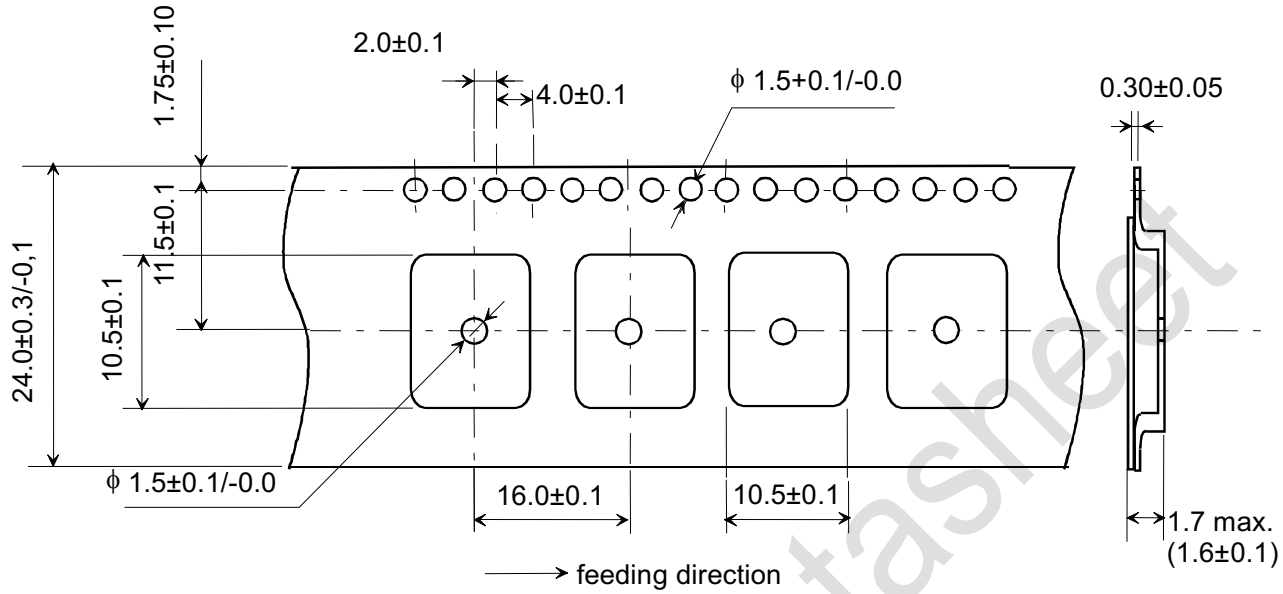
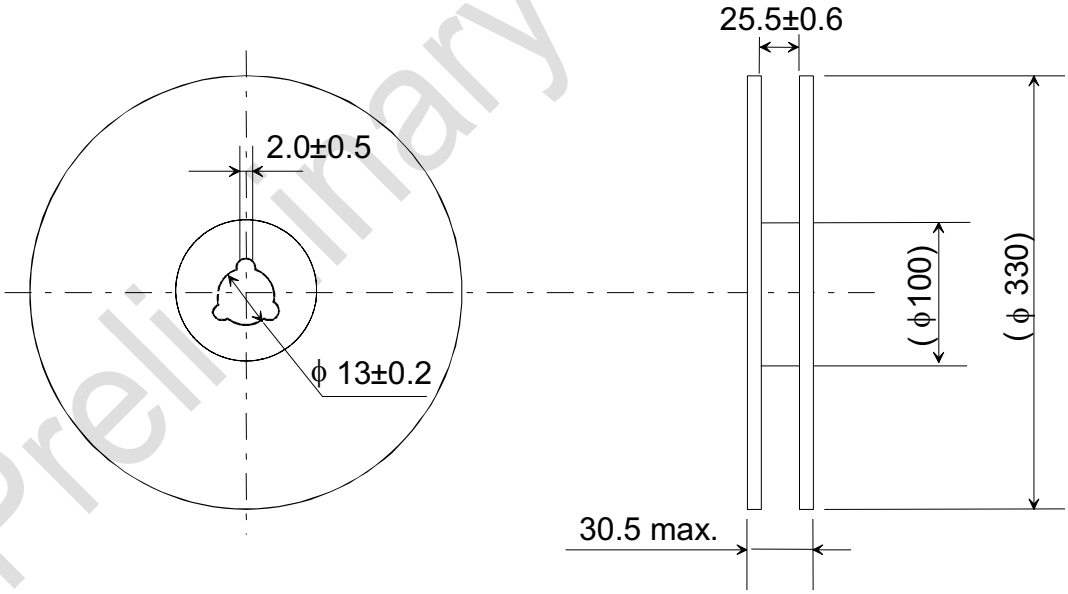
16. Tape and Reel Packing

(1) Dimensions of Tape (Plastic tape)



1) The corner and ridge radiuses (R) of inside cavity are 0.3mm max.
2) Cumulative tolerance of 10 pitches of the sprocket hole is +/-0.2mm
3) Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

(2) Dimensions of Reel



(unit : mm)

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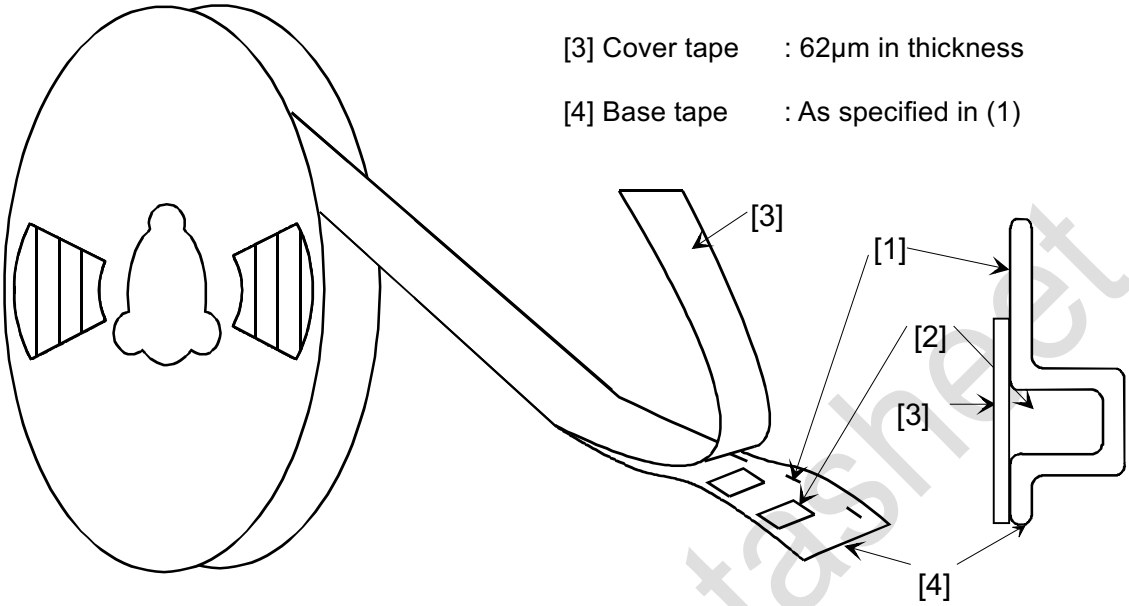
(3) Taping Diagrams

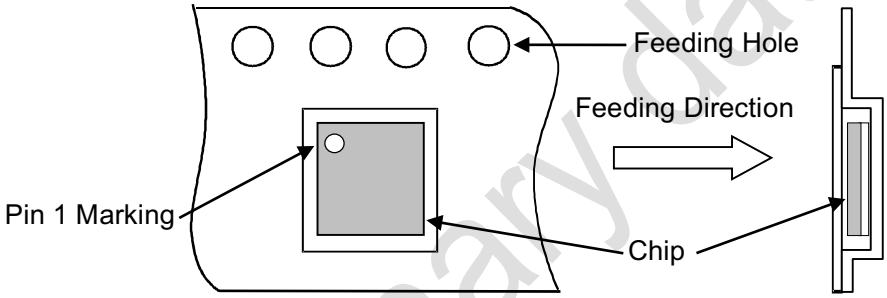
[1] Feeding Hole : As specified in (1)

[2] Hole for chip : As specified in (1)

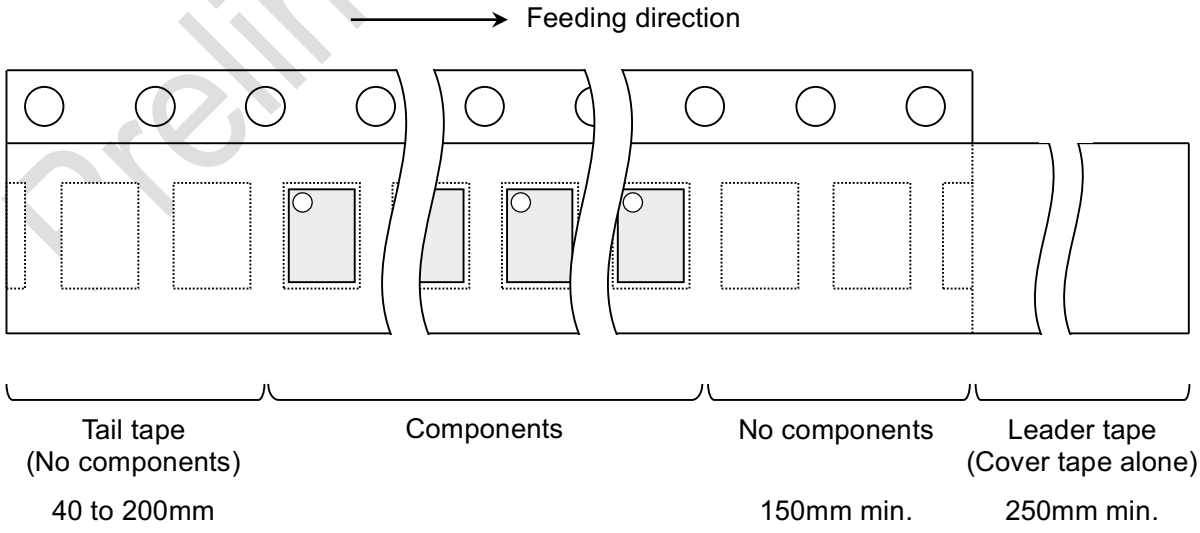
[3] Cover tape : 62μm in thickness

[4] Base tape : As specified in (1)





(4) Leader and Tail tape



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(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

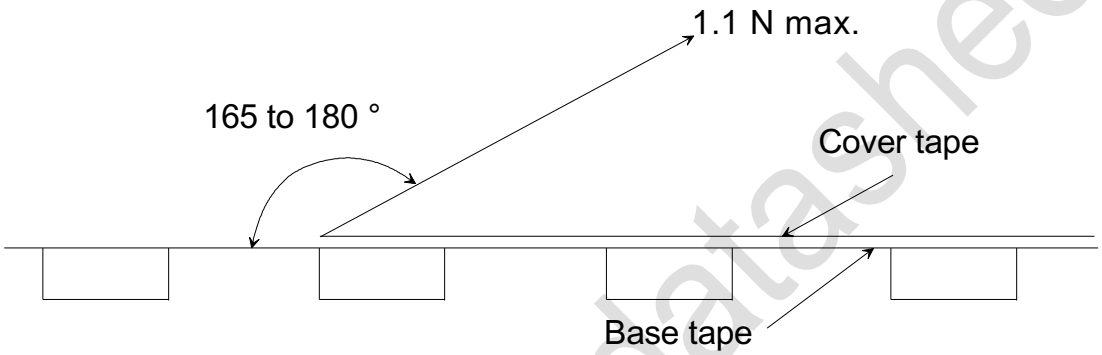
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape : 5N min.

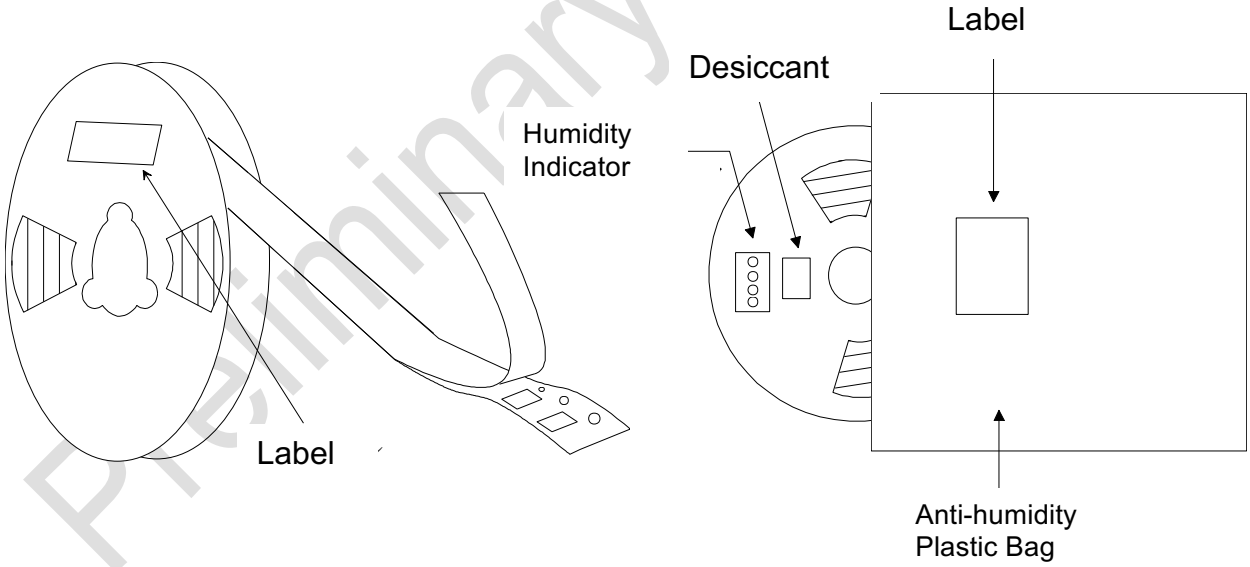
(8) Packaging unit : 1000pcs./ reel

(9) material : Base tape : Plastic
Real : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force : 1.1N max. in the direction of peeling as shown below.



(11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

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