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LC450210PCH

1/8 to 1/16 Duty Dot Matrix LCD Controller Driver

ON Semiconductor®

www.onsemi.com

Overview

The LC450210PCH is the 1/8 to 1/16 duty dot matrix LCD controller driver. By controlling this driver with a microcontroller, it is used in applications such as character display and simple graphic display etc. This driver can drive a LCD panel of up to 3,200 dots (16 × 16 dot font: 1-line display of up to 12 digits and 128 segments, 5 × 7 dot font: 2-line display of up to 40 digits). The operating temperature range is from −40 to +105°C.

Features

1. Selectable duty ratio by serial data: 1/8 duty to 1/16 duty

1/8 duty: 8 × 200 = 1,600 dots	1/11 duty: 11 × 200 = 2,200 dots	1/14 duty: 14 × 200 = 2,800 dots
1/9 duty: 9 × 200 = 1,800 dots	1/12 duty: 12 × 200 = 2,400 dots	1/15 duty: 15 × 200 = 3,000 dots
1/10 duty: 10 × 200 = 2,000 dots	1/13 duty: 13 × 200 = 2,600 dots	1/16 duty: 16 × 200 = 3,200 dots

2. Selectable LCD bias voltage ratio by serial data: 1/4 bias or 1/5 bias
3. Selectable inversion drive of LCD drive waveform by serial data: line inversion or frame inversion
4. Adjustable frame frequency of common and segment output waveforms and clock frequency of voltage booster by serial data, for preventing interference with the frequency of the backlight.
5. Selectable operation modes by serial data: power-saving mode (maintains display data),
   the state of display (ON, all ON, all OFF, all forced OFF)
6. Built-in oscillator circuit (built-in resistor and capacitor for oscillation)
7. Selectable fundamental clock operating modes by serial data: internal oscillator operating mode or external clock operating mode
8. Input of serial data supports CCB* format (for 5 V and 3 V)
9. Selectable voltage range of power supply for logic block by setting REGE pad
   (V_{DD}): +4.5 V to +5.5 V (5 V power supply (REGE = VDD))
   +2.7 V to +3.6 V (3 V power supply (REGE = VSS))
10. Built-in quadruple and quintuple voltage booster with discharge function
    Base voltage of boosting ($V_{BTI}2$): +3.2 V (Typ.) (5 V power supply (REGE = VDD))
    ($V_{BTI}1$=$V_{BTI}2$): +2.7 V to V_{DD}[V] (3 V power supply (REGE = VSS))
11. Power supply for LCD driver block (V_{LCD}): +16.0 V (Typ.) (V_{DD} = 5 V, Quintuple voltage booster is used.)
    +16.5 V (V_{DD} = 3.3 V, Quintuple voltage booster is used.)
    +4.5 V to +16.5 V (range with external power supply)
12. Built-in contrast adjuster
    LCD drive bias voltage ($V_{LCD}0$): +4.65 V to +13.5 V (Typ.) (V_{DD} = 5 V, Quintuple voltage booster is used.)
    +4.65 V to +14.1 V (V_{DD} = 3.3 V, Quintuple voltage booster is used.)
    +4.65 V to +14.1 V (V_{LCD} = 16.5 V with external power supply)
13. The initialization of this driver and the prevention of an unintended display are controllable by setting $\overline{RES}$ pad.
14. Wide range of operating temperature: −40 to +105°C
15. CMOS process and chip with Au bumps

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 53 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD} max	VDD, REGE = VDD	–0.3 to +6.0	V
		VDD, REGE = VSS	–0.3 to +4.2	
	V_{LCD} max	VLCD (Note.1)	–0.3 to +17.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{RES}$, TSIN1 to TSIN4, OSCI	–0.3 to +4.2	V
		CE, CL, DI, $\overline{RES}$, TSIN1 to TSIN4, OSCI, Supply more than 2.7 V to V_{DD} before $V_{IN}1$ is input.	–0.3 to +6.0	
	$V_{IN}2$	VBTI1	–0.3 to V_{DD}+0.3	
	$V_{IN}3$	REGE	–0.3 to +6.0	
	$V_{IN}4$	VLCD5 (Note.1)	–0.3 to V_{LCD}+0.3	
Output voltage	$V_{OUT}1$	VLCD	–0.3 to V_{LCD}+0.3	V
	$V_{OUT}2$	S1 to S200, COM1 to COM16	–0.3 to V_{LCD}+0.3	
	$V_{OUT}3$	CP12N, CP34N, VLOGIC, TSOUT1 to TSOUT3, TSO, V_{DD} ≤ 3.9V (REGE=VSS)	–0.3 to V_{DD}+0.3	
		CP12N, CP34N, VLOGIC, TSOUT1 to TSOUT3, TSO, V_{DD} > 3.9V (REGE=VDD)	–0.3 to +4.2	
Input / Output voltage	$V_{INOUT}1$	CP1P, CP2P, CP3P, CP4P	–0.3 to V_{LCD}+0.3	V
	$V_{INOUT}2$	VLCD0, VLCD1, VLCD2, VLCD3, VLCD4 (Note.1)	–0.3 to V_{LCD}+0.3	
	$V_{INOUT}3$	VBTI2, $V_{BTI}1$ ≤ 3.9 V (REGE = VSS)	–0.3 to $V_{BTI}1$+0.3	
		VBTI2, $V_{BTI}1$ > 3.9 V (REGE = VDD)	-0.3 to +4.2	
Output current	$I_{OUT}1$	VLCD	8	mA
	$I_{OUT}2$	S1 to S200	0.3	
	$I_{OUT}3$	COM1 to COM16	1	
Operating temperature	Topr		–40 to +105	°C
Storage temperature	Tstg		–55 to +125	°C

(Note.1) Follow a condition of $V_{LCD} \geq V_{LCD}0 > V_{LCD}1 > V_{LCD}2 > V_{LCD}3 > V_{LCD}4 > V_{LCD}5$.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = –40 to +105°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
Supply voltage	V_{DD}	VDD, REGE = VDD	4.5		5.5	V
		VDD, REGE = VSS	2.7		3.6	
	V_{LCD}	VLCD, When VLCD is supplied from the outside.	4.5		16.5	
Input base voltage for voltage booster	$V_{BTI}1$	VBTI1, V_{DD} = 4.5 V to 5.5 V (REGE = VDD), Quadruple/Quintuple voltage booster is used.	4.5		V_{DD}	V
	$V_{BTI}2$	VBTI1, VBTI2 (VBTI1 = VBTI2), V_{DD} = 2.7 V to 3.6 V (REGE = VSS), Quadruple voltage booster is used.	2.7		V_{DD} (≤ 3.6)	V
		VBTI1, VBTI2 (VBTI1 = VBTI2), V_{DD} = 2.7 V to 3.3 V (REGE = VSS), Quintuple voltage booster is used.	2.7		V_{DD} (≤ 3.3)	
Input voltage for LCD drive bias voltage generator	$V_{LCD}0$	VLCD0, Contrast adjuster is not used.	4.5 (Note. 1)	(Note. 1)	V_{LCD} (Note. 1)	V
	$V_{LCD}1$ $V_{LCD}2$ $V_{LCD}3$ $V_{LCD}4$	VLCD1, VLCD2, VLCD3, VLCD4, LCD drive bias voltage generator is not used.		(Note.1)		V
	$V_{LCD}5$	VLCD5		0 (Note.1)		V
Input High-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{RES}$, OSCI V_{DD} = 4.5 V to 5.5 V (REGE = VDD)	$0.5V_{DD}$		5.5	V
		CE, CL, DI, $\overline{RES}$, OSCI V_{DD} = 2.7 V to 3.6 V (REGE = VSS)	$0.8V_{DD}$		3.6	
	$V_{IH}2$	REGE	$0.8V_{DD}$		5.5	
Input Low-level voltage	$V_{IL}1$	CE, CL, DI, $\overline{RES}$, TSIN1 to TSIN4, OSCI V_{DD} = 4.5 V to 5.5 V (REGE = VDD)	0		$0.2V_{DD}$	V
		CE, CL, DI, $\overline{RES}$, TSIN1 to TSIN4, OSCI V_{DD} = 2.7 V to 3.6 V (REGE = VSS)	0		$0.2V_{DD}$	
	$V_{IL}2$	REGE	0		$0.2V_{DD}$	
External clock input frequency	f_{CK}	OSCI, External clock operating mode [Fig.1]	100	300	600	kHz
External clock duty	D_{CK}	OSCI, External clock operating mode [Fig.1]	30	50	70	%
Data setup time	tds	CL, DI [Fig.2], [Fig.3]	160			ns
Data hold time	tdh	CL, DI [Fig.2], [Fig.3]	160			ns
CE wait time	tcp	CE, CL [Fig.2], [Fig.3]	160			ns
CE setup time	tcs	CE, CL [Fig.2], [Fig.3]	160			ns
CE hold time	tch	CE, CL [Fig.2], [Fig.3]	160			ns
High-level clock pulse width	tϕH	CL [Fig.2], [Fig.3]	160			ns
Low-level clock pulse width	tϕL	CL [Fig.2], [Fig.3]	160			ns
Rise time	tr	CE, CL, DI [Fig.2], [Fig.3]		160		ns
Fall time	tf	CE, CL, DI [Fig.2], [Fig.3]		160		ns
Reset pulse minimum width	twres	$\overline{RES}$ [Fig.5] to [Fig.8]	1.0			ms

(Note.1) Follow a condition of $V_{LCD} \geq V_{LCD}0 > V_{LCD}1 > V_{LCD}2 > V_{LCD}3 > V_{LCD}4 > V_{LCD}5$.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	PAD	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Hysteresis	V_H	CE, CL, DI, $\overline{RES}$, OSCI	V_{DD} = 4.5 V to 5.5 V (REGE = VDD)		$0.03V_{DD}$		V
			V_{DD} = 2.7 V to 3.6 V (REGE = VSS)		$0.05V_{DD}$		
Input High-level current	$I_{IH}1$	CE, CL, DI, $\overline{RES}$, OSCI	V_I = 3.6 V			5.0	μA
			V_I = 5.5 V, Supply more than 2.7 V to V_{DD} before V_I is input.			5.0	
	$I_{IH}2$	REGE	V_I = 5.5 V			5.0	
Input Low-level current	$I_{IL}1$	CE, CL, DI, $\overline{RES}$, TSIN1 to TSIN4, REGE, OSCI	V_I = 0 V	–5.0			μA
Input current for voltage booster	$I_{BTI}1$	VBTI1	V_{DD} = 5.5 V, $V_{BTI}1$ = 5.5 V, REGE = VDD, Quadruple voltage booster is used. Contrast adjuster is used. LCD drive bias voltage generator is used. Common and segment outputs are open. display on (normal display)		2,050	4,100	μA
			V_{DD} = 5.5 V, $V_{BTI}1$ = 5.5 V, REGE = VDD, Quintuple voltage booster is used. Contrast adjuster is used. LCD drive bias voltage generator is used. Common and segment outputs are open. display on (normal display)		2,550	5,100	
	$I_{BTI}2$	VBTI2	V_{DD} = 3.6 V, $V_{BTI}1$ = $V_{BTI}2$ = 3.6 V, REGE = VSS, Quadruple voltage booster is used. Contrast adjuster is used. LCD drive bias voltage generator is used. Common and segment outputs are open. display on (normal display)		2,000	4,000	
			V_{DD} = 3.3 V, $V_{BTI}1$ = $V_{BTI}2$ = 3.3 V, REGE = VSS, Quintuple voltage booster is used. Contrast adjuster is used. LCD drive bias voltage generator is used. Common and segment outputs are open. display on (normal display)		2,500	5,000	
ON-resistance of segment driver output	R_{ONS}	S1 to S200	V_{LCD} = 4.5 V (with external supply), $V_{LCD}0$ = 4.5 V (with external input), $V_{LCD}1$ to $V_{LCD}5$ = 1/5 bias (with external input)			20	kΩ
ON-resistance of common driver output	R_{ONC}	COM1 to COM16	V_{LCD} = 4.5 V (with external supply), $V_{LCD}0$ = 4.5 V (with external input), $V_{LCD}1$ to $V_{LCD}5$ = 1/5 bias (with external input)			20	kΩ
Output voltage	$V_{BTI}2$	VBTI2	$V_{BTI}1$ = 4.5 V to 5.5 V (REGE = VDD) Voltage booster is used. Contrast adjuster is not used. LCD drive bias voltage generator is not used. No-load.	3.09	3.2	3.3	V
	V_{LCD}	VLCD	Quadruple voltage booster is used. Contrast adjuster is not used. LCD drive bias voltage generator is not used. No-load.	$(V_{BTI}2\times4)$ –0.4	$V_{BTI}2\times4$	$(V_{BTI}2\times4)$ +0.4	
			Quintuple voltage booster is used. Contrast adjuster is not used. LCD drive bias voltage generator is not used. No-load.	$(V_{BTI}2\times5)$ –0.4	$V_{BTI}2\times5$	16.5	
Oscillator frequency	fosc	Internal clock generator	Internal oscillator operating mode	210	300	390	kHz

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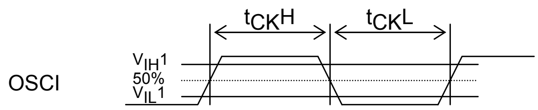
Parameter	Symbol	PAD	Conditions	Ratings			Unit
				Min.	Typ.	Max.	
Power current	$I_{DD}1$	V_{DD}	<Power-saving mode> V_{DD} = 3.6 V (REGE = VSS), communication inactive, Input level is V_{SS} or V_{DD}.			15	μA
			< Power-saving mode > V_{DD} = 5.5 V (REGE = VDD), communication inactive, Input level is V_{SS} or V_{DD}.		50	120	
	$I_{DD}2$	V_{DD}	<Normal mode> V_{DD} = 3.6 V (REGE = VSS), display on (normal display), internal oscillator operating mode, communication inactive, Input level is V_{SS} or V_{DD}.		100	500	
			< Normal mode > V_{DD} = 5.5 V (REGE = VDD), display on (normal display), internal oscillator operating mode, communication inactive, Input level is V_{SS} or V_{DD}.		150	600	
	I_{LCD}	V_{LCD}	< Normal mode > V_{LCD} = 16.5 V (with external supply), display on (normal display), Voltage booster is not used. Contrast adjuster is used. LCD drive bias voltage generator is used. Common and segment outputs are open.		500	1,000	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(1) Clock timing of OSCI pad in the external clock operating mode

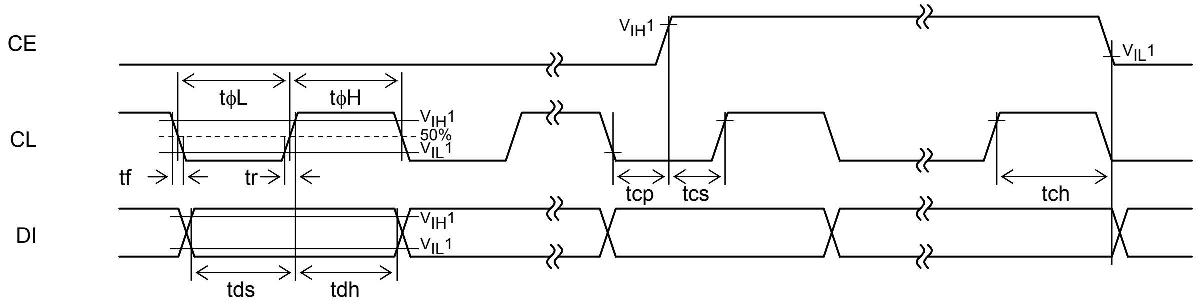


$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \quad \text{[kHz]}$$

$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

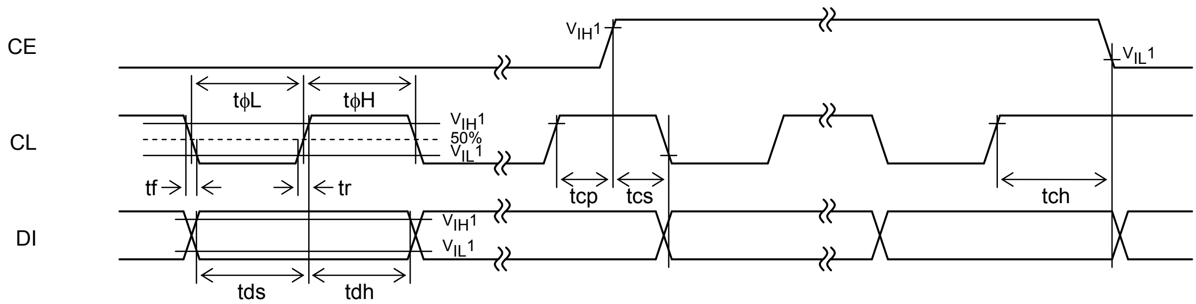
[Fig.1]

(2) When CL is stopped at the low level



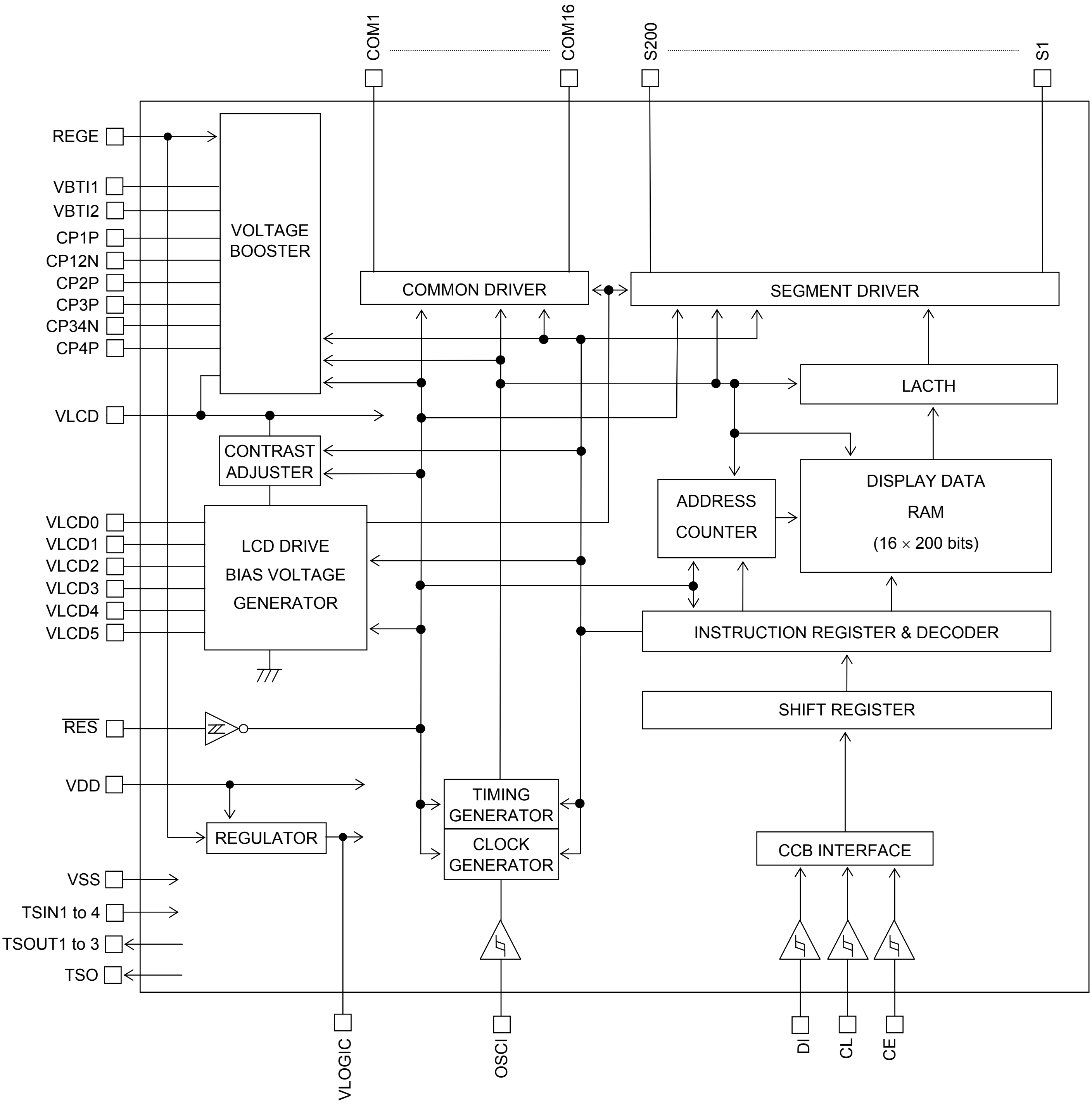
[Fig.2]

(3) When CL is stopped at the high level



[Fig.3]

Block Diagram



Pad Functions

Pad Name	Pad No.	Function	Active	I/O	Handling when unused
VDD	231 to 234	This is a power supply for logic block. REGE = VDD: Supply a voltage from 4.5 V to 5.5 V to VDD. REGE = VSS: Supply a voltage from 2.7 V to 3.6 V to VDD. In addition, make sure to connect a capacitor between VDD and VSS.	-	-	-
VSS	226 to 229, 235 to 243	Make sure to connect VSS to ground.	-	-	-
VLOGIC	216	This is a monitor of a regulator output for logic power supply. Do not use VLOGIC with an external circuit.	-	O	OPEN
REGE	230	This is an input for controlling the regulator of logic power supply and the regulator of voltage booster. Depending on specification of power supply, make sure to connect REGE to VDD or VSS. REGE = VDD: 5 V Power supply is used. The regulator of logic power supply runs. The regulator of voltage booster runs. REGE = VSS: 3 V Power supply is used. The regulator of logic power supply stops. The regulator of voltage booster stops.	-	I	-
S1 to 200	2 to 201	These are segment driver outputs.	-	O	OPEN
COM1 to 8, COM9 to16	313 to 320, 210 to 203	These are common driver outputs.	-	O	OPEN
VBTI1	244 to 248	This is an input for a base voltage for voltage booster. < When voltage booster is used > Make sure to connect a capacitor between VBTI1 and VSS. REGE = VDD: Input the voltage from 4.5 V to V_{DD}[V] to VBTI1. REGE = VSS: Connect VBTI1 to VBTI2, and Input the voltage from 2.7 V to V_{DD}[V] to VBTI1. (When quadruple booster is used : $V_{BTI}1 \leq 3.6$ V, When quintuple booster is used : $V_{BTI}1 \leq 3.3$ V) < When voltage booster is not used > Make sure to open VBTI1.	-	I	OPEN
VBTI2	249 to 253	This is an input-output for a base voltage for voltage booster. < When voltage booster is used > Make sure to connect a capacitor between VBTI2 and VSS. REGE = VDD: VBTI2 outputs a base voltage for voltage booster. REGE = VSS: Connect VBTI1 to VBTI2, and Input the voltage from 2.7 V to V_{DD}[V] to VBTI1. (When quadruple booster is used : $V_{BTI}1 \leq 3.6$ V, When quintuple booster is used : $V_{BTI}1 \leq 3.3$ V) < When voltage booster is not used > Make sure to open VBTI2.	-	I/O	OPEN
CP1P, CP12N, CP2P, CP3P, CP34N, CP4P	254 to 257, 258 to 264, 265 to 268, 269 to 272, 273 to 279, 280 to 283	These are Input-outputs for voltage booster. < When quadruple voltage booster is used > Make sure to connect a capacitor between CP1P(+) and CP12N(-). Make sure to connect a capacitor between CP2P(+) and CP12N(-). Make sure to connect a capacitor between CP3P(+) and CP34N(-). Make sure to connect CP4P and VLCD. < When quintuple voltage booster is used > Make sure to connect a capacitor between CP1P(+) and CP12N(-). Make sure to connect a capacitor between CP2P(+) and CP12N(-). Make sure to connect a capacitor between CP3P(+) and CP34N(-). Make sure to connect a capacitor between CP4P(+) and CP34N(-). < When voltage booster is not used > Make sure to open CP1P, CP12N, CP2P, CP3P, CP34N and CP4P.	-	I/O	OPEN

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Pad Name	Pad No.	Function	Active	I/O	Handling when unused
VLCD	284 to 289	This is a power supply for LCD driver block. Make sure to connect a capacitor between VLCD and VSS. < When voltage booster is used > (i) When quadruple booster is used: VLCD outputs the booster voltage ($V_{BTI}2 \times 4$). (ii) When quintuple booster is used: VLCD outputs the booster voltage ($V_{BTI}2 \times 5$). < When voltage booster is not used > Supply a voltage from 4.5 V to 16.5 V to VLCD. When contrast adjuster is used, follow a condition of $V_{LCD} \geq V_{LCD}0 + 2.4$ V.	-	I/O	-
VLCD0	290 to 294	This is an input-output for the LCD drive bias voltage (High level). Make sure to connect a capacitor between VLCD0 and VLCD5. < When contrast adjuster is used > VLCD0 outputs the LCD drive bias voltage (High level) set by “Set of display contrast” instruction (CT0 to CT5). Follow a condition of $V_{LCD}0 \leq V_{LCD} - 2.4$ V. < When contrast adjuster is not used > Input the LCD drive bias voltage (High level) to $V_{LCD}0$ from the outside, and follow a condition of $V_{LCD}1 < V_{LCD}0 \leq V_{LCD}$.	-	I/O	OPEN
VLCD1	306 to 308	This is an input-output for the LCD drive bias voltage (3/4 level, 4/5 level). Make sure to connect a capacitor between VLCD1 and VLCD5. < When LCD drive bias voltage generator is used > (i) When 1/4 bias is used: VLCD1 outputs the LCD drive bias voltage ($3/4 \times V_{LCD}0$). (ii) When 1/5 bias is used: VLCD1 outputs the LCD drive bias voltage ($4/5 \times V_{LCD}0$). < When LCD drive bias voltage generator is not used > (i) When 1/4 bias is used: Input the LCD drive bias voltage ($3/4 \times V_{LCD}0$) to VLCD1 from the outside, and follow a condition of $V_{LCD}2 < V_{LCD}1 < V_{LCD}0$. (ii) When 1/5 bias is used: Input the LCD drive bias voltage ($4/5 \times V_{LCD}0$) to VLCD1 from the outside, and follow a condition of $V_{LCD}2 < V_{LCD}1 < V_{LCD}0$.	-	I/O	OPEN
VLCD2	300 to 302	This is an input-output for the LCD drive bias voltage (2/4 level, 3/5 level). Make sure to connect a capacitor between VLCD2 and VLCD5. < When LCD drive bias voltage generator is used > (i) When 1/4 bias is used: VLCD2 outputs the LCD drive bias voltage ($2/4 \times V_{LCD}0$). (ii) When 1/5 bias is used: VLCD2 outputs the LCD drive bias voltage ($3/5 \times V_{LCD}0$). < When LCD drive bias voltage generator is not used > (i) When 1/4 bias is used: Input the LCD drive bias voltage ($2/4 \times V_{LCD}0$) to VLCD2 from the outside, and follow a condition of $V_{LCD}4 < V_{LCD}2 < V_{LCD}1$. (ii) When 1/5 bias is used: Input the LCD drive bias voltage ($3/5 \times V_{LCD}0$) to VLCD2 from the outside, and follow a condition of $V_{LCD}3 < V_{LCD}2 < V_{LCD}1$.	-	I/O	OPEN
VLCD3	303 to 305	This is an input-output for the LCD drive bias voltage (2/5 level). < When LCD drive bias voltage generator is used > (i) When 1/4 bias is used: Make sure to open VLCD3. (ii) When 1/5 bias is used: VLCD3 outputs the LCD drive bias voltage ($2/5 \times V_{LCD}0$). Make sure to connect a capacitor between VLCD3 and VLCD5. < When LCD drive bias voltage generator is not used > (i) When 1/4 bias is used: Make sure to open VLCD3. (ii) When 1/5 bias is used: Make sure to connect a capacitor between VLCD3 and VLCD5. Input the LCD drive bias voltage ($2/5 \times V_{LCD}0$) to VLCD3 from the outside, and follow a condition of $V_{LCD}4 < V_{LCD}3 < V_{LCD}2$.	-	I/O	OPEN

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Pad Name	Pad No.	Function	Active	I/O	Handling when unused
VLCD4	309 to 311	This is an input-output for the LCD drive bias voltage (1/4 level, 1/5 level). Make sure to connect a capacitor between VLCD4 and VLCD5. < When LCD drive bias voltage generator is used > (i) When 1/4 bias is used: VLCD4 outputs the LCD drive bias voltage (1/4 × $V_{LCD}0$). (ii) When 1/5 bias is used: VLCD4 outputs the LCD drive bias voltage (1/5 × $V_{LCD}0$). < When LCD drive bias voltage generator is not used > (i) When 1/4 bias is used: Input the LCD drive bias voltage (1/4 × $V_{LCD}0$) to VLCD4 from the outside, and follow a condition of $V_{LCD}5 < V_{LCD}4 < V_{LCD}2$. (ii) When 1/5 bias is used: Input the LCD drive bias voltage (1/5 × $V_{LCD}0$) to VLCD4 from the outside, and follow a condition of $V_{LCD}5 < V_{LCD}4 < V_{LCD}3$.	-	I/O	OPEN
VLCD5	295 to 299	This is an input-output for the LCD drive bias voltage (Low level). Make sure to connect VLCD5 to VSS even if the LCD drive bias generator is not used.	-	I	VSS
OSCI	221	This is an input for the external clock, when external clock operating mode is selected. By “Set of display method” instruction, OC = 0 (internal oscillator operating mode): Make sure to connect OSCI to VSS. OC = 1 (external clock operating mode): OSCI is used to input the external clock.	-	I	VSS
CE	218	These are Inputs for transferring serial data. These pads are connected to a controller. CE: Chip enables. CL: Synchronous clock. DI: Transfer data.	H	I	VSS
CL	220		↑	I	
DI	219		-	I	
$\overline{\text{RES}}$	217	This is an input for reset of this LSI. $\overline{\text{RES}}$ = VSS: The state of this LSI is reset. Refer to about the “System Reset”. $\overline{\text{RES}}$ = VDD: Normal state.	L	I	VSS
TSIN1 to TSIN4	222 to 225	These are inputs for a test. Make sure to connect these pads to VSS.	-	I	VSS
TSOUT1 to TSOUT3	212 to 214	These are outputs for a test. Make sure to open these pads.	-	O	OPEN
TSO	215	These are output for a test. Make sure to open this pad.	-	O	OPEN
DUMMY	1, 202, 211, 312	These are dummy pads. These pads are not available. Don’t connect between dummy pads. Moreover, don’t use them with an external circuit.	-	-	OPEN

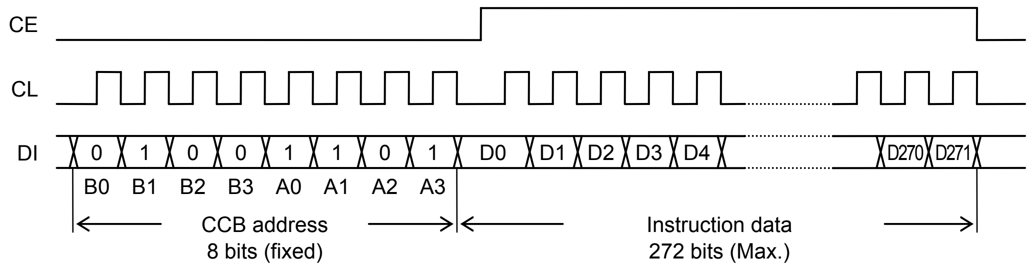
Correspondence of RAM and Segment Output Pad

		Segment output pad																				
Set of column address direction	Normal direction (SDIR = “0”)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	……	S193	S194	S195	S196	S197	S198	S199	S200		
	Reversed direction (SDIR = “1”)	S200	S199	S198	S197	S196	S195	S194	S193	S192	S191	……	S8	S7	S6	S5	S4	S3	S2	S1		
Page address PGA	0	D1_1	D2_1	D3_1	D4_1	D5_1	D6_1	D7_1	D8_1	D9_1	D10_1	……	D193_1	D194_1	D195_1	D196_1	D197_1	D198_1	D199_1	D200_1	0H	Line address LNA0 to LNA3
		D1_2	D2_2	D3_2	D4_2	D5_2	D6_2	D7_2	D8_2	D9_2	D10_2	……	D193_2	D194_2	D195_2	D196_2	D197_2	D198_2	D199_2	D200_2	1H	
		D1_3	D2_3	D3_3	D4_3	D5_3	D6_3	D7_3	D8_3	D9_3	D10_3	……	D193_3	D194_3	D195_3	D196_3	D197_3	D198_3	D199_3	D200_3	2H	
		D1_4	D2_4	D3_4	D4_4	D5_4	D6_4	D7_4	D8_4	D9_4	D10_4	……	D193_4	D194_4	D195_4	D196_4	D197_4	D198_4	D199_4	D200_4	3H	
		D1_5	D2_5	D3_5	D4_5	D5_5	D6_5	D7_5	D8_5	D9_5	D10_5	……	D193_5	D194_5	D195_5	D196_5	D197_5	D198_5	D199_5	D200_5	4H	
		D1_6	D2_6	D3_6	D4_6	D5_6	D6_6	D7_6	D8_6	D9_6	D10_6	……	D193_6	D194_6	D195_6	D196_6	D197_6	D198_6	D199_6	D200_6	5H	
		D1_7	D2_7	D3_7	D4_7	D5_7	D6_7	D7_7	D8_7	D9_7	D10_7	……	D193_7	D194_7	D195_7	D196_7	D197_7	D198_7	D199_7	D200_7	6H	
		D1_8	D2_8	D3_8	D4_8	D5_8	D6_8	D7_8	D8_8	D9_8	D10_8	……	D193_8	D194_8	D195_8	D196_8	D197_8	D198_8	D199_8	D200_8	7H	
	1	D1_9	D2_9	D3_9	D4_9	D5_9	D6_9	D7_9	D8_9	D9_9	D10_9	……	D193_9	D194_9	D195_9	D196_9	D197_9	D198_9	D199_9	D200_9	8H	
		D1_10	D2_10	D3_10	D4_10	D5_10	D6_10	D7_10	D8_10	D9_10	D10_10	……	D193_10	D194_10	D195_10	D196_10	D197_10	D198_10	D199_10	D200_10	9H	
		D1_11	D2_11	D3_11	D4_11	D5_11	D6_11	D7_11	D8_11	D9_11	D10_11	……	D193_11	D194_11	D195_11	D196_11	D197_11	D198_11	D199_11	D200_11	AH	
		D1_12	D2_12	D3_12	D4_12	D5_12	D6_12	D7_12	D8_12	D9_12	D10_12	……	D193_12	D194_12	D195_12	D196_12	D197_12	D198_12	D199_12	D200_12	BH	
		D1_13	D2_13	D3_13	D4_13	D5_13	D6_13	D7_13	D8_13	D9_13	D10_13	……	D193_13	D194_13	D195_13	D196_13	D197_13	D198_13	D199_13	D200_13	CH	
		D1_14	D2_14	D3_14	D4_14	D5_14	D6_14	D7_14	D8_14	D9_14	D10_14	……	D193_14	D194_14	D195_14	D196_14	D197_14	D198_14	D199_14	D200_14	DH	
		D1_15	D2_15	D3_15	D4_15	D5_15	D6_15	D7_15	D8_15	D9_15	D10_15	……	D193_15	D194_15	D195_15	D196_15	D197_15	D198_15	D199_15	D200_15	EH	
		D1_16	D2_16	D3_16	D4_16	D5_16	D6_16	D7_16	D8_16	D9_16	D10_16	……	D193_16	D194_16	D195_16	D196_16	D197_16	D198_16	D199_16	D200_16	FH	
		00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	……	C0H	C1H	C2H	C3H	C4H	C5H	C6H	C7H		
		Column address CRA0 to CRA7																				

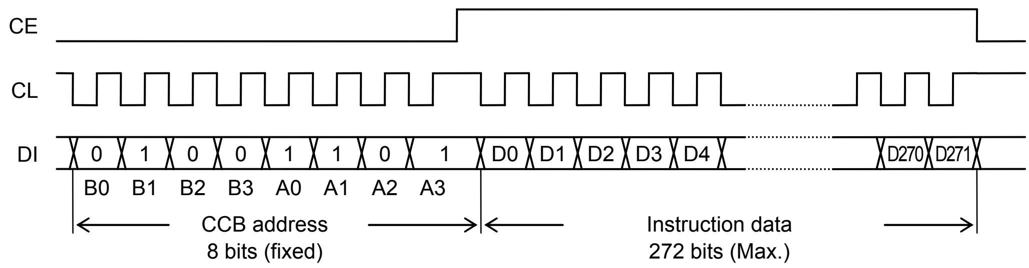
Transfer Format of Serial Data

This LSI has several internal registers. These internal registers are written by CCB interface. Structure of transfer bits consists of CCB address and instruction data. First 8 bits are CCB address. The subsequent bits are instruction data. The bit number of instruction data is different depending on an instruction, and these bits are from 16 bits to 272 bits.
The serial data is taken by the positive edge of the CL signal, which is latched by the negative edge of the CE signal. When the number of data in CE = “High level” period is different from the defined number, LSI does not execute the instruction and holds the old state. For more information about the number of instruction data, refer to “Instruction Table”.

(1) When CL is stopped at the low level



(2) When CL is stopped at the high level



- B0 to B3, A0 to A3 ········· CCB address is “B2H”
- D0 to D271 ········· Instruction data (from 16 bits to 272 bits)

Instruction Table

Instruction	D0	D1	D2	D3	…	D126	D127	D128	D129	D130	D131	…	D236	D237	D238	D239
Set of display method (Note.1)					…							…				
Control of display ON / OFF (Note.2)					…							…				
Set of line address					…							…				
Write display data to RAM (8×15 bits in a lump) (Note.4)					…			Dn_m	Dn_m+1	Dn_m+2	Dn_m+3	…	D n+13_m+4	D n+13_m+5	D n+13_m+6	D n+13_m+7
Write display data to RAM (16×16 bits in a lump) (Note.5)	Dn_m	Dn_m+1	Dn_m+2	Dn_m+3	…	D n+7_m+14	D n+7_m+15	D n+8_m	D n+8_m+1	D n+8_m+2	D n+8_m+3	…	D n+14_m+12	D n+14_m+13	D n+14_m+14	D n+14_m+15
Set of display contrast					…							…				

Instruction	D240	D241	D242	D243	D244	D245	D246	D247	D248	D249	D250	D251	D252	D253	D254	D255	D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271	Total bits (Note.3)
Set of display method (Note.1)	OC	0	1	0	DBC	CTC0	CTC1	0	DT0	DT1	DT2	DT3	DR	WVC	1	0	CDIR	SDIR	1	0	DBF0	DBF1	DBF2	0	FC0	FC1	FC2	FC3	0	0	0	1	32
Control of display ON / OFF (Note.2)																	PNC	0	1	0	SC0	SC1	0	BU	0	0	1	0	0	0	1	0	16
Set of line address																	LNA0	LNA1	LNA2	LNA3	0	0	0	0	0	1	0	0	0	0	1	1	16
Write display data to RAM (8×15 bits in a lump) (Note.4)	D n+14_m	D n+14_m+1	D n+14_m+2	D n+14_m+3	D n+14_m+4	D n+14_m+5	D n+14_m+6	D n+14_m+7	0	0	0	0	0	0	0	0	CRA0	CRA1	CRA2	CRA3	CRA4	CRA5	CRA6	CRA7	PGA	0	0	0	0	1	0	0	144
Write display data to RAM (16×16 bits in a lump) (Note.5)	D n+15_m	D n+15_m+1	D n+15_m+2	D n+15_m+3	D n+15_m+4	D n+15_m+5	D n+15_m+6	D n+15_m+7	D n+15_m+8	D n+15_m+9	D n+15_m+10	D n+15_m+11	D n+15_m+12	D n+15_m+13	D n+15_m+14	D n+15_m+15	CRA0	CRA1	CRA2	CRA3	CRA4	CRA5	CRA6	CRA7	PGA	0	0	0	0	1	0	1	272
Set of display contrast																	CT0	CT1	CT2	CT3	CT4	CT5	0	0	0	0	0	1	0	1	1	0	16

(Note.1) “Set of display method” instruction must be executed first. If voltage booster, contrast adjuster and LCD drive bias voltage generator are used, wait time shown from (1) to (3) is needed for stabilization of each circuit after having reset a system by $\overline{\mathrm{RES}}$=“Low level”.
(Note.2) When power-saving mode is changed to normal mode (BU=“1” to “0”), wait time shown from (1) to (3) is needed for stabilization of each circuit. When normal mode is changed to power-saving mode (BU=“0” to “1”), secure a stop transition time (discharge time) more than 200[msec].

(1) When voltage booster, contrast adjuster and LCD drive bias voltage generator are used (DBC=“1”, CTC0,CTC1=“1,1”), the stabilization time of these circuits is 200[msec].
(2) When contrast adjuster and LCD drive bias voltage generator are used (DBC=“0”, CTC0,CTC1=“1,1”), the stabilization time of these circuits is 20[msec].
(3) When LCD drive bias voltage generator is used (DBC=“0”, CTC0,CTC1=“0,1”), the stabilization time of this circuit is 20[msec].
* Refer from [Fig.5] to [Fig.9].

(Note.3) When the number of instruction data which want to execute is different from the number of transferred instruction data, the transferred instruction data is ignored.
(Note.4) n=1 to 186, n+14=15 to 200, m=1, 9
(Note.5) n=1 to 185, n+15=16 to 200, m=1

Explanation of Instruction Data

1. "Set of display method" instruction

The display method is set by "Set of display method" instruction.
After having reset a system by $\overline{\text{RES}}$ = "Low level", make sure to execute "Set of display method" first.

Instruction data (32 bits)																															
D240	D241	D242	D243	D244	D245	D246	D247	D248	D249	D250	D251	D252	D253	D254	D255	D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271
OC	0	1	0	DBC	CTC0	CTC1	0	DT0	DT1	DT2	DT3	DR	WVC	1	0	CDIR	SDIR	1	0	DBF0	DBF1	DBF2	0	FC0	FC1	FC2	FC3	0	0	0	1
								(LSB)			(MSB)									(LSB)		(MSB)		(LSB)			(MSB)				

(1-1) OC ··· This is control data to set a fundamental clock operating mode.
Internal oscillator operating mode and external clock operating mode are set by this control data.
When the internal oscillator operating mode is set, clock generator begins to run after power-saving mode is canceled (BU = "0").

OC	Fundamental clock operating mode	The state of OSCI
0	Internal oscillator operating mode	Make sure to connect OSCI to VSS.
1	External clock operating mode	Input the clock f_{CK} from 100 to 600 [kHz].

(1-2) DBC ··· This is control data to set a state of voltage booster.
Run or Stop of voltage booster is set by this control data.
About the combination of DBC, CTC0 and CTC1, refer to the following table.

(1-3) CTC0, CTC1 ··· These are control data to set a state of contrast adjuster and LCD drive bias voltage generator.
Run or Stop of contrast adjuster and LCD drive bias voltage generator is set by these control data.
About the combination of DBC, CTC0 and CTC1, refer to the following table.

DBC	CTC0	CTC1	Voltage booster	Contrast adjuster	LCD drive bias voltage generator
0	0	0	Stop	Stop	Stop
0	0	1	Stop	Stop	Run
0	1	0	Stop	Run	Stop
0	1	1	Stop	Run	Run
1	0	0	Run	Stop	Stop
1	0	1	Run	Stop	Run
1	1	0	Run	Run	Stop
1	1	1	Run	Run	Run

About the state of Voltage booster, VBTI1, VBTI2 and VLCD, refer to the following table.

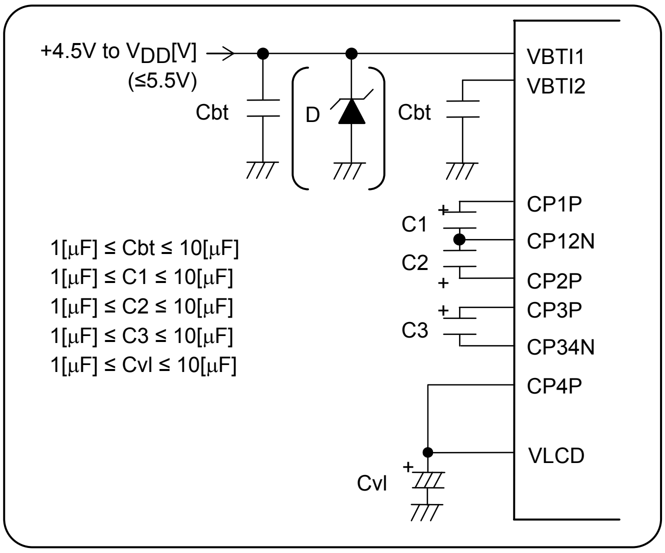
The state of voltage booster	The state of VBTI1	The state of VBTI2	The state of VLCD
Unused	Make sure to open VBTI1.	Make sure to open VBTI2.	Supply a voltage from 4.5 V to 16.5 V to VLCD from the outside.
Quadruple voltage booster is used.	< REGE = VDD > Input the voltage from 4.5 V to V_{DD}[V] to VBTI1. < REGE = VSS > Connect VBTI1 to VBTI2.	< REGE = VDD > VBTI2 outputs a base voltage for voltage booster. < REGE = VSS > Connect VBTI1 to VBTI2, and Input the voltage from 2.7 V to V_{DD}[V] (≤3.6 V) to VBTI1.	VLCD outputs the ($V_{BTI}2 \times 4$) voltage
Quintuple voltage booster is used.	< REGE = VDD > Input the voltage from 4.5 V to V_{DD}[V] to VBTI1. < REGE = VSS > Connect VBTI1 to VBTI2.	< REGE = VDD > VBTI2 outputs a base voltage for voltage booster. < REGE = VSS > Connect VBTI1 to VBTI2, and Input the voltage from 2.7 V to V_{DD}[V] (≤3.3 V) to VBTI1.	VLCD outputs the ($V_{BTI}2 \times 5$) voltage

(Note.1) During (1) or (2) time, voltage booster stops forcibly and is the discharge state. In the discharge state, the electric potential of VLCD is same as VBTI1.

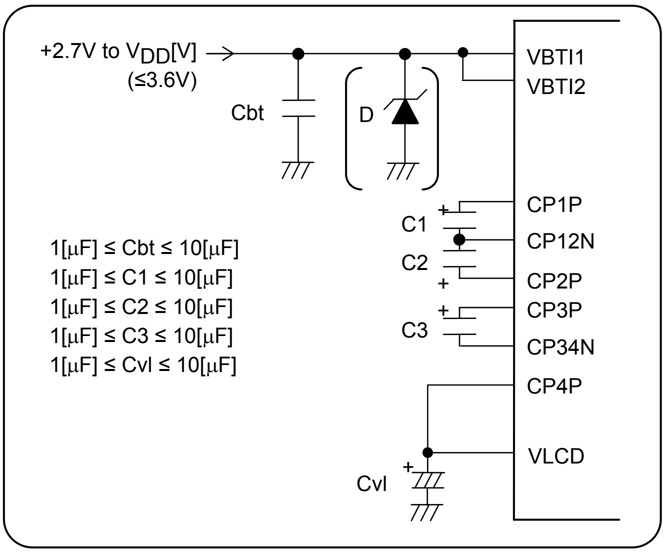
(1) The period of $\overline{\text{RES}}$ = “Low level” (Regardless of the setting of voltage booster)
(2) DBC = “1” is set by “Set of display method” instruction, and power-saving mode (BU = “1”) is set by “Control of display ON / OFF” instruction.

(Note.2) The peripheral circuit of VBTI1, VBTI2, CP1P, CP12N, CP2P, CP3P, CP34N, CP4P and VLCD is as follows.
Only changing the connection of CP4P, a multiple of the voltage booster is selectable.

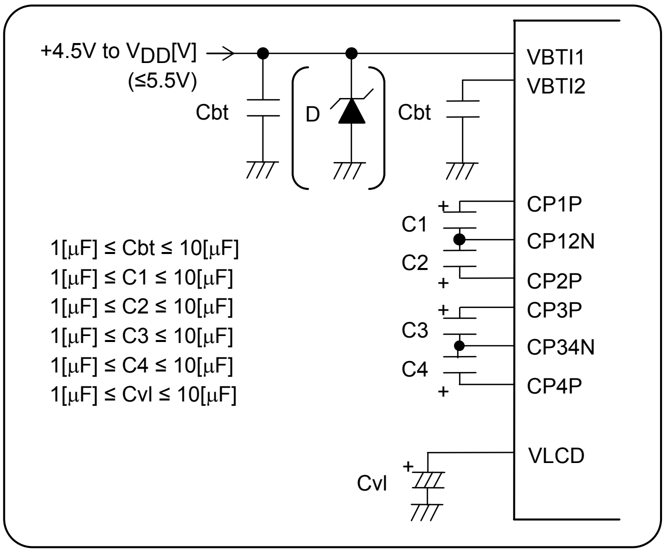
< 5 V Power supply (REGE=VDD),
Quadruple voltage booster is used (DBC="1") >



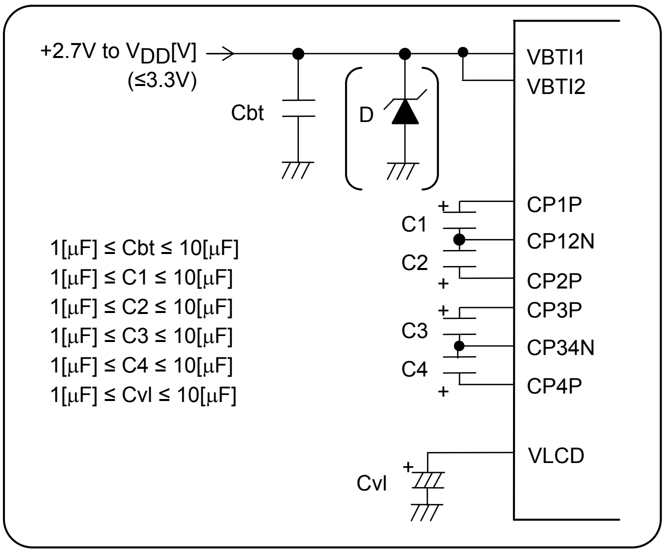
< 3 V Power supply (REGE=VSS),
Quadruple voltage booster is used (DBC="1") >



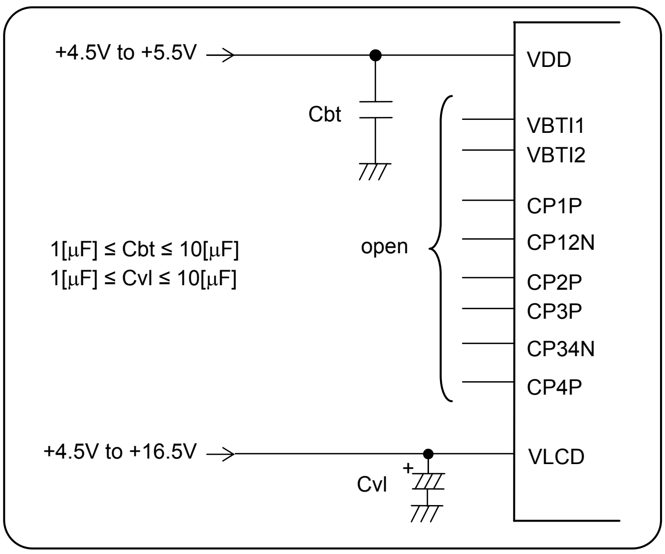
< 5 V Power supply (REGE=VDD),
Quintuple voltage boost is used (DBC="1") >



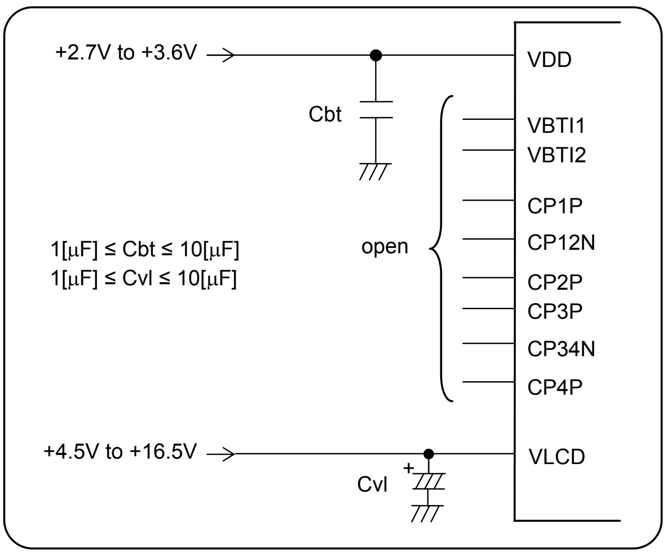
< 3 V Power supply (REGE=VSS),
Quintuple voltage boost is used (DBC="1") >



< 5 V Power supply (REGE=VDD),
Voltage booster is not used (DBC="0") >



< 3 V Power supply (REGE=VSS),
Voltage booster is not used (DBC="0") >



About the state of contrast adjuster, LCD drive bias voltage generator and the state from VLCD1 to VLCD4, refer to the following table.

The state of contrast adjuster	The state of LCD drive bias voltage generator	The state of VLCD0	The state from VLCD1 to VLCD4
Unused	Unused	Input LCD drive bias voltage (High level) to VLCD0 from the outside.	Input LCD drive bias voltage (Middle level) to pads from VLCD1 to VLCD4 from the outside. (When 1/4 bias is used, make sure to open VLCD3.)
Use	Unused	VLCD0 outputs the LCD drive bias voltage (High level) set by “Set of display contrast” instruction (CT0 to CT5). Make sure to connect a capacitor between VLCD0 and VLCD5.	Input LCD drive bias voltage (Middle level) to pads from VLCD1 to VLCD4 from the outside. (When 1/4 bias is used, make sure to open VLCD3.)
Unused	Use	Input LCD drive bias voltage (High level) to VLCD0 from the outside.	Pads from VLCD1 to VLCD4 outputs LCD drive bias voltage (Middle level). Make sure to connect a capacitor between pads from VLCD1 to VLCD4 and VLCD5. (When 1/4 bias is used, make sure to open VLCD3.)
Use	Use	VLCD0 outputs the LCD drive bias voltage (High level) set by “Set of display contrast” instruction (CT0 to CT5). Make sure to connect a capacitor between VLCD0 and VLCD5.	Pads from VLCD1 to VLCD4 outputs LCD drive bias voltage (Middle level). Make sure to connect a capacitor between pads from VLCD1 to VLCD4 and VLCD5. (When 1/4 bias is used, make sure to open VLCD3.)

(Note.1) During (1) or (2) or (3) time, contrast adjuster and LCD drive bias voltage generator stop forcibly, and are the discharge state. In the discharge state, the electric potential of VLCD0, VLCD1, VLCD2, VLCD3 and VLCD4 are same as VLCD5.

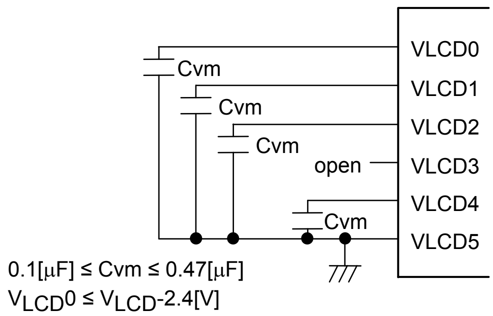
(1) The period of $\overline{\text{RES}}$ = “Low level” (Regardless of the setting of contrast adjuster and LCD drive bias voltage generator)

(2) CTC0 = “1” is set by “Set of display method” instruction, and power-saving mode (BU = “1”) is set by “Control of display ON / OFF” instruction.

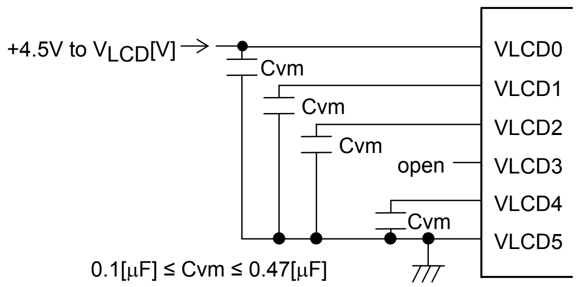
(3) CTC1 = “1” is set by “Set of display method” instruction, and power-saving mode (BU = “1”) is set by “Control of display ON / OFF” instruction.

(Note.2) When 1/4 bias is set (DR = “0”), set a peripheral circuit from VLCD0 to VLCD5 as follows.

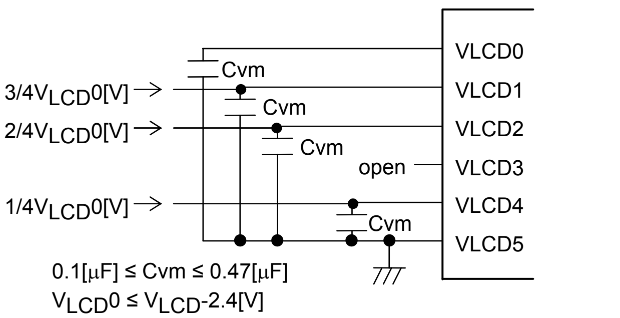
< Contrast adjuster and LCD drive bias voltage generator are used. (CTC0,CTC1=“1,1”) >



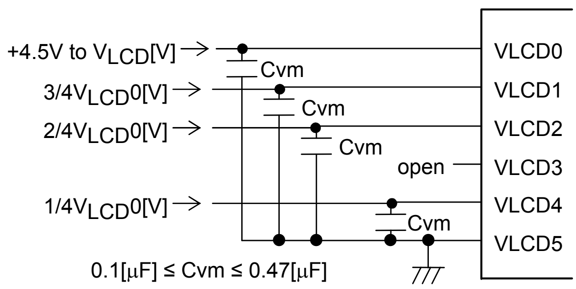
< Contrast adjuster is not used, and LCD drive bias voltage generator is used. (CTC0,CTC1=“0,1”) >



< Contrast adjuster is used, and LCD drive bias voltage generator is not used. (CTC0,CTC1=“1,0”) >

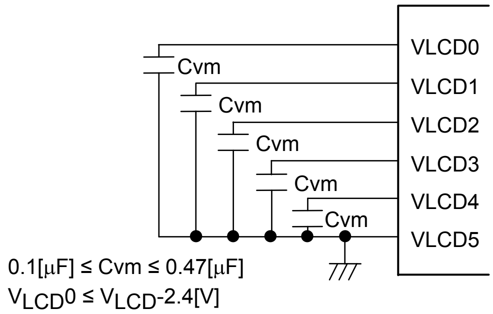


< Contrast adjuster and LCD drive bias voltage generator are not used. (CTC0,CTC1=“0,0”) >

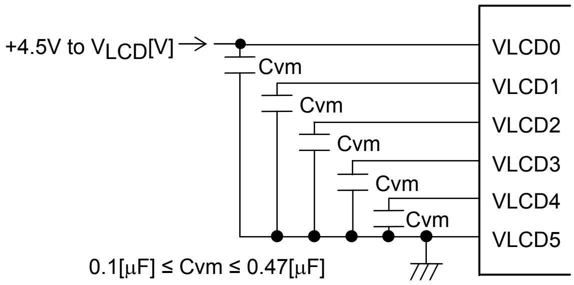


(Note.3) When 1/5 bias is set (DR=“1”), set a peripheral circuit from VLCD0 to VLCD5 as follows.

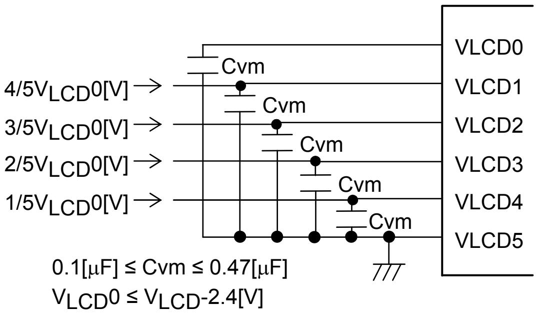
< Contrast adjuster and LCD drive bias voltage generator are used. (CTC0,CTC1=“1,1”) >



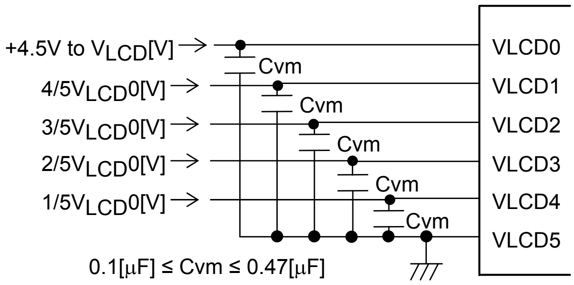
< Contrast adjuster is not used, and LCD drive bias voltage generator is used. (CTC0,CTC1=“0,1”) >



< Contrast adjuster is used, and LCD drive bias voltage generator is not used. (CTC0,CTC1=“1,0”) >



< Contrast adjuster and LCD drive bias voltage generator are not used. (CTC0,CTC1=“0,0”) >



(1-4) DT0 to DT3 ··· These are control data to set duty from 1/8 to 1/16.
Duty from 1/8 to 1/16 is set by these control data.

DT0	DT1	DT2	DT3	Duty	The state from COM1 to COM16			
					Pads which output scan pulse		Pads which output pulse of display off	
					Normal scan CDIR = “0”	Reversed scan CDIR = “1”	Normal scan CDIR = “0”	Reversed scan CDIR = “1”
0	0	0	0	1/8 duty	COM1 to COM8	COM16 to COM9	COM9 to COM16	COM8 to COM1
1	0	0	0	1/9 duty	COM1 to COM9	COM16 to COM8	COM10 to COM16	COM7 to COM1
0	1	0	0	1/10 duty	COM1 to COM10	COM16 to COM7	COM11 to COM16	COM6 to COM1
1	1	0	0	1/11 duty	COM1 to COM11	COM16 to COM6	COM12 to COM16	COM5 to COM1
0	0	1	0	1/12 duty	COM1 to COM12	COM16 to COM5	COM13 to COM16	COM4 to COM1
1	0	1	0	1/13 duty	COM1 to COM13	COM16 to COM4	COM14 to COM16	COM3 to COM1
0	1	1	0	1/14 duty	COM1 to COM14	COM16 to COM3	COM15, COM16	COM2, COM1
1	1	1	0	1/15 duty	COM1 to COM15	COM16 to COM2	COM16	COM1
X	X	X	1	1/16 duty	COM1 to COM16	COM16 to COM1	-	-

X: don’t care

(1-5) DR ··· This is control data to set 1/4 bias or 1/5 bias.
1/4 bias or 1/5 bias is set by this control data.

DR	Bias	VLCD1 voltage	VLCD2 voltage	VLCD3 voltage	VLCD4 voltage
0	1/4 bias	3/4 $V_{LCD}0$	2/4 $V_{LCD}0$	Make sure to open VLCD3	1/4 $V_{LCD}0$
1	1/5 bias	4/5 $V_{LCD}0$	3/5 $V_{LCD}0$	2/5 $V_{LCD}0$	1/5 $V_{LCD}0$

(1-6) WVC ··· This is control data to set inversion drive of LCD drive waveform.
Line inversion or frame inversion is set by this control data.

WVC	LCD drive waveform
0	Line inversion
1	Frame inversion

(1-7) CDIR ··· This is control data to set scan direction of common outputs.
Scan direction of common outputs is set by this control data.

CDIR	Scan direction of common outputs
0	Normal scan (COM1 → COM2 → COM3 → ······ → COM15 → COM16)
1	Reversed scan (COM16 → COM15 → COM14 → ······ → COM2 → COM1)

(1-8) SDIR ··· This is control data to set a correspondence of a segment output and a column address of RAM.
A correspondence of a segment output and a column address of RAM are set by this control data.
Only just changing the setting of SDIR data does not change the display of LCD. When display data is written to RAM, column address of RAM is converted. Then display data is saved to there.

SDIR	Correspondence of a segment output and a column address of RAM
0	Normal direction (Column address “CRA0 to CRA7=00H, 01H, 02H, → C5H, C6H, C7H” of RAM corresponds to segment output “S1, S2, S3, → , S198, S199, S200”.)
1	Reversed direction (Column address “CRA0 to CRA7=00H, 01H, 02H, → C5H, C6H, C7H” of RAM corresponds to segment output “S200, S199, S198, → , S3, S2, S1”.)

(1-9) DBF0 to DBF2 ··· These are control data to set clock frequency of voltage booster.
A clock frequency of voltage booster is set by these control data.

DBF0	DBF1	DBF2	Clock frequency of voltage booster (fcp)
0	0	0	fosc/12 or $f_{CK}/12$
1	0	0	fosc/14 or $f_{CK}/14$
0	1	0	fosc/18 or $f_{CK}/18$
1	1	0	fosc/22 or $f_{CK}/22$
0	0	1	fosc/26 or $f_{CK}/26$
1	0	1	fosc/28 or $f_{CK}/28$
0	1	1	fosc/30 or $f_{CK}/30$
1	1	1	fosc/34 or $f_{CK}/34$

(1-10) FC0 to FC3 ··· These are control data to set frame frequency of common and segment output waveforms.
A frame frequency of common and segment output waveforms are set by these control data.

FC0	FC1	FC2	FC3	Frame frequency fo[Hz]				
				1/8 duty	1/9 duty	1/10 duty	1/11 duty	1/12 duty
0	0	0	0	fosc(f_{CK})/4352 < 68.9[Hz] >	fosc(f_{CK})/4320 < 69.4[Hz] >	fosc(f_{CK})/4320 < 69.4[Hz] >	fosc(f_{CK})/4400 < 68.2[Hz] >	fosc(f_{CK})/4320 < 69.4[Hz] >
1	0	0	0	fosc(f_{CK})/3712 < 80.8[Hz] >	fosc(f_{CK})/3744 < 80.1[Hz] >	fosc(f_{CK})/3760 < 79.8[Hz] >	fosc(f_{CK})/3784 < 79.3[Hz] >	fosc(f_{CK})/3744 < 80.1[Hz] >
0	1	0	0	fosc(f_{CK})/2944 < 101.9[Hz] >	fosc(f_{CK})/2952 < 101.6[Hz] >	fosc(f_{CK})/2960 < 101.4[Hz] >	fosc(f_{CK})/2992 < 100.3[Hz] >	fosc(f_{CK})/2976 < 100.8[Hz] >
1	1	0	0	fosc(f_{CK})/2368 < 126.7[Hz] >	fosc(f_{CK})/2376 < 126.3[Hz] >	fosc(f_{CK})/2400 < 125.0[Hz] >	fosc(f_{CK})/2376 < 126.3[Hz] >	fosc(f_{CK})/2400 < 125.0[Hz] >
0	0	1	0	fosc(f_{CK})/1984 < 151.2[Hz] >	fosc(f_{CK})/1944 < 154.3[Hz] >	fosc(f_{CK})/2000 < 150.0[Hz] >	fosc(f_{CK})/1936 < 155.0[Hz] >	fosc(f_{CK})/1968 < 152.4[Hz] >
1	0	1	0	fosc(f_{CK})/1696 < 176.9[Hz] >	fosc(f_{CK})/1692 < 177.3[Hz] >	fosc(f_{CK})/1720 < 174.4[Hz] >	fosc(f_{CK})/1672 < 179.4[Hz] >	fosc(f_{CK})/1728 < 173.6[Hz] >
0	1	1	0	fosc(f_{CK})/1472 < 203.8[Hz] >	fosc(f_{CK})/1476 < 203.3[Hz] >	fosc(f_{CK})/1480 < 202.7[Hz] >	fosc(f_{CK})/1496 < 200.5[Hz] >	fosc(f_{CK})/1488 < 201.6[Hz] >
1	1	1	0	fosc(f_{CK})/1312 < 228.7[Hz] >	fosc(f_{CK})/1332 < 225.2[Hz] >	fosc(f_{CK})/1320 < 227.3[Hz] >	fosc(f_{CK})/1320 < 227.3[Hz] >	fosc(f_{CK})/1320 < 227.3[Hz] >
0	0	0	1	fosc(f_{CK})/1184 < 253.4[Hz] >	fosc(f_{CK})/1188 < 252.5[Hz] >	fosc(f_{CK})/1200 < 250.0[Hz] >	fosc(f_{CK})/1188 < 252.5[Hz] >	fosc(f_{CK})/1200 < 250.0[Hz] >
1	0	0	1	fosc(f_{CK})/1088 < 275.7[Hz] >	fosc(f_{CK})/1080 < 277.8[Hz] >	fosc(f_{CK})/1080 < 277.8[Hz] >	fosc(f_{CK})/1100 < 272.7[Hz] >	fosc(f_{CK})/1104 < 271.7[Hz] >
0	1	0	1	fosc(f_{CK})/1056 < 284.1[Hz] >	fosc(f_{CK})/1044 < 287.4[Hz] >	fosc(f_{CK})/1040 < 288.5[Hz] >	fosc(f_{CK})/1056 < 284.1[Hz] >	fosc(f_{CK})/1056 < 284.1[Hz] >
1	1	0	1	fosc(f_{CK})/992 < 302.4[Hz] >	fosc(f_{CK})/1008 < 297.6[Hz] >	fosc(f_{CK})/1000 < 300.0[Hz] >	fosc(f_{CK})/990 < 303.0[Hz] >	fosc(f_{CK})/984 < 304.9[Hz] >
0	0	1	1	fosc(f_{CK})/960 < 312.5[Hz] >	fosc(f_{CK})/972 < 308.6[Hz] >	fosc(f_{CK})/960 < 312.5[Hz] >	fosc(f_{CK})/946 < 317.1[Hz] >	fosc(f_{CK})/960 < 312.5[Hz] >
1	0	1	1	fosc(f_{CK})/928 < 323.3[Hz] >	fosc(f_{CK})/936 < 320.5[Hz] >	fosc(f_{CK})/920 < 326.1[Hz] >	fosc(f_{CK})/924 < 324.7[Hz] >	fosc(f_{CK})/936 < 320.5[Hz] >
0	1	1	1	fosc(f_{CK})/896 < 334.8[Hz] >	fosc(f_{CK})/900 < 333.3[Hz] >	fosc(f_{CK})/900 < 333.3[Hz] >	fosc(f_{CK})/902 < 332.6[Hz] >	fosc(f_{CK})/888 < 337.8[Hz] >
1	1	1	1	fosc(f_{CK})/864 < 347.2[Hz] >	fosc(f_{CK})/864 < 347.2[Hz] >	fosc(f_{CK})/860 < 348.8[Hz] >	fosc(f_{CK})/858 < 349.7[Hz] >	fosc(f_{CK})/864 < 347.2[Hz] >

FC0	FC1	FC2	FC3	Frame frequency fo[Hz]			
				1/13 duty	1/14 duty	1/15 duty	1/16 duty
0	0	0	0	fosc(f_{CK})/4264 < 70.4[Hz] >	fosc(f_{CK})/4256 < 70.5[Hz] >	fosc(f_{CK})/4320 < 69.4[Hz] >	fosc(f_{CK})/4352 < 68.9[Hz] >
1	0	0	0	fosc(f_{CK})/3744 < 80.1[Hz] >	fosc(f_{CK})/3808 < 78.8[Hz] >	fosc(f_{CK})/3720 < 80.7[Hz] >	fosc(f_{CK})/3712 < 80.8[Hz] >
0	1	0	0	fosc(f_{CK})/2964 < 101.2[Hz] >	fosc(f_{CK})/2968 < 101.1[Hz] >	fosc(f_{CK})/3000 < 100.0[Hz] >	fosc(f_{CK})/2944 < 101.9[Hz] >
1	1	0	0	fosc(f_{CK})/2392 < 125.4[Hz] >	fosc(f_{CK})/2408 < 124.6[Hz] >	fosc(f_{CK})/2400 < 125.0[Hz] >	fosc(f_{CK})/2368 < 126.7[Hz] >
0	0	1	0	fosc(f_{CK})/1976 < 151.8[Hz] >	fosc(f_{CK})/1960 < 153.1[Hz] >	fosc(f_{CK})/1980 < 151.5[Hz] >	fosc(f_{CK})/1984 < 151.2[Hz] >
1	0	1	0	fosc(f_{CK})/1716 < 174.8[Hz] >	fosc(f_{CK})/1708 < 175.6[Hz] >	fosc(f_{CK})/1710 < 175.4[Hz] >	fosc(f_{CK})/1696 < 176.9[Hz] >
0	1	1	0	fosc(f_{CK})/1482 < 202.4[Hz] >	fosc(f_{CK})/1456 < 206.0[Hz] >	fosc(f_{CK})/1500 < 200.0[Hz] >	fosc(f_{CK})/1472 < 203.8[Hz] >
1	1	1	0	fosc(f_{CK})/1326 < 226.2[Hz] >	fosc(f_{CK})/1316 < 228.0[Hz] >	fosc(f_{CK})/1350 < 222.2[Hz] >	fosc(f_{CK})/1312 < 228.7[Hz] >
0	0	0	1	fosc(f_{CK})/1196 < 250.8[Hz] >	fosc(f_{CK})/1204 < 249.2[Hz] >	fosc(f_{CK})/1200 < 250.0[Hz] >	fosc(f_{CK})/1184 < 253.4[Hz] >
1	0	0	1	fosc(f_{CK})/1118 < 268.3[Hz] >	fosc(f_{CK})/1092 < 274.7[Hz] >	fosc(f_{CK})/1080 < 277.8[Hz] >	fosc(f_{CK})/1088 < 275.7[Hz] >
0	1	0	1	fosc(f_{CK})/1040 < 288.5[Hz] >	fosc(f_{CK})/1036 < 289.6[Hz] >	fosc(f_{CK})/1050 < 285.7[Hz] >	fosc(f_{CK})/1056 < 284.1[Hz] >
1	1	0	1	fosc(f_{CK})/988 < 303.6[Hz] >	fosc(f_{CK})/980 < 306.1[Hz] >	fosc(f_{CK})/990 < 303.0[Hz] >	fosc(f_{CK})/992 < 302.4[Hz] >
0	0	1	1	fosc(f_{CK})/962 < 311.9[Hz] >	fosc(f_{CK})/952 < 315.1[Hz] >	fosc(f_{CK})/960 < 312.5[Hz] >	fosc(f_{CK})/960 < 312.5[Hz] >
1	0	1	1	fosc(f_{CK})/936 < 320.5[Hz] >	fosc(f_{CK})/924 < 324.7[Hz] >	fosc(f_{CK})/930 < 322.6[Hz] >	fosc(f_{CK})/928 < 323.3[Hz] >
0	1	1	1	fosc(f_{CK})/884 < 339.4[Hz] >	fosc(f_{CK})/896 < 334.8[Hz] >	fosc(f_{CK})/900 < 333.3[Hz] >	fosc(f_{CK})/896 < 334.8[Hz] >
1	1	1	1	fosc(f_{CK})/858 < 349.7[Hz] >	fosc(f_{CK})/868 < 345.6[Hz] >	fosc(f_{CK})/870 < 344.8[Hz] >	fosc(f_{CK})/864 < 347.2[Hz] >

(Note.1) The value of "< >" is a frame frequency when fosc(f_{CK}) is 300[kHz].

2. "Control of display ON / OFF" instruction

A state of display is set by "Control of display ON / OFF" instruction.

Instruction data (16 bits)															
D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271
PNC	0	1	0	SC0	SC1	0	BU	0	0	1	0	0	0	1	0

(2-1) PNC ··· This is control data to set normal display or reversed display.
Normal display or reversed display is set by this control data. When a state of display is ON (SC0, SC1="0, 0"), the setting of PNC becomes effective.

PNC	Normal display or Reversed display	Display data Dn_m="0"	Display data Dn_m="1"
0	Normal display	OFF	ON
1	Reversed display	ON	OFF

(Note.1) Display data "Dn_m" is from D1_1 to D200_16.

(2-2) SC0, SC1 ··· These are control data to set a state of display.
A state of display is set by these control data.

SC0	SC1	The state of display	The state of segment outputs	The state of common outputs
0	0	ON	Waveform corresponding to display data	Scan pulse
1	0	All OFF	OFF waveform	Scan pulse
0	1	All ON	ON waveform	Scan pulse
1	1	All forced OFF	$V_{LCD}5$ level	$V_{LCD}5$ level

(2-3) BU ··· This is control data to set normal mode or power-saving mode.
Normal mode or power-saving mode (low current) is set by this control data.

BU	Mode	The state of common and segment outputs	Voltage booster	Contrast adjuster	LCD drive bias voltage generator	Internal oscillator (Reception state of the external clock)
0	Normal mode	Normal display operation	These circuits can run (depend on the setting of DBC,CTC0 and CTC1).			Run (The external clock reception is possible)
1	Power-saving mode	$V_{LCD}5$ level	Stop and discharge (Note.1)	Stop and discharge (Note.1)	Stop and discharge (Note.1)	Stop (The external clock is not received.)

(Note.1) During (1) or (2) or (3) or (4) time, voltage booster, contrast adjuster and LCD drive bias voltage generator stop forcibly. And each circuit is the discharge state.

(1) The period of $\overline{\text{RES}}$="Low level" (Regardless of the setting of voltage booster, contrast adjuster or LCD drive bias voltage generator)
In the discharge state, the electric potential of VLCD is same as VBTI1. And the electric potential of VLCD0, VLCD1, VLCD2, VLCD3 and VLCD4 are same as VLCD5.

(2) DBC="1" is set by "Set of display method" instruction, and power-saving mode (BU="1") is set by "Control of display ON / OFF" instruction. In the discharge state, the electric potential of VLCD is same as VBTI1.

(3) CTC0="1" is set by "Set of display method" instruction, and power-saving mode (BU="1") is set by "Control of display ON / OFF" instruction. In the discharge state, the electric potential of VLCD0 is same as VLCD5.

(4) CTC1="1" is set by "Set of display method" instruction, and power-saving mode (BU="1") is set by "Control of display ON / OFF" instruction. In the discharge state, the electric potential of VLCD1, VLCD2, VLCD3 and VLCD4 are same as VLCD5.

(Note.2) When the setting is changed from normal mode to power-saving mode (BU="0"→"1"), secure a stop transition time more than 200 [msec]. When the setting is changed from power-saving mode to normal mode (BU="1"→"0"), a time shown from (1) to (3) is needed for stabilization of each circuit. (Refer to [Fig.9])

(1) When voltage booster, contrast adjuster and LCD drive bias voltage generator are used (DBC="1", CTC0,CTC1="1,1"), the stabilization time of these circuits is 200 [msec].

(2) When contrast adjuster and LCD drive bias voltage generator are used (DBC="0", CTC0,CTC1="1,1"), the stabilization time of these circuits is 20 [msec].

(3) When LCD drive bias voltage generator is used (DBC="0", CTC0,CTC1="0,1"), the stabilization time of this circuit is 20 [msec].

3. “Set of line address” instruction

A line address of RAM to specify a start display position is set by “Set of line address” instruction.

Instruction data (16 bits)															
D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271
LNA0	LNA1	LNA2	LNA3	0	0	0	0	0	1	0	0	0	0	1	1
(LSB)			(MSB)												

(3-1) LNA0 to LNA3 ··· These are control data to set a line address of RAM.
A line address of RAM to specify a start display position is set by these control data.

(ex.1) When a line address is “8H”, the relation between the common output and RAM at the normal scan (CDIR=“0”) is as follows.

Line address of RAM LSB MSB				A start display position								
LNA0	LNA1	LNA2	LNA3	1/8 duty	1/9 duty	1/10 duty	1/11 duty	1/12 duty	1/13 duty	1/14 duty	1/15 duty	1/16 duty
0	0	0	1	COM1	COM1	COM1	COM1	COM1	COM1	COM1	COM1	COM1
1	0	0	1	COM2	COM2	COM2	COM2	COM2	COM2	COM2	COM2	COM2
0	1	0	1	COM3	COM3	COM3	COM3	COM3	COM3	COM3	COM3	COM3
1	1	0	1	COM4	COM4	COM4	COM4	COM4	COM4	COM4	COM4	COM4
0	0	1	1	COM5	COM5	COM5	COM5	COM5	COM5	COM5	COM5	COM5
1	0	1	1	COM6	COM6	COM6	COM6	COM6	COM6	COM6	COM6	COM6
0	1	1	1	COM7	COM7	COM7	COM7	COM7	COM7	COM7	COM7	COM7
1	1	1	1	COM8	COM8	COM8	COM8	COM8	COM8	COM8	COM8	COM8
0	0	0	0	-	COM9	COM9	COM9	COM9	COM9	COM9	COM9	COM9
1	0	0	0	-	-	COM10	COM10	COM10	COM10	COM10	COM10	COM10
0	1	0	0	-	-	-	COM11	COM11	COM11	COM11	COM11	COM11
1	1	0	0	-	-	-	-	COM12	COM12	COM12	COM12	COM12
0	0	1	0	-	-	-	-	-	COM13	COM13	COM13	COM13
1	0	1	0	-	-	-	-	-	-	COM14	COM14	COM14
0	1	1	0	-	-	-	-	-	-	-	COM15	COM15
1	1	1	0	-	-	-	-	-	-	-	-	COM16

(ex.2) When a line address is “8H”, the relation between the common output and RAM at the reversed scan (CDIR=“1”) is as follows.

Line address of RAM LSB MSB				A start display position								
LNA0	LNA1	LNA2	LNA3	1/8 duty	1/9 duty	1/10 duty	1/11 duty	1/12 duty	1/13 duty	1/14 duty	1/15 duty	1/16 duty
0	0	0	1	COM16	COM16	COM16	COM16	COM16	COM16	COM16	COM16	COM16
1	0	0	1	COM15	COM15	COM15	COM15	COM15	COM15	COM15	COM15	COM15
0	1	0	1	COM14	COM14	COM14	COM14	COM14	COM14	COM14	COM14	COM14
1	1	0	1	COM13	COM13	COM13	COM13	COM13	COM13	COM13	COM13	COM13
0	0	1	1	COM12	COM12	COM12	COM12	COM12	COM12	COM12	COM12	COM12
1	0	1	1	COM11	COM11	COM11	COM11	COM11	COM11	COM11	COM11	COM11
0	1	1	1	COM10	COM10	COM10	COM10	COM10	COM10	COM10	COM10	COM10
1	1	1	1	COM9	COM9	COM9	COM9	COM9	COM9	COM9	COM9	COM9
0	0	0	0	-	COM8	COM8	COM8	COM8	COM8	COM8	COM8	COM8
1	0	0	0	-	-	COM7	COM7	COM7	COM7	COM7	COM7	COM7
0	1	0	0	-	-	-	COM6	COM6	COM6	COM6	COM6	COM6
1	1	0	0	-	-	-	-	COM5	COM5	COM5	COM5	COM5
0	0	1	0	-	-	-	-	-	COM4	COM4	COM4	COM4
1	0	1	0	-	-	-	-	-	-	COM3	COM3	COM3
0	1	1	0	-	-	-	-	-	-	-	COM2	COM2
1	1	1	0	-	-	-	-	-	-	-	-	COM1

4. "Write display data to RAM (8 × 15 bits in a lump)" instruction

The page address and column address of RAM are set by the "Write display data to RAM (8 × 15 bits in a lump)" instruction. And the display data of "8 × 15 bits (8 common outputs × 15 segment outputs)" are written to the specified page address and column address of RAM in a lump by this instruction.

Instruction data (144 bits)										
D128	D129	D130	D131	D132	……	D243	D244	D245	D246	D247
Dn_m	Dn_m+1	Dn_m+2	Dn_m+3	Dn_m+4	……	Dn+14_m+3	Dn+14_m+4	Dn+14_m+5	Dn+14_m+6	Dn+14_m+7

(Note.1) n=1 to 186, n+14=15 to 200, m=1, 9

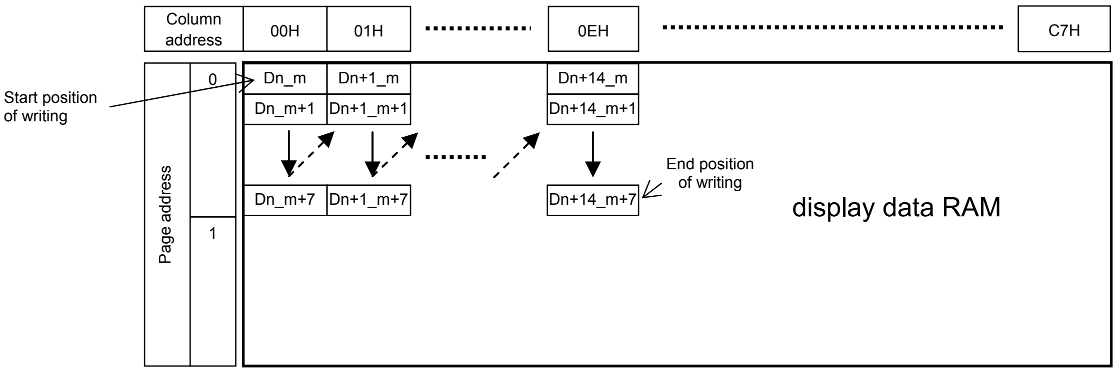
Instruction data (continuance)																							
D248	D249	D250	D251	D252	D253	D254	D255	D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271
0	0	0	0	0	0	0	0	CRA0	CRA1	CRA2	CRA3	CRA4	CRA5	CRA6	CRA7	PGA	0	0	0	0	1	0	0
								(LSB)							(MSB)								

(4-1) CRA0 to CRA7 ··· These are control data to set a column address of RAM.
The settable range of a column address from CRA0 to CRA7 is from 00H to C7H.
When a column address is set more than BAH, display data is written from start position and the overflowed data from RAM is canceled.

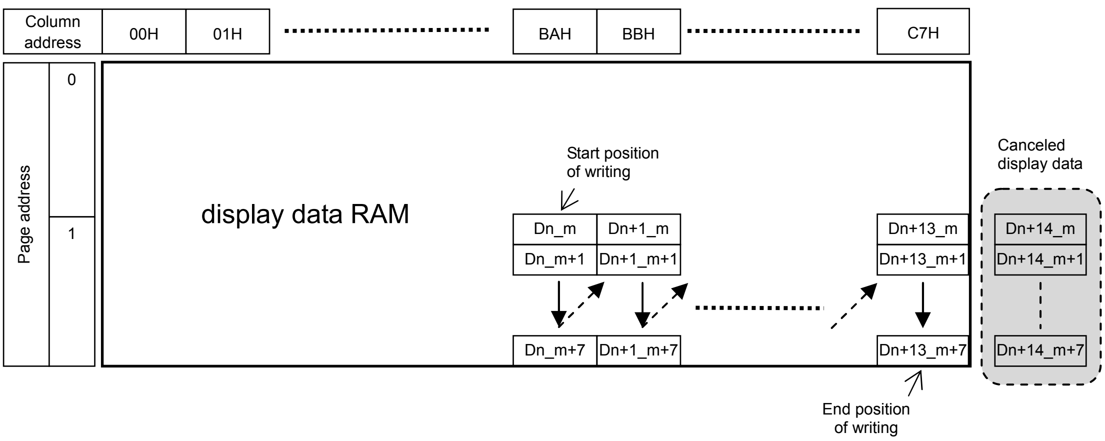
(4-2) PGA ··· This is control data to set a page address of RAM.

(4-3) Dn_m, Dn_m+1 to Dn+14_m+7 ··· These are display data which are written to RAM.
A start position of writing to RAM is set by PGA and the data from CRA0 to CRA7.

(ex.1) When a page address PGA is set to 0 and a column address from CRA0 to CRA7 is set to 00H, the relation between instruction data and a direction of writing to RAM is as follows.



(ex.2) When a page address PGA is set to 1 and a column address from CRA0 to CRA7 is set to BAH, the relation between instruction data and a direction of writing to RAM is as follows.



5. "Write display data to RAM (16 × 16 bits in a lump)" instruction

The page address and column address of RAM are set by the "Write display data to RAM (16 × 16 bits in a lump)" instruction. And the display data of "16 × 16 bits (16 common outputs × 16 segment outputs)" are written to the specified page address and column address of RAM in a lump by this instruction.

Instruction data (272 bits)										
D0	D1	D2	D3	D4	……	D251	D252	D253	D254	D255
Dn_m	Dn_m+1	Dn_m+2	Dn_m+3	Dn_m+4	……	Dn+15_m+11	Dn+15_m+12	Dn+15_m+13	Dn+15_m+14	Dn+15_m+15

(Note.1) n=1 to 185, n+15=16 to 200, m=1

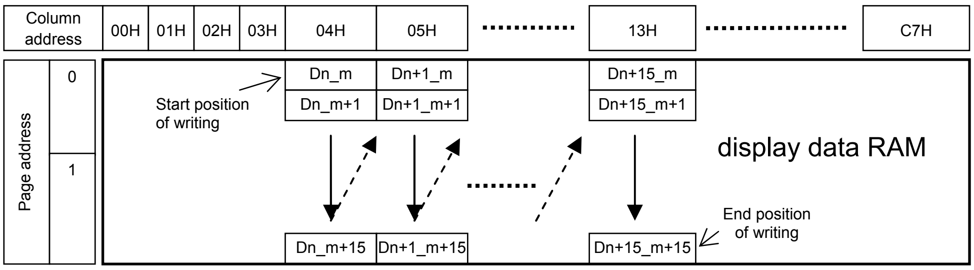
Instruction data (continuance)															
D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271
CRA0	CRA1	CRA2	CRA3	CRA4	CRA5	CRA6	CRA7	PGA	0	0	0	0	1	0	1
(LSB)							(MSB)								

(5-1) CRA0 to CRA7 ··· These are control data to set a column address of RAM.
The settable range of a column address from CRA0 to CRA7 is from 00H to C7H.
When a column address is set more than B9H, display data is written from start position and the overflowed data from RAM is canceled.

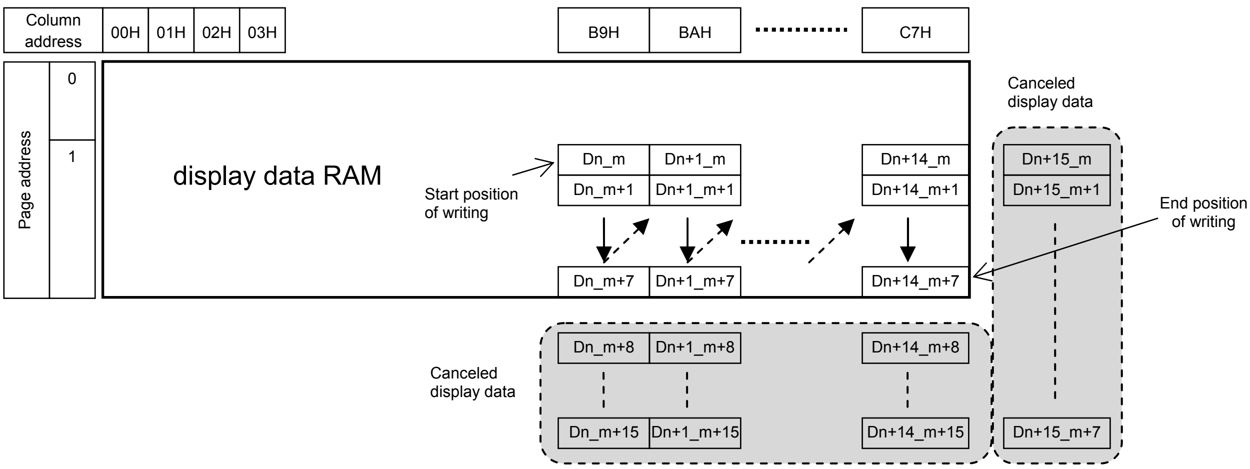
(5-2) PGA ··· This is control data to set a page address of RAM.
When PGA is set to 1, display data is written from start position and the overflowed data from RAM is canceled.

(5-3) Dn_m, Dn_m+1 to Dn+15_m+15 ··· These are display data which are written to RAM.
The start position of writing to RAM is set by PGA and the data from CRA0 to CRA7.

(ex.1) When a page address PGA is set to 0 and a column address from CRA0 to CRA7 is set to 04H, the relation between instruction data and a direction of writing to RAM is as follows.



(ex.2) When a page address PGA is set to 1 and a column address from CRA0 to CRA7 is set to B9H, the relation between instruction data and a direction of writing to RAM is as follows.



6. "Set of display contrast" instruction

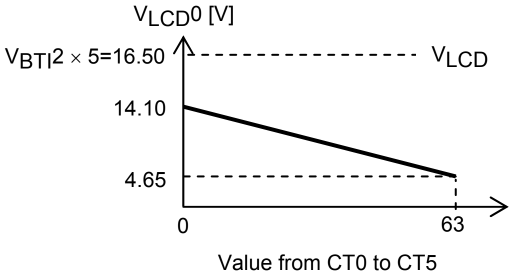
When contrast adjuster is used, LCD drive bias voltage $V_{LCD}0$ (High level) is set by "Set of display contrast" instruction.

Instruction data (16 bits)															
D256	D257	D258	D259	D260	D261	D262	D263	D264	D265	D266	D267	D268	D269	D270	D271
CT0	CT1	CT2	CT3	CT4	CT5	0	0	0	0	0	1	0	1	1	0

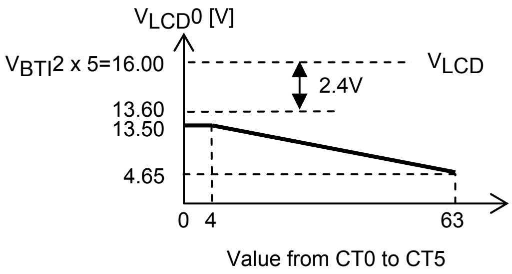
(LSB) (MSB)

(6-1) CT0 to CT5 ··· These are control data to set a display contrast.
LCD drive bias voltage $V_{LCD}0$ (High level) is set by these control data.
Follow a condition of $V_{LCD}0 \leq V_{LCD}$ - 2.4[V]. (Reference example: from (ex.1) to (ex.4))

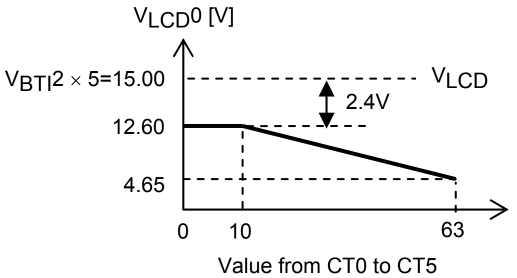
(ex.1) $V_{BTI}1=V_{BTI}2$=3.3V, REGE=VSS, Quintuple voltage booster and contrast adjuster are used.



(ex.2) $V_{BTI}1$=5.0V, REGE=VDD, $V_{BTI}2$=3.2V (Output, Typ.), Quintuple voltage booster and contrast adjuster are used.



(ex.3) $V_{BTI}1$=VBTI2=3.0V, REGE=VSS, Quintuple voltage booster and contrast adjuster are used.



(ex.4) $V_{BTI}1$=5.0V, REGE=VDD, $V_{BTI}2$=3.2V (Output, Typ.), Quadruple voltage booster and contrast adjuster are used.