Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ispXPLD™ Evaluation Board

User's Guide

October 2003
ebug02_01

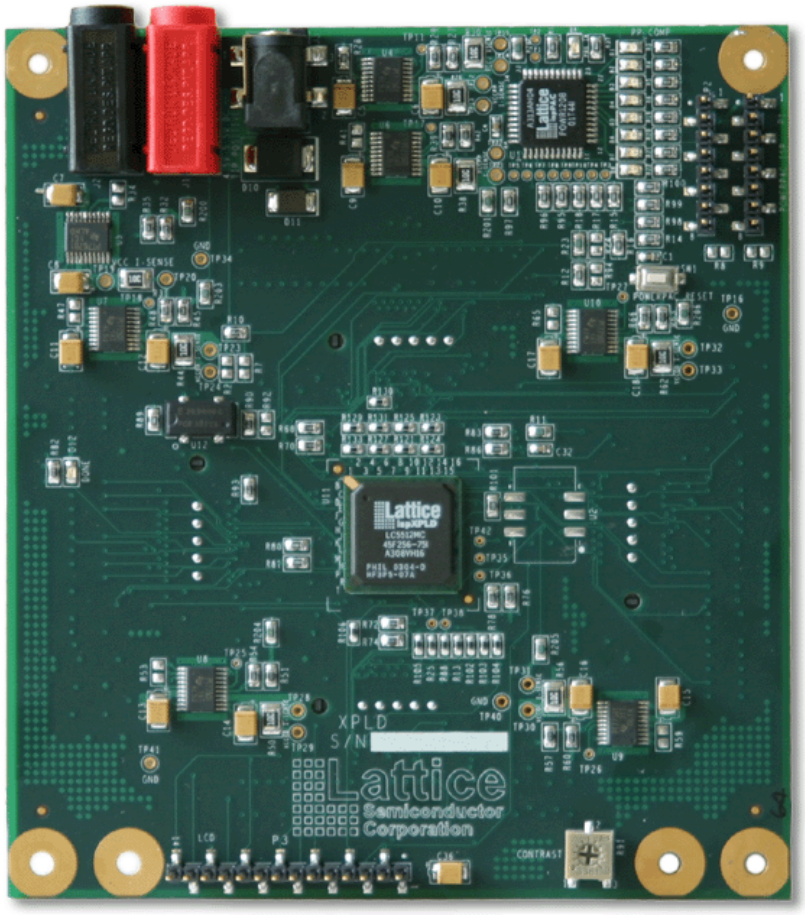
Introduction

The ispXPLD Evaluation Board is a platform to evaluate the Lattice ispXPLD device. The board features a 512-macrocell ispXPLD device. Connectors are provided to access general purpose I/Os. Termination is provided for selected I/Os for LVDS operation.

Features

- Power management provided via Lattice ispPAC® Power Manager device
- On-board 20MHz oscillator
- Multiple integrated Low Drop-Out (LDO) regulators provide power from single 5V supply
- Labeled test-points allow current measurement of each individual supply
- ispVM™ programming support
- Jumperless implementation
- ispDOWNLOAD® Cable (pDS4102-DL2) included

Figure 1. ispXPLD Evaluation Board



Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 4.5 inches by 5 inches. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: < 95% without condensation
- 5VDC input, accessible via banana jacks or the included 5V, 4A AC adapter

Holes are included at the corners of the PCB to provide attachment of vertical stand-offs. The pads at these holes are electrically floating.

Resources relating to the ispXPLD evaluation board, including a simple demonstration design, can be found on the Lattice web site at www.latticesemi.com.

Table 1. Embedded Functions

Description	Source	ispXPLD Pin	Notes
20MHz clock	On-board oscillator	GCLK0 (H2)	3.3V TTL output
Reset	ispPAC device	Global RST (J11) AND I/O pin R9	Active low by default, programmable via ispPAC

ispPAC-POWR1208 Power Manager Device

The Power Manager device controls the sequencing and monitoring of the various independent power supplies available on the ispXPLD board. Each supply can be activated in stages, with programmable delay increments. As the Power Manager device enables each LDO, a corresponding LED deactivates for visual confirmation.

The Power Manager design and JEDEC files can be downloaded from the Latttice web site. The device is shipped preprogrammed with this default configuration.

For a complete description of the operation of the ispPAC-POWR1208 device and the default design used on this board, refer to the ispPAC-POWR1208 data sheet and PAC-Designer® documentation (PAC-Designer is the design software for the ispPAC-POWR1208). These are available on the Lattice web site at www.latticesemi.com.

V_{CCO} Configurations

The ispXPLD device supports multiple I/O standards, and features individual I/O bank supply pins for simultaneous support of different interfaces. The ispXPLD evaluation board is set by default to supply 2.5V to all I/O banks. This is adjustable via the addition of resistors. For alternate supply levels, specific resistor values can be installed as described in Figure 2.

Figure 2. I/O Voltage Adjustments

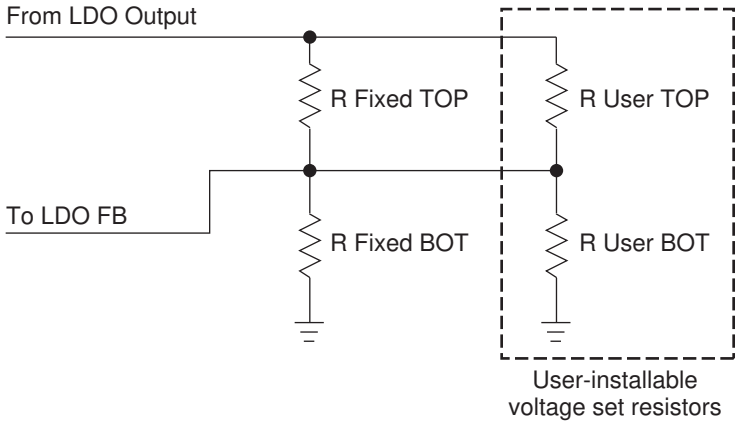


Table 2. VCCOX LDO Adjustments

VCCOX	R Fixed TOP	R Fixed BOT	R User TOP	R User BOT
2.5V	127.0K	110.0K	DNP	DNP
3.3V	127.0K	110.0K	DNP	200.0K
1.8V	127.0K	110.0K	110.0K	DNP
1.5V	127.0K	110.0K	402K	DNP

Resistor numbers and physical locations can be found in the schematic and bottom silkscreen drawing, in Appendix B of this document.

Switches

One push-button reset switch (SW1) is provided to force a reset of the ispPAC-POWR1208 device. When this switch is activated, the power-up cycle of the ispPAC-POWR1208 device is re-started. This, in turn, cycles power to the rest of the board. The ispXPLD device contains power-on reset circuitry, for predicable initialization.

Programming Headers

Separate 1x8 headers are provided to allow independent configuration of the ispXPLD and ispPAC devices. Pin 1 of both headers is VCC (red wire from download cable). Table 3 shows the programming header locations.

Table 3. Programming Connectors

Connector	Target Device
JTAG Connector P1	ispPAC-POWR1208
JTAG Connector P2	ispXPLD

I/O Connectors

Connectivity for general-purpose I/O pins is provided by both 2mm DIP headers and Mictor connectors on the underside of the board. Tables 4 through 7 provide locations for the ispXPLD I/Os.

Table 4. I/O Bank 0

P4 (2mm)	J4 (Mictor)	Description	ispXPLD Pin	Notes
1	1	GCLK0	H2	Unpopulated Series Resistor for 2mm Header
2	2	GND	-	
3	3	M30_91N_IOB0_LVD	B7	100-ohm LVDS Termination
4	4	M26_92N_IOB0_LVD	D7	100-ohm LVDS Termination
5	5	M28_91P_IOB0_LVD	A7	100-ohm LVDS Termination
6	6	M24_92P_IOB0_LVD	C7	100-ohm LVDS Termination
7	7	M22_93N_IOB0_LVD	B6	100-ohm LVDS Termination
8	8	M20_94N_IOB0_LVD	E6	100-ohm LVDS Termination
9	9	M21_93P_IOB0_LVD	E7	100-ohm LVDS Termination
10	10	M18_94P_IOB0_LVD	A6	100-ohm LVDS Termination
11	11	M10_96P_IOB0_LVD	A3	100-ohm LVDS Termination
12	12	M6_97P_IOB0_LVD	B3	100-ohm LVDS Termination
13	13	M12_96N_IOB0_LVD	B5	100-ohm LVDS Termination
14	14	M8_97N_IOB0_LVD	B4	100-ohm LVDS Termination
15	15	M4_98P_IOB0_LVD	C6	100-ohm LVDS Termination
16	16	M0_99P_IOB0_LVD	D6	100-ohm LVDS Termination
17	17	M5_98N_IOB0_LVD	C5	100-ohm LVDS Termination
18	18	M2_99N_IOB0_LVD	D5	100-ohm LVDS Termination
19	19	N4_107P_IOB0_LVD	B2	100-ohm LVDS Termination
20	20	112P_IOB0_LVDT	D2	
21	21	M5_107N_IOB0_LVD	A2	100-ohm LVDS Termination
22	22	112N_IOB0_LVDT	E3	
23	-	GND	-	
24	-	GND	-	
25	25	117P_IOB0_LVDT	E1	
26	26	118P_IOB0_LVDT	F5	
27	29	117N_IOB0_LVDT	D1	
28	28	118N_IOB0_LVDT	F4	
29	29	119P_IOB0_LVDT	F2	
30	30	120P_IOB0_LVDT	G1	
31	31	119N_IOB0_LVDT	E2	
32	32	120N_IOB0_LVDT	F1	
33	33	121P_IOB0_LVDT	G5	
34	34	122P_IOB0_LVDT	G4	
35	35	121N_IOB0_LVDT	F3	
36	36	122N_IOB0_LVDT	H5	
37	37	123P_IOB0_LVDT	H3	
38	-	124P_IOB0_LVDT	H1	
39	38	123N_IOB0_LVDT	G3	

Table 4. I/O Bank 0 (Continued)

P4 (2mm)	J4 (Mictor)	Description	ispXPLD Pin	Notes
40	-	124N_IOB0_LVDT	G2	
41	-	O24_110P_IOB0	C1	
42	-	GND	-	
43	-	O24_110N_IOB0	B1	
44	-	M14_95P_IOB0	A4	
45	-	O24_109P_IOB0	E4	
46	-	O20_111P_IOB0	C2	
47	-	O24_109N_IOB0	C4	
48	-	O22_111N_IOB0	D3	
49	-	GND	-	
50	-	GND	-	

Table 5. I/O Bank 1

P5(2mm)	J5(Mictor)	Description	ispXPLD Pin	Notes
1	1	GCLK1	J2	
2	2	GND	-	
3	3	A0_DATA0_0N_IOB1	K3	
4	4	A2_DATA1_0N_IOB1	J3	
5	5	A4_DATA2_0N_IOB1	J5	
6	6	A6_DATA3_0N_IOB1	J4	
7	7	A8_DATA4_0N_IOB1	L2	
8	8	A10_DATA5_0N_IOB1	M1	
9	9	A12_DATA6_0N_IOB1	K4	
10	10	A14_DATA7_0N_IOB1	L3	
11	11	A16_INITF_4P_IOB1	K5	
12	12	A18_CSF_4N_IOB1	L5	
13	13	A20_READ_5P_IOB1	N1	
14	14	A22_CCLK_5N_IOB1	M2	
15	15	PGMF	R3	10k-ohm Resistor to V_{CCJ}
16	16	DONE	M4	Drives LED, see Schematic Figure 8
17	17	CFG0	L8	10k-ohm Resistor to V_{CCJ}
18	18	GND	-	
19	19	B2_8N_IOB1	P2	
20	20	B0_8P_IOB1	N2	
21	21	B5_9N_IOB1	R2	
22	22	B4_9P_IOB1	R1	
23	23	B8_10N_IOB1	T3	
24	24	B6_10P_IOB1	T2	
25	25	B16_11N_IOB1	P4	
26	26	B14_11P_IOB1	N3	
27	27	B20_12N_IOB1	M6	

Table 5. I/O Bank 1 (Continued)

P5(2mm)	J5(Mictor)	Description	ispXPLD Pin	Notes
28	28	B18_12P_IOB1	N5	
29	29	B24_13P_IOB1	T4	
30	36	B22_IOB1	P5	
31	31	B28_14P_IOB1	R4	
32	30	B26_13N_IOB1	T5	
33	33	C0_15P_IOB1	R5	
34	32	B30_14N_IOB1	N6	
35	35	C12_IOB1	M7	
36	34	C2_15N_IOB1	P6	
37	37	C18_18N_IOB1	R6	
38	38	C16_18P_IOB1	T6	
39	-	C26_19N_IOB1	R7	
40	-	C24_19P_IOB1	T7	
41	-	D0_20N_IOB1	P7	
42	-	C28_20P_IOB1	N7	
43	-	D4_21N_IOB1	R8	
44	-	D2_21P_IOB1	T8	
45	-	D8_22N_IOB1	P8	
46	-	D6_22P_IOB1	M8	
47	-	D16_23N_IOB1	M9	
48	-	D12_23P_IOB1	N8	
49	-	GND	-	
50	-	GND	-	

Table 6. I/O Bank 2

P6(2mm)	J6(Mictor)	Description	ispXPLD Pin	Notes
1	-	GND	-	
2	-	GND	-	
3	1	E0_27P_IOB2	T11	24.9-ohm Series Resistor
4	2	E2_27N_IOB2	T12	24.9-ohm Series Resistor
5	3	E4_28P_IOB2	P10	24.9-ohm Series Resistor
6	4	E6_28N_IOB2	R10	24.9-ohm Series Resistor
7	5	E8_29P_IOB2	R11	49.9-ohm Resistor to V_{CCOC}
8	6	E10_29N_IOB2	M10	49.9-ohm Resistor to V_{CCOC}
9	7	E12_30P_IOB2	M11	49.9-ohm Resistor to V_{CCOC}
10	8	E16_30P_IOB2	T13	49.9-ohm Resistor to V_{CCOC}
11	9	E18_IOB2	P11	
12	10	GND	-	
13	11	E24_32N_IOB2	R13	
14	12	E22_32P_IOB2	R12	
15	13	E28_33N_IOB2	T15	

Table 6. I/O Bank 2 (Continued)

P6(2mm)	J6(Mictor)	Description	ispXPLD Pin	Notes
16	14	E26_33P_IOB2	N11	
17	15	F2_34N_IOB2	N12	
18	16	F0_34P_IOB2	R14	
19	17	F6_35N_IOB2	R15	
20	18	F4_35P_IOB2	P12	
21	19	G6_42N_IOB2	P15	
22	20	G4_42P_IOB2	P13	
23	21	GOE0	H11	
24	22	GND	-	
25	23	G10_43N_IOB2	P14	
26	24	G8_43P_IOB2	M13	
27	25	G22_46N_IOB2	P16	
28	26	G20_46P_IOB2	R16	
29	27	G26_47N_IOB2	N14	
30	28	G24_47P_IOB2	N15	
31	29	G30_48N_IOB2	M16	
32	30	G28_48P_IOB2	N16	
33	31	H0_49N_IOB2	M15	
34	32	H0_49P_IOB2	M14	
35	-	GND	-	
36	-	GND	-	
37	33	H10_51N_IOB2	L12	
38	34	H8_51P_IOB2	L13	
39	35	H14_52N_IOB2	L16	
40	36	H12_52P_IOB2	L15	
41	37	H20_53N_IOB2	K15	
42	38	H16_53P_IOB2	L14	
43	-	H22_54N_IOB2	K12	
44	-	H12_54P_IOB2	K14	
45	-	H26_55N_IOB2	J13	
46	-	H12_55P_IOB2	K13	
47	-	H30_56N_IOB2	J12	
48	-	H12_56P_IOB2	J14	
49	-	GND	-	
50	-	GND	-	

Table 7. I/O Bank 3

P7(2mm)	J7(Mictor)	Description	ispXPLD Pin	Notes
1	1	GND	-	
2	2	GND	-	
3	3	I30_57N_IOB3	H14	

Table 7. I/O Bank 3 (Continued)

P7(2mm)	J7(Mictor)	Description	ispXPLD Pin	Notes
4	4	I28_57P_IOB3	G16	
5	5	I26_58N_IOB3	G15	
6	6	I24_PLLFBK1_58P	F15	
7	7	I22_PLLRST1_59N	H12	
8	8	I20_59P_IOB3	G14	
9	9	I28_60N_IOB3	F16	
10	10	I16_60P_IOB3	E16	
11	11	I14_61N_IOB3	G13	
12	12	I12_61P_IOB3	G12	
13	13	I10_62N_IOB3	F14	
14	14	I8_CLKOUT1_62P_IOB3	E15	
15	15	I6_63N_IOB3	F12	
16	16	I4_63P_IOB3	F13	
17	17	I2_64N_IOB3	D16	
18	18	IO_64P_IOB3	D15	
19	19	J14_69N_IOB3	C16	
20	20	J12_69P_IOB3	B16	
21	21	J10_70N_IOB3	C15	
22	22	J8_70P_IOB3	B15	
23	23	J6_71N_IOB3	E14	
24	24	J4_71P_IOB3	D14	
25	25	J2_72N_IOB3	E13	
26	26	J0_72P_IOB3	A15	
27	27	K30_73N_IOB3	D12	
28	28	K28_73P_IOB3	B14	
29	29	K26_74N_IOB3	C13	
30	30	K24_74P_IOB3	A14	
31	31	K22_75N_IOB3	A13	
32	32	K21_75P_IOB3	B13	
33	33	K20_76N_IOB3	D11	
34	34	K18_76P_IOB3	B12	
35	35	K16_77N_IOB3	C12	
36	36	K14_77P_IOB3	E11	
37	-	GND	-	
38	-	GOE1	H13	
39	37	K0_81P_IOB3	A11	
40	38	K2_81N_IOB3	A12	
41	-	L28_82P_IOB3	C11	
42	-	L30_82N_IOB3	B11	
43	-	L24_83P_IOB3	A10	
44	-	L26_83N_IOB3	B10	
45	-	No Connect	-	
46	-	L22_84N_IOB3	C10	

Table 7. I/O Bank 3 (Continued)

P7(2mm)	J7(Mictor)	Description	ispXPLD Pin	Notes
47	-	L18_85P_IOB3_LCD2	E9	
48	-	L20_85N_IOB3_LCD1	C9	
49	-	GND	-	
50	-	GND	-	

The top side of the board also contains a 14-pin header, which is suitable for connection to an LCD display. 5V Power and GND are provided in addition to 11 I/Os from the ispXPLD device. A contrast control is also available via a 20K-ohm potentiometer mounted near the header. A compatible display is the Optrex DMC16207 (or equivalent) 16x2 character LCD module. Table 8 lists the pin locations for this feature.

Table 8. LCD Header

P3	Description	ispXPLD Pin
1	GND	-
2	+5V	-
3	Contrast	-
4	L20_85N_IOB3_LCD1	C9
5	L18_85P_IOB3_LCD2	E9
6	L14_IOB3_LCD3	F9
7	L12_87N_IOB3_LCD4	A9
8	L10_87P_IOB3_LCD5	F8
9	L8_88N_IOB3_LCD6	E8
10	L6_88P_IOB3_LCD7	A8
11	L5_89N_IOB3_LCD8	B9
12	L4_89P_IOB3_LCD9	D8
13	L2_90N_IOB3_LCDA	B8
14	L0_90P_IOB3_LCDB	C8

Running the Sample Program

Requirements

- PC with ispVM System software version 13.1 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). Note: An option to install these drivers is included as part of the ispVM System setup.
- ispDOWNLOAD Cable (pDS4102-DL2, HW7265-DL3 or HW-USB-1A)

This sample program consists of a 10-bit counter running from the on-board 20MHz oscillator. The 10-bit counter value is routed to output pins, as described below in Table 9.

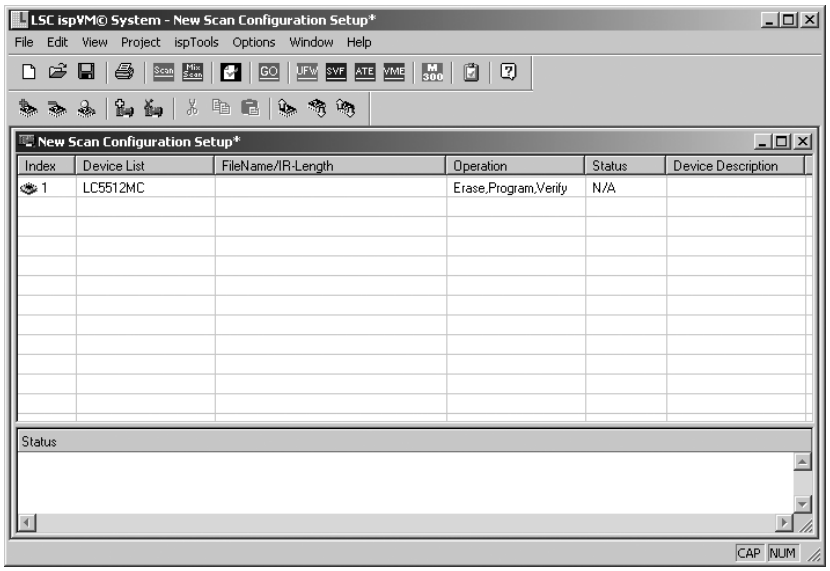
Table 9. Counter Output Locations

Output	Board Location	Function
Counter[9]	P3, pin 14	Counter MSB output
Counter[8]	P3, pin 13	
Counter[7]	P3, pin 12	
Counter[6]	P3, pin 11	
Counter[5]	P3, pin 10	
Counter[4]	P3, pin 9	
Counter[3]	P3, pin 8	
Counter[2]	P3, pin 7	
Counter[1]	P3, pin 6	
Counter[0]	P3, pin 5	Counter LSB output

Download Procedures

1. Connect the ispXPLD Evaluation Board to the AC adaptor or an external 5V supply.
2. Connect the ispDOWNLOAD Cable to connector P2 to access the ispXPLD device. Pin 1 corresponds to V_{CC} (red wire on cable).
3. Start the ispVM System software.
4. Click the 'SCAN' button located in the toolbar. The ispXPLD should be automatically detected. The resulting screen should be similar to Figure 3..

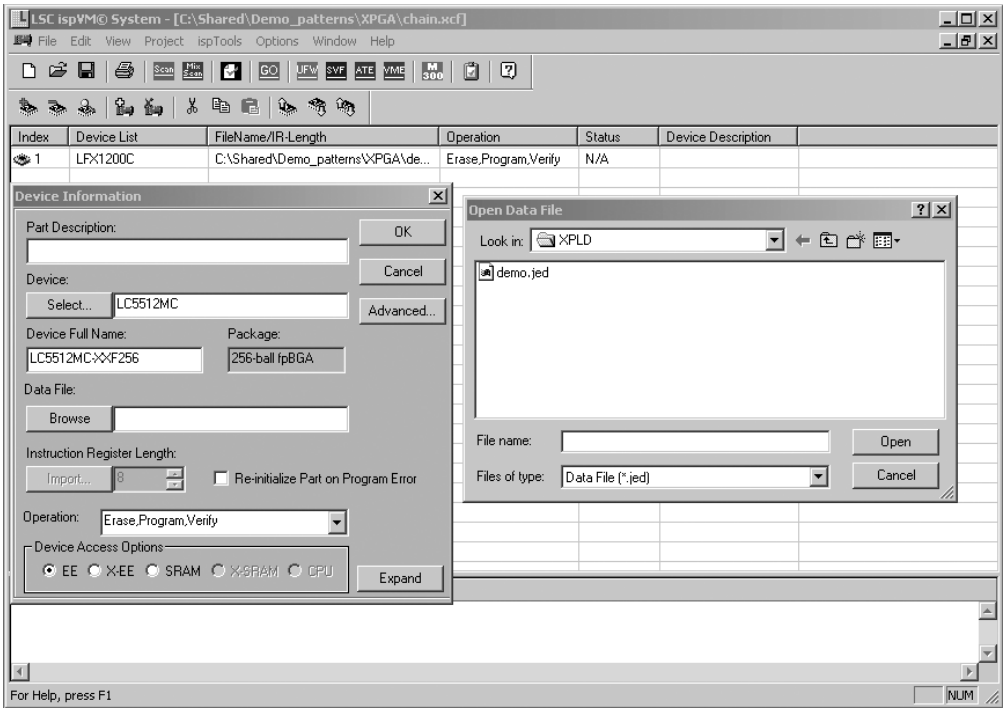
Figure 3. ispVM System Software Interface



5. Double-click the ispXPLD to open the device properties dialog.

In the device properties dialog, click the Browse button located under 'Data File'. Locate the 'demo.isc' file. Click Ok to both dialog boxes.

Figure 4. Selecting the Data File



6. Click the green 'GO' button. This will begin the download process.

Once the download is complete, the counter outputs should be viewable in the corresponding locations.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-408-826-6002 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Appendix A. Schematic

Figure 5. Lattice ispXPLD Evaluation Board Schematic

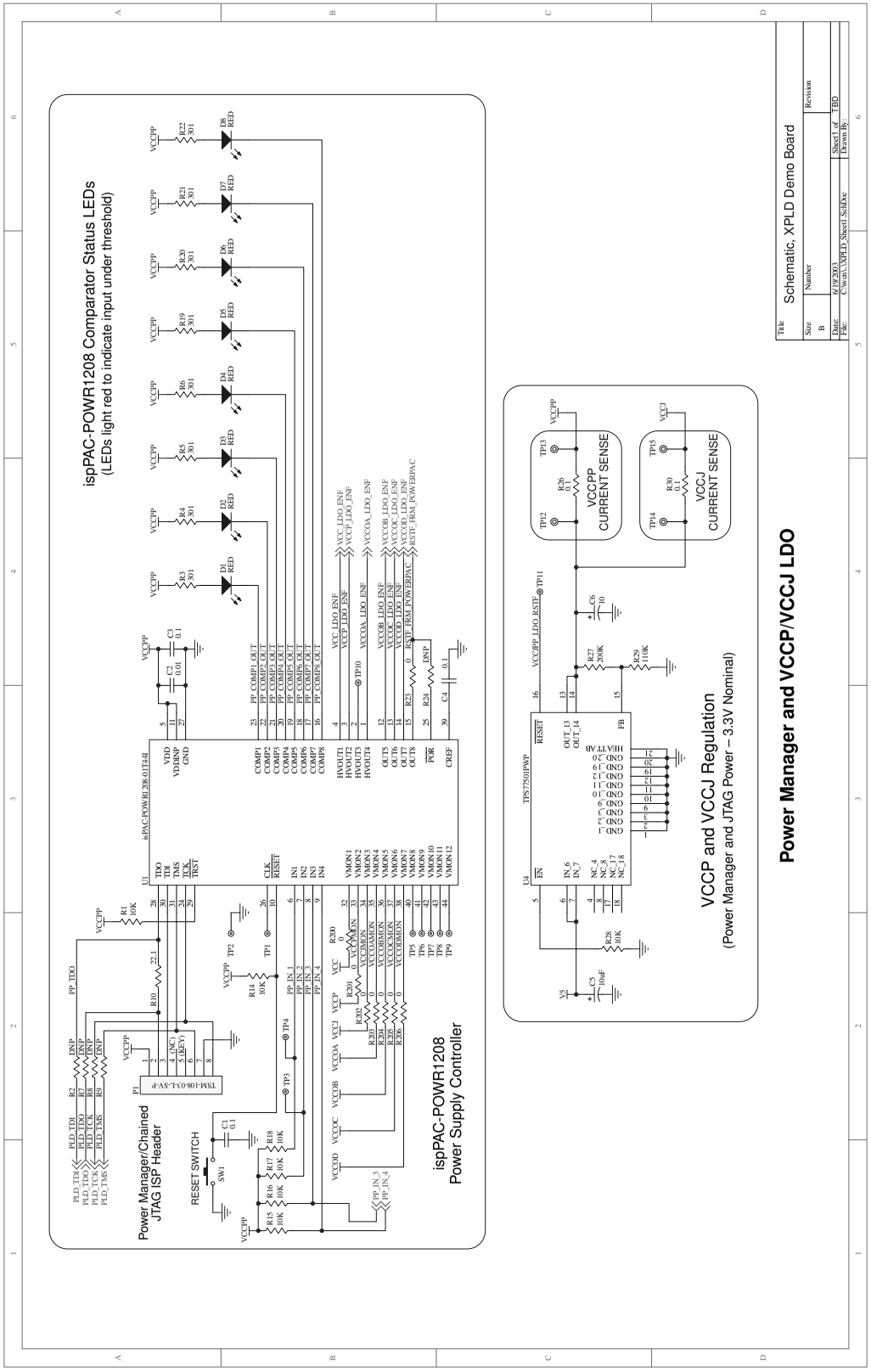


Figure 6. Lattice ispXPLD Evaluation Board Schematic

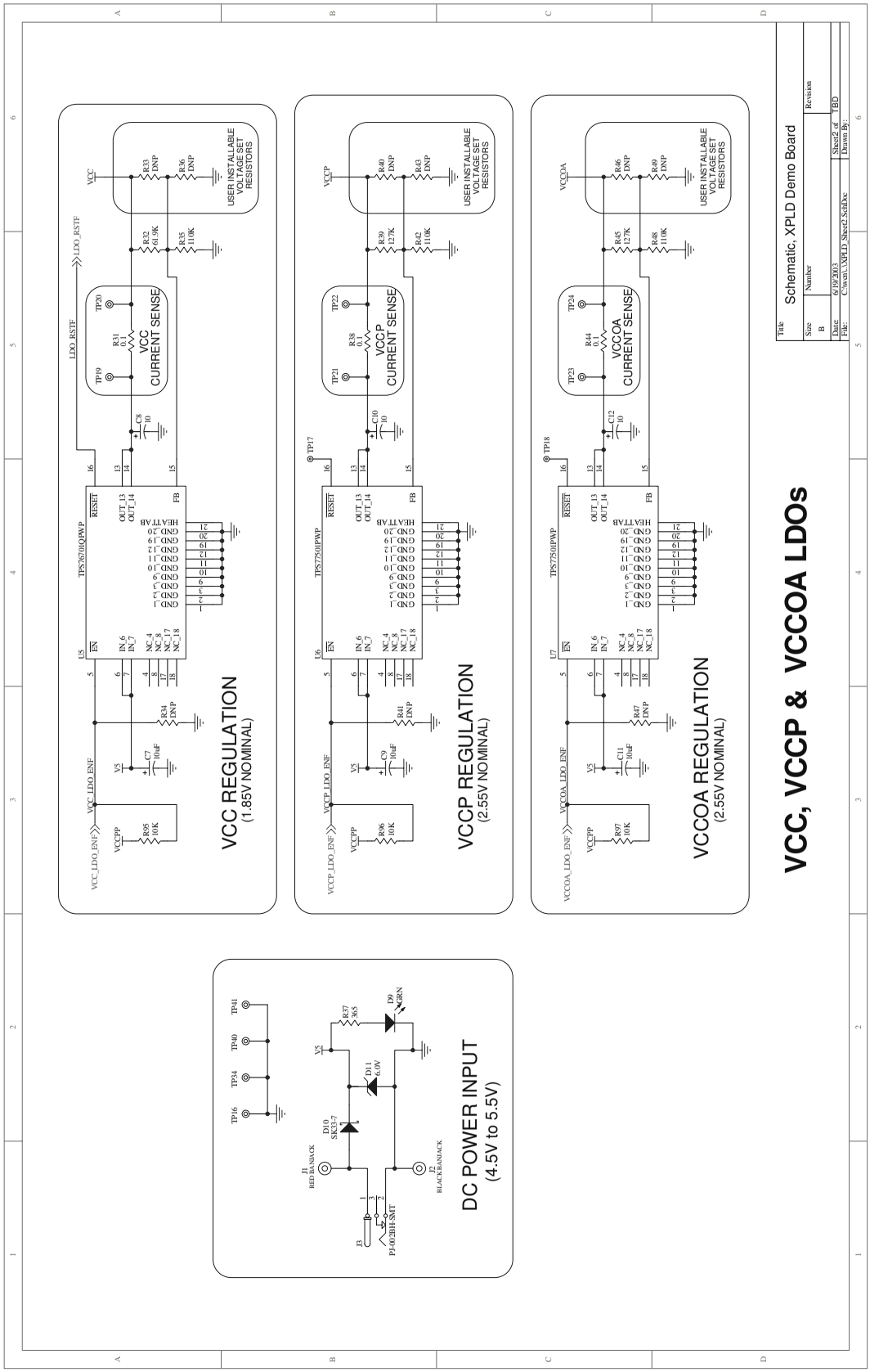
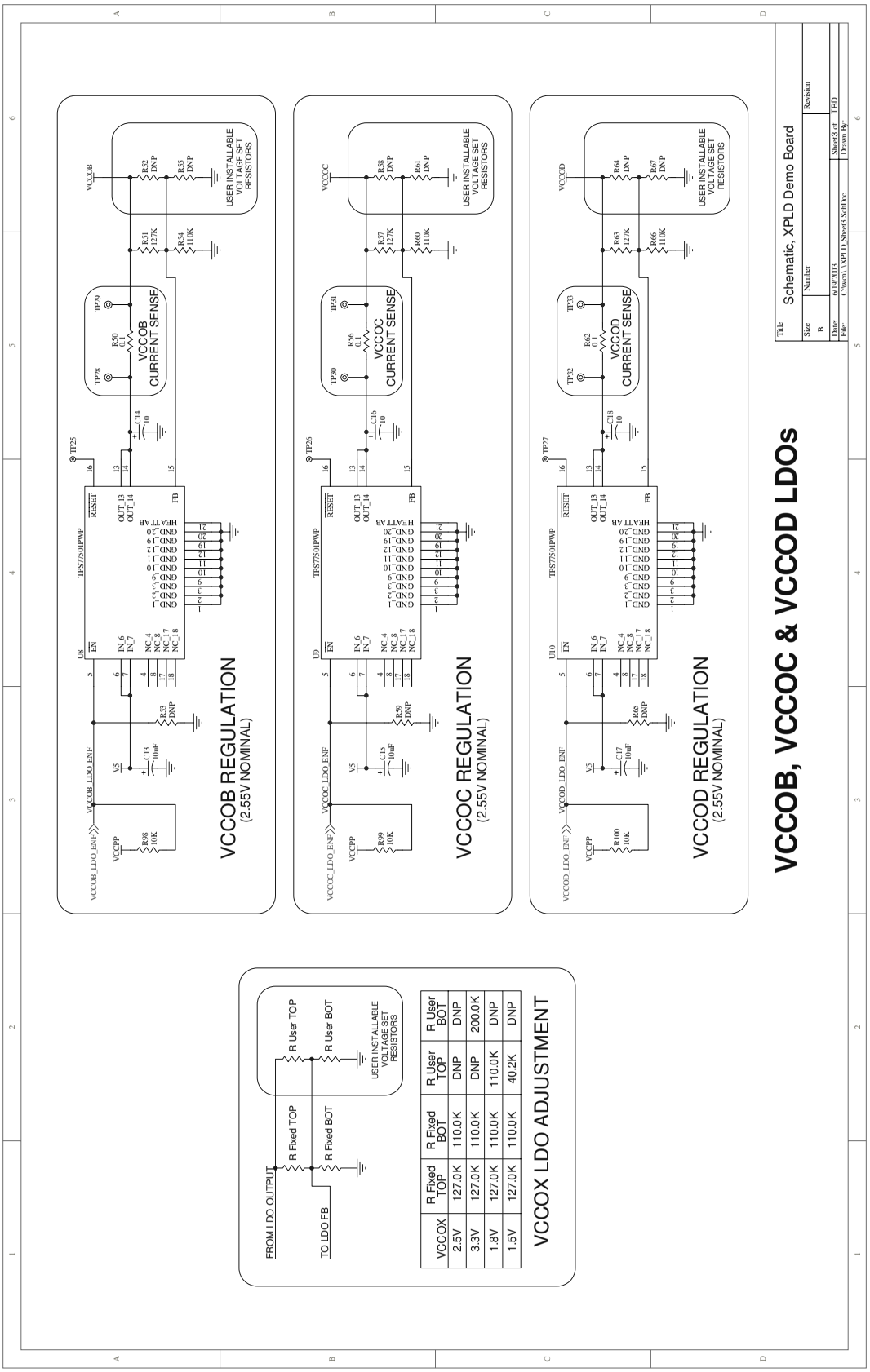


Figure 7. Lattice ispXPLD Evaluation Board Schematic



VCCOX	R Fixed TOP	R Fixed BOT	R User TOP	R User BOT
2.5V	127.0K	110.0K	DNP	DNP
3.3V	127.0K	110.0K	DNP	200.0K
1.8V	127.0K	110.0K	110.0K	DNP
1.5V	127.0K	110.0K	40.2K	DNP

Figure 8. Lattice ispXPLD Evaluation Board Schematic

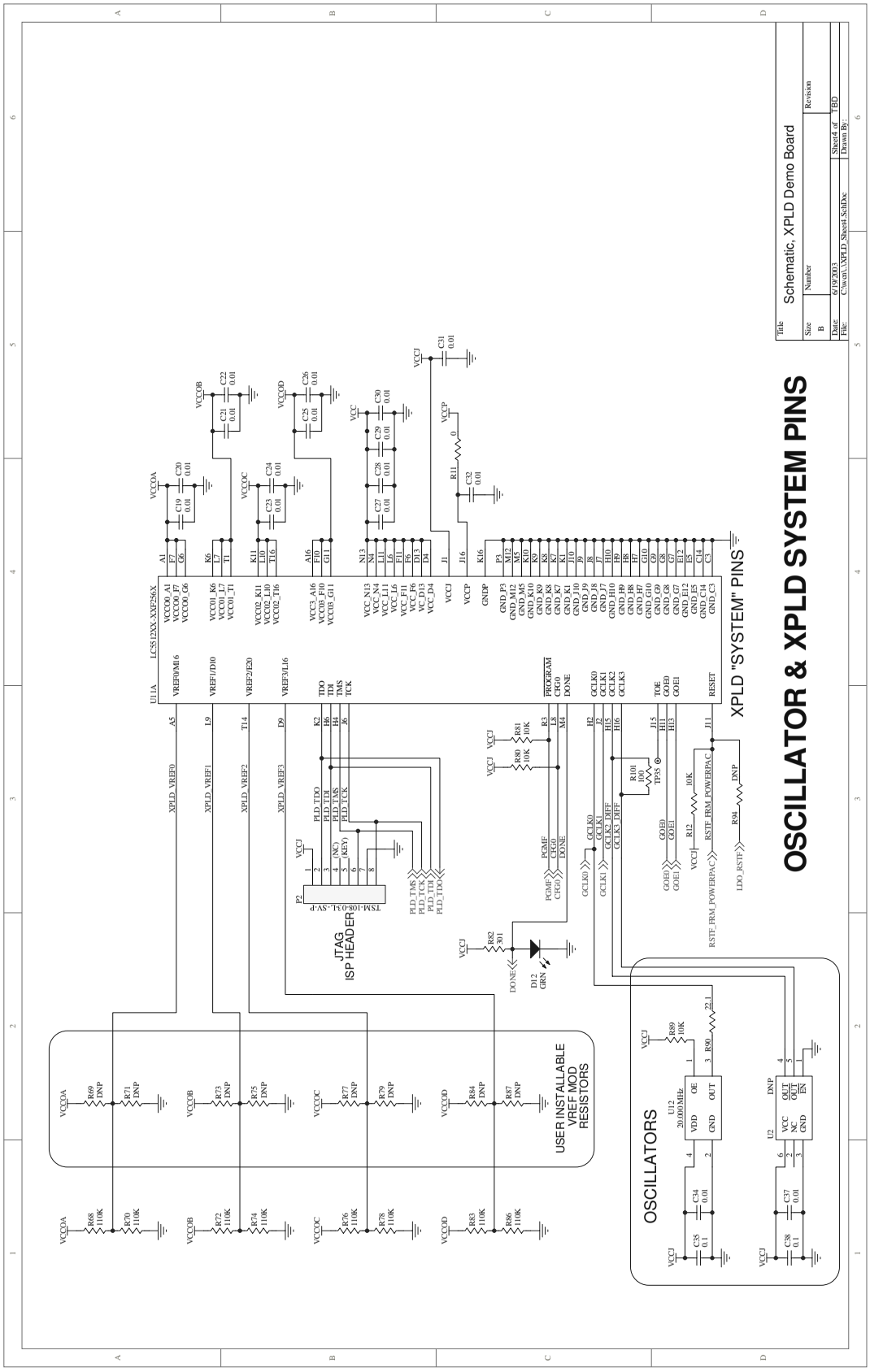


Figure 9. Lattice ispXPLD Evaluation Board Schematic

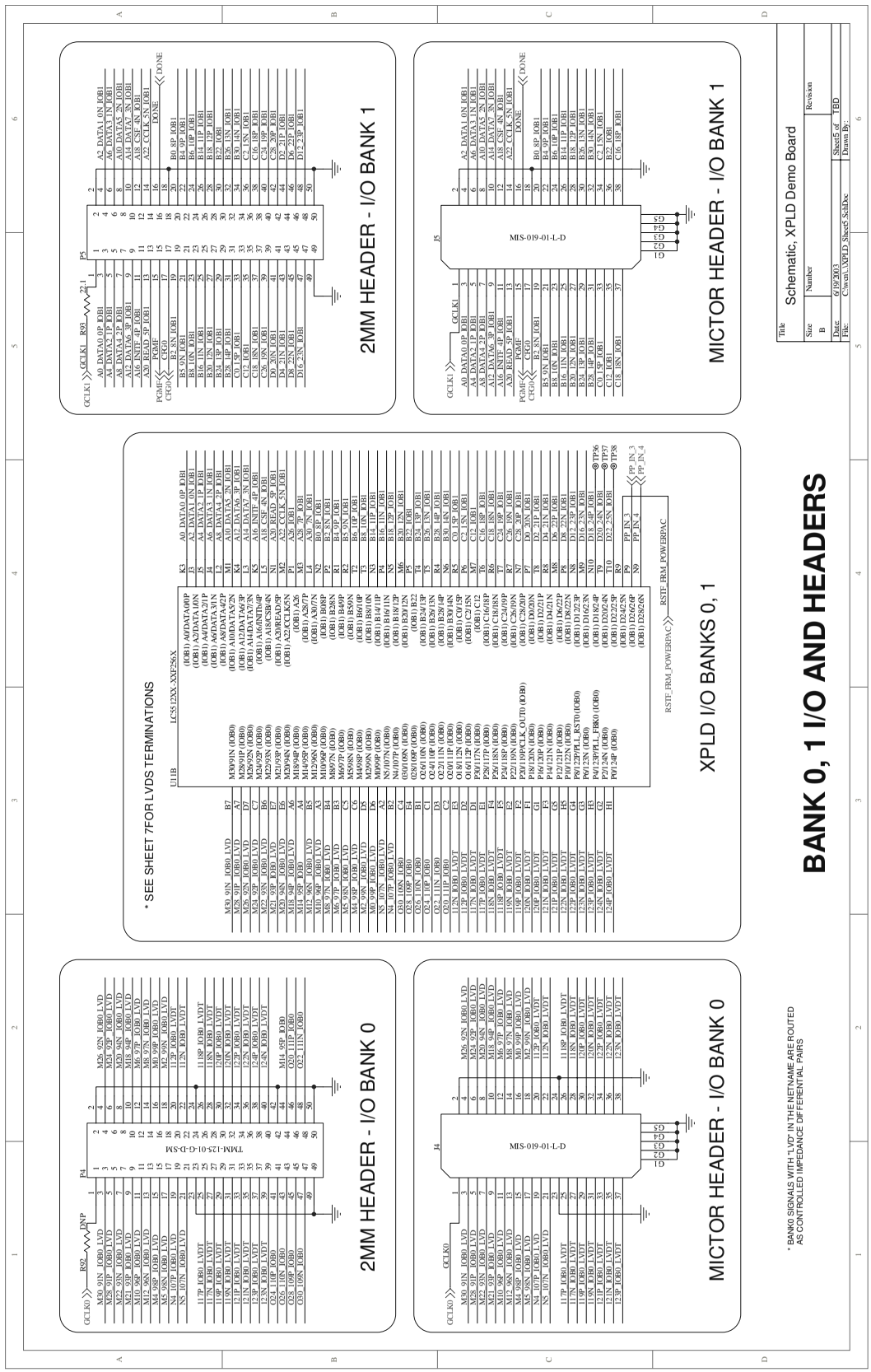


Figure 10. Lattice ispXPLD Evaluation Board Schematic

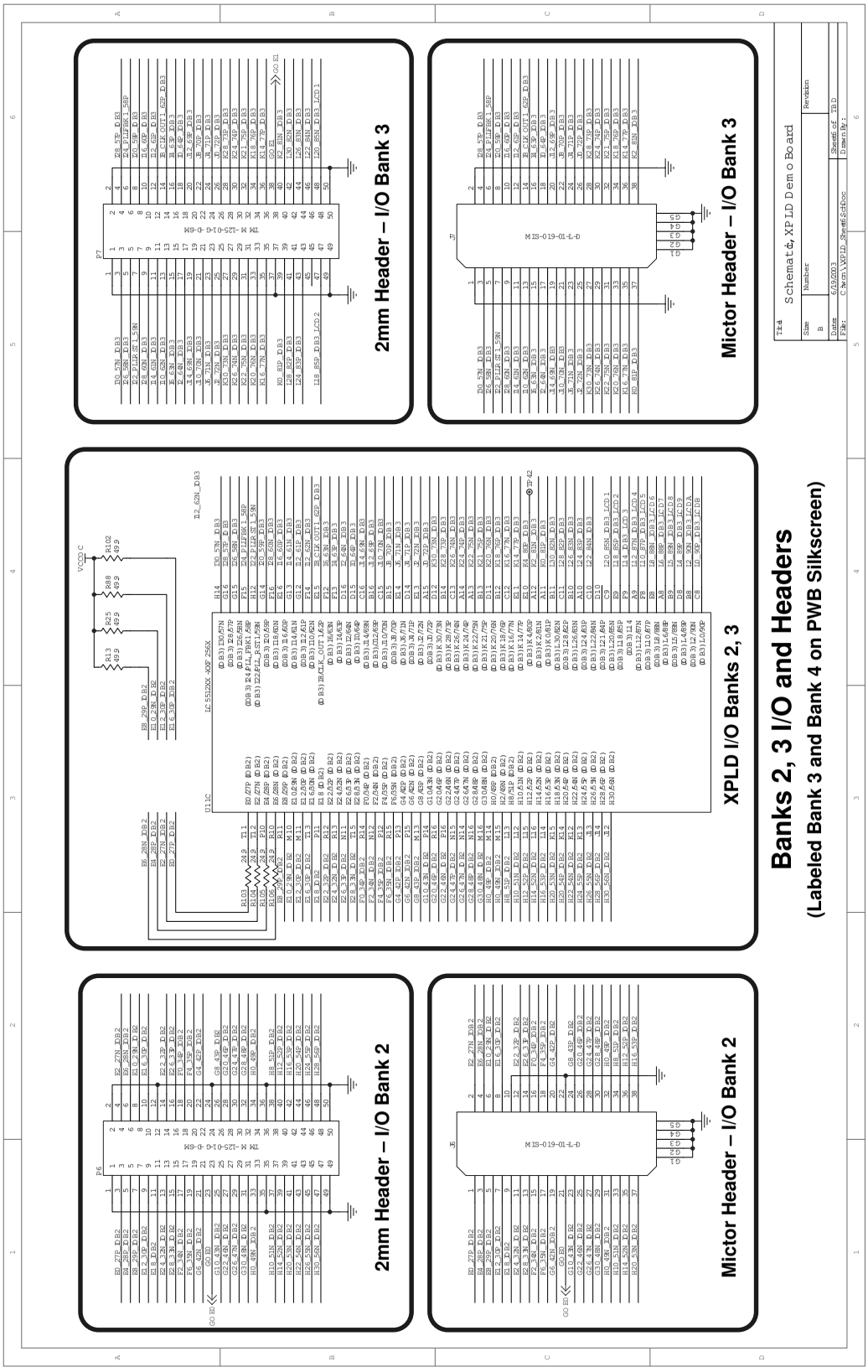
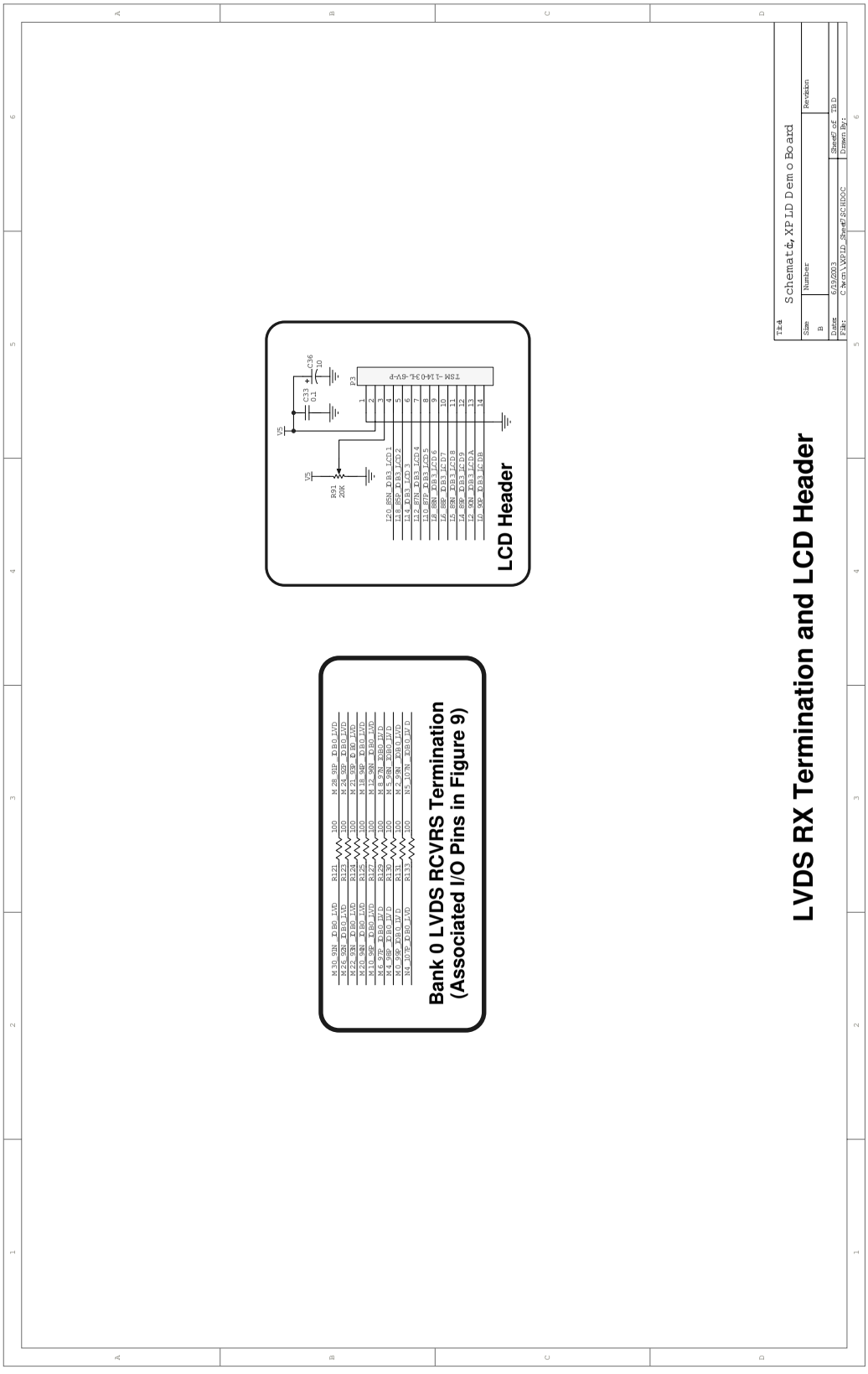


Figure 11. Lattice ispXPLD Evaluation Board Schematic



Appendix B. Bottom Silkscreen Drawing