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LC703200AW

Advance Information

ON Semiconductor®

http://onsemi.com

CMOS LSI

Speech Processing IC

Overview

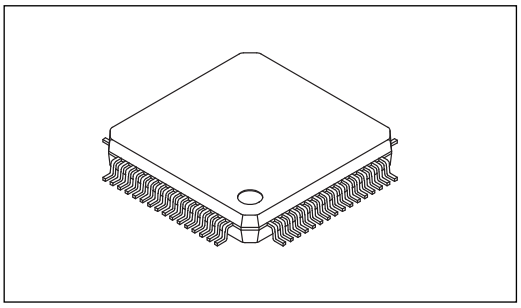
LC703200AW is a Speech Processing LSI which equips original DSP, ADC/DAC, PCM Interface, I^2C Interface and Flash memory. The LSI realizes speech processing functions such as Noise Canceller, Voice Speed Control, S-LIVE (Original Low Boost), Center Enhancement and Stereo Enhancement. And the LSI Realize small standalone system by supporting Timer and many I/O functions.

Features

1) DSP Block
   32bit DSP : Max Frequency = 68MHz, Power Save Mode Support
2) I^2C Interface : Master/Slave : 1ch
3) 24bit ADC/DAC : 2ch, Fs = 8kHz / 11.025kHz / 12kHz / 16kHz / 22.05kHz / 24kHz / 32kHz / 44.1kHz / 48kHz
4) PCM Interface : Master mode 2ch, I^2S, Left/Right Justified, Long frame Sync., Short Frame Sync.
   Fs = 8kHz / 11.025kHz / 12kHz / 16kHz / 22.05kHz / 24kHz / 32kHz / 44.1kHz / 48kHz
   Note : Slave mode only support PCM Interface, it doesn't support ADC/DAC.
5) TIMER/PWM (MTM) : 6ch(resolution 16bit)
   TIMER (PTM) : 1ch(resolution 16bit)
6) WDT : 1ch (Max period 32.7S at 8.192MHz oscillation)
7) SIO : 2ch (8bit/16bit mode)
8) External interrupt request input : 8ch
9) GPIO : 21port (Including CPU I/F, SIO, PCM I/F, PWM/TIMER, INT2B - INT7B)
10) MIC AMP : 2ch, Gain : 30dB / 27dB / 24dB / 21dB / 18dB / 15dB / 12dB / 0dB
    Including MIC bias circuit
11) Oscillation frequency : 8.192MHz / 11.2896MHz / 12.288MHz
12) Supply Voltage : from 3.0V to 3.6V (IO, OSC, PLL), 1.5V±10% (Internal Logic)

Package

SQFP64(10mm × 10mm)



SPQFP64 10x10 / SQFP64

Figure 1

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

Semiconductor Components Industries, LLC, 2013

December, 2013

Block Diagram

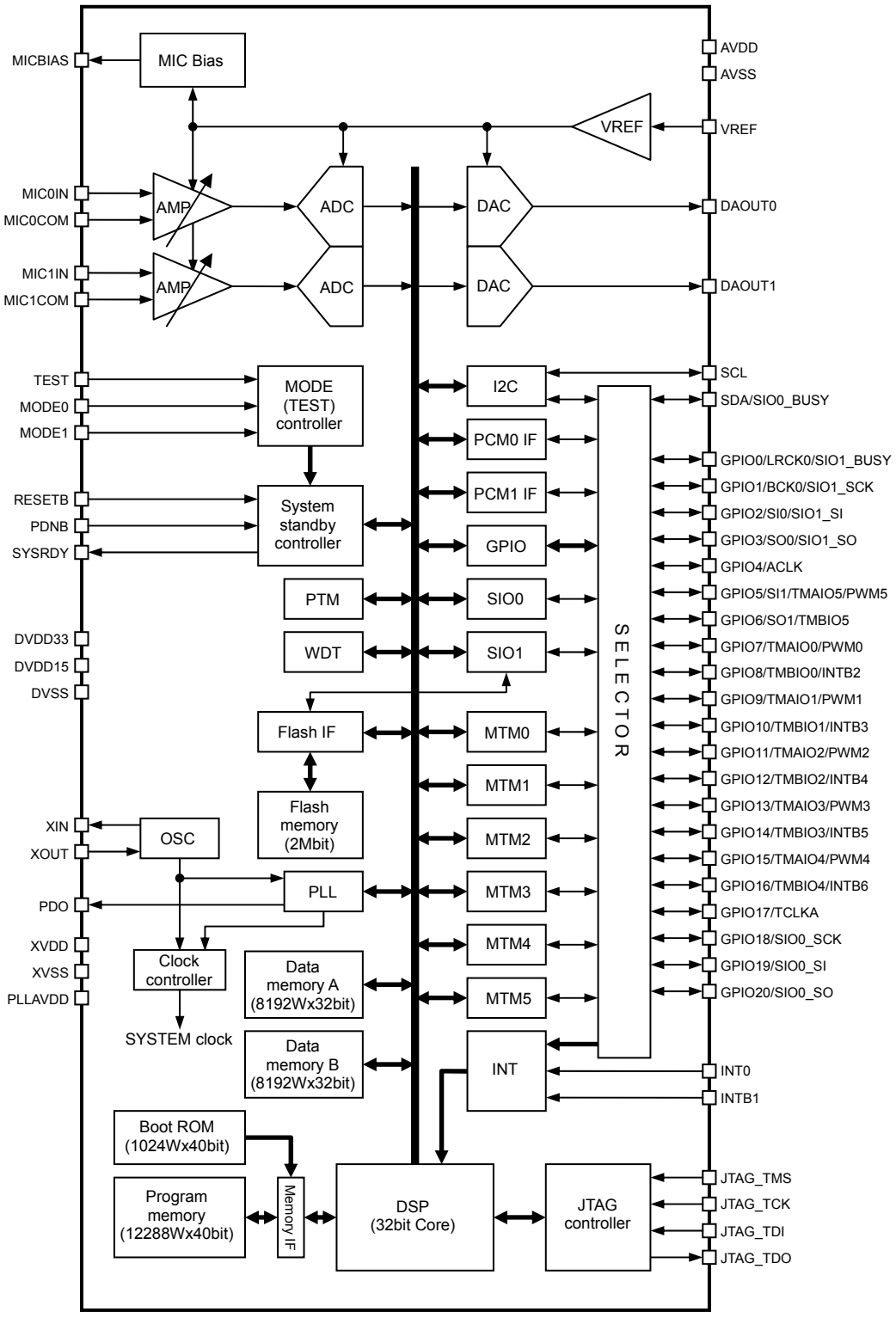


Figure 2

Pin Assignment

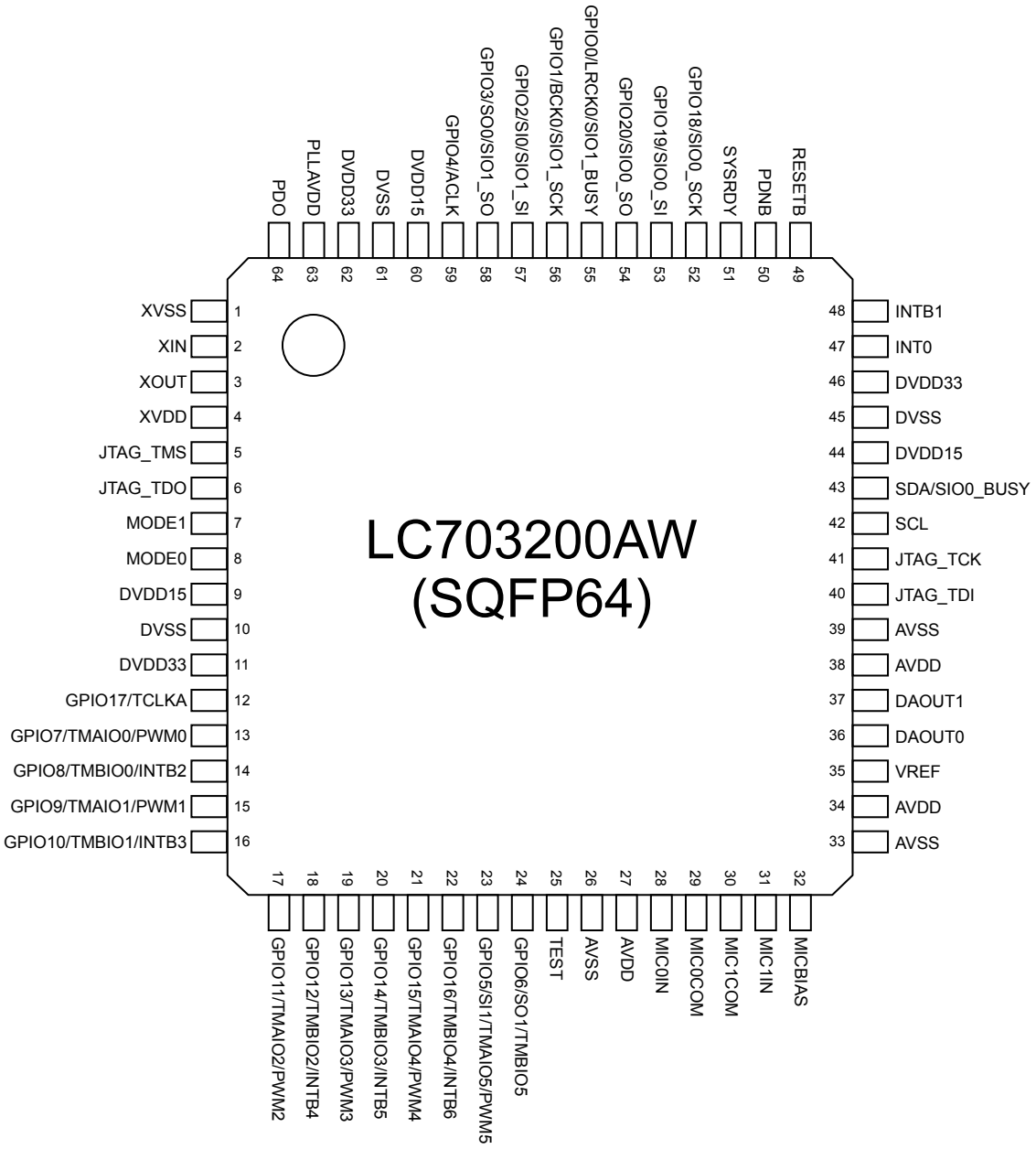


Figure 3 Pin layout

Table.1A Pin Assignment

Pin No.	Pin Name	IO	Reset Period	Standby Period	Power Supply	Function
1	XVSS	PS	-	-	GND	Oscillation circuit GND
2	XIN	DI				Oscillation circuit input
3	XOUT	DO				Oscillation circuit output
4	XVDD	PS	-	-	3.3V	Oscillation circuit 3.3V power supply
5	JTAG_TMS	DI				JTAG test mode select
6	JTAG_TDO	DO				JTAG test mode output
7	MODE1	DI				Mode setting pin 1
8	MODE0	DI				Mode setting pin 0
9	DVDD15	PS	-	-	1.5V	Digital 1.5V power supply
10	DVSS	PS	-	-	GND	Digital GND
11	DVDD33	PS	-	-	3.3V	I/O 3.3V power supply
12	GPIO17/TCLKA	DB	DI	=		GPIO17, Timer clock input
13	GPIO7/TMAIO0/PWM0	DB	DI	=		GPIO7, Timer 0A I/O, PWM0 output
14	GPIO8/TMBIO0/INTB2	DB	DI	=		GPIO8, Timer 0B I/O, Interrupt 2
15	GPIO9/TMAIO1/PWM1	DB	DI	=		GPIO9, Timer 1A I/O, PWM1output
16	GPIO10/TMBIO1/INTB3	DB	DI	=		GPIO10, Timer 1B I/O, Interrupt 3
17	GPIO11/TMAIO2/PWM2	DB	DI	=		GPIO11, Timer 2A I/O, PWM2 output
18	GPIO12/TMBIO2/INTB4	DB	DI	=		GPIO12, Timer 2B I/O, Interrupt 4
19	GPIO13/TMAIO3/PWM3	DB	DI	=		GPIO13, Timer 3A I/O, PWM3 output
20	GPIO14/TMBIO3/INTB5	DB	DI	=		GPIO14, Timer 3B I/O, Interrupt 5
21	GPIO15/TMAIO4/PWM4	DB	DI	=		GPIO15, Timer 4A I/O, PWM4 output
22	GPIO16/TMBIO4/INTB6	DB	DI	=		GPIO16, Timer 4B I/O, Interrupt 6
23	GPIO5/SI1/TMAIO5/PWM5	DB	DI	=		GPIO5, PCMIF1 SI, Timer5A I/O, PWM4 output
24	GPIO6/SO1/TMBIO5	DB	DI	=		GPIO6, PCMIF1 SO, Timer 5B I/O
25	TEST	DI	L	L		TEST pin (normally tied to low)
26	AVSS	PS	-	-	GND	Analog GND
27	AVDD	PS	-	-	3.3V	Analog 3.3V power supply
28	MIC0IN	AI				MIC input 0 (Lch)
29	MIC0COM	AI				MIC common input 0 (Lch)
30	MIC1COM	AI				MIC common input 1 (Rch)
31	MIC1IN	AI				MIC input 1 (Rch)
32	MICBIAS	AO				MIC BIAS output
33	AVSS	PS	-	-	GND	Analog GND
34	AVDD	PS	-	-	3.3V	Analog 3.3V power supply
35	VREF	AO				Analog reference voltage output
36	DAOUT0	AO				DAC output 0 (Lch)
37	DAOUT1	AO				DAC output 1 (Rch)
38	AVDD	PS	-	-	3.3V	Analog 3.3V power supply
39	AVSS	PS	-	-	GND	Analog GND
40	JTAG_TDI	DI				JTAG test data input
41	JTAG_TCK	DI				JTAG test clock
42	SCL	DB	DI	=		I2C SCL clock
43	SDA/SIO0_BUSY	DB	DI	=		I2C SDA data, SIO BUSY output
44	DVDD15	PS	-	-	1.5V	Digital 1.5V power supply
45	DVSS	PS	-	-	GND	Digital GND
46	DVDD33	PS	-	-	3.3V	I/O pin 3.3V power supply
47	INT0	DI				Interrupt 0
48	INTB1	DI				Interrupt 1
49	RESETB	DI	L	H		Reset input
50	PDNB	DI	-	L		Standby control input
51	SYSRDY	DO	L	L		System ready output
52	GPIO18/SIO0_SCK	DB	DI	=		GPIO18, SIO0 clock
53	GPIO19/SIO0_SI	DB	DI	=		GPIO19/SIO0 serial input
54	GPIO20/SIO0_SO	DB	DI	=		GPIO20/SIO0 serial output
55	GPIO0/LRCK0/SIO1_BUSY	DB	DI	=		GPIO0, PCMIF LRCK, SIO1 Busy output
56	GPIO1/BCK0/SIO1_SCK	DB	DI	=		GPIO1, PCMIF bit clock, SIO1 clock
57	GPIO2/SI0/SIO1_SI	DB	DI	=		GPIO2, PCMIF0 serial input, SIO1 serial input
58	GPIO3/SO0/SIO1_SO	DB	DI	=		GPIO3, PCMIF0 serial output, SIO1 serial output
59	GPIO4/ACLK	DB	DI	=		GPIO4, PCMIF master clock
60	DVDD15	PS	-	-	1.5V	Digital 1.5V power supply
61	DVSS	PS	-	-	GND	Digital GND
62	DVDD33	PS	-	-	3.3V	I/O 3.3V power supply
63	PLLAVDD	PS	-	-	1.5V	PLL 1.5V power supply
64	PDO	AO				PLL filter output

*) = means hold previous status.

*) TEST pins should be set to L level.

Table.1B I/O Functions

I/O Symbol	Function
DI	Digital Input
DO	Digital Output
DB	Digital Input/output
AI	Analog Input
AO	Analog Output
PS	Power Supply, GND

Electrical Characteristics

(1) Absolute Maximum Ratings

Table.2 Absolute Maximum Ratings

VSS = AVSS = XVSS = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	VDD33max	DVDD33	−0.3 to +3.96	V
	VDD15max	DVDD15	−0.3 to +1.8	
	XVDD33max	XVDD	−0.3 to +3.96	
	AVDD33max	AVDD	−0.3 to +3.96	
	AVDD15max	PLLAVDD	−0.3 to +1.8	
Input Voltage	VI	3.3V Digital I/O	−0.3 to DVDD33+0.3	
	VIA	3.3V Analog input	−0.3 to AVDD33+0.3	
Output Voltage	VO	3.3V Digital I/O	−0.3 to DVDD33+0.3	
	VOA1	3.3V Analog output	−0.3 to AVDD+0.3	
	VOA2	1.5V Analog output	−0.3 to PLLAVDD+0.3	
Allowable power dissipation	Pdmax	SQFP64 (10x10) | Ta = −30°C to +70°C	260	mW
Operating Ambient Temperature	Topr		−30 to +70	°C
Storage Ambient Temperature	Tstg		−55 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

(2) Allowable Operating Range

Table.3 Allowable Operating Range

Ta = −30°C to +70°C, VSS = AVSS = XVSS = 0V

Parameter	Symbol	Pins	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD33	DVDD33		3.0	3.3	3.6	V
	VDD15	DVDD15		1.35	1.5	1.65	
	XVDD33	XVDD		3.0	3.3	3.6	
	AVDD33	AVDD		3.0	3.3	3.6	
	AVDD15	PLLAVDD		1.35	1.5	1.65	
Input Voltage	VI33	TEST,MODE0-1, RESETB,PDNB,INT0,INTB1, GPIO0-20, SCL,SDA, JTAG_TCK,JTAG_TSM,JTAG_TDI		0	-	VDD33	
	VIA33	MIC0IN,MIC1IN, MIC0COM,MIC1COM		0	-	AVDD33	
	VIX33	XIN		0	-	XVDD33	
Oscillation Frequency	Fopr	XIN,XOUT			8.192 11.2896 12.288		MHz

*) The following relations must be satisfied during power on and power off sequence.

AVDD33 ≥ XVDD33 ≥ VDD33 ≥ AVDD15 ≥ VDD15

(3) DC Characteristics

Table.4 DC Characteristics(Digital Block)

Ta = –30°C to +70°C, VDD33 = XVDD33 = 3.0V to 3.6V, VDD15 = 1.35V to 1.65V, DVSS = XVSS = 0V

Parameter	Symbol	Pins	Conditions	Min	Typ	Max	Unit
Input “H” level voltage	VIH	TEST, MODE0-1, RESETB, PDNB, INT0, INTB1, GPIO0-20, SCL, SDA, JTAG_TCK, JTAG_TSM, JTAG_TDI		0.7VDD33	-	-	V
Input “L” level voltage	VIL			-	-	0.3VDD33	
Input “H” level current	IIH		VI=VDD33	–10	-	+10	µA
Input “L” level current	IIL		VI=VSS	–10	-	+10	
Output“H” level voltage	VOH2	SYSRDY, JTAG_TDO GPIO0-3, GPIO5-20	IOH=-2mA	VDD33–0.4	-	-	V
Output “L” level voltage	VOL2		IOL=2mA	-	-	0.4	
Output “H” level voltage	VOH4	SCL, SDA, GPIO4	IOH=-4mA	VDD33–0.4	-	-	
Output “L” level voltage	VOL4		IOL=4mA	-	-	0.4	
Output leakage current	IOZ	GPIO0-20,SCL, SDA	VO=Hi_z	-10	-	+10	µA

Table.5 DC Characteristics (Analog Block)

Ta = 25°C, AVDD33 = 3.3V, AVSS = 0V

MIC amp circuit (Analog input)							
Parameter	Symbol	Pins	Conditions	Min	Typ	Max	Unit
Input resistance	MIC_Rin	MIC0IN, MIC1IN, MIC0COM, MIC1COM	Gain = 0dB		52.8		KΩ
			Gain = 27dB		5.34		KΩ
Input voltage	MIC_Vin		Gain = 0dB Single end input			0.85AVDD33	Vp-p
			Gain = 0dB Differential input			0.425AVDD33	Vp-p
MIC amp gain	MIC_gain		MIC_GAIN=111b		30		dB
			MIC_GAIN=110b		27		dB
			MIC_GAIN=101b		24		dB
			MIC_GAIN=100b		21		dB
			MIC_GAIN=011b		18		dB
			MIC_GAIN=010b		15		dB
			MIC_GAIN=001b		12		dB
			MIC_GAIN=000b		0		dB

MIC bias circuit							
Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
MIC bias output voltage	MIC_Vbias	MICBIAS	AVDD = 3.3V		2.31		V
MIC bias output current	MIC_Ibias		@RL = 5KΩ			20	mA

ADC Block (MIC0IN / MIC1IN / MIC0COM / MIC1COM → MICAMP → ADC → SO0 / SO1(PCM-I/F))							
Parameter	Symbol	Pins	Conditions	Min	Typ	Max	Unit
Resolution	ADC_RES			-	24	-	bit
S/N	ADC_SNR		MIC_GAIN=0dB A-weighted	85	90	-	dB
			MIC_GAIN=27dB A-weighted	75	80	-	dB
Dynamic Range	ADC_DR		MIC_GAIN=0dB A-weighted	85	90	-	dB
			MIC_GAIN=27dB A-weighted	75	80	-	dB
THD+N	ADC_THD+N		MIC_GAIN=0dB	-	–86	–75	dB
			MIC_GAIN=27dB	-	–76	–72	dB
Inter channel Isolation	ADC_ISO		MIC_GAIN=0dB	-	–100	–90	dB
			MIC_GAIN=27dB	-	–90	–80	dB

DAC Block							
Parameter	Symbol	Pins	Condition	Min	Typ	Max	Unit
Resolution	DAC_RES			-	24	-	bit
S/N	DAC_SNR		A-weighted	85	90	-	dB
Dynamic Range	DAC_DR		A-weighted	85	90	-	dB
THD+N	DAC_THD+N			-	–86	–75	dB
Inter channel isolation	DAC_ISO		f=1KHz	-	–90	–85	dB
Output Voltage	DAC_VO			-	-	0.85AVDD33	Vp-p
Output load resistance	DAC_RL			10	-	-	KΩ
Output load capacity	DAC_CL			-	-	30	pF

Analog Block Reference Voltage Generator Circuit							
Parameter	Symbol	Pins	Condition	Min	Typ	Max	Unit
Reference voltage	VREF	VREF		-	1.65	-	V
Startup time (*)	ST		C=10µF	-	80	-	ms

(*) The definition of Startup time is the time VREF output reach 98% of reference voltage (= 0.98AVDD33/2) from power down release.

(4) Current Consumption

Table.6 Current consumption

Ta= –30°C to +70°C,VDD33 = XDD33 = AVDD33 = 3.0V to 3.6V, VDD15 = 1.35V to 1.65V, VSS = XVSS = AVSS = 0V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby current (*)	IDDS	Sum of VDD33, XVDD33, VDD15, AVDD33, PLLAVDD		10		μA
Current consumption(**)	IDD15D	Digital 1.5V for Logic		24		mA
	IDD15A	Analog 1.5V for PLL		1		mA
	IDD33D	Digital 3.3V for IO, XVDD		1		mA
	IDD33A	Analog 3.3V		14		mA
	IDD	Total		40		mA

(*) Both oscillation and PLL halt

(**) The value is example that the LSI executes noise cancel processing at 50MHz system clock.

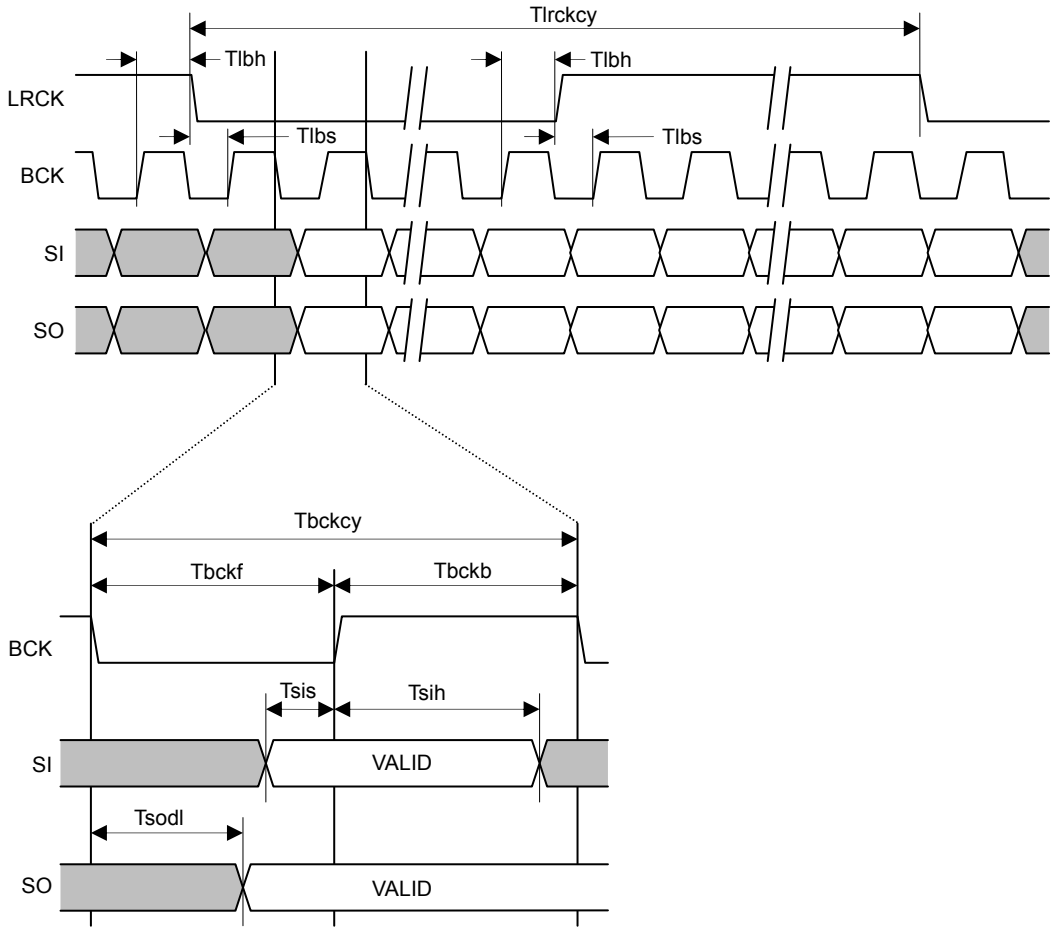
AC characteristics

(1) PCM Interface

I^2S Format

Parameter	Symbol	Min	Typ	Max	Unit
LRCK period	Tlrckcy	-	1/Fs	-	nS
LRCK setup time	Tlrs	3Tsys+2	-	-	nS
LRCK hold time	Tlrh	Tsys+2	-	-	nS
BCK period	Tbckcy	-	1/32Fs or 1/64Fs	-	nS
BCK period(1st half)	Tbckf	3Tsys	-	-	nS
BCK period(2nd half)	Tbckb	3Tsys	-	-	nS
SI setup time	Tsis	15	-	-	nS
SI hold time	tsih	2Tsys+5	-	-	nS
SO delay	Tsodl	2Tsys+29	-	-	nS

*) Tsys is system clock frequency.
*) Fs is sampling frequency.

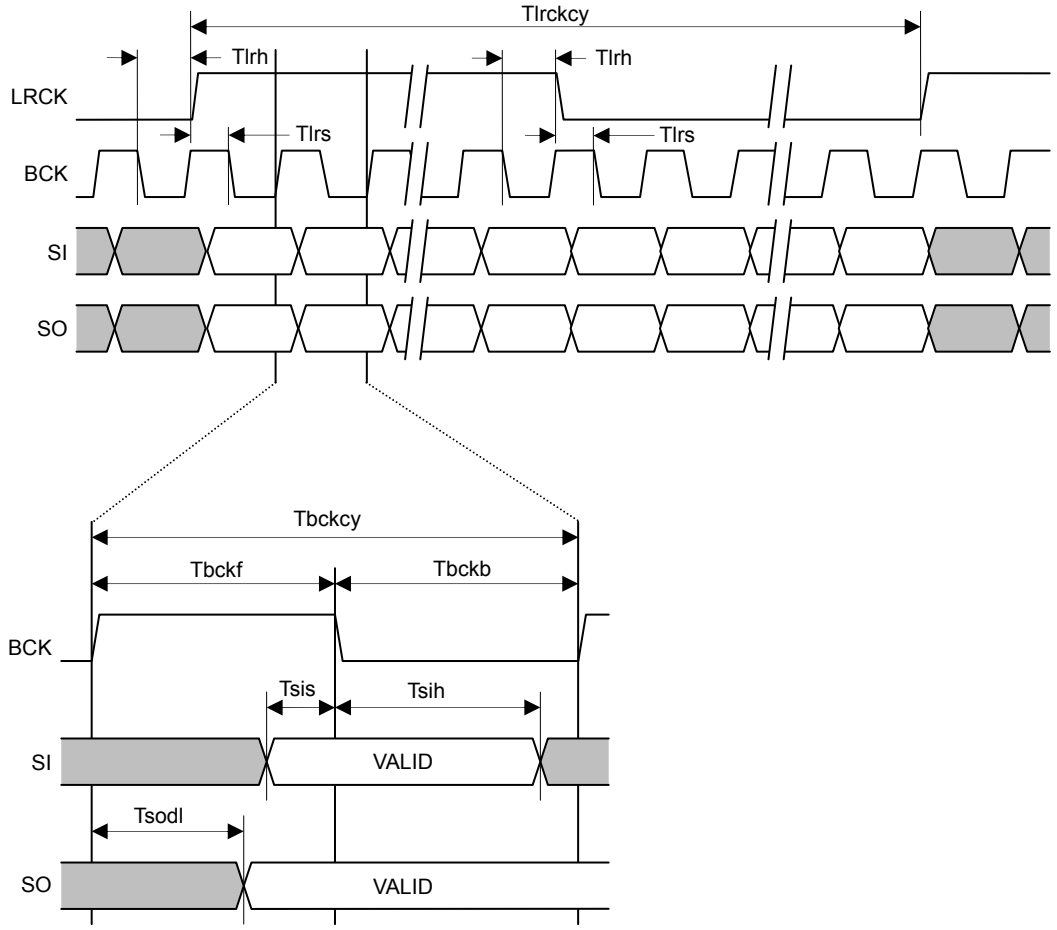


PCM format

Parameter	Symbol	Min	Typ	Max	Unit
LRCK period	Tlrckcy	-	1/Fs	-	nS
LRCK setup time	Tlrs	3Tsys+2	-	-	nS
LRCK hold time	Tlrh	Tsys+2	-	-	nS
BCK period	Tbckcy	-	1/(32Fs) or 1/(64Fs)	-	nS
BCK period(1st half)	Tbckf	3Tsys	-	-	nS
BCK period(2nd half)	Tbckb	3Tsys	-	-	nS
SI setup time	Tsis	15	-	-	nS
SI hold time	tsih	2Tsys+5	-	-	nS
SO delay	Tsodl	2Tsys+29	-	-	nS

*) Tsys is system clock frequency.

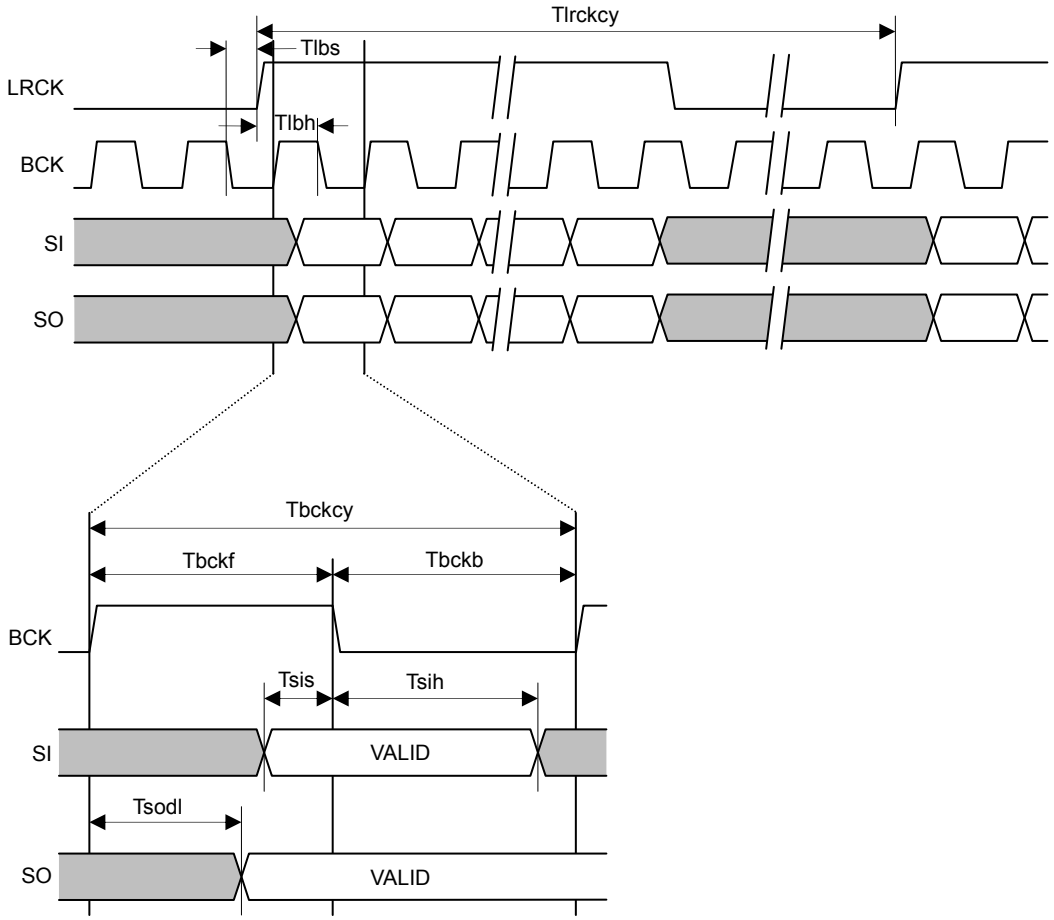
*) Fs is sampling frequency.



Long flame synchronous format

Parameter	Symbol	Min	Typ	Max	Unit
LRCK period	Tlrckcy	-	1/Fs	-	nS
LRCK setup time	Tlrs	3Tsys+2	-	-	nS
LRCK hold time	Tlrh	Tsys+2	-	-	nS
BCK period	Tbckcy	-	1/(32Fs) or 1/(64Fs)	-	nS
BCK period (1st half)	Tbckf	3Tsys	-	-	nS
BCK period (2nd half)	Tbckb	3Tsys	-	-	nS
SI setup time	Tsis	15	-	-	nS
SI hold time	tsih	2Tsys+5	-	-	nS
SO delay	Tsodl	2Tsys+29	-	-	nS

*) Tsys is system clock frequency.
*) Fs is sampling frequency.

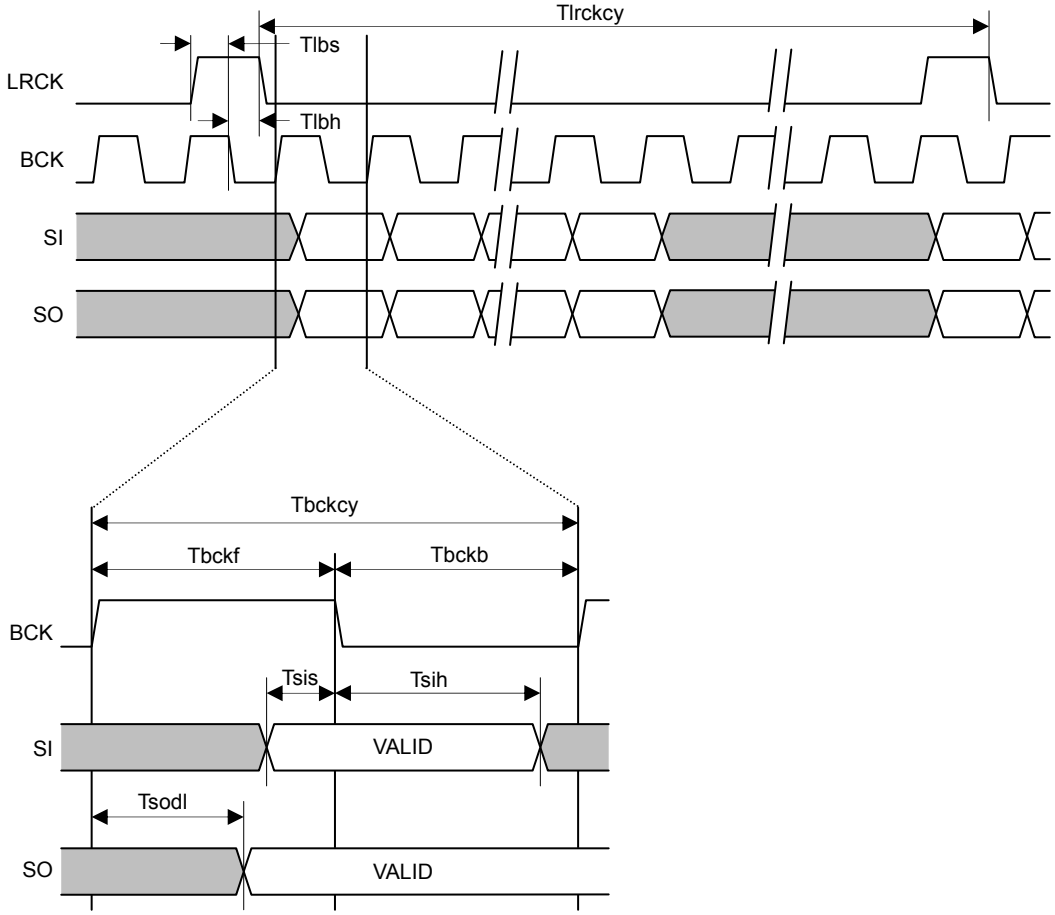


Short frame synchronous format

Parameter	Symbol	Min	Typ	Max	Unit
LRCK period	Tlrckcy	-	1/Fs	-	nS
LRCK setup time	Tlrs	3Tsys+2	-	-	nS
LRCK hold time	Tlrh	Tsys+2	-	-	nS
BCK period	Tbckcy	-	1/(32Fs) or 1/(64Fs)	-	nS
BCK period (1st half)	Tbckf	3Tsys	-	-	nS
BCK period (2nd half)	Tbckb	3Tsys	-	-	nS
SI setup time	Tsis	15	-	-	nS
SI hold time	tsih	2Tsys+5	-	-	nS
SO delay	Tsodl	2Tsys+29	-	-	nS

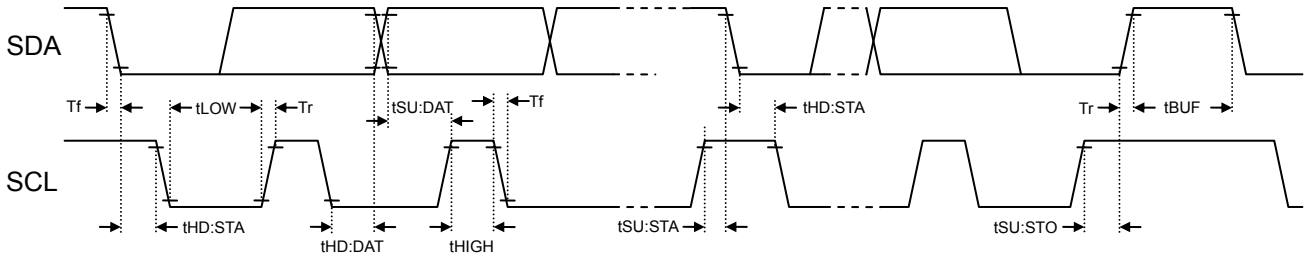
*) Tsys is system clock frequency.

*) Fs is sampling frequency.



(2) I^2C Interface

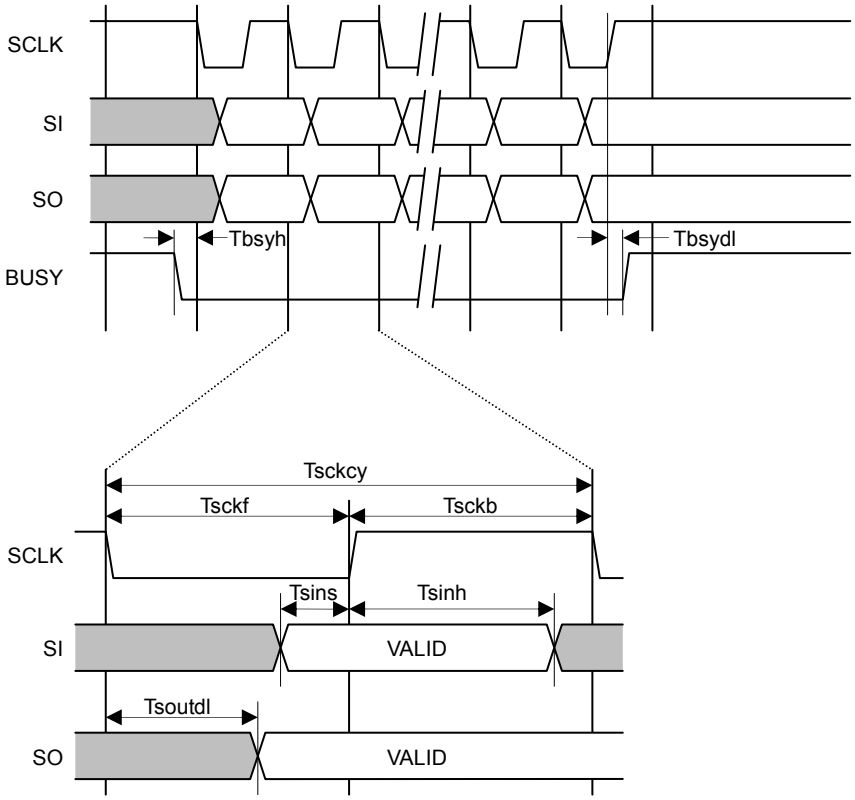
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCL frequency	fSCL	0	100	0	400	kHz
Hold time (repeated) START condition	tHD;STA	4.0	-	0.6	-	μS
Low period of SCL clock	tLOW	4.7	-	1.3	-	μS
High period of SCL clock	tHIGH	4.0	-	0.6	-	μS
Setup time for a repeated Start condition	tSU;STA	4.7	-	0.6	-	μS
Data hold time	tHD;DAT	0	3.45	0	0.9	μS
Data setup time	tSU;DAT	250	-	100	-	nS
Rise time of both SDA and SCL signals	Tr	-	1000	-	300	nS
Fall time of both SDA and SCL signals	Tf	-	300	-	300	nS
Setup time for STOP condition	tSU;STO	4.0	-	0.6	-	μS
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	μS



(3) SIO Interface

Parameter	Symbol	Min	Typ	Max	Unit
SCLK period	Tsckcy	8Tsys	-	-	nS
SCLK period (1st half)	Tsckf	3Tsys	-	-	nS
SCLK period (2nd half)	Tsckb	3Tsys	-	-	nS
SI setup time	Tsins	0	-	-	nS
SI hold time	Tsinh	2Tsys+5	-	-	nS
SO delay	Tsoutdl	-	-	2Tsys+27	nS
BUSY-SCLK hold time	Tbsyh	0	-	-	nS
BUSY output delay	Tbsydl	-	-	2Tsys+27	nS

*) Tsys is system clock period.



(4) Timer (MTM)

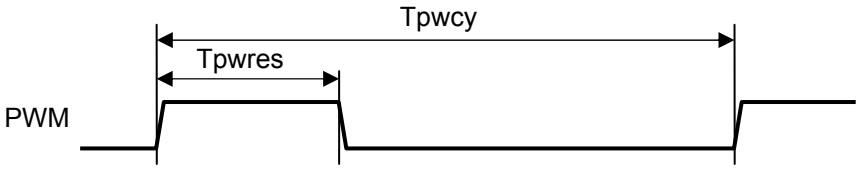
Parameter	Symbol	Min	Typ	Max	Unit
Timer resolution	Ttmres	3Tmtm	-	65536Tmtm	nS
Timer period	Tleng	Ttmres	-	65536Ttmres	nS

*) Tmtm is MTM clock period and selectable between OSC clock and PLL clock.

(5) PWM (MTM)

Parameter	Symbol	Min	Typ	Max	Unit
PWM resolution	Tpwres	3Tmtm	-	65536Tmtm	nS
PWM period	Tpwcy	Tpwres	-	65536Tpwres	nS

*) Tmtm is MTM clock period and selectable between OSC clock and PLL clock.



(6) Timer (PTM)

Parameter	Symbol	Min	Typ	Max	Unit
Timer resolution	Tptres	Tosc	-	8Tosc	nS
Timer period	Tptcy	Tptres	-	65536Tptres	nS

*) Tosc is OSC clock period.

(7) WDT

Parameter	Symbol	Min	Typ	Max	Unit
WDT period	Twdcy	131072Tosc	-	268435456Tosc	nS

*) Tosc is OSC clock period.

(8) System clock/Reset

Table.7 System clock

VDD = XVDD = 3.0V to 3.6V, VSS = XVSS = 0V, Ta = -30°C to +70°C

Parameter	Symbols	Condition	Min	Typ	Max	Unit
Oscillation frequency	fop		-	8.192 11.2896 12.288	-	MHz

*) Recommended Oscillator

Murata Manufacturing Co., Ltd.

CERALOCK© : CSTCE8M19G55-R0 (8.192MHz)
CSTCE11M2896G55-R0 (11.2896MHz)
CSTCE12M288G55-R0 (12.288MHz)

Table.8 System clock and sampling frequency

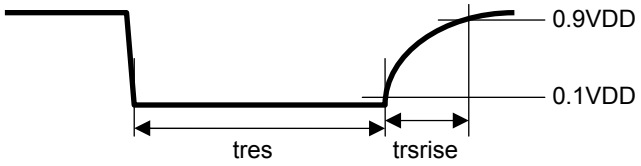
Relationship between system clock and sampling frequency

System clock (MHz)	Sampling frequency (KHz)			comment
8.192	32	16	8	
11.2896	44.1	22.05	11.025	
12.288	48	24	12	

Table.9 Reset

VDD = XVDD = 3.0V to 3.6V, VSS = XVSS = 0V, Ta = –30°C to 70°C

Parameter	Symbol	Min	Typ	Max	Unit
Hold time of Reset	tres	500	-	-	μs
Rising time of Reset	trsrise	1			mS



Power Supply

LC703200AW has a power supply of two kinds of voltage of 3.3V and 1.5V, and it is necessary to maintain the following power requirement to power on / off.

Power requirement

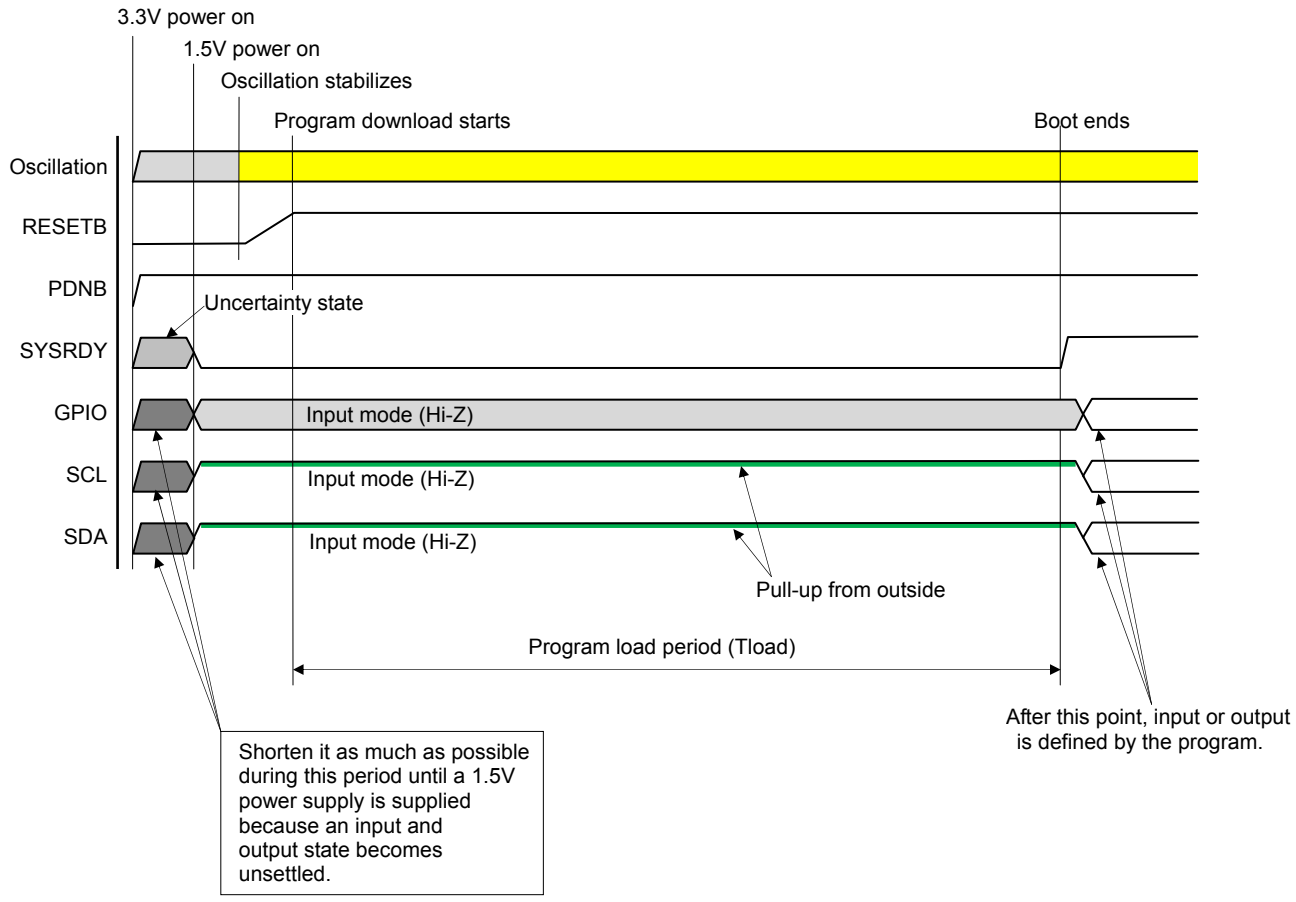
•The power supply to belong to same voltage system start supply at the same time.
3.3V power supply: AVDD33, XVDD33, VDD33
1.5V power supply: AVDD15, VDD15

•The voltage of the power supply of the 3.3V preventing you from being less than the voltage of the power supply of the 1.5V under any circumstance.
Specialy, when the power supply on / off, be careful the period of the voltage rise / fall.

•Reducing time difference as much as possible when I make time difference between voltage system and perform power supply on / off.
Listing not to intend may affect the external circuit without the state (input /"L" listing /"H" listing) of a terminal (GPIO, SCL, SDA) having an input and output function being settled because 1.5V system is a state of non-supply after a setup in 3.3V system, and a system reset signal does not arrive at it inside.

Startup sequence

LC703200AW starts a program stored away by built-in flash memory after download in program memory. Each terminal pin state sequence at the time of the start is a street of the chart belows.



*) It is as follows during the period required for a program road.

$$Tload = \frac{2384 + word * 706}{OSC * 1000}$$

Tload : Program load period [mS]

word : Program size [word length]

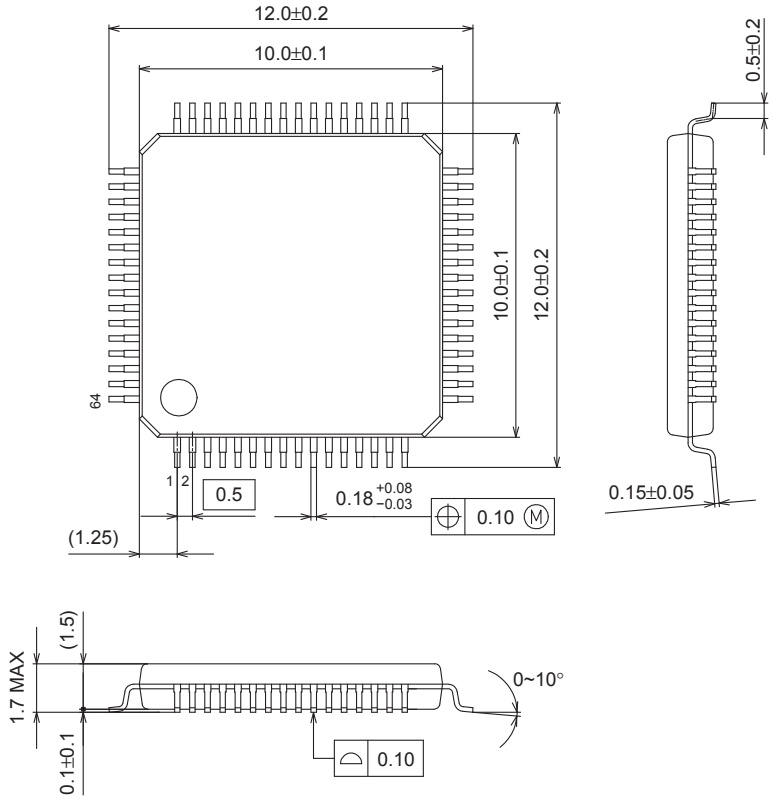
OSC : Osccilation frequency [MHz]

(1word length = 40bit)

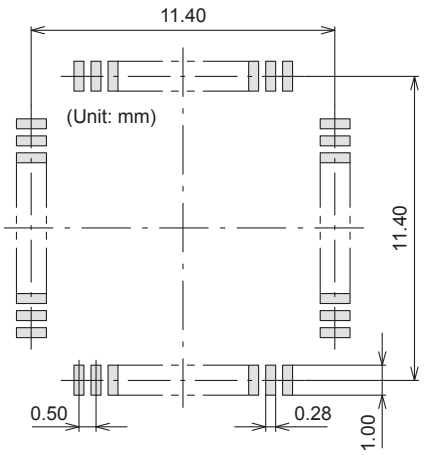
Package Dimensions

unit : mm

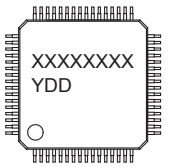
SPQFP64 10x10 / SQFP64
CASE 131AK
ISSUE A



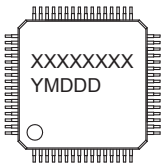
SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC703200AW-8C99-H	SPQFP64 10x10 / SQFP64 (Pb-Free / Halogen Free)	500 / Tray Foam

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