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LC74736PT

CMOS IC

On-Screen Display Controller

ON Semiconductor®

http://onsemi.com

Overview

The LC74736PT is an on-screen display CMOS IC that displays characters and patterns on a TV screen under the control of a microcontroller.
For QVGA display, the LC74736PT supports the use of both a 16 × 16 dot character font and a 16 × 16 dot graphic font with 16 colors.
For WVGA display, the LC74736PT supports the use of both a 24 × 32 dot character font and a 24 × 32 dot graphic font with 16 colors.
The LC74736PT can also implement extremely varied displays by the use of an external ROM.
The LC74736PT supports both QVGA (480×234) and WVGA (800×480).

Features

(1) Screen structure
- Main: 2 screens (1 screen for WVGA display)
  - 30 characters×15 lines (up to 450 characters) on a QVGA panel
  - 33 characters×15 lines (up to 495 characters) on a WVGA panel
  - (Up to 34 characters×18 lines)
- Wallpaper display screen:
  - QVGA mode: maximum Permanent repetition of a 4×4 (horizontal×vertical) character pattern
  - WVGA mode: maximum Permanent repetition of a 2×2 (horizontal×vertical) character pattern

(2) Character structure
QVGA mode: About 9MHz
16 dots (horizontal) ×16 dots (vertical): Character display
16 dots (horizontal) ×16 dots (vertical): Graphic glyph display
WVGA mode: About 33.2MHz
24 dots (horizontal) ×32 dots (vertical): Character display
24 dots (horizontal) ×32 dots (vertical): Graphic glyph display
Character display clock:
LC oscillator (about 10MHz)
External clock signal input (up to 40MHz)
Built-in PLL (VCO) (7 to 40MHz)

(3) Number of characters
QVGA mode
Up to 16384 characters when an external 16-bit 16M ROM is used.
WVGA mode
Up to 4096 characters when an external 16-bit 16M ROM is used.
No internal ROM
Internal character RAM QVGA: 4 characters, WVGA: 1 character

(4) Character sizes: Four horizontal sizes (1×, 2×, 3×, and 4×)
Four vertical sizes (1×, 2×, 3×, and 4×)
(The character size is specified in line units.)

(5) Display start positions: 1024 positions in the horizontal direction and 512 positions in the vertical direction.
Setting units: Horizontal: 1 dot (in screen units)
Vertical: 1 dot (in screen units)

(6) Display functions
- Blinking specification (in character units)
  Period: 1/64, 1/32, and 1/16 of the vertical sync signal (in screen units)
  Duty: Fixed at 50%
- Box (raised or recessed) display
  Raised/recessed specification (in character units)
  Left: Off/on specification (in character units)
  Right: Off/on specification (in character units)
  Top: Off/on specification (in character units)
  Bottom: Off/on specification (in character units)
- Border specification (in line units): Only valid with glyphs from the character font.

(7) Color specification
Character
- Character color (in character units): 1 of 16 colors can be specified.
- Character background color (in character units): 1 of 16 colors can be specified.
- Border color (in line units): 1 of 16 colors can be specified.

Graphic
- 16 types can be specified by ROM data

Graphic 2
- 16 types can be specified by ROM data
  1 color type can be changed.

Graphic 3
- 16 types can be specified by ROM data
  1 color table type can be changed.
- Box (raised or recessed) color (line units): 1 of 16 colors can be specified.
- Background color (screen units): 1 of 16 colors can be specified.

(8) Color table (palette)
- Sixteen colors can be selected from a set of 4096 colors (One of which is specified to be transparent.)
- Number of color tables: 4. This allows up to 64 colors to be displayed at the same time.

(9) Wallpaper screen (Graphics glyphs only)
Wallpaper display: Repeated display under the main screen
(up to 4 characters horizontally by 4 characters vertically).
Sprite character display: Displayed above the main screen
(up to 4 characters horizontally by 4 characters vertically).

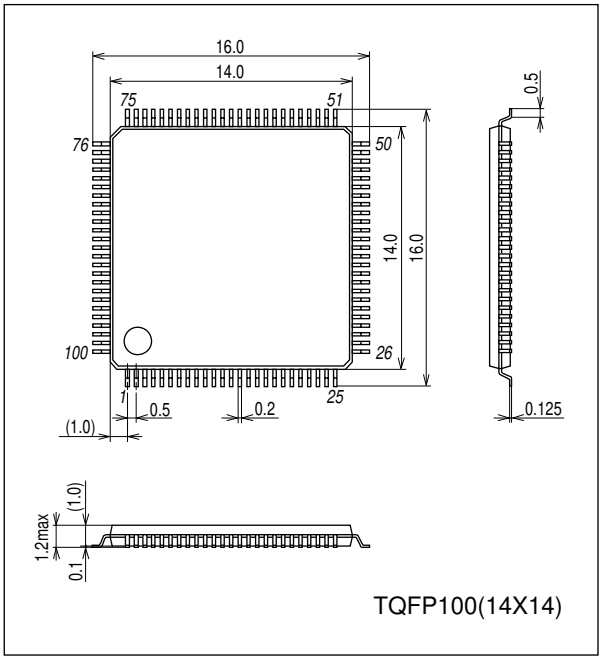
(10) Line spacing control
0-15 scan lines (in line units)

(11) Output
Analog RGB output(to 20MHz)
Digital RGB output (4 bits per color)
BLK (OSD display period signal)

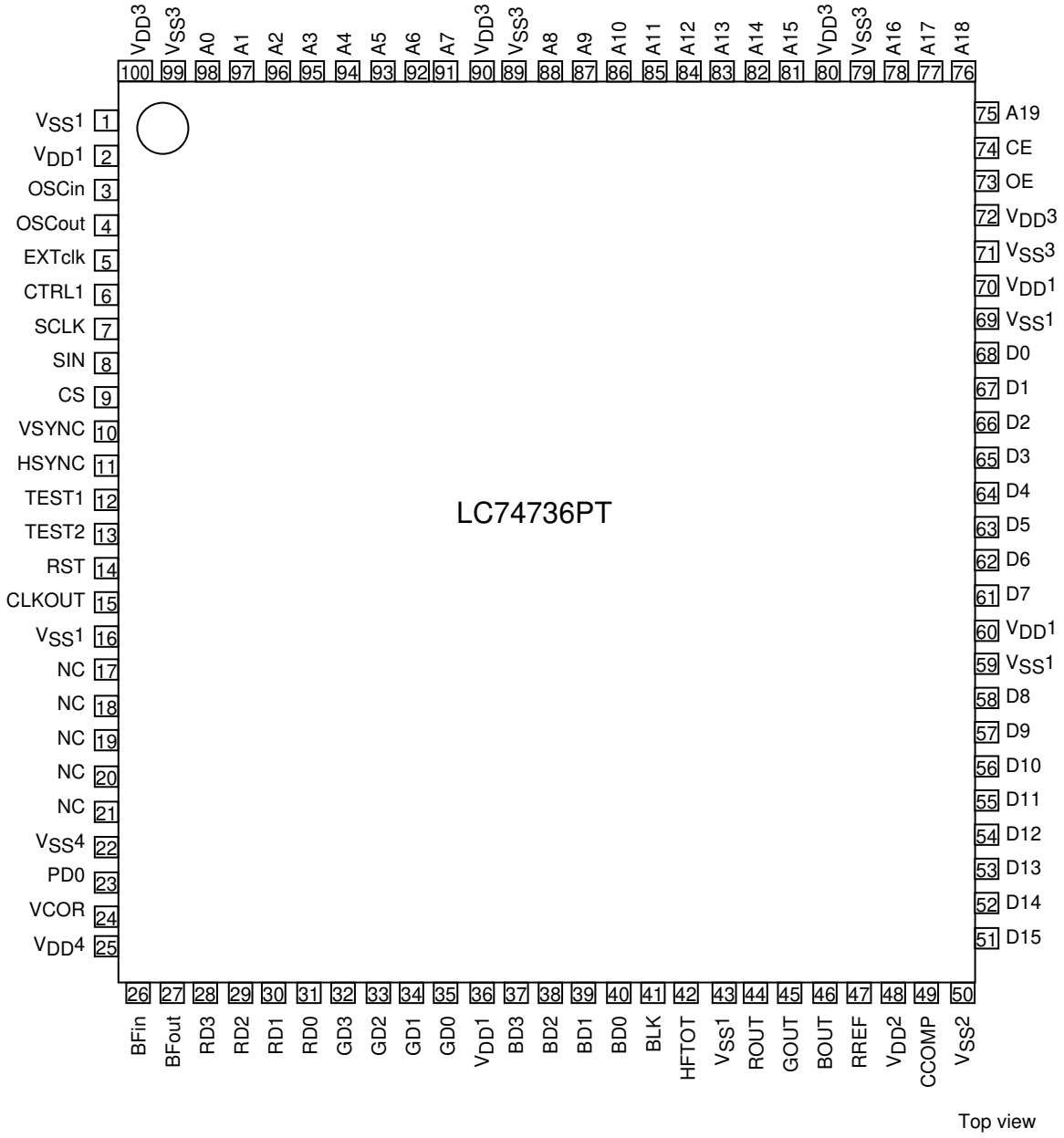
Package: TQFP100
Voltage: 3.3V

Package Dimensions

unit : mm (typ)
3274



Pin Assignment



Top view

Pin Functions

Pin No.	Symbol	Type	Functional description
1	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
2	$V_{DD}1$	Power supply (+3.3V)	Digital system power supply: +3.3V
3	OSCin	LC oscillator	Connect to the character output dot clock generator oscillator coil and capacitor.
4	OSCout		
5	EXTclk	External clock signal input	Receives an external clock signal. Capacitor coupling, 50% duty cycle, 0.5Vp-p or higher
6	CTRL1	OSCin oscillator input control	Switches between external clock input mode and LC oscillator mode. Low: LC oscillator, high: external clock input MORE+ OR control with MORE+ command
7	SCLK	Clock input	Clock input for the serial data input system MORE+ (This input has hysteresis characteristics.)
8	SIN	Data input	Serial data input MORE+ (This input has hysteresis characteristics.)
9	$\overline{CS}$	Enable input	Enable input for the serial data input system. Serial data input is enabled when this pin is set low. MORE+ (This input has hysteresis characteristics.)
10	VSYNC	Vertical sync signal input	Vertical sync signal input MORE+ (This input has hysteresis characteristics.)
11	HSYNC	Horizontal sync signal input	Horizontal sync signal input MORE+ (This input has hysteresis characteristics.)
12	TEST1	Test mode control 1	Test mode control 1 Low: normal operation, high: test mode MORE+
13	TEST2	Test mode control 2	Test mode control 2 Low: normal operation, high: test mode (scan mode) MORE+
14	$\overline{RST}$	Reset input	System reset input MORE+ (This input has hysteresis characteristics.)
15	CLKOUT	Clock output	Clock output
16	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
17	NC		
18	NC		
19	NC		
20	NC		
21	NC		
22	$V_{SS}4$	Ground	Connect a ground tro this pin. (PLL system power supply)
23	PD0	PLL charge pump output PLL VCO control voltage input	Charge pump output Connect a LPF (lug lead filter) to this pin. Voltage input for internal VCO control
24	VCOR	VCO variable range adjustment	Used to adjust variable voltage range of internal VCO. Connect a resistor to this pin.
25	$V_{DD}4$	Power supply (+3.3V)	PLL system power supply: +3.3V
26	BFin	Amplifier input	Oscillation input for external VCO
27	BFout	Amplifier output	Oscillation output for external VCO
28	RD3	Rout output: bit 3	Rout output This is a 4-bit digital output with values from 0000 to 1111.
29	RD2	Rout output: bit 2	
30	RD1	Rout output: bit 1	
31	RD0	Rout output: bit 0	
32	GD3	Gout output: bit 3	Gout output This is a 4-bit digital output with values from 0000 to 1111.
33	GD2	Gout output: bit 2	
34	GD1	Gout output: bit 1	
35	GD0	Gout output: bit 0	
36	$V_{DD}1$	Power supply (+3.3V)	Digital system power supply: +3.3V

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Pin No.	Symbol	Type	Functional description
37	BD3	Bout output: bit 3	Bout output This is a 4-bit digital output with values from 0000 to 1111.
38	BD2	Bout output: bit 2	
39	BD1	Bout output: bit 1	
40	BD0	Bout output: bit 0	
41	BLK	Blanking signal output	This signal indicates the OSD display period.
42	HFTOT	Halftone control signal output	OSD halftone period control signal Synthesized in the next stage IC.
43	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
44	Rout	Rout output: analog	D/A converter (4 bits) output. Connect a resistor Ro to this pin.
45	Gout	Gout output: analog	D/A converter (4 bits) output. Connect a resistor Ro to this pin.
46	Bout	Bout output: analog	D/A converter (4 bits) output. Connect a resistor Ro to this pin.
47	RREF	Reference resistor connection	Connect a reference register to this pin.
48	$V_{DD}2$	Power supply (+3.3V)	D/A converter power supply: +3.3V
49	CCOMP	Phase correction capacitor connection	Capacitor connection: 1.5µF
50	$V_{SS}2$	Ground	Connect a ground to this pin. (D/A converter ground)
51	D15	Data input 15	ROM data input 15. MORE+ [MSB]
52	D14	Data input 14	ROM data input 14. MORE+
53	D13	Data input 13	ROM data input 13. MORE+
54	D12	Data input 12	ROM data input 12. MORE+
55	D11	Data input 11	ROM data input 11. MORE+ [MSB]
56	D10	Data input 10	ROM data input 10. MORE+
57	D9	Data input 9	ROM data input 9. MORE+
58	D8	Data input 8	ROM data input 8. MORE+
59	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
60	$V_{DD}1$	Power supply (+3.3V)	Digital system power supply: +3.3V
61	D7	Data input 7	ROM data input 7. MORE+
62	D6	Data input 6	ROM data input 6. MORE+
63	D5	Data input 5	ROM data input 5. MORE+
64	D4	Data input 4	ROM data input 4. MORE+
65	D3	Data input 3	ROM data input 3. MORE+
66	D2	Data input 2	ROM data input 2. MORE+
67	D1	Data input 1	ROM data input 1. MORE+
68	D0	Data input 0	ROM data input 0. MORE+ [LSB][LSB]
69	$V_{SS}1$	Ground	Connect a ground to this pin. (Digital system ground)
70	$V_{DD}1$	Power supply (+3.3V)	Power supply: (+3.3V: Digital system)
71	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
72	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)
73	$\overline{OE}$	Output enable	ROM output enable output. This is an active low output.
74	$\overline{CE}$	Chip enable	ROM chip enable output. This is an active low output.
75	A19	Address output 19	ROM address output 19
76	A18	Address output 18	ROM address output 18
77	A17	Address output 17	ROM address output 17
78	A16	Address output 16	ROM address output 16
79	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
80	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)
81	A15	Address output 15	ROM address output 15
82	A14	Address output 14	ROM address output 14
83	A13	Address output 13	ROM address output 13
84	A12	Address output 12	ROM address output 12
85	A11	Address output 11	ROM address output 11

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Pin No.	Symbol	Type	Functional description
86	A10	Address output 10	ROM address output 10
87	A9	Address output 9	ROM address output 9
88	A8	Address output 8	ROM address output 8
89	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
90	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)
91	A7	Address output 7	ROM address output 7
92	A6	Address output 6	ROM address output 6
93	A5	Address output 5	ROM address output 5
94	A4	Address output 4	ROM address output 4
95	A3	Address output 3	ROM address output 3
96	A2	Address output 2	ROM address output 2
97	A1	Address output 1	ROM address output 1
98	A0	Address output 0	ROM address output 0
99	$V_{SS}3$	Ground	Connect a ground to this pin. (External ROM output system ground)
100	$V_{DD}3$	Power supply (+3.3 or +5.5V)	Power supply (External ROM output system power supply)

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}1$	$V_{DD}1$,$V_{DD}2$, and $V_{DD}4$	V_{SS}-0.3 to V_{SS}+4.6	V
	$V_{DD}3$	$V_{DD}3$	V_{SS}-0.3 to V_{SS}+6.0	V
Input voltage	V_{IN}	All input pins	V_{SS}-0.3 to $V_{DD}1$+0.3	V
Output voltage	$V_{OUT}1$	RD3 to RD0, GD3 to GD0, BD3 to BD0, BLK, HFTOT outputs	V_{SS}-0.3 to $V_{DD}1$+0.3	V
	$V_{OUT}2$	A0 to 19, $\overline{CE}$, $\overline{OE}$ outputs	V_{SS}-0.3 to $V_{DD}3$+0.3	V
Maximum power dissipation	Pd max		275	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$, 2, and $V_{DD}4$	3.0	3.3	3.6	V
	$V_{DD}3$	$V_{DD}3$	3.0	3.3	5.5	V
Input high-level voltage	$V_{IH}1$	CTRL1, TEST1, TEST2	0.7$V_{DD}1$		5.5	V
	$V_{IH}2$	SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC, $\overline{RST}$	0.8$V_{DD}1$		5.5	V
	$V_{IH}3$	D0 to D15	0.7$V_{DD}1$		5.5	V
Input low-level voltage	$V_{IL}1$	CTRL1, TEST1, TEST2	V_{SS}-0.3		0.3$V_{DD}1$	V
	$V_{IL}2$	SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC, $\overline{RST}$	V_{SS}-0.3		0.2$V_{DD}1$	V
	$V_{IH}3$	D0 to D11	V_{SS}-0.3		0.3$V_{DD}1$	V
Oscillator frequency (LC)	FOSC1	OSCin and OSCout oscillator pins (LC oscillator)		10		MHz
External clock input	FOSC2	OSCin, $V_{DD}1$ = 3.3V		33	40	MHz
	$V_{IN}1$	$V_{DD}1$ = 3.3V CTRL1 = high	0.5		3.3	Vp-p
Oscillator frequency (VCO)	FOSC3	VCO oscillator (internal)	7		40	MHz
D/A converter (4-bit, 3 ch) When maximum output voltage = 0.7V	Vrefda	Reference voltage		1.1		V
	Rfda	Output load resistance ROUT, GOUT, BOUT	120		225	Ω
	Rref	Reference load resistance, RREF		1100		Ω

Electrical Characteristics at Ta = -40 to +85°C, V_{DD} = 3.3V unless otherwise specified

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Output high-level voltage	$V_{OH}1$	RD3 to RD0, GD3 to GD0, BD3 to BD0, BLK, and HFTOT outputs	$V_{DD}1$ = 3.0V $I_{OH}1$ = -8mA	$V_{DD}1$ -0.8			V
	$V_{OH}2$	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 3.0V $I_{OH}2$ = -8mA	$V_{DD}3$ -0.8			V
	VOH3	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 4.5V $I_{OH}3$ = -8mA	$V_{DD}3$ -0.8			V
Output low-level voltage	$V_{OL}1$	RD3 to RD0, GD3 to GD0, BD3 to BD0, BLK, and HFTOT outputs	$V_{DD}1$ = 3.0V $I_{OL}1$ = 8mA			0.4	V
	$V_{OL}2$	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 3.0V $I_{OL}2$ = 8mA			0.4	V
	$V_{OL}3$	A0 to A19, $\overline{CE}$, and $\overline{OE}$	$V_{DD}3$ = 4.5V $I_{OL}3$ = 8mA			0.4	V
Input current	$I_{IH}1$	CTRL1, TEST1, TEST2 SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC, $\overline{RST}$	V_{IN} = $V_{DD}1$			10	µA
	$I_{IH}2$	D0 to D15	V_{IN} = $V_{DD}3$			10	µA
	$I_{IL}1$	CTRL1, TEST1, TEST2 SCLK, SIN, $\overline{CS}$, VSYNC, HSYNC	V_{IN} = V_{SS}	-10			µA
	$I_{IL}2$	D0 to D15	V_{IN} = V_{SS}	-10			µA
Operating current drain	$I_{DD}1$	$V_{DD}1$	All outputs open OSCin: 20MHz			25	mA
	$I_{DD}2$	$V_{DD}2$	D/A on			22	mA
	$I_{DD}3$	$V_{DD}3$				10	mA
	$I_{DD}4$	$V_{DD}4$	VCO on			22	mA
D/A converter	CLK	Clock frequency				20	MHz
	V max	Maximum output voltage	$V_{DD}2$ = 3.3V	0.25		1.5	V
	V min0	Minimum output voltage	$V_{DD}2$ = 3.3V		0		V

Timing Characteristics

OSD Write (See figure 1.) at Ta = -40 to +85°C, $V_{DD}1$ = 3.3V ± 0.3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	t_w(sclk)	SCLK	200			ns
	t_w(cs)	$\overline{CS}$ (The period $\overline{CS}$ is high)	1			µs
Data setup time	t_{su}(cs)	$\overline{CS}$	200			ns
	t_{su}(sin)	SIN	200			ns
Data hold time	t_h(cs)	$\overline{CS}$	2			µs
	t_h(sin)	SIN	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	RAM data write time	1			µs

Supplementary Materials

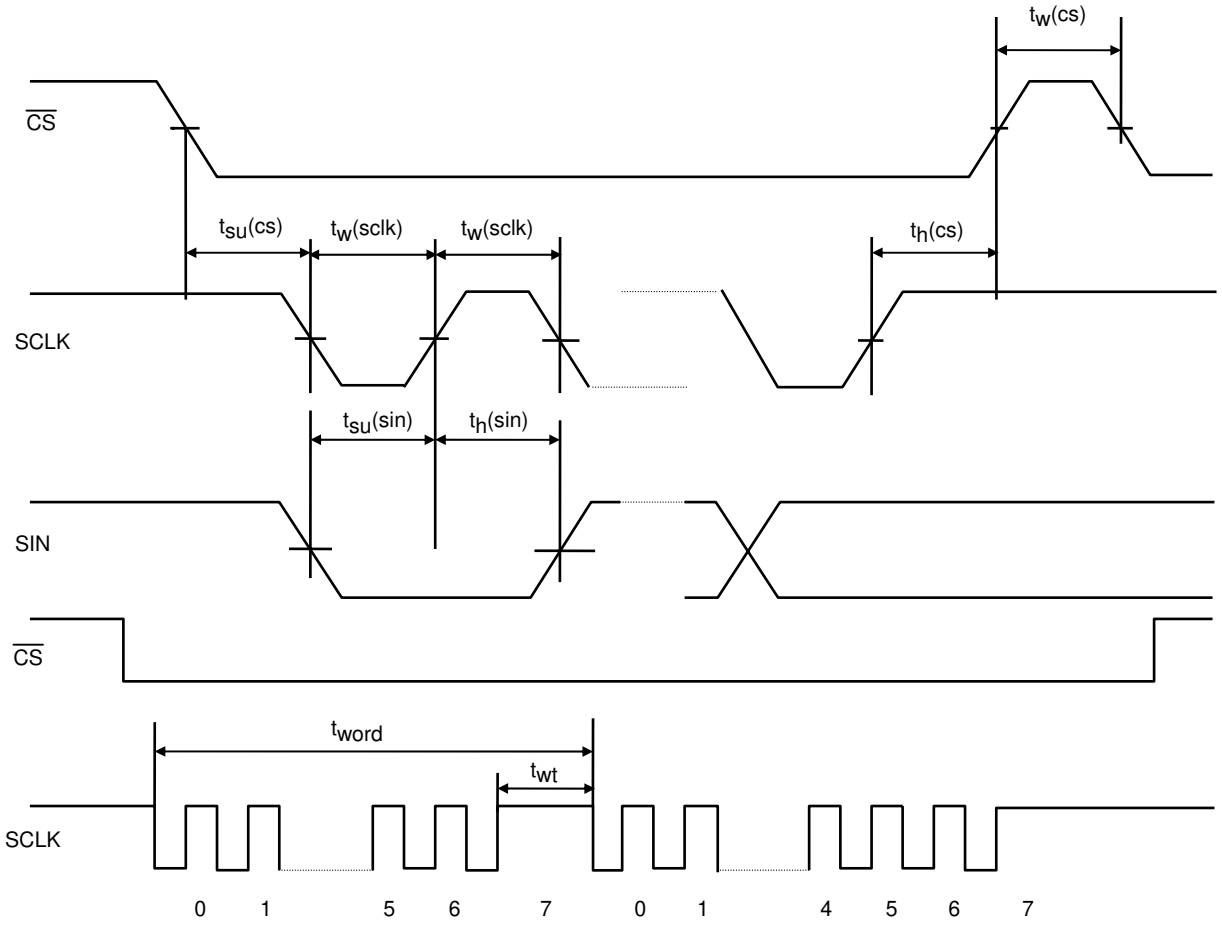
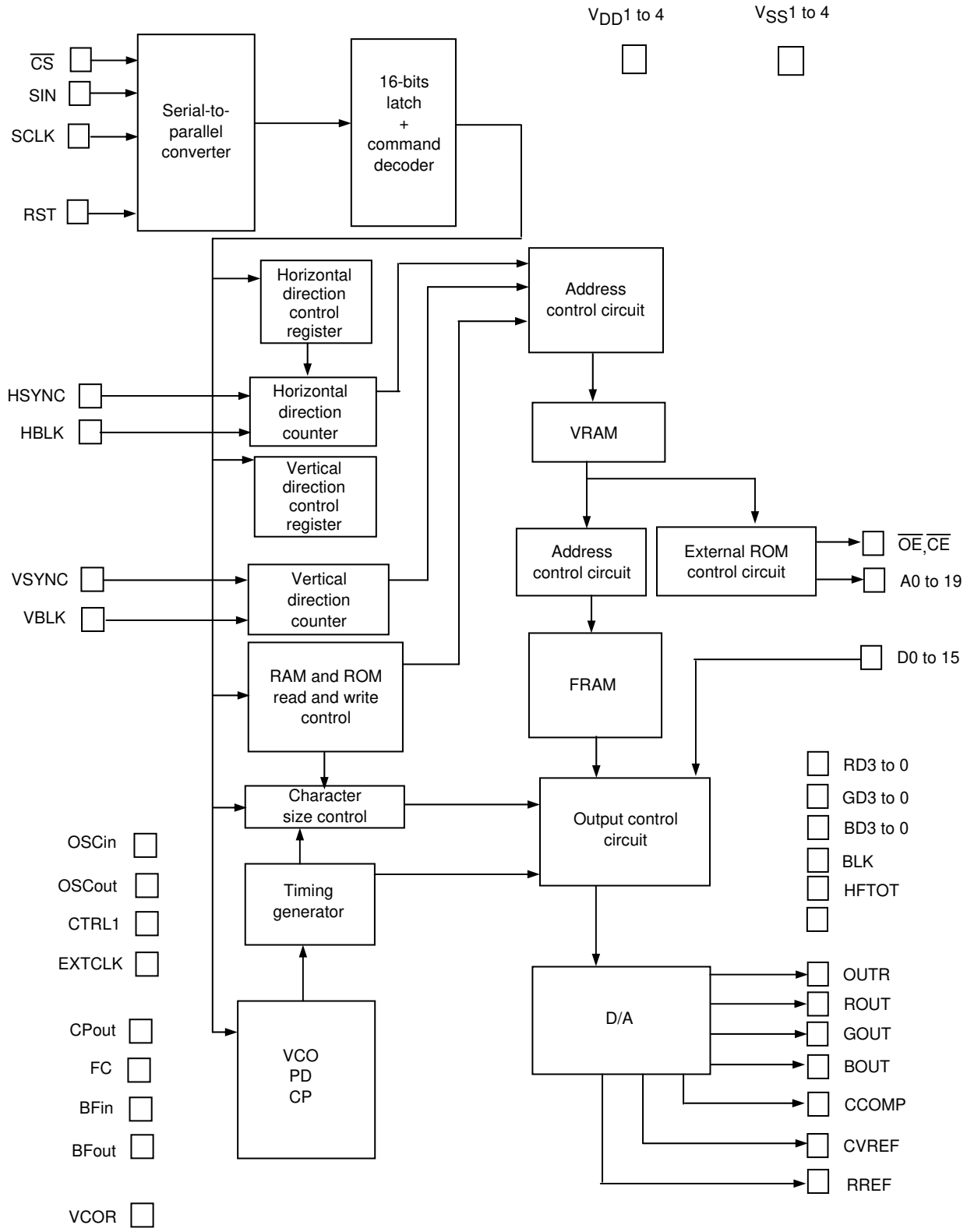


Figure 1 OSD Serial Data Input Timing

System Block Diagram



Display Control Commands

The display control commands have serial input format that consists of 8-bit units transmitted LSB first. A commands consists of a command identification code in the first byte and data in the second and following bytes. Both a first byte and a second byte (16 bits) must be transmitted for each command. Commands 10, 11, 12, 6C1, and 701 set the IC to continuous write mode. (Continuous write mode is cleared by setting the CS pin high.)

Display Control Command Table

Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND00 (Write address) Main 1: V	1	0	0	0	0	0	0	0	0	0	0	V14	V13	V12	V11	V10
COMMAND01 (Write address) Main 1: H	1	0	0	0	0	0	1	0	0	0	H15	H14	H13	H12	H11	H10
COMMAND02 (Write address) Main 2: V	1	0	0	0	0	1	0	0	0	0	0	V24	V23	V22	V21	V20
COMMAND03 (Write address) Main 2: H	1	0	0	0	0	1	1	0	0	0	H25	H24	H23	H22	H21	H20
COMMAND04 (Write address) Sub	1	0	0	0	1	0	0	0	SV1	SV0	0	0	0	0	SH1	SH0
COMMAND10 (Character write) Main 1	1	0	0	1	0	0	RM2	RM1[1]	HF1	HF0	at	BXS	BXL	BXR	BXU	BXD
								[2]	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
								[3]	0	CTB1	CTB0	I/E	MG1	MG0	RO1	RO0
								[4]	0	0	C13	C12	C11	C10	C9	C8
								[5]	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND11 (Character write) Main 2	1	0	0	1	0	1	RM2	RM1[1]	HF1	HF0	at	BXS	BXL	BXR	BXU	BXD
								[2]	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
								[3]	0	CTB1	CTB0	I/E	MG1	MG0	RO1	RO0
								[4]	0	0	C13	C12	C11	C10	C9	C8
								[5]	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND12 (Character write) Sub	1	0	0	1	1	0	RM2	RM1[1]	0	0	0	0	0	0	0	0
								[2]	0	0	0	0	0	0	0	0
								[3]	0	CTB1	CTB0	I/E	MG1	MG0	RO1	RO0
								[4]	0	0	C13	C12	C11	C10	C9	C8
								[5]	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND20 (System control)	1	0	1	0	0	0	0	0	TST MD2	TST MD1	SYS RST	FRM ERS	CT ERS	SRM ERS	MRM ER2	MRM ERS1
COMMAND21 (Display control)	1	0	1	0	0	0	0	1	BK 12	BK 02	BK 11	BK 01	DSP BG	DSP GS	DSP GM2	DSP GM1
COMMAND22 (I/O polarity control 1)	1	0	1	0	0	0	1	0	0	BLOP	BLO 2	BLO 1	BLO 0	CKP	VIP	HIP
COMMAND23 (Screen background color)	1	0	1	0	0	0	1	1	DPM HC1	DPM HC0	BGC T1	BGC T0	BGC 3	BGC 2	BGC 1	BGC 0
COMMAND24 (I/O polarity control 2)	1	0	1	0	0	1	0	0	DPM MD	DPM VC	DA SEL	SBG SL	GD 2	GD 1	GD 0	CKOP

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND25 (Output control 1)	1	0	1	0	0	1	0	1	CEHSL	TOKSL	VIPSL	LCSSP2	OTM1	OTM0	LCSSTP	LCSOFF
COMMAND26 (Output control 2)	1	0	1	0	0	1	1	0	HFOFF	TBLOFF	KBL2	BL1	BL0	OTM2	ROTOFF	DOTOFF
COMMAND27 (Output control 3)	1	0	1	0	0	1	1	1	0	HFT2	HFT1	HFT0	TOKCB4	TOKCB3	TOKCB2	TOKCB1
COMMAND28 (Output control 4)	1	0	1	0	1	0	0	0	HPG9	HPS9	HPM29	HPM19	VPG8	VPS8	VPM28	VPM18
COMMAND29 (Output control 5)	1	0	1	0	1	0	0	1	0	SVH1	SVH0	SHH1	SHH0	0	0	MLCH
COMMAND2A (Display area control 1)	1	0	1	0	1	0	1	0	0	HINDIN	HID1	HID0	VID1	VID0	0	0
COMMAND30 (Vertical display start position: main 1)	1	0	1	1	0	0	0	0	VPM17	VPM16	VPM15	VPM14	VPM1	VPM12	VPM11	VPM10
COMMAND31 (Horizontal display start position: main 1)	1	0	1	1	0	0	1	HPM18	HPM17	HPM16	HPM15	HPM14	HPM13	HPM12	HPM11	HPM10
COMMAND32 (Vertical display start position: main 2)	1	0	1	1	0	1	0	0	VPM27	VPM26	VPM25	VPM24	VPM23	VPM22	VPM21	VPM20
COMMAND33 (Horizontal display start position: main 2)	1	0	1	1	0	1	1	HPM28	HPM27	HPM26	HPM25	HPM24	HPM23	HPM22	HPM21	HPM20
COMMAND34 (Vertical display start positions: sub)	1	0	1	1	1	0	0	0	VPS7	VPS6	VPS5	VPS4	VPS3	VPS2	VPS1	VPS0
COMMAND35 (Horizontal display start position: sub)	1	0	1	1	1	0	1	HPS8	HPS7	HPS6	HPS5	HPS4	HPS3	HPS2	HPS1	HPS0
COMMAND36 (Vertical display start positions: screen)	1	0	1	1	1	1	0	0	VPG7	VPG6	VPG5	VPG4	VPG3	VPG2	VPG1	VPG0
COMMAND37 (Horizontal display start position: screen)	1	0	1	1	1	1	1	HPG8	HPG7	HPG6	HPG5	HPG4	HPG3	HPG2	HPG1	HPG0

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND40 (Character size control)	1	1	0	0	0	0	0	0	0	0	0	0	SZV1	SZV0	SZH1	SZH0
COMMAND41 main 1 (Character size control: line setting U)	1	1	0	0	0	0	0	1	LSZ 7	LSZ 6	LSZ 5	LSZ 4	LSZ 3	LSZ 2	LSZ 1	LSZ 0
COMMAND42 main 1 (Character size control: line setting D)	1	1	0	0	0	0	1	0	LSZ 15	LSZ 14	LSZ 13	LSZ 12	LSZ 11	LSZ 10	LSZ 9	LSZ 8
COMMAND43 main 1 (Character size control: line setting D2)	1	1	0	0	0	0	1	1	0	0	0	0	0	0	LSZ 17	LSZ 16
COMMAND44 main 2 (Character size control: line setting U)	1	1	0	0	0	1	0	0	LSZ 7	LSZ 6	LSZ 5	LSZ 4	LSZ 3	LSZ 2	LSZ 1	LSZ 0
COMMAND45 main 2 (Character size control: line setting D)	1	1	0	0	0	1	0	1	LSZ 15	LSZ 14	LSZ 13	LSZ 12	LSZ 11	LSZ 10	LSZ 9	LSZ 8
COMMAND46 main 2 (Character size control: line setting D2)	1	1	0	0	0	1	1	0	0	0	0	0	0	0	LSZ 17	LSZ 16
COMMAND50 (BOX control U)	1	1	0	1	0	0	0	0	BXL W1	BXL W0	BXU CT1	BXU CT0	BXU C3	BXU C2	BXU C1	BXU C0
COMMAND51 (BOX control D)	1	1	0	1	0	0	0	1	BXR W1	BXR W0	BXD CT1	BXD CT0	BXD C3	BXD C2	BXD C1	BXD C0
COMMAND52 main 1 (BOX control: line setting U)	1	1	0	1	0	0	1	0	LBX 7	LBX 6	LBX 5	LBX 4	LBX 3	LBX 2	LBX 1	LBX 0
COMMAND53 main 1 (BOX control: line setting D)	1	1	0	1	0	0	1	1	LBX 15	LBX 14	LBX 13	LBX 12	LBX 11	LBX 10	LBX 9	LBX 8
COMMAND54 main 1 (BOX control: line setting D2)	1	1	0	1	0	1	0	0	0	0	0	0	0	0	LBX 17	LBX 16
COMMAND55 main 2 (BOX control: line setting U)	1	1	0	1	0	1	0	1	LBX 7	LBX 6	LBX 5	LBX 4	LBX 3	LBX 2	LBX 1	LBX 0
COMMAND56 main 2 (BOX control: line setting D)	1	1	0	1	0	1	1	0	LBX 15	LBX 14	LBX 13	LBX 12	LBX 11	LBX 10	LBX 9	LBX 8
COMMAND57 main 2 (BOX control: line setting D2)	1	1	0	1	0	1	1	1	0	0	0	0	0	0	LBX 17	LBX 16

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND58 (Line spacing control 1)	1	1	0	1	1	0	0	0	0	GYBCK	GS1	GS0	GY3	GY2	GY1	GY0
COMMAND59 (Line spacing control 2)	1	1	0	1	1	0	0	1	BXDW	BXUW	GYHSL	BXHSL	FCHSL	BXC3	BXC2	BXC1
COMMAND5A main 1 (Line spacing control: line setting U)	1	1	0	1	1	0	1	0	LGY7	LGY6	LGY5	LGY4	LGY3	LGY2	LGY1	LGY0
COMMAND5B main 1 (Line spacing control: line setting U)	1	1	0	1	1	0	1	1	LGY15	LGY14	LGY13	LGY12	LGY11	LGY10	LGY9	LGY8
COMMAND5C main 1 (Line spacing control: line setting D2)	1	1	0	1	1	1	0	0	0	0	0	0	0	0	LGY17	LGY16
COMMAND5D main 2 (Line spacing control: line setting U)	1	1	0	1	1	1	0	1	LGY7	LGY6	LGY5	LGY4	LGY3	LGY2	LGY1	LGY0
COMMAND5E main 2 (Line spacing control: line setting D)	1	1	0	1	1	1	1	0	LGY15	LGY14	LGY13	LGY12	LGY11	LGY10	LGY9	LGY8
COMMAND5F main 2 (Line spacing control: line setting D2)	1	1	0	1	1	1	1	1	0	0	0	0	0	0	LGY17	LGY16
COMMAND60 (Border control)	1	1	1	0	0	0	0	0	BLK	BLK	EGCT1	EGCT0	EGC3	EGC2	EGC1	EGC0
COMMAND61 main 1 (Border control: line setting U)	1	1	1	0	0	0	0	1	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
COMMAND62 main 1 (Border control: line setting D)	1	1	1	0	0	0	1	0	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
COMMAND63 main 1 (Border control: line setting D2)	1	1	1	0	0	0	1	1	0	0	0	0	0	0	LFC17	LFC16
COMMAND64 main 2 (Border control: line setting U)	1	1	1	0	0	1	0	0	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
COMMAND65 main 2 (Border control: line setting D)	1	1	1	0	0	1	0	1	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
COMMAND66 main 2 (Border control: line setting D2)	1	1	1	0	0	1	1	0	0	0	0	0	0	0	LFC17	LFC16
COMMAND67 (PLL control 1)	1	1	1	0	0	1	1	1	EVOOFF	LCOFF	ECKOFF	VCOOFF	VCS1	VCS0	CKSL1	CKSL0
COMMAND68 (PLL control 2)	1	1	1	0	1	0	0	0	0	0	0	DIV12	DIV11	DIV10	DIV9	DIV8
COMMAND69 (PLL control 3)	1	1	1	0	1	0	0	1	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
COMMAND6A (PLL control 5)	1	1	1	0	1	0	1	0	0	HDSL	DZ1	DZ0	HRSL	DID2	DID1	DID0
COMMAND6C0 (Write address) Color table	1	1	1	0	1	1	0	0	0	0	CTN1	CTN0	CTA3	CTA2	CTA1	CTA0
COMMAND6C1 (Data write) Color table	1	1	1	0	1	1	1	RM3[1][2]	0TG3	0TG2	HFTTG1	TOKTG0	TB3TR3	TB2TR2	TB1TR1	TB0TR0

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Command	First byte								Second byte							
	Command identification code data								Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND700 (character ram1) writeaddress	1	1	1	1	0	0	0	0	FAD 1	FAD 0	FRN 1	FRN 0	FVA 3	FVA 2	FVA 1	FVA 0
COMMAND701 (character ram2) write	1	1	1	1	0	0	1	RM3[1] [2]	D15 D7	D14 D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0
COMMAND710 (WVGA ROM)	1	1	1	1	0	1	0	0	0	0	CKO S1	CKO S0	WFC MD	WRA M2	WRA M1	WRA M0
COMMAND711 (PLL control 6)	1	1	1	1	0	1	0	1	RSTB	0	VCRS	VCRS 1	CP 0	0 X2	CP I11	CP I0
COMMAND712 (PLL control 7)	1	1	1	1	0	1	1	0	0	STB CP	RES CP	SCP CP	DIV ECP	GAN 2	GAN 1	GAN 0

1 COMMAND00 (Main screen 1: horizontal write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 1 memory horizontal write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 0	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	V14 [MSB]	0	Main screen 1 memory line address (0 to 11, hexadecimal) 15 lines: 0E (hexadecimal) 18 lines: 11 (hexadecimal)	COM24-2: Line number specification
		1		
3	V13	0		
		1		
2	V12	0		
		1		
1	V11	0		
		1		
0	V10 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

2 COMMAND01 (Main screen 1: vertical write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 1 memory vertical write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 1	
2	-	0		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	H15 [MSB]	0	Main screen 1 memory character position address (0 to 21, hexadecimal) 30 characters: 1D (hexadecimal) 33 characters: 20 (hexadecimal) 34 characters: 21 (hexadecimal)	COM23-2: Character number specification
		1		
4	H14	0		
		1		
3	H13	0		
		1		
2	H12	0		
		1		
1	H11	0		
		1		
0	H10 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

3 COMMAND02 (Main screen 2: horizontal write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 2 memory horizontal write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 2	
2	-	1		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	V24 [MSB]	0	Main screen 2 memory line address (0 to 0E, hexadecimal) 15 lines: 0E (hexadecimal) 18 lines: 11 (hexadecimal)	COM24-2: Line number specification
		1		
3	V23	0		
		1		
2	V22	0		
		1		
1	V21	0		
		1		
0	V20 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

4 COMMAND03 (Main screen 2: vertical write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Main screen 2 memory vertical write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	0	Sub-identification code: 3	
2	-	1		
1	-	1		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	-	0		
4	H25 [MSB]	0	Main screen 2 memory character position address (0 to 21, hexadecimal) 30 characters: 1D (hexadecimal) 33 characters: 20 (hexadecimal) 34 characters: 21 (hexadecimal)	COM23-3: Character number specification
		1		
4	H24	0		
		1		
3	H23	0		
		1		
2	H22	0		
		1		
1	H21	0		
		1		
0	H20 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

5 COMMAND04 (Subscreen write address setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 0 identification code Subscreen write address setting	
6	-	0		
5	-	0		
4	-	0		
3	-	1	Sub-identification code: 4	
2	-	0		
1	-	0		
0	-	0		

(2) Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	SV1	0	Subscreen memory line address 0 to 3 (hexadecimal) 4 lines (maximum)	COM29-2: Line number specification
		1		
6	SV0	0		
		1		
5	-	0		
4	-	0		
3	-	0		
2	-	0		
1	SH1	0	Subscreen memory character position address 0 to 3 (hexadecimal) 4 characters (maximum)	COM29-2: Character number specification
		1		
0	SH0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

6 COMMAND10 (Main screen 1 display character data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 1 identification code Display character data write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	0		
5	-	0		
4	-	1		
3	-	0	Sub-identification code: 0	
2	-	0		
1	RM2	0	RM2 RM1 Mode 0 0 [1][2][3][4][5] End 0 1 [1][2][3][4][5] Continuous 1 0 [3][4][5] Continuous 1 1 [2][3][4][5] Continuous	Continuous write mode selection
		1		
0	RM1	0		
		1		

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	HFT1	0	HFT1 HFT0 0 0 None 0 1 Character only 1 0 Character background only 1 1 Character+Character background	Halftone specification Graphic is processed as a character. COM59-2
		1		
6	HFT0	0		
		1		
5	at	0	Blinking off	Blinking specification
		1	Blinking on	
4	BXS	0	Raised	Box specification: raised/recessed
		1	Recessed	
3	BXL	0	None	Box specification: left side
		1	Box displayed	
2	BXR	0	None	Box specification: right side
		1	Box displayed	
1	BXU	0	None	Box specification: upper
		1	Box displayed	
0	BXD	0	None	Box specification: down
		1	Box displayed	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	CB3 [MSB]	0	Character background color specification 0000 to 1111, or 0 to F (hexadecimal)	Character background color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
6	CB2	0		
		1		
5	CB1	0		
		1		
4	CB0 [LSB]	0		
		1		
3	CC3 [MSB]	0	Character color specification 0000 to 1111, or 0 to F (hexadecimal)	Character color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
2	CC2	0		
		1		
1	CC1	0		
		1		
0	CC0 [LSB]	0		
		1		

(4) Second byte-[3]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	CTB1	0	CTB1 CTB0 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Color table selection
		1		
5	CTB0	0		
		1		
4	I/E	0	Character RAM (internal)	ROM selection
		1	External ROM	
3	M/G1	0	MG1 MG0 0 0 Character 0 1 Graphic 1(CB, CC invalid) 1 0 Graphic 2 CTB address shown with CB → Chantged to CTB address shown with CC 1 1 Graphic 3 CTBNo of address shown with CB → Changed to CTBNo shown with CC1, CC0	Character/graphic specification
		1		
2	M/G0	0		
		1		
		1		
1	ROM1	0	ROM1 ROM0 0 0 ROM area number 1 0 1 ROM area number 2 1 0 ROM area number 3 1 1 ROM area number 4	ROM area selection
		1		
0	ROM0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

(5) Second byte-[4]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	C13 [MSB]	0		Character code specification
		1		
4	C12	0		
		1		
3	C11	0		
		1		
2	C10	0		
		1		
1	C9	0		
		1		
0	C8	0		
		1		

(6) Second byte-[5]

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code External ROM: 16384 characters 0000 to 3FFF (hexadecimal) 0 to 16383 Character RAM (internal): QVGA mode: 0 to 3, hexadecimal, 4 characters WVGA mode: 0 hexadecimal, 1 character * Transparent character specification I/E = 0 (Internal character RAM) M/G10 = 00 (Character) Code = FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

7 COMMAND11 (Main screen 2 display character data write setting command)

(1) First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	1	Command 1 identification code Display character data write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.
6	-	0		
5	-	0		
4	-	1		
3	-	0	Sub-identification code: 1	
2	-	0		
1	RM2	0	RM2 RM1 Mode 0 0 [1][2][3][4][5] End 0 1 [1][2][3][4][5] Continuous 1 0 [3][4][5] Continuous 1 1 [2][3][4][5] Continuous	Continuous write mode selection
		1		
0	RM1	0		
		1		

(2) Second byte-[1]

DA0 to 7	Register	Content		Notes
		State	Function	
7	HFT1	0	HFT1 HFT0 0 0 None 0 1 Character only 1 0 Character background only 1 1 Character+Character background	Halftone specification Graphic is processed as a character. COM59-2
		1		
6	HFT0	0		
		1		
5	at	0	Blinking off	Blinking specification
		1	Blinking on	
4	BXS	0	Raised	Box specification: raised/recessed
		1	Recessed	
3	BXL	0	None	Box specification: left side
		1	Box displayed	
2	BXR	0	None	Box specification: right side
		1	Box displayed	
1	BXU	0	None	Box specification: upper
		1	Box displayed	
0	BXD	0	None	Box specification: down
		1	Box displayed	

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{RST}$ pin.

(3) Second byte-[2]

DA0 to 7	Register	Content		Notes
		State	Function	
7	CB3 [MSB]	0	Character background color specification 0000 to 1111, or 0 to F (hexadecimal)	Character background color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
6	CB2	0		
		1		
5	CB1	0		
		1		
4	CB0 [LSB]	0		
		1		
3	CC3 [MSB]	0	Character color specification 0000 to 1111, or 0 to F (hexadecimal)	Character color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
2	CC2	0		
		1		
1	CC1	0		
		1		
0	CC0 [LSB]	0		
		1		

(4) Second byte-[3]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	CTB1	0	CTB1 CTB0 0 0 Color table number 1 0 1 Color table number 2 1 0 Color table number 3 1 1 Color table number 4	Color table selection
		1		
5	CTB0	0		
		1		
4	I/E	0	Character RAM (internal)	ROM selection
		1	External ROM	
3	M/G1	0	MG1 MG0 0 0 Character 0 1 Graphic 1 (CB, CC invalid) 1 0 Graphic 2 CTB address shown with CB → Changed to CTB address shown with CC. 1 1 Graphic 3 CTBNo of address shown with CB. → Changed to CTBNo shown with CC1, CC0.	Character/graphic specification
		1		
2	M/G0	0		
		1		
		1		
1	ROM1	0	ROM1 ROM0 0 0 ROM area number 1 0 1 ROM area number 2 1 0 ROM area number 3 1 1 ROM area number 4	ROM area selection
		1		
0	ROM0	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

(5) Second byte-[4]

DA0 to 7	Register	Content		Notes
		State	Function	
7	-	0		
6	-	0		
5	C13 [MSB]	0		Character code specification
		1		
4	C12	0		
		1		
3	C11	0		
		1		
2	C10	0		
		1		
1	C9	0		
		1		
0	C8	0		
		1		

(6) Second byte-[5]

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code External ROM: 16384 characters 0000 to 3FFF (hexadecimal) 0 to 16383 Character RAM (internal): QVGA mode: 0 to 3, hexadecimal, 4 characters WVGA mode: 0 hexadecimal, 1 character * Transparent character specification I/E = 0 (Internal character RAM) M/G10 = 00 (Character) Code = FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

*: This resistor is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.