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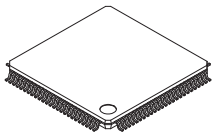
LC75809PT

1/4 and 1/3-Duty General-Purpose LCD Driver

ON Semiconductor®

www.onsemi.com



TQFP100 14x14 / TQFP100

Overview

The LC75809PT is the 1/4 duty and 1/3 duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as frequency display in products with electronic tuning. In addition to being able to drive up to 352 segments directly, the LC75809PT can also control up to 12 general-purpose output ports. Because it has the PWM output of a maximum of 6 ch, the brightness control of the LED backlight of RGB ×2 can be done. Incorporation of an oscillation circuit helps to reduce the number of external resistors and capacitors required.

Features

- Support for 1/4-duty 1/3-bias or 1/3-duty 1/3-bias drive techniques under serial data control.
  - When 1/4-duty : Capable of driving up to 352 segments
  - When 1/3-duty : Capable of driving up to 267 segments
- Serial data input supports CCB* format communication with the system controller. (Support 3.3 V and 5 V operation)
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port function.
  (Support for up to 12 general-purpose output ports)
- Support for the PWM output function of a maximum of 6 ch.
  (It can output from the general-purpose output port).
- Support for clock output function of 1 ch.
  (It can output from the general-purpose output port).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- Built-in display contrast adjustment circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit.
  (Incorporation of resistor and capacitor for an oscillation)

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 43 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +6.8	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +6.8	V
	$V_{IN}2$	OSCI, $V_{DD}1$, $V_{DD}2$	−0.3 to V_{DD}+0.3	
Output voltage	V_{OUT}	S1 to S89, COM1 to COM4, P1 to P12	−0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	S1 to S88	300	μA
	$I_{OUT}2$	COM1 to COM4, S89	3	mA
	$I_{OUT}3$	P1 to P12	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = −40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.3	V
Input voltage *1	$V_{DD}1$	$V_{DD}1$		2/3$V_{DD}0$	$V_{DD}0$	V
	$V_{DD}2$	$V_{DD}2$		1/3$V_{DD}0$	$V_{DD}0$	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.4V_{DD}		6.3	V
	$V_{IH}2$	OSCI: External clock operating mode	0.4V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSCI: External clock operating mode	0		0.2V_{DD}	
External clock operating frequency	f_{CK}	OSCI: External clock operating mode [Figure4]	10	300	600	kHz
External clock duty cycle	D_{CK}	OSCI: External clock operating mode [Figure4]	30	50	70	%
Data setup time	tds	CL, DI [Figure2], [Figure3]	160			ns
Data hold time	tdh	CL, DI [Figure2], [Figure3]	160			ns
CE wait time	tcp	CE, CL [Figure2], [Figure3]	160			ns
CE setup time	tcs	CE, CL [Figure2], [Figure3]	160			ns
CE hold time	tch	CE, CL [Figure2], [Figure3]	160			ns
High level clock pulse width	tϕH	CL [Figure2], [Figure3]	160			ns
Low level clock pulse width	tϕL	CL [Figure2], [Figure3]	160			ns
Rise time	tr	CE, CL, DI [Figure2], [Figure3]		160		ns
Fall time	tf	CE, CL, DI [Figure2], [Figure3]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure5], [Figure6] [Figure7], [Figure8]	10			μs

Note : *1. $V_{DD}0$ = 0.70V_{DD} to V_{DD}

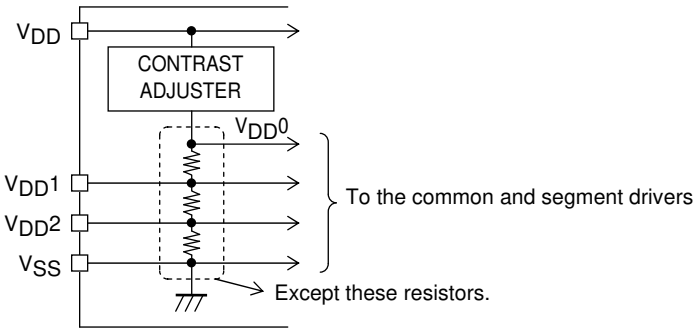
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.03V_{DD}$		V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 6.3 V			5.0	μA
	$I_{IH}2$	OSCI	$V_I = V_{DD}$: External clock operating mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0 V	−5.0			μA
	$I_{IL}2$	OSCI	V_I = 0 V: External clock operating mode	−5.0			
Output high level voltage *1	$V_{OH}1$	S1 to S89	I_O = −20 μA	$V_{DD}0$−0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = −100 μA	$V_{DD}0$−0.9			
	$V_{OH}3$	P1 to P12	I_O = −1 mA	V_{DD}−0.9			
Output low level voltage	$V_{OL}1$	S1 to S89	I_O = 20 μA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O = 100 μA			0.9	
	$V_{OL}3$	P1 to P12	I_O = 1 mA			0.9	
Output middle level voltage *1 *2	$V_{MID}1$	S1 to S89	1/3 bias I_O = ±20 μA	$2/3V_{DD}0$ −0.9		$2/3V_{DD}0$ +0.9	V
	$V_{MID}2$	S1 to S89	1/3 bias I_O = ±20 μA	$1/3V_{DD}0$ −0.9		$1/3V_{DD}0$ +0.9	
	$V_{MID}3$	COM1 to COM4	1/3 bias I_O = ±100 μA	$2/3V_{DD}0$ −0.9		$2/3V_{DD}0$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias I_O = ±100 μA	$1/3V_{DD}0$ −0.9		$1/3V_{DD}0$ +0.9	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	240	300	360	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			100	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.3 V Output open Internal oscillator operating mode		1000	2000	
	$I_{DD}3$	V_{DD}	V_{DD} = 6.3 V Output open External clock operating mode f_{CK} = 300 kHz $V_{IH}2 = 0.5V_{DD}$ $V_{IL}2 = 0.1V_{DD}$		1000	2000	

Note: *1. $V_{DD}0 = 0.70V_{DD}$ to V_{DD}

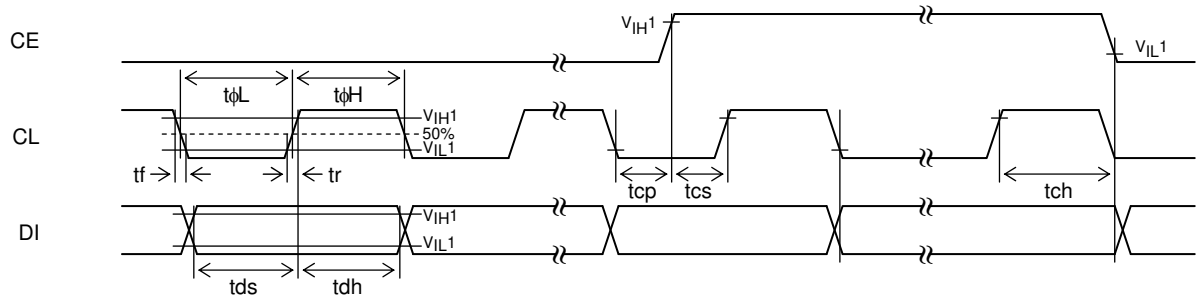
Note: *2. Excluding the bias voltage generation divider resistors built in the $V_{DD}1$ and $V_{DD}2$. (See Figure 1.)



[Figure 1]

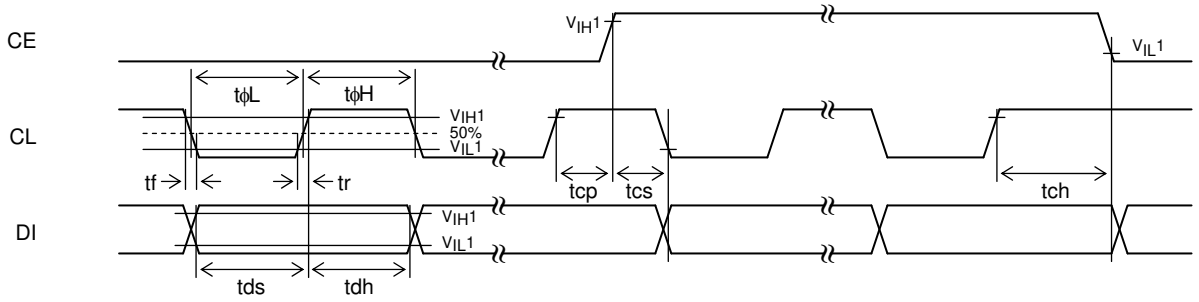
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When CL is stopped at the low level



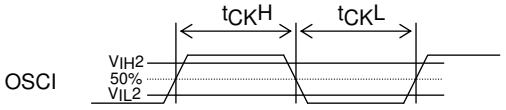
[Figure 2]

2. When CL is stopped at the high level



[Figure 3]

3. OSCI pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \text{ [kHz]}$$

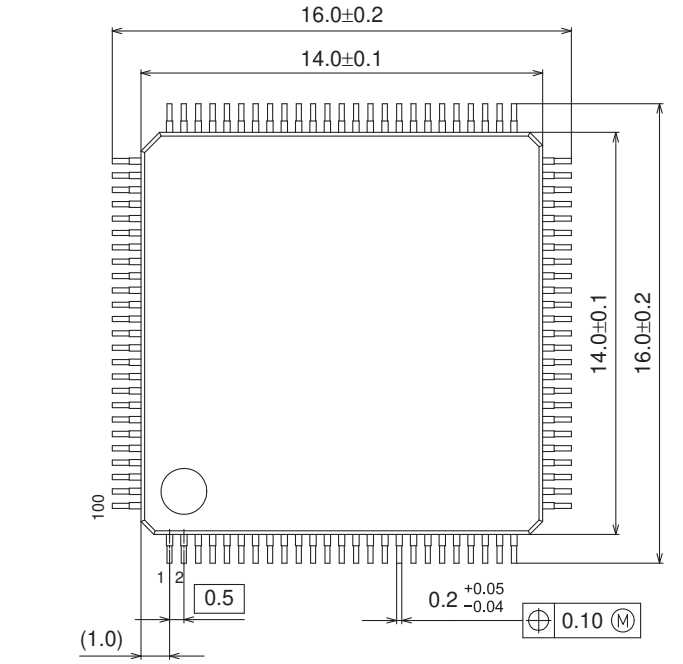
$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

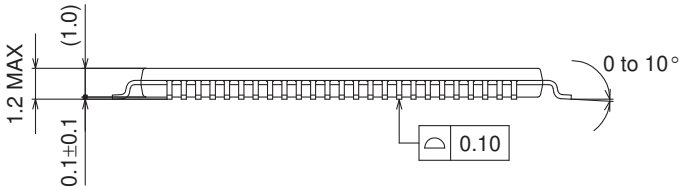
[Figure 4]

Package Dimensions

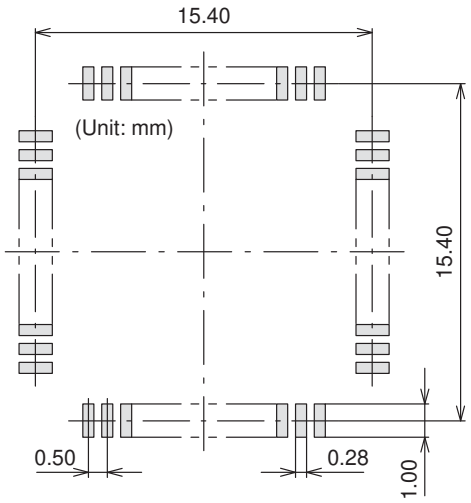
unit : mm

TQFP100 14x14 / TQFP100
CASE 932AY
ISSUE A

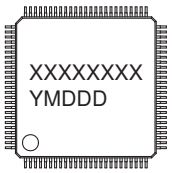




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



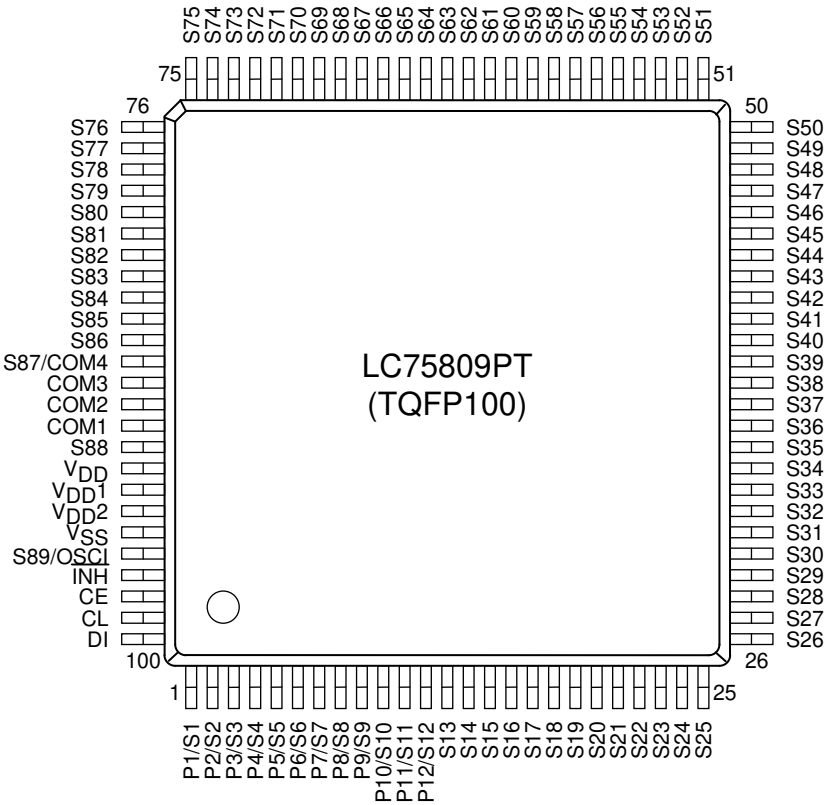
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

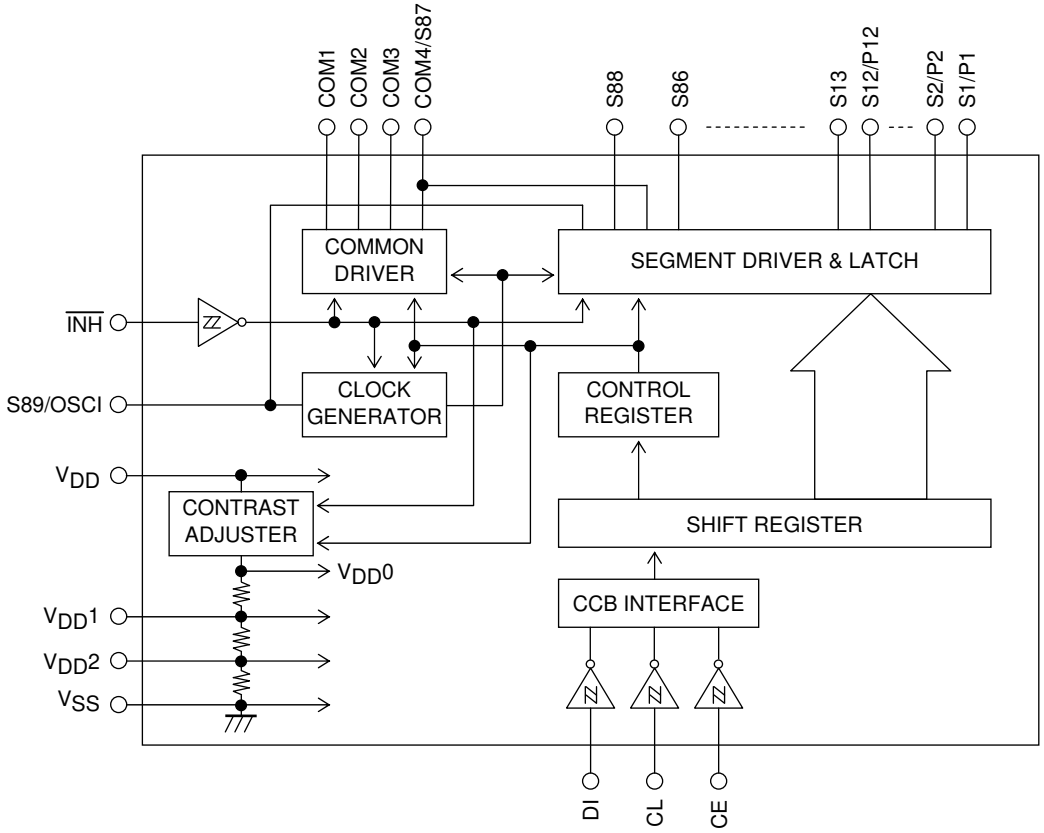
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Top view

Block Diagram



Pin Functions

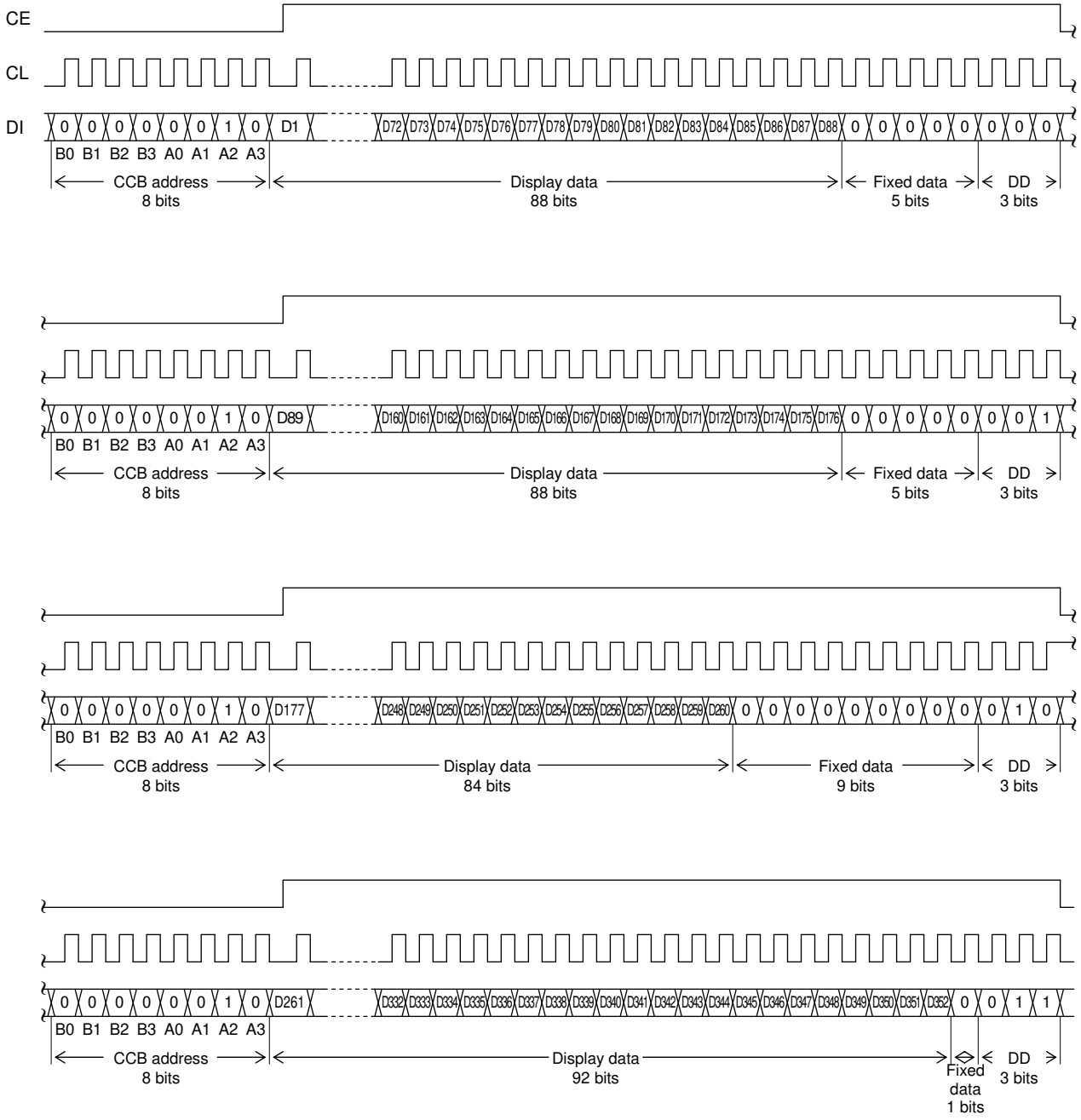
Pin	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S12/P12 S13 to S86 S88	1 to 12 13 to 86 91	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S12/P12 pins can be used as general-purpose output ports under serial data control.	-	O	OPEN
COM1 to COM3 COM4/S87	90 to 88 87	Common driver outputs The frame frequency is fo[Hz]. The COM4/S87 pin can be used as a segment output in 1/3 duty.	-	O	OPEN
S89/OSCI	96	Segment output. This pin can also be used as the external clock input pin when the external clock operating mode is selected by control data.	-	I/O	OPEN
CE CL DI	98 99 100	Serial data transfer inputs. Must be connected to the controller. CE : Chip enable CL : Synchronization clock DI : Transfer data	H ↑ -	I I I	 GND
$\overline{INH}$	97	Display off control input •$\overline{INH}$=low(V_{SS})….Display forced off S1/P1 to S12/P12=low (V_{SS}) (These pins are forcibly set to the general-purpose output port function and held at the V_{SS} level.) S13 to S86, S88=low(V_{SS}) COM1 to COM3=low(V_{SS}) COM4/S87=low(V_{SS}) S89/OSCI=low(V_{SS}) (This pin is forcibly set to the segment output port function and held at the V_{SS} level.) Stops the internal oscillator. Inhibits external clock input. Display contrast adjustment circuit stopped. •$\overline{INH}$=high(V_{DD})…Display on Enables the internal oscillator circuit. (Internal oscillator operating mode) Enables external clock input. (External clock operating mode) Display contrast adjustment circuit operation is enabled. However, serial data transfer is possible when the display is forced off.	L	I	GND
$V_{DD}1$	93	Used to apply the LCD drive 2/3 bias voltage externally.	-	I	OPEN
$V_{DD}2$	94	Used to apply the LCD drive 1/3 bias voltage externally.	-	I	OPEN
V_{DD}	92	Power supply pin. A power voltage of 4.5 to 6.3V must be applied to this pin.	-	-	-
V_{SS}	95	Ground pin. Must be connected to ground.	-	-	-

Serial Data Input

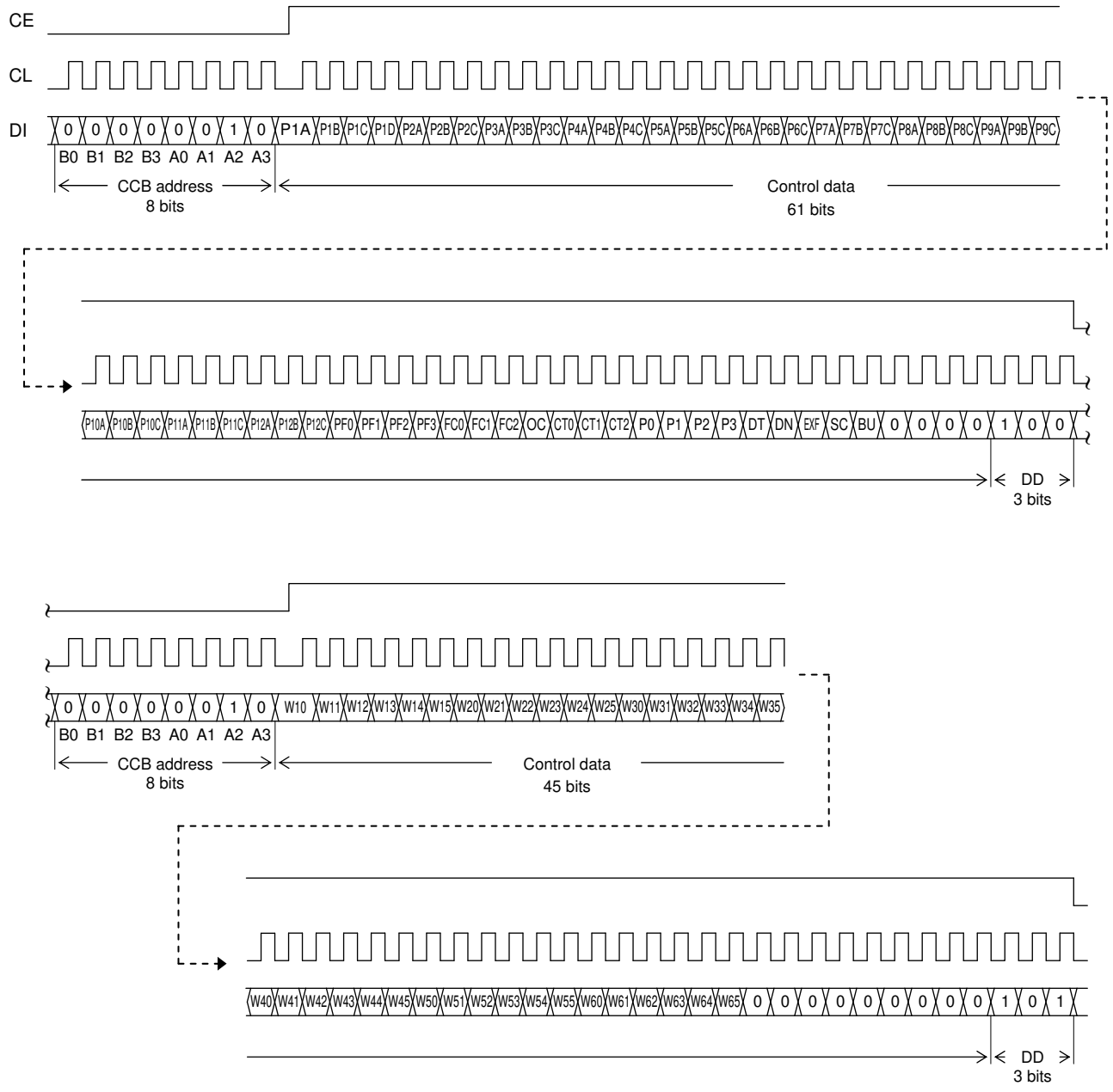
1. 1/4 duty

(1) When CL is stopped at the low level

• When the display data is transferred



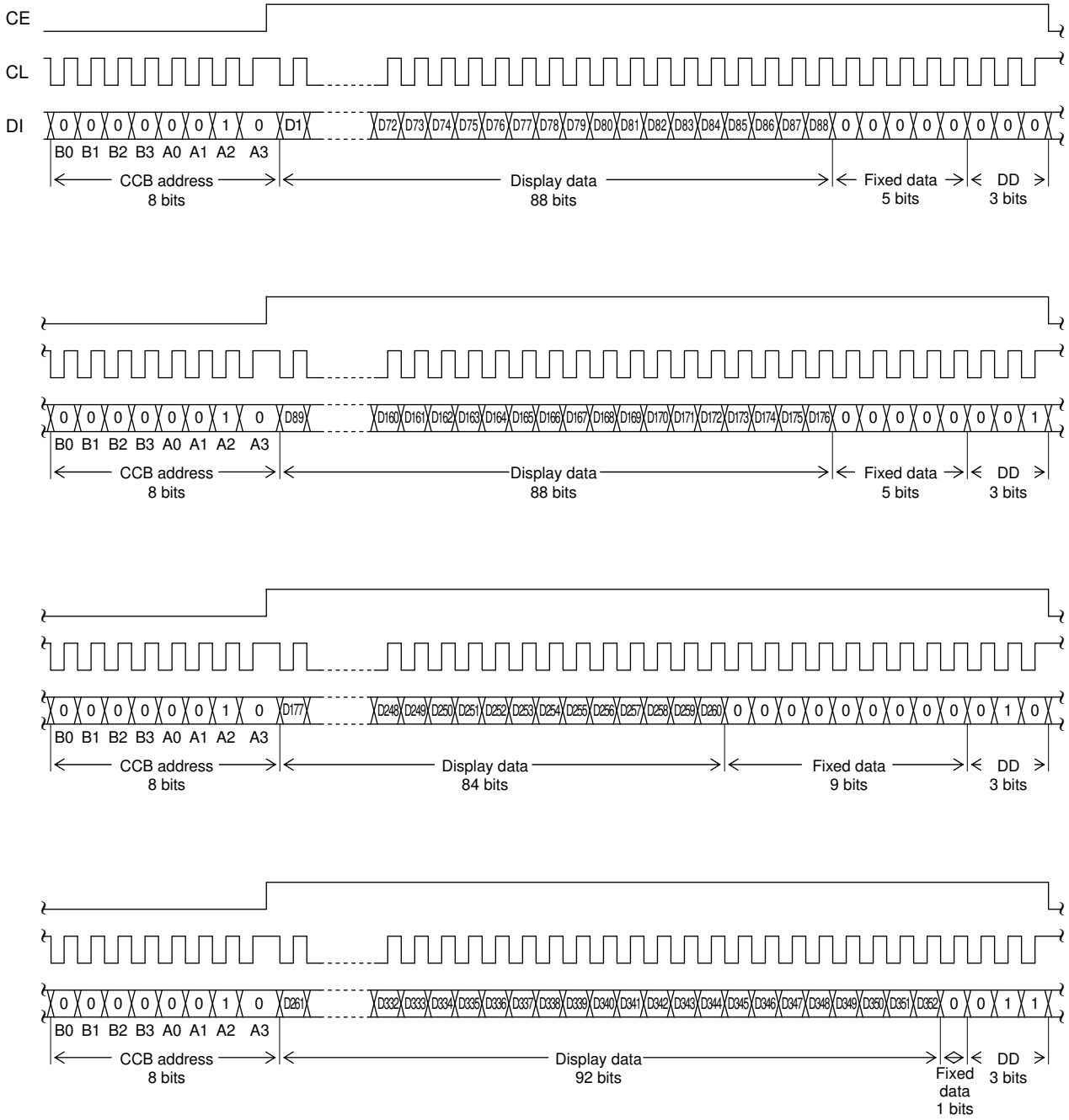
• When the control data is transferred



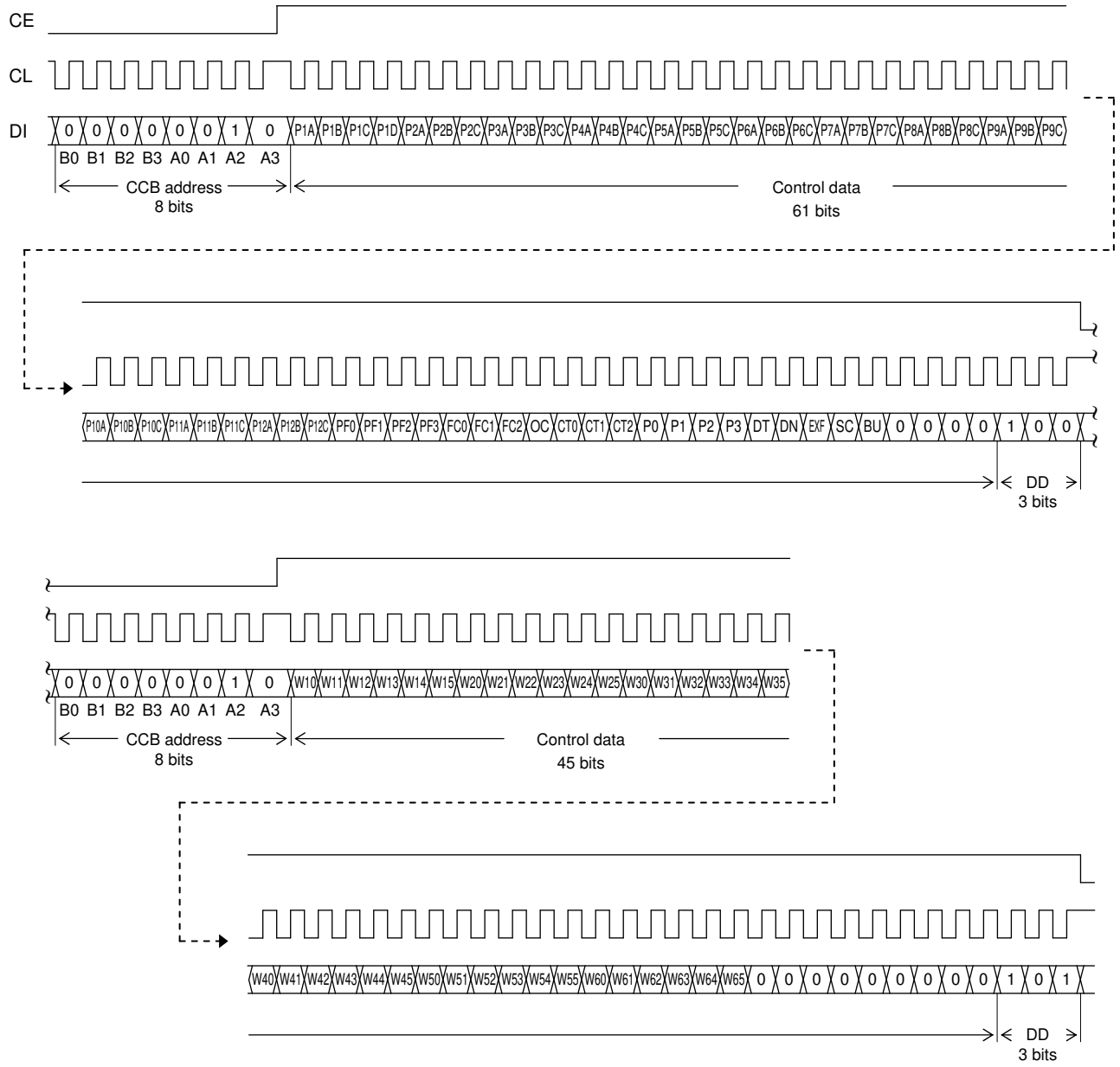
Note: DD is the direction data.

(2) When CL is stopped at the high level

• When the display data is transferred



• When the control data is transferred



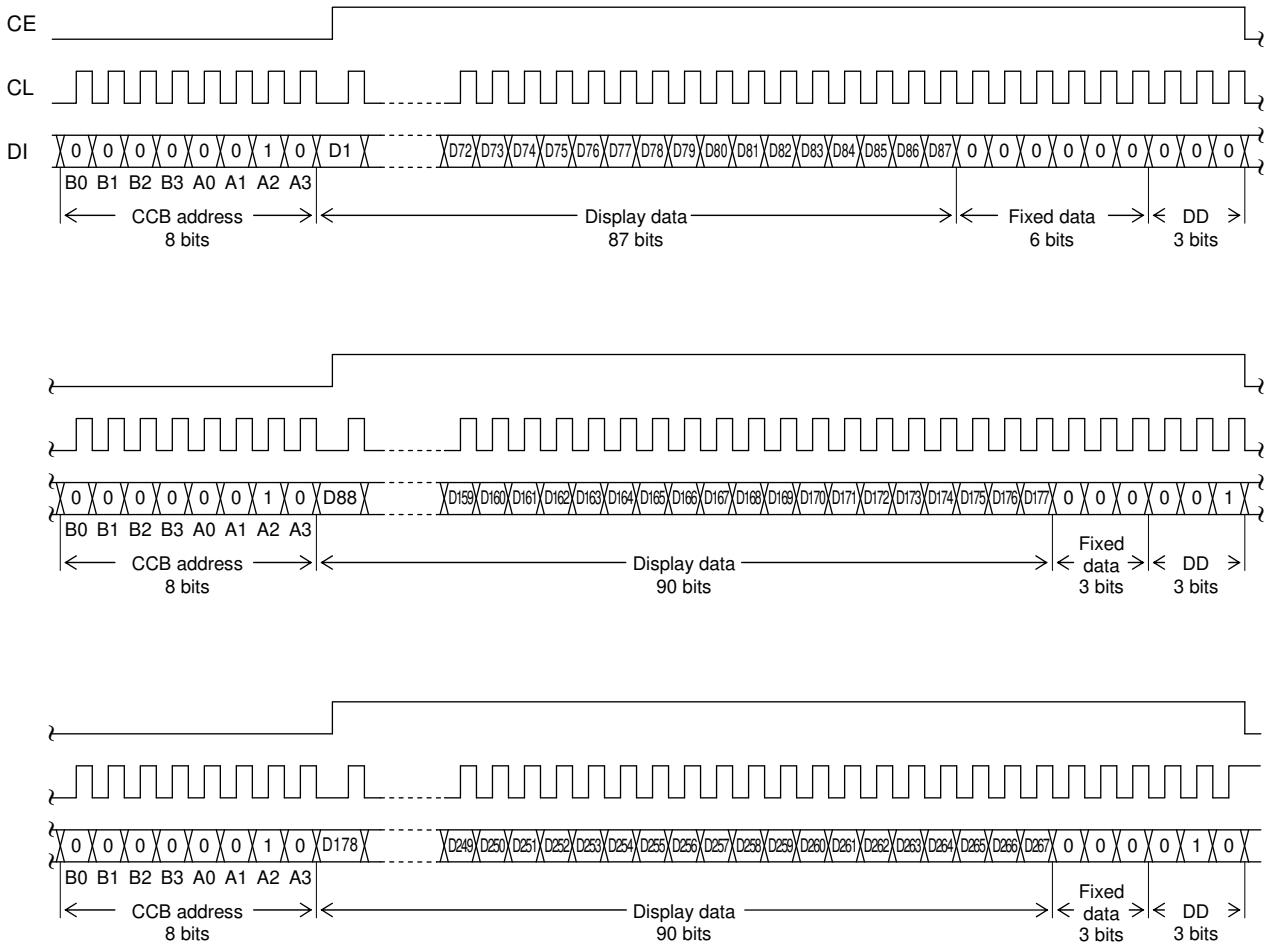
Note: DD is the direction data

- CCB address ..... "40H"
- D1 to D352 ..... Display data
- P1A, P1B, P1C, P1D ..... General-purpose output port (P1) function setting control data
- P2A, P2B, P2C to P12A, P12B, P12C ..... General-purpose output port (P2 to P12) function setting control data
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- CT0 to CT2 ..... Display contrast setting control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- DN ..... S88 pin and S89/OSCI pin state setting control data
- EXF ..... External clock operating frequency setting control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55, W60 to W65 ..... PWM data of the PWM output

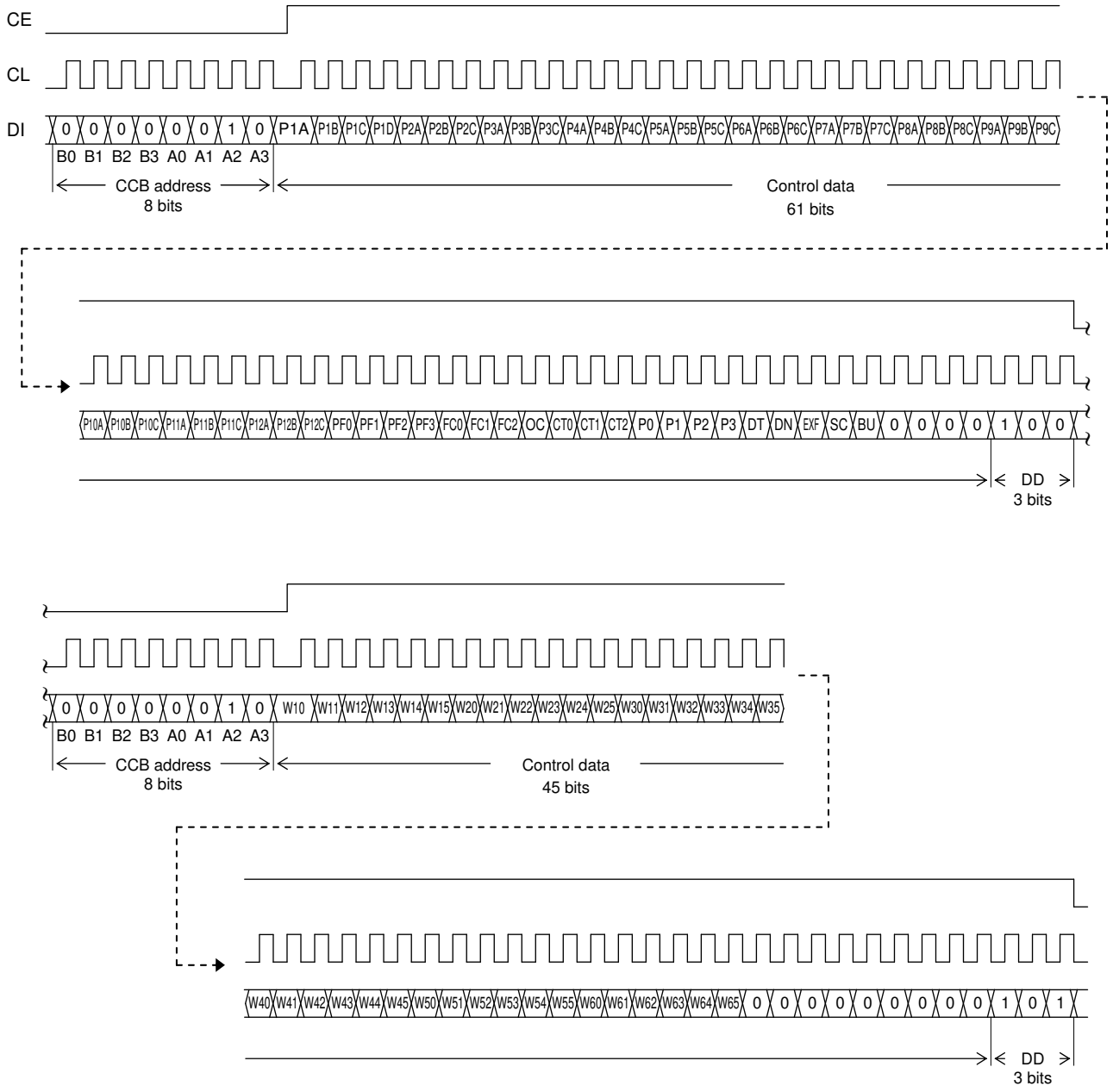
2. 1/3 duty

(1) When CL is stopped at the low level

• When the display data is transferred



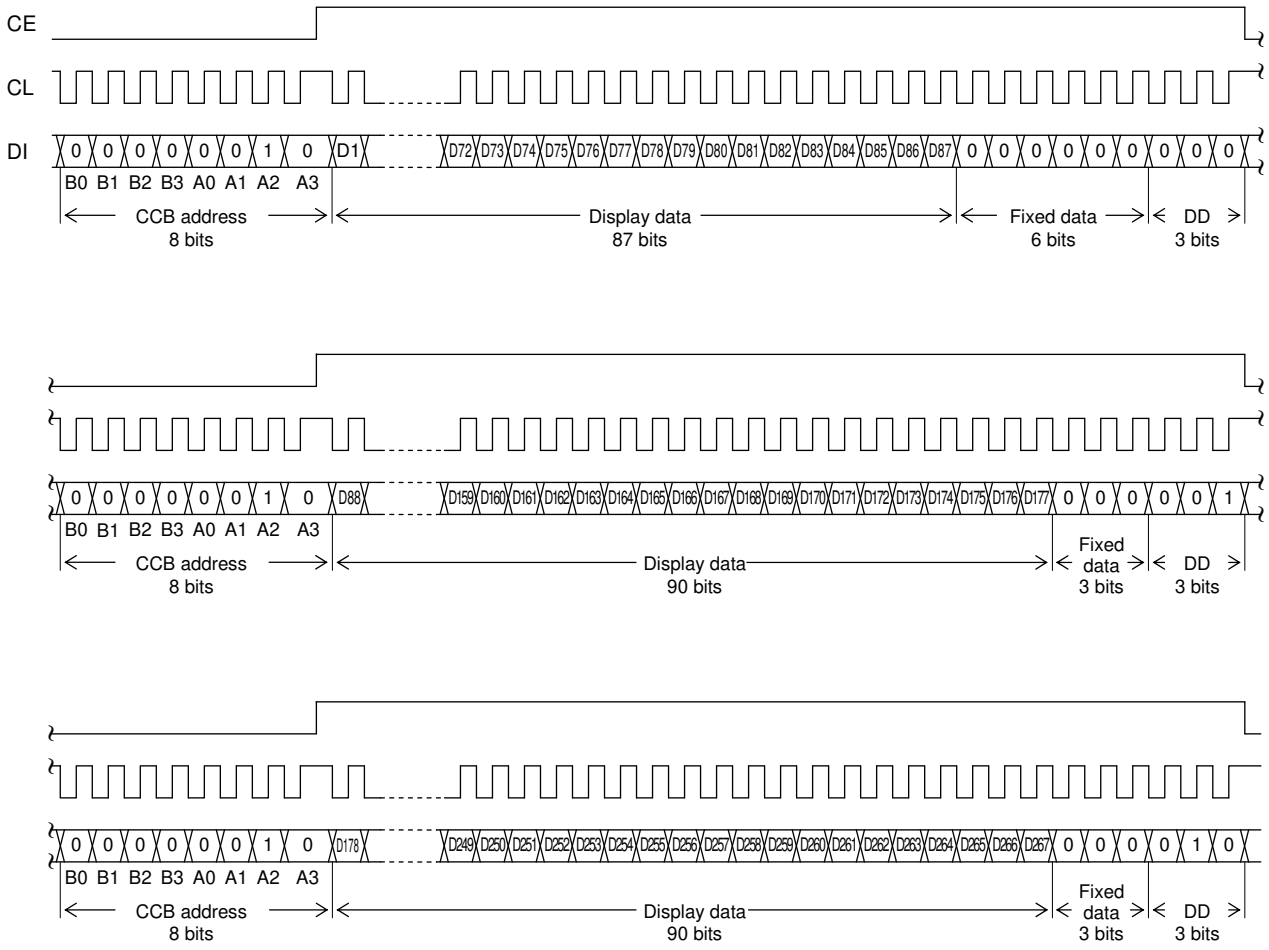
• When the control data is transferred



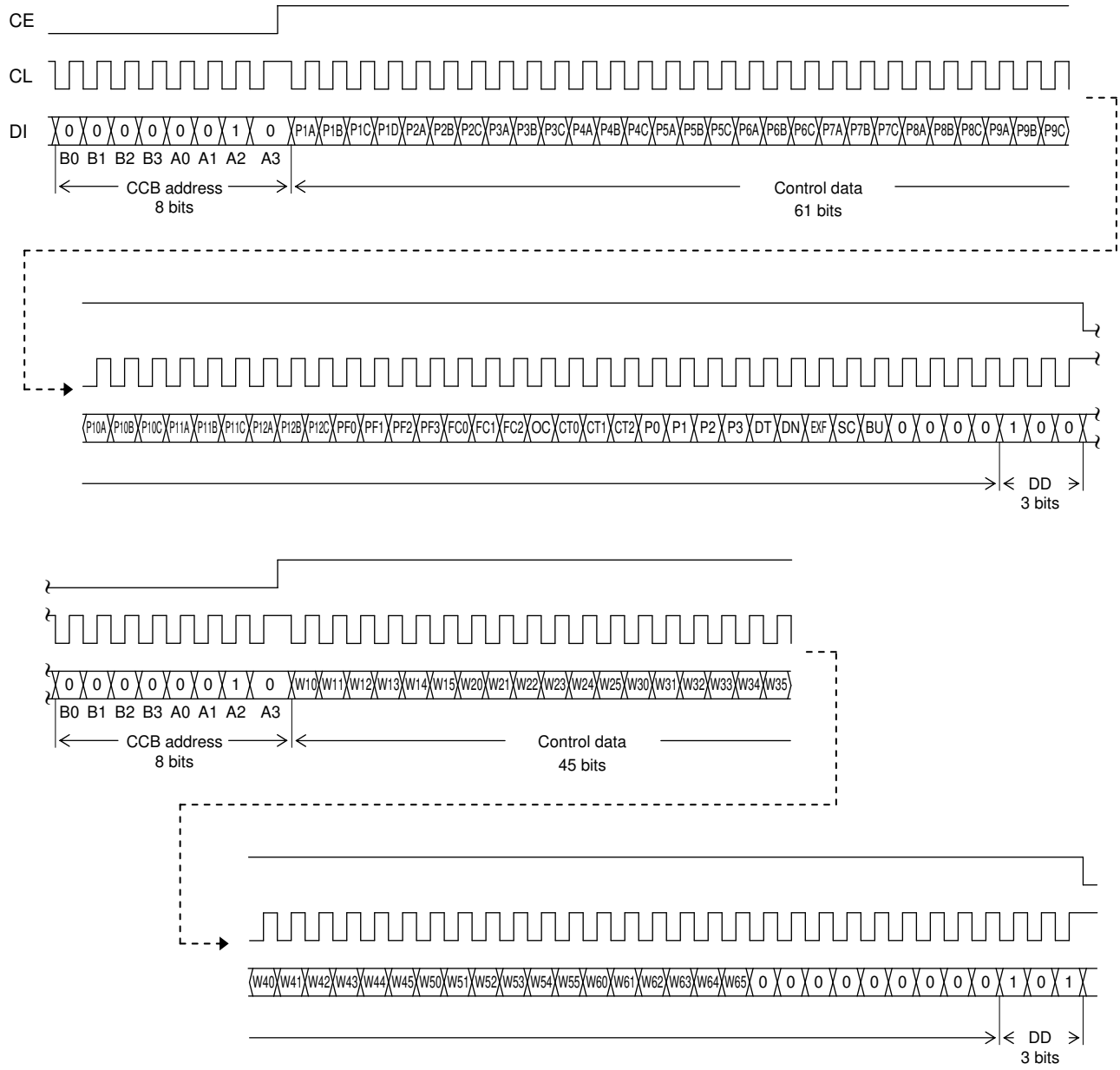
Note: DD is the direction data.

(2) When CL is stopped at the high level

• When the display data is transferred



• When the control data is transferred

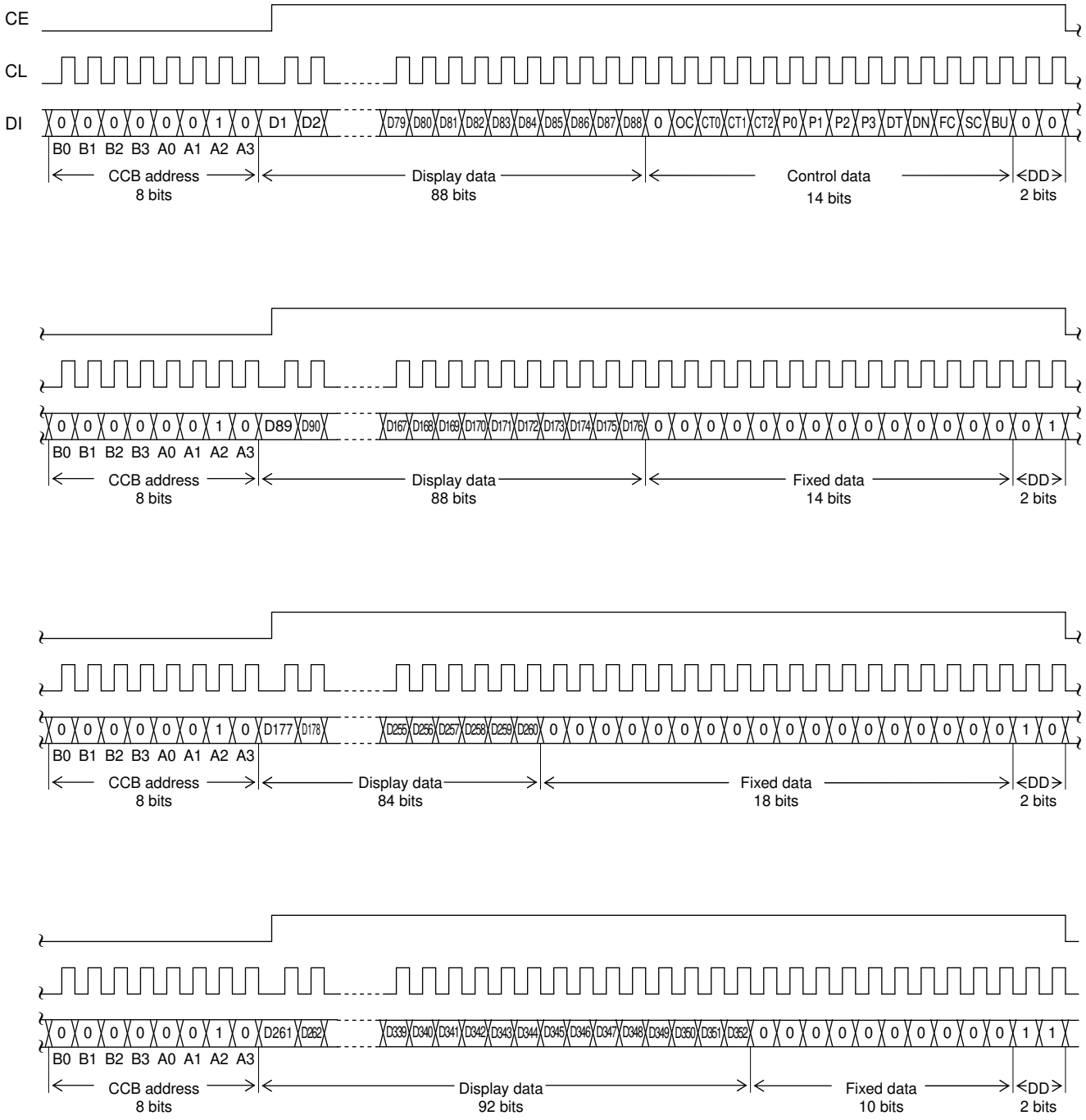


Note: DD is the direction data

- CCB address ..... "40H"
- D1 to D267 ..... Display data
- P1A, P1B, P1C, P1D ..... General-purpose output port (P1) function setting control data
- P2A, P2B, P2C to P12A, P12B, P12C ..... General-purpose output port (P2 to P12) function setting control data
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- CT0 to CT2 ..... Display contrast setting control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- DN ..... S88 pin and S89/OSCI pin state setting control data
- EXF ..... External clock operating frequency setting control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55, W60 to W65 ..... PWM data of the PWM output

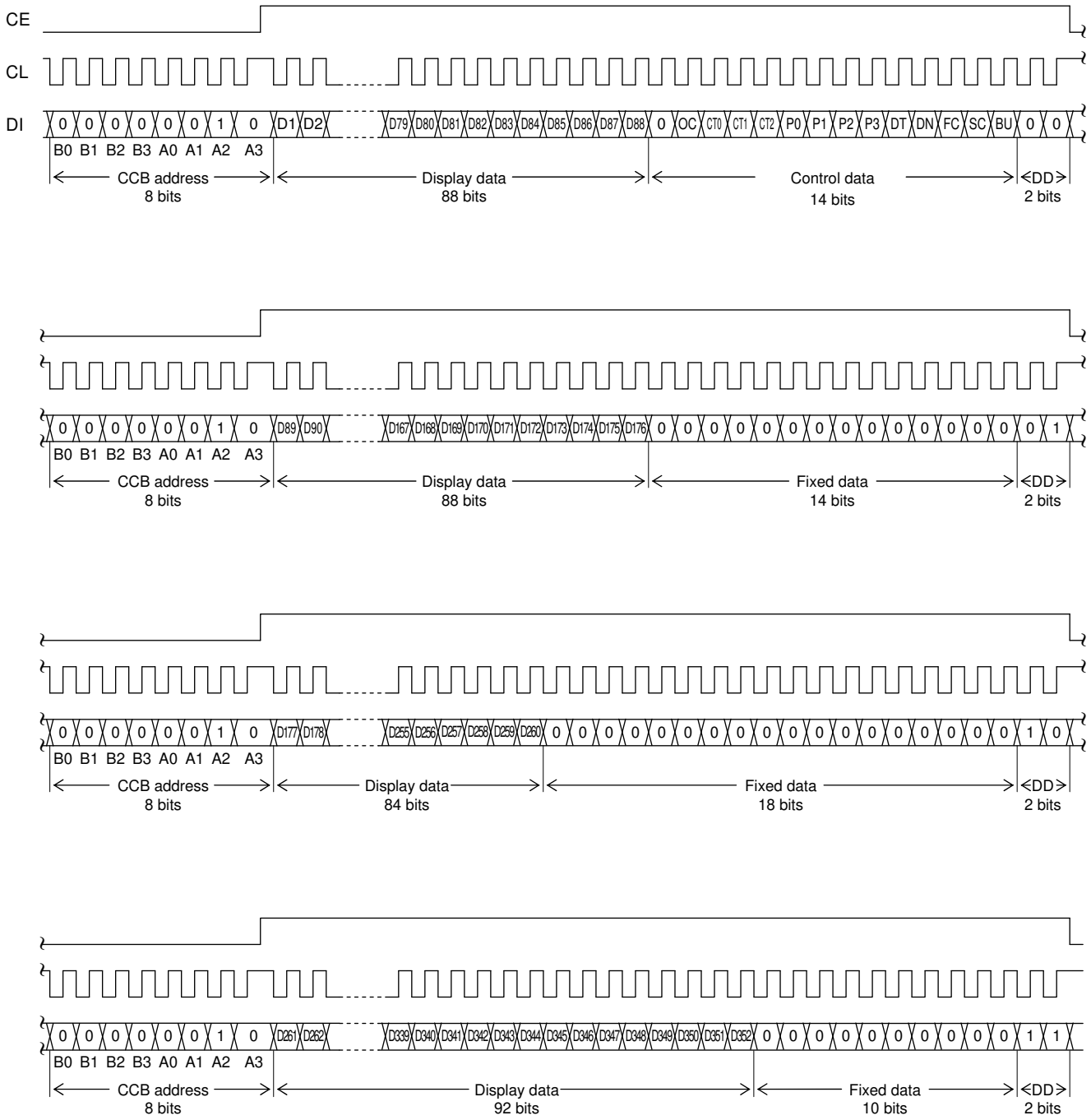
3. 1/4 duty (Simple mode transfer)

(1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the high level

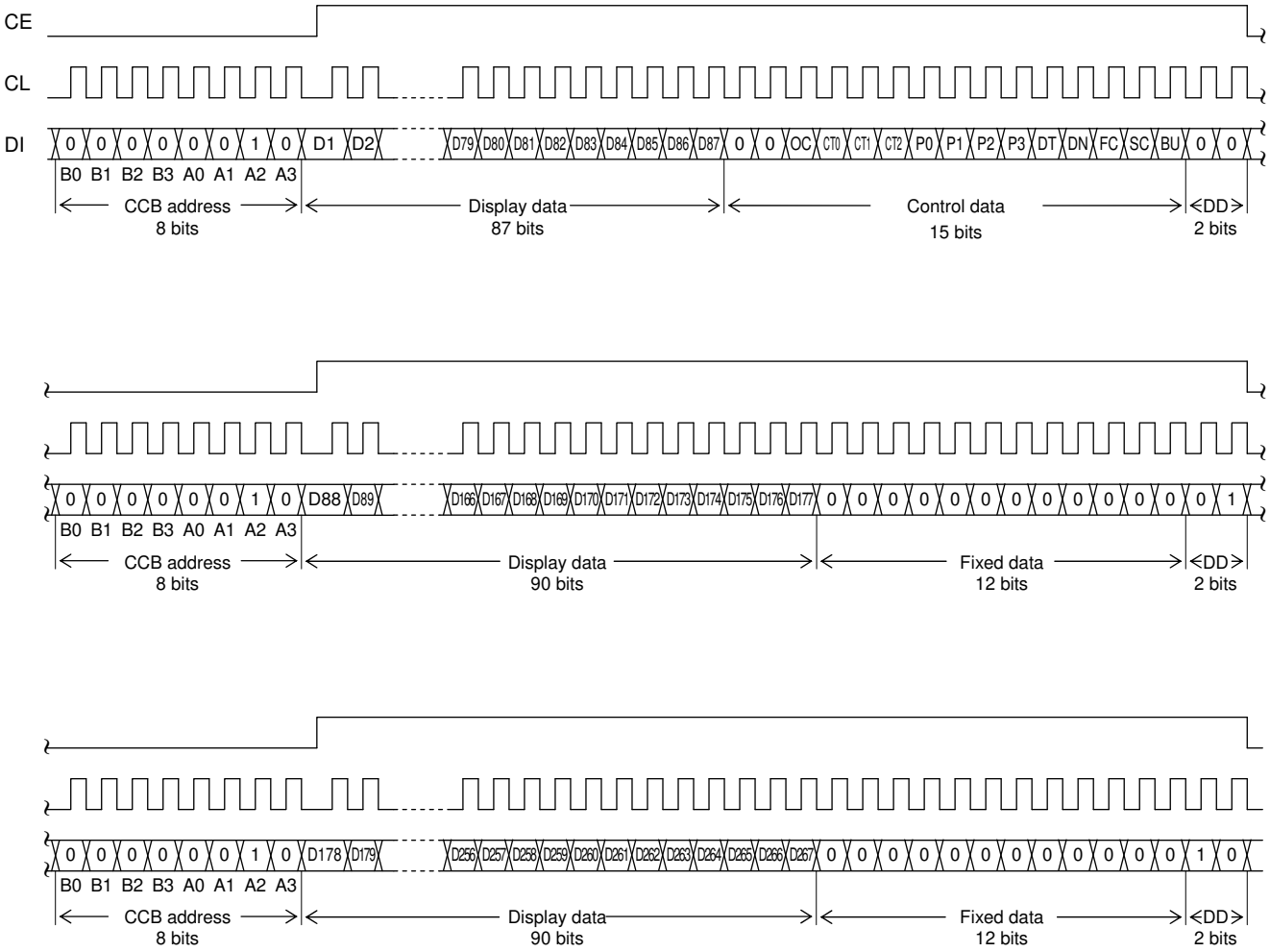


Note: DD is the direction data

- CCB address ..... "40H"
- D1 to D352 ..... Display data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- CT0 to CT2 ..... Display contrast setting control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- DN ..... S88 pin and S89/OSCI pin state setting control data
- FC ..... Common/segment output waveform frame frequency setting control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

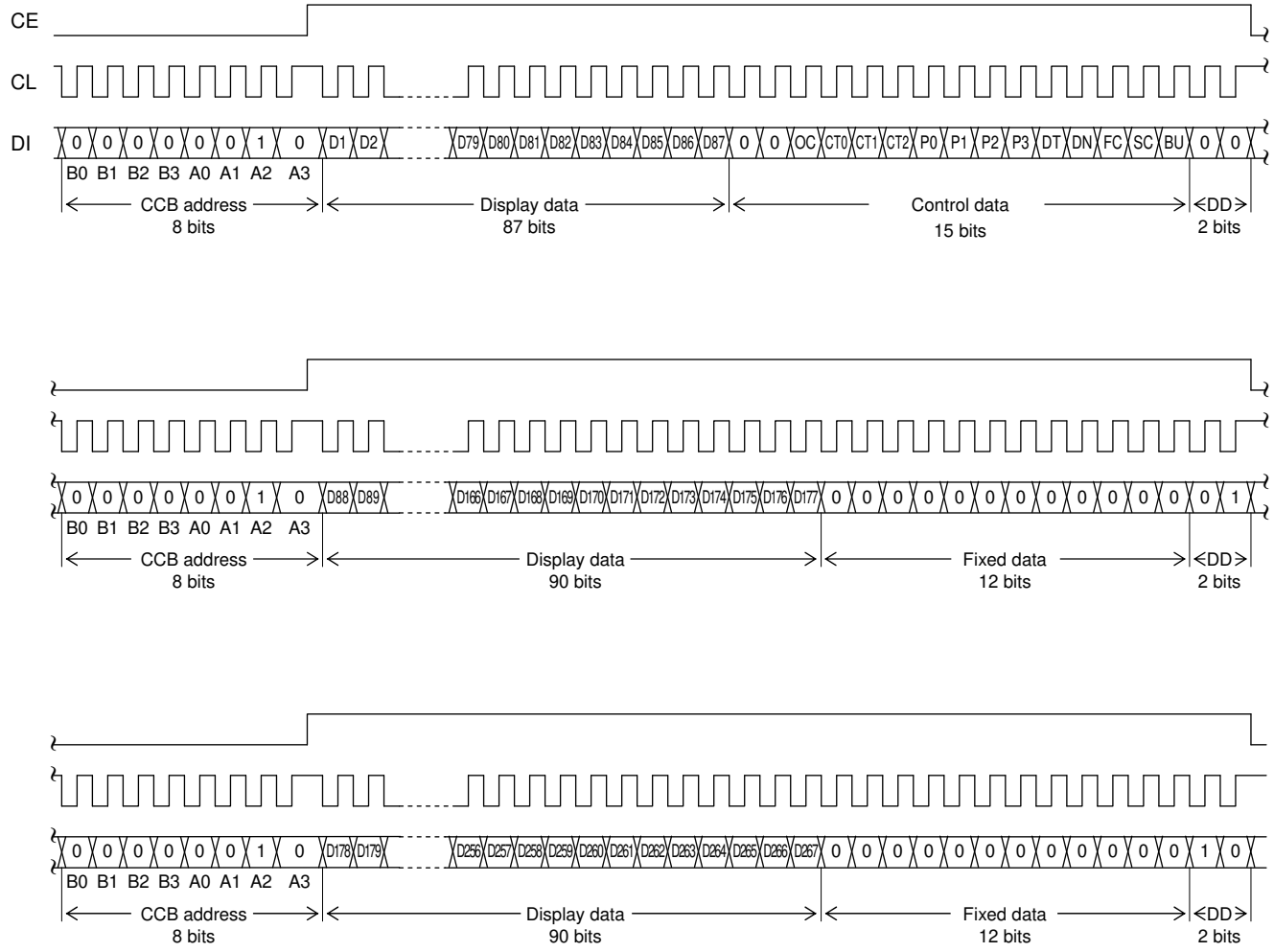
4. 1/3 duty (Simple mode transfer)

(1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the high level



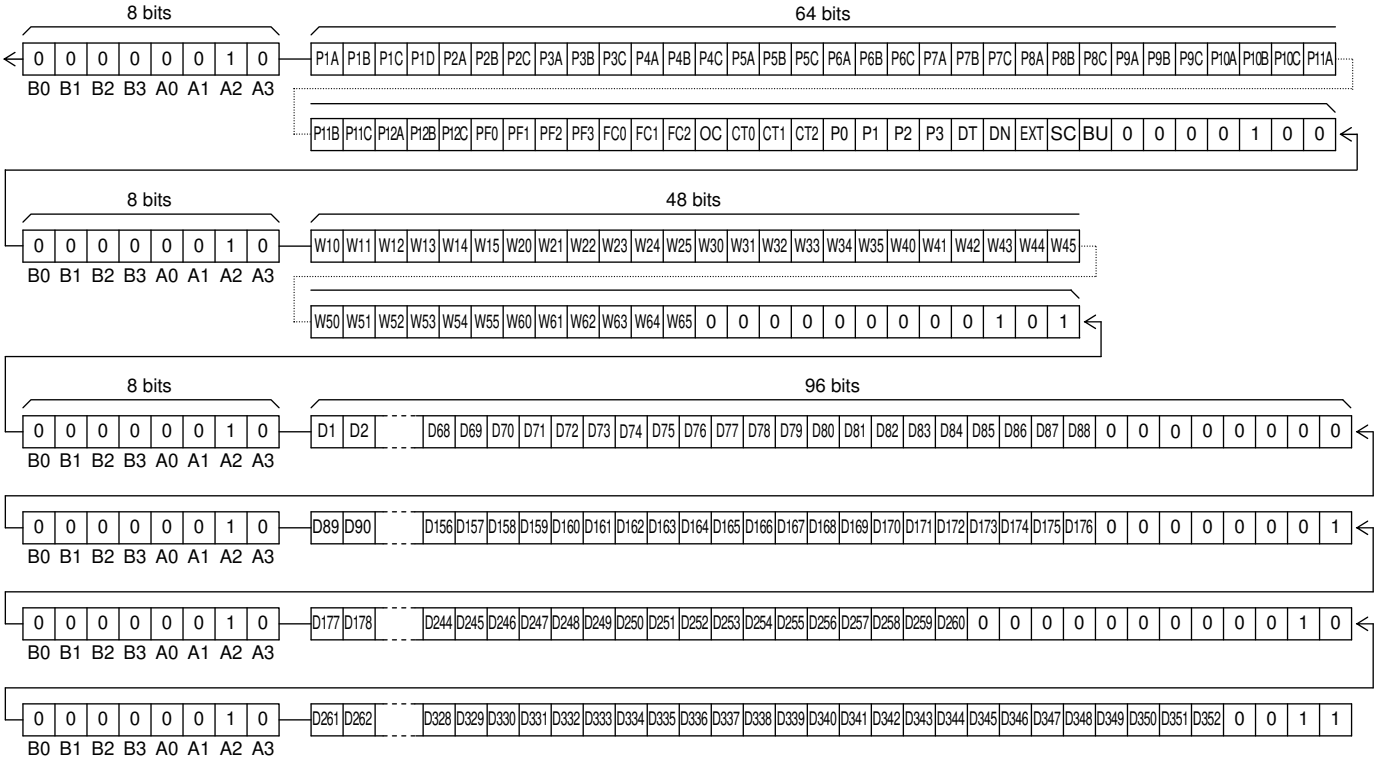
Note: DD is the direction data

- CCB address ..... "40H"
- D1 to D267 ..... Display data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- CT0 to CT2 ..... Display contrast setting control data
- P0 to P3 ..... Segment output port/general-purpose output port switching control data
- DT ..... 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- DN ..... S88 pin and S89/OSCI pin state setting control data
- FC ..... Common/segment output waveform frame frequency setting control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

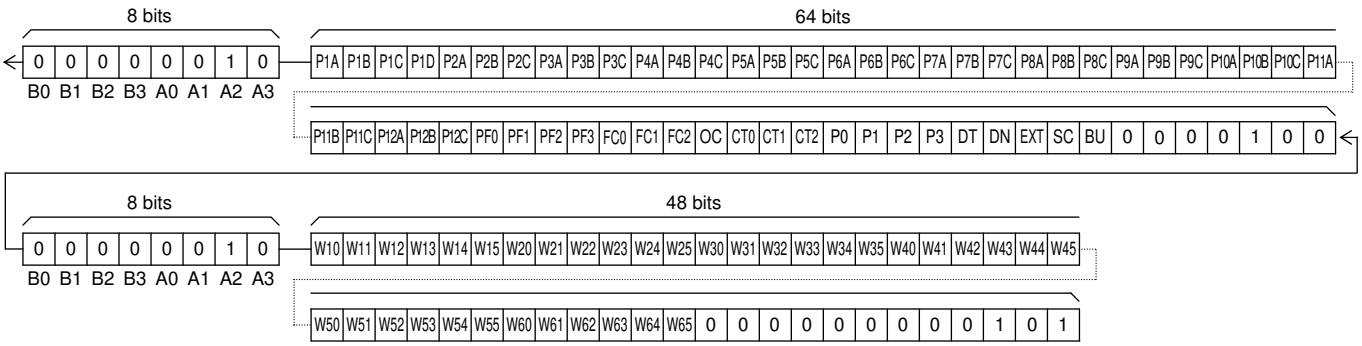
Serial Data Transfer Example

1. 1/4 duty

- When 261 or more segments are used
  All 496 bits of serial data must be sent.

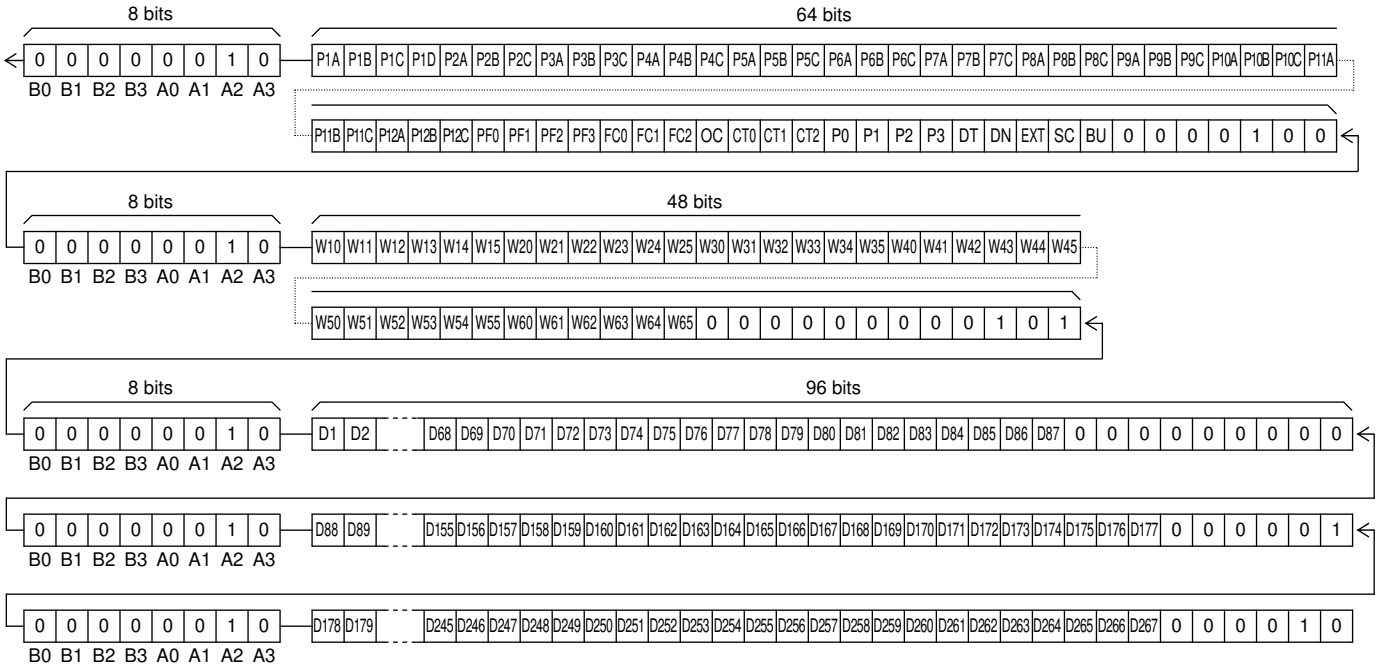


- When fewer than 261 segments are used
  The serial data shown below (the control data) must always be sent.

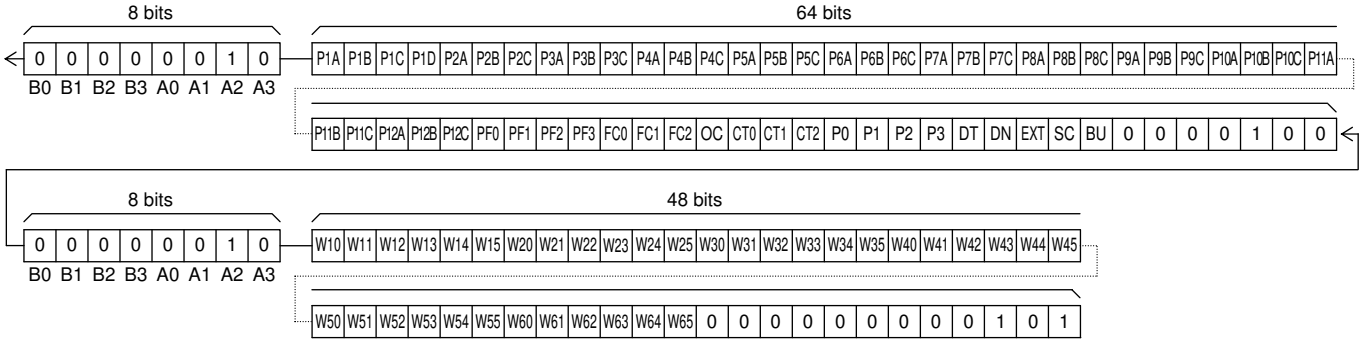


2. 1/3 duty

- When 178 or more segments are used
  All 400 bits of serial data must be sent.

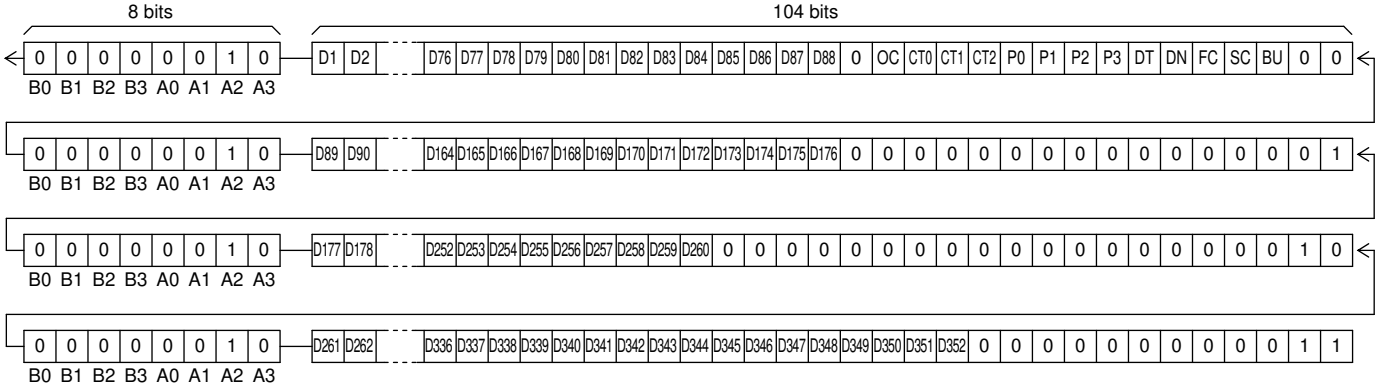


- When fewer than 178 segments are used
  The serial data shown below (the control data) must always be sent.

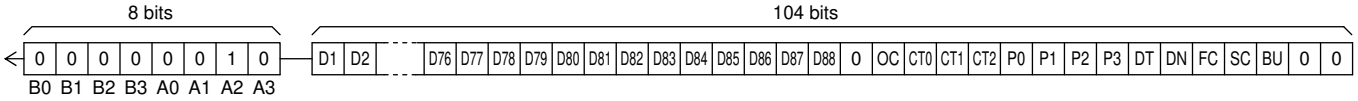


3. 1/4 duty (Simple mode transfer)

- When 261 or more segments are used
  All 416 bits of serial data must be sent.

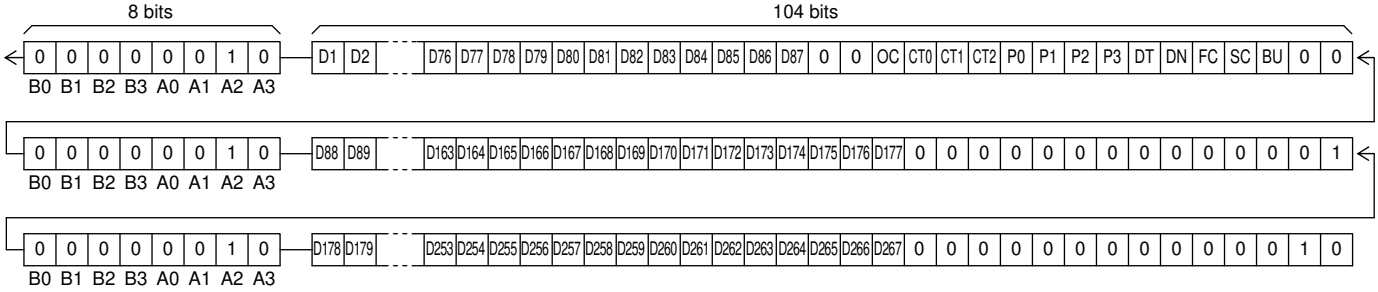


- When fewer than 261 segments are used
  Either 104, 208 or 312 bits of serial data must be sent, depending on the number of segments to be used.
  However, the serial data shown below (the D1 to D88 display data and the control data) must always be sent.

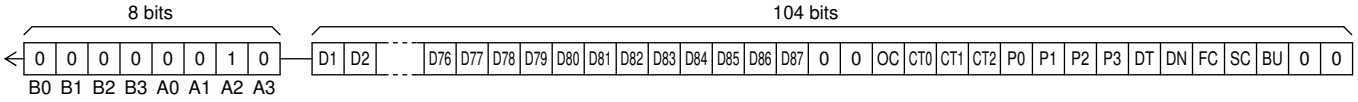


4. 1/3duty (Simple mode transfer)

- When 178 or more segments are used
  All 312 bits of serial data must be sent.



- When fewer than 178 segments are used
  Either 104 or 208 bits of serial data must be sent, depending on the number of segments to be used.
  However, the serial data shown below (the D1 to D87 display data and the control data) must always be sent.



Control Data Functions

(1) P1A,P1B,P1C,P1D ……. General-purpose output port (P1) function setting control data
P2A,P2B,P2C to P12A,P12B,P12C … General-purpose output port (P2 to P12) function setting control data
These control data bits set the general-purpose output function (High or low level output), PWM output function or clock output function of the P1 output pin, and the general-purpose output function (High or low level output) or PWM output function of the P2 to P12 output pins.
However, be careful of being unable to set a PWM output function when the external clock operating frequency is set the $f_{CK}2$=38[kHz]typ (EXF="1") in external clock operating mode (OC= "1").
In addition, be careful of setting of the general-purpose output function (High or low level output) in the case of the simple mode transfer forcibly.

P1A	P1B	P1C	P1D	General-purpose output port (P1) function
0	0	0	0	General-purpose output function (High or low level output)
1	0	0	0	PWM output function (Ch1) (Support for PWM data W10 to W15)
0	1	0	0	PWM output function (Ch2) (Support for PWM data W20 to W25)
1	1	0	0	PWM output function (Ch3) (Support for PWM data W30 to W35)
0	0	1	0	PWM output function (Ch4) (Support for PWM data W40 to W45)
1	0	1	0	PWM output function (Ch5) (Support for PWM data W50 to W55)
0	1	1	0	PWM output function (Ch6) (Support for PWM data W60 to W65)
1	1	1	0	Clock output function (Clock frequency : fosc/2, $f_{CK}/2$)
0	0	0	1	Clock output function (Clock frequency : fosc/8, $f_{CK}/8$)

Note : When are setting (P1A,P1B,P1C,P1D)=(1,X,X,1), (X,1,X,1), and (X,X,1,1), the function of general-purpose output ports P1 is set the general-purpose output function (High or low level output). X: don't care

PnA	PnB	PnC	General-purpose output port (P2 to P12) function
0	0	0	General-purpose output function (High or low level output)
1	0	0	PWM output function (Ch1) (Support for PWM data W10 to W15)
0	1	0	PWM output function (Ch2) (Support for PWM data W20 to W25)
1	1	0	PWM output function (Ch3) (Support for PWM data W30 to W35)
0	0	1	PWM output function (Ch4) (Support for PWM data W40 to W45)
1	0	1	PWM output function (Ch5) (Support for PWM data W50 to W55)
0	1	1	PWM output function (Ch6) (Support for PWM data W60 to W65)

Note1 : The data PnA, PnB and PnC (Note : n=2 to 12) are the control data switching the general-purpose output function or PWM output function of the general-purpose output ports Pn (Note : n=2 to 12).
For example, if the S10/P10 output pin is set the general-purpose output port, the general-purpose output port P10 pin is selected the PWM output function (Ch1)
when (P10A,P10B,P10C)=(1,0,0).

Note2 : When are setting (PnA,PnB,PnC)=(1,1,1) / (Note : n=2 to 12), the function of general-purpose output ports Pn (Note : n=2 to 12) is set the general-purpose output function (High or low level output).

(2) PF0 to PF3 … PWM output waveform frame frequency setting control data

These control data bits set the frame frequency of the PWM output waveforms. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2$=38[kHz]typ (EXF="1") in external clock operating mode (OC= "1") or when the serial data transfer is the simple mode transfer, these control data bits become invalid.

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)
0	0	0	0	fosc/1536	$f_{CK}1$/1536
1	0	0	0	fosc/1408	$f_{CK}1$/1408
0	1	0	0	fosc/1280	$f_{CK}1$/1280
1	1	0	0	fosc/1152	$f_{CK}1$/1152
0	0	1	0	fosc/1024	$f_{CK}1$/1024
1	0	1	0	fosc/896	$f_{CK}1$/896
0	1	1	0	fosc/768	$f_{CK}1$/768
1	1	1	0	fosc/640	$f_{CK}1$/640
0	0	0	1	fosc/512	$f_{CK}1$/512
1	0	0	1	fosc/384	$f_{CK}1$/384
0	1	0	1	fosc/256	$f_{CK}1$/256

Note : When is setting (PF0,PF1,PF2,PF3)=(1,1,0,1) and (X,X,1,1), the frame frequency is same as frame frequency at the time of the (PF0,PF1,PF2,PF3)=(1,0,1,0) setting (fosc/896, $f_{CK}1$/896). X: don't care

(3) FC0 to FC2 … Common/segment output waveform fram frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz] typ)
0	0	0	fosc/6144	$f_{CK}1$/6144	$f_{CK}2$/768
0	0	1	fosc/4608	$f_{CK}1$/4608	$f_{CK}2$/576
0	1	0	fosc/3072	$f_{CK}1$/3072	$f_{CK}2$/384
0	1	1	fosc/2304	$f_{CK}1$/2304	$f_{CK}2$/288
1	0	0	fosc/1536	$f_{CK}1$/1536	$f_{CK}2$/192
1	0	1	fosc/1152	$f_{CK}1$/1152	$f_{CK}2$/144
1	1	0	fosc/768	$f_{CK}1$/768	$f_{CK}2$/96

Note : When is setting (FC0,FC1,FC2)=(1,1,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,1,0) setting (fosc/3072, $f_{CK}1$/3072, $f_{CK}2$/384).

However, in the case of the simple mode transfer, the frame frequency of the common and segment output waveforms is set as following by the control data FC.

Control data	Common/segment output waveform frame frequency fo[Hz]	
FC	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 $f_{CK}1$=300[kHz] typ)
0	fosc/3072	$f_{CK}1$/3072
1	fosc/1536	$f_{CK}1$/1536

(4) OC … Internal oscillator operating mode/external clock operating mode switching control data
This control data bit selects either the internal oscillator operating mode or external clock operating mode.

OC	Fundamental clock operating mode	I/O pin (S89/OSCI) state
0	Internal oscillator operating mode	S89
1	External clock operating mode	OSCI

Note : S89 : Segment output
OSCI : External clock input

(5) CT0 to CT2 … Display contrast setting control data
These control data bits set display contrast.

CT0 to CT2 : Sets the display contrast (7 steps)

CT0	CT1	CT2	LCD drive 3/3 bias voltage $V_{DD}0$ level
0	0	0	$1.00V_{DD}=V_{DD}-(0.05V_{DD}\times0)$
1	0	0	$0.95V_{DD}=V_{DD}-(0.05V_{DD}\times1)$
0	1	0	$0.90V_{DD}=V_{DD}-(0.05V_{DD}\times2)$
1	1	0	$0.85V_{DD}=V_{DD}-(0.05V_{DD}\times3)$
0	0	1	$0.80V_{DD}=V_{DD}-(0.05V_{DD}\times4)$
1	0	1	$0.75V_{DD}=V_{DD}-(0.05V_{DD}\times5)$
0	1	1	$0.70V_{DD}=V_{DD}-(0.05V_{DD}\times6)$

Note : When is setting (CT0,CT1,CT2)=(1,1,1), the LCD drive 3/3 bias voltage $V_{DD}0$ level is $1.00V_{DD}$.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it can also be adjusted by modifying the supply pin V_{DD} voltage level.

(6) P0 to P3 … Segment output port/general-purpose output port switching control data
These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S12/P12 output pins.

Control data				Output pin state											
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8	S9/P9	S10/P10	S11/P11	S12/P12
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8	S9	S10	S11	S12
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8	S9	S10	S11	S12
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8	S9	S10	S11	S12
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8	S9	S10	S11	S12
1	0	0	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	S10	S11	S12
1	0	1	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	S11	S12
1	0	1	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	S12
1	1	0	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12

Note1 : Sn(n=1 to 12) : Segment output ports
Pn(n=1 to 12) : General-purpose output ports
Note2 : When are setting (P0,P1,P2,P3)=(1,1,0,1), (1,1,1,0), and (1,1,1,1), the all P1/S1 to P12/S12 output pins selects the segment output port.