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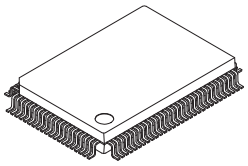
LC75810E, LC75810T

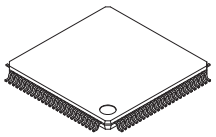
1/8 to 1/10-Duty Dot Matrix LCD Controller / Driver

ON Semiconductor®

www.onsemi.com



PQFP100 14x20 / QIP100E
[LC75810E]



TQFP100 14x14 / TQIP100
[LC75810T]

Overview

The LC75810E and LC75810T are 1/8 to 1/10 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75810E and LC75810T also provide on-chip character display ROM and RAM to allow display systems to be implemented easily.

Features

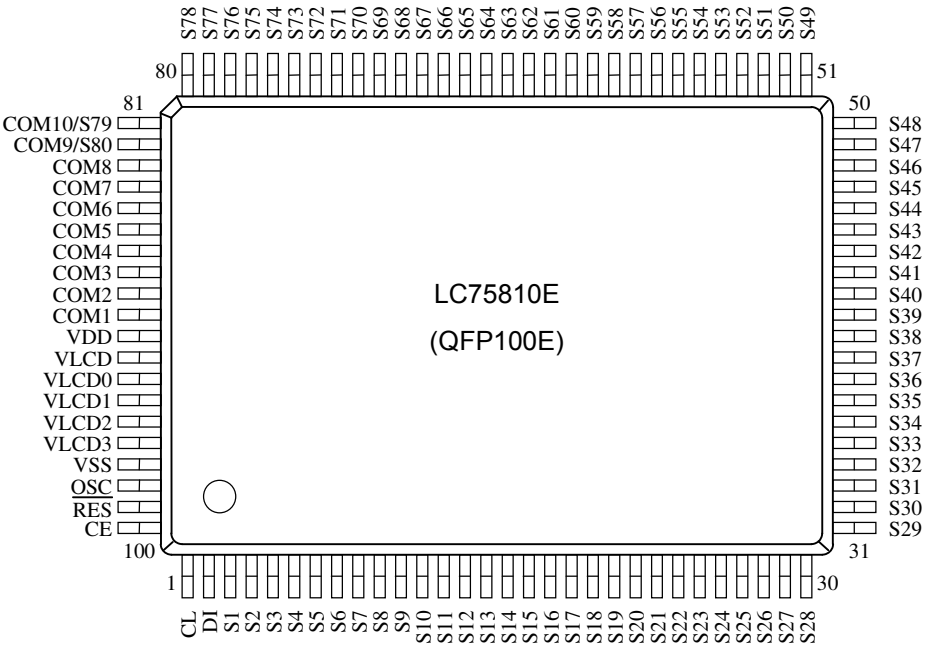
- Controls and drives a 5 × 7, 5 × 8, or 5 × 9 dot matrix LCD.
- Supports accessory display segment drive (up to 80 segments)
- Display technique:
  1/8-duty, 1/4-bias drive (5 × 7 dots, 6 × 7 dots)
  1/9-duty, 1/4-bias drive (5 × 8 dots, 6 × 8 dots)
  1/10-duty, 1/4-bias drive (5 × 9 dots, 6 × 9 dots)
- Display digits:
  16 digits × 1 line (5 × 7 dots),
  15 digits × 1 line (5 × 8 or 5 × 9 dots)
  13 digits × 1 line (6 × 7, 6 × 8, or 6 × 9 dots)
- Display control memory
  CGROM: 240 characters (5 × 7, 5 × 8, or 5 × 9 dots)
  CGRAM: 16 characters (5 × 7, 5 × 8, or 5 × 9 dots)
  DCRAM: 64 × 8 bits
  ALATCH: 80 bits
- Instruction function
  Display on/off control
  Smooth up, down, left, and right scrolling of the display
- Provides a backup function based on power saving mode
- The frame frequency of the common and segment output waveforms can be controlled by instructions.
- Built-in display contrast adjustment circuit
- Serial data input supports CCB* format communication with the system controller
- Independent LCD driver block power supply V_{LCD}
- Provides a $\overline{RES}$ pin for IC internal initialization.
- RC oscillator circuit

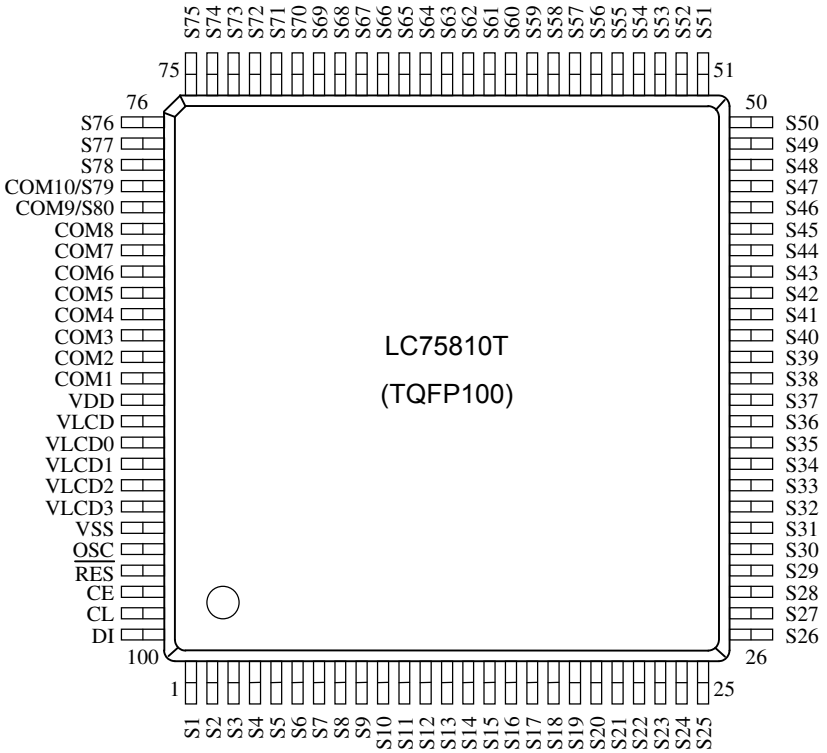
* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 55 of this data sheet.

Pin Assignments (Top view)





Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	−0.3 to +11.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{RES}$	−0.3 to +7.0	V
	$V_{IN}2$	OSC	−0.3 to V_{DD} + 0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$	−0.3 to V_{LCD} + 0.3	
Output voltage	$V_{OUT}1$	OSC	−0.3 to V_{DD}+ 0.3	V
	$V_{OUT}2$	$V_{LCD}0$, S1 to S80, COM1 to COM10	−0.3 to V_{LCD} + 0.3	
Output current	$I_{OUT}1$	S1 to S80	300	μA
	$I_{OUT}2$	COM1 to COM10	3	mA
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = −40 to + 85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	When the display contrast adjustment circuit is used.	7.0		10.0	
		When the display contrast adjustment circuit is not used.	4.5		10.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4 $V_{LCD}0$	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4 $V_{LCD}0$	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4 $V_{LCD}0$	$V_{LCD}0$	
Input high level voltage	V_{IH}	CE, CL, DI, $\overline{RES}$	0.8 V_{DD}		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{RES}$	0		0.2 V_{DD}	V
Recommended external resistance	Rosc	OSC		10		kΩ
Recommended external capacitance	Cosc	OSC		470		pF
Guaranteed oscillation range	fosc	OSC	150	300	600	kHz
Data setup time	tds	CL, DI (Figure 2)	160			ns
Data hold time	tdh	CL, DI (Figure 2)	160			ns
CE wait time	tcp	CE, CL (Figure 2)	160			ns
CE setup time	tcs	CE, CL (Figure 2)	160			ns
CE hold time	tch	CE, CL (Figure 2)	160			ns
High level clock pulse width	tϕH	CL (Figure 2)	160			ns
Low level clock pulse width	tϕL	CL (Figure 2)	160			ns
Minimum reset pulse width	tWRES	$\overline{RES}$ (Figure 3)	1			μs

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings min.	Ratings typ.	Ratings max.	Unit
Hysteresis	V_H	CE, CL, DI, $\overline{RES}$		$0.1V_{DD}$		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{RES}$: V_I = 6.0 V			5.0	μA
Input low level current	I_{IL}	CE, CL, DI, $\overline{RES}$: V_I = 0 V	−5.0			μA
Output high level voltage	$V_{OH}1$	S1 to S80: I_O = −20 μA	$V_{LCD}0$−0.6			V
	$V_{OH}2$	COM1 to COM10: I_O = −100 μA	$V_{LCD}0$−0.6			
Output low level voltage	$V_{OL}1$	S1 to S80: I_O = 20 μA			0.6	V
	$V_{OL}2$	COM1 to COM10: I_O = 100 μA			0.6	
Output middle level voltage ∗1	$V_{MID}1$	S1 to S80: I_O = ±20 μA	2/4 $V_{LCD}0$ −0.6		2/4 $V_{LCD}0$ +0.6	V
	$V_{MID}2$	COM1 to COM10: I_O = ±100 μA	3/4 $V_{LCD}0$ −0.6		3/4 $V_{LCD}0$ +0.6	
	$V_{MID}3$	COM1 to COM10: I_O = ±100 μA	1/4 $V_{LCD}0$ −0.6		1/4 $V_{LCD}0$ +0.6	
Oscillator frequency	fosc	OSC: R_{OSC} = 10 kΩ, C_{OSC} = 470 pF	210	300	390	kHz
Current drain	$I_{DD}1$	V_{DD}: Power saving mode			5	μA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, Output open, f_{OSC} = 300 kHz		700	1400	
	$I_{LCD}1$	V_{LCD}: Power saving mode			5	
	$I_{LCD}2$	V_{LCD}: V_{LCD} = 10.0 V, Output open, f_{OSC} = 300 kHz, When the display contrast adjustment circuit is used		450	900	
	$I_{LCD}3$	V_{LCD}: V_{LCD} = 10.0 V, Output open, f_{OSC} = 300 kHz, When the display contrast adjustment circuit is not used		200	400	

Note ∗1: Excluding the bias voltage generation divider resistors built into the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and V_{SS} pins. (See figure 1.)

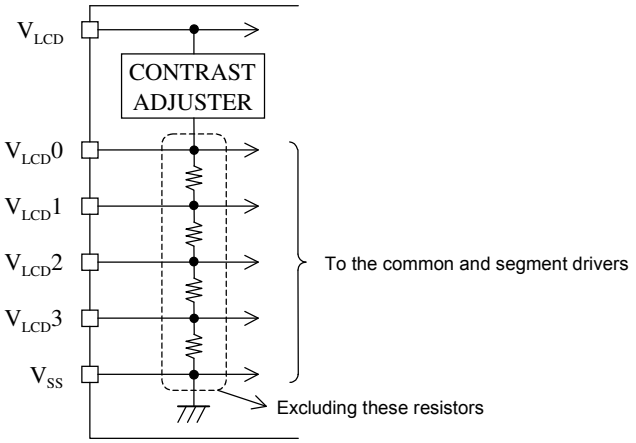
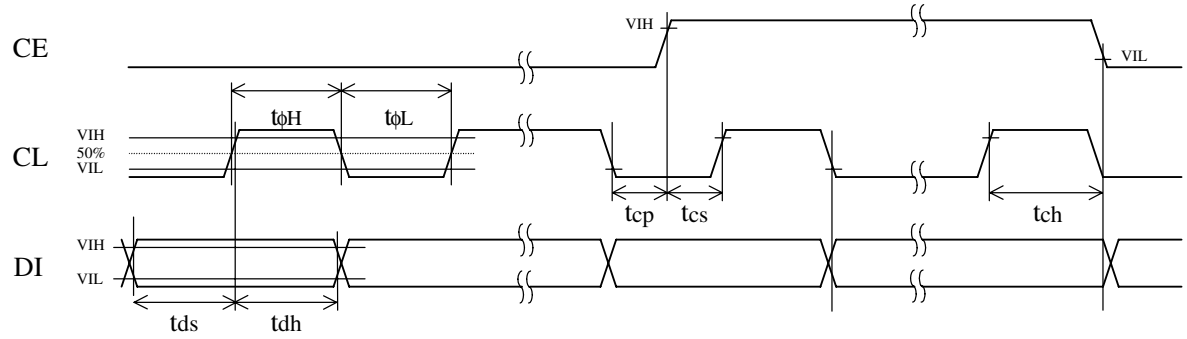


Figure 1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

• When CL is stopped at the low level



• When CL is stopped at the high level

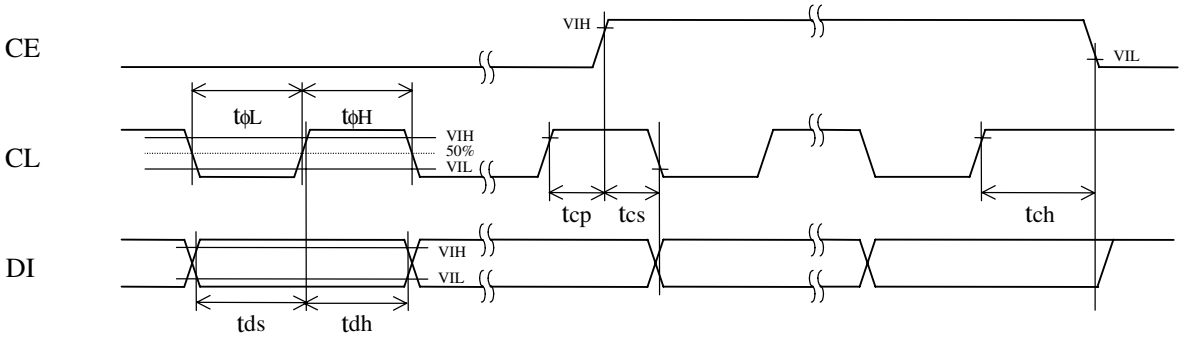
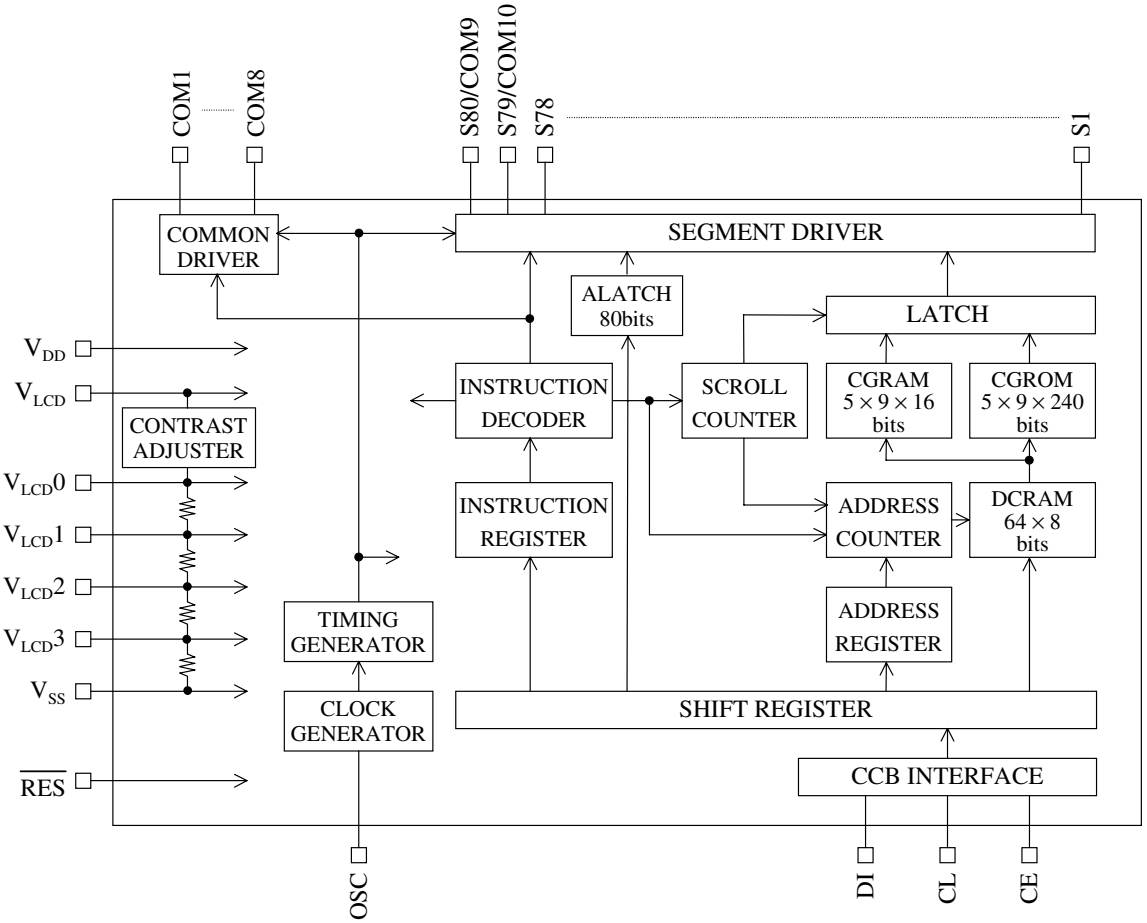


Figure 2

Block Diagram



Pin Functions

Pin	Pin No.		Function	Active level	I/O	Handling when unused
	LC75810E	LC75810T				
S1 to S78 S79/COM10 S80/COM9	3 to 80 81 82	1 to 78 79 80	Segment driver outputs The S79/COM10 and S80/COM9 pins can be used as common driver outputs under the “set display technique” instruction.	–	O	OPEN
COM1 to COM8	90 to 83	88 to 81	Common driver outputs	–	O	OPEN
OSC	98	96	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	–	I/O	VDD
CE	100	98	Serial data transfer inputs. These pins are connected to the microcontroller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H	I	GND
CL	1	99		↑	I	
DI	2	100		–	I	
$\overline{RES}$	99	97	Reset signal input • When $\overline{RES}$ is low (V_{SS}) – Display off S1 to S78 = “L” (V_{SS}) S79/COM10 and S80/COM9 = “L” (V_{SS}) COM1 to COM8 = “L” (V_{SS}) – Serial data transfer is disabled. – The OSC pin oscillator is stopped. • When $\overline{RES}$ is high (V_{DD}) – Display on after a “display on/off control” (display on state setting) instruction is executed. – Serial data transfers are enabled. – The OSC pin oscillator operates.	L	I	GND
$V_{LCD}0$	93	91	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, $V_{LCD}0$ must be greater than or equal to 4.5 V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	–	O	OPEN
$V_{LCD}1$	94	92	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 $V_{LCD}0$ voltage level externally.	–	I	OPEN
$V_{LCD}2$	95	93	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 $V_{LCD}0$ voltage level externally.	–	I	OPEN
$V_{LCD}3$	96	94	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 $V_{LCD}0$ voltage level externally.	–	I	OPEN
V_{DD}	91	89	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0 V.	–	–	–
V_{LCD}	92	90	LCD driver block power supply connection. Provide a voltage of between 7.0 and 10.0 V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 and 10.0 V when the circuit is not used.	–	–	–
V_{SS}	97	95	Power supply connection. Connect to ground.	–	–	–

Block Functions

• AC (Address counter)
AC is a counter that provides the DCRAM address.
The address is automatically modified internally, and the LCD display state is retained.

• DCRAM (Data control RAM)
DCRAM is the RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns using CGROM or CGRAM.)
DCRAM has a capacity of 64 × 8 bits, and can hold 64 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

・For a 64 digits × 1 line display structure (For a "set display technique" instruction with 0Z1 = 0 and 0Z2 = 0)
When the DCRAM address loaded into AC is 00H

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		61	62	63	64
DCRAM address (hexadecimal)	First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11		3C	3D	3E	3F

However, when the display smooth scrolling is performed, the DCRAM address shifts as follows.

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		61	62	63	64	
DCRAM address (hexadecimal)	First line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12		3D	3E	3F	00	Shift to the left by 1 character digit

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		61	62	63	64	
DCRAM address (hexadecimal)	First line	3F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10		3B	3C	3D	3E	Shift to the right by 1 character digit

Note that the display area on the LCD is display digits 1 to 16 on the first line when a display technique is 5 × 7, 5 × 8, or 5 × 9 dots, and it is display digits 1 to 13 on the first line when a display technique is 6 × 7, 6 × 8, or 6 × 9 dots.

・For a 32 digits × 2 lines display structure (For a "set display technique" instruction with 0Z1 = 1 and 0Z2 = 0)
When the DCRAM address loaded into AC is 00H

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		29	30	31	32
DCRAM address (hexadecimal)	First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11		1C	1D	1E	1F
	Second line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31		3C	3D	3E	3F

However, when the display smooth scrolling is performed, the DCRAM address shifts as follows.

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		29	30	31	32	
DCRAM address (hexadecimal)	First line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12		1D	1E	1F	00	Shift to the left by 1 character digit
	Second line	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32		3D	3E	3F	20	

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		29	30	31	32	
DCRAM address (hexadecimal)	First line	1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10		1B	1C	1D	1E	Shift to the right by 1 character digit
	Second line	3F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30		3B	3C	3D	3E	

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		29	30	31	32	
DCRAM address (hexadecimal)	First line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31		3C	3D	3E	3F	Shift to the up or down by 1 character digit
	Second line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11		1C	1D	1E	1F	

Note that the display area on the LCD is display digits 1 to 16 on the first line when a display technique is 5 × 7, 5 × 8, or 5 × 9 dots, and it is display digits 1 to 13 on the first line when a display technique is 6 × 7, 6 × 8, or 6 × 9 dots.

・For a 16 digits × 4 lines display structure (For a "set display technique" instruction with 0Z1 = 0 and 0Z2 = 1)
When the DCRAM address loaded into AC is 00H

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (hexadecimal)	First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	Second line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
	Third line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
	Fourth line	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F

However, when the display smooth scrolling is performed, the DCRAM address shifts as follows.

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
DCRAM address (hexadecimal)	First line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00	Shift to the left by 1 character digit
	Second line	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	
	Third line	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	20	
	Fourth line	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	30	

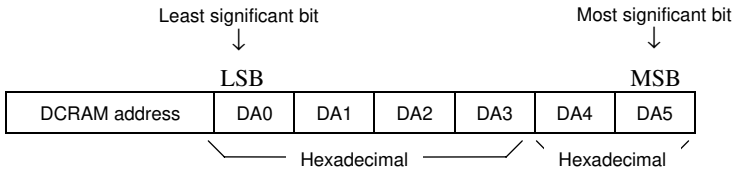
Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
DCRAM address (hexadecimal)	First line	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	Shift to the right by 1 character digit
	Second line	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	
	Third line	2F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	
	Fourth line	3F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
DCRAM address (hexadecimal)	First line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
	Second line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	Shift to the up by 1 character digit
	Third line	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	
	Fourth line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
DCRAM address (hexadecimal)	First line	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	
	Second line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	Shift to the down by 1 character digit
	Third line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
	Fourth line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	

Note that the display area on the LCD is display digits 1 to 16 on the first line when a display technique is 5 × 7, 5 × 8, or 5 × 9 dots, and it is display digits 1 to 13 on the first line when a display technique is 6 × 7, 6 × 8, or 6 × 9 dots.

Note ∗2: The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is 2EH

DA0	DA1	DA2	DA3	DA4	DA5
0	1	1	1	0	1

Note ∗3: 5 × 7 dots ··· 16-digit display 5 × 7 dots.
5 × 8 dots ··· 16-digit display 4 × 8 dots.
5 × 9 dots ··· 16-digit display 3 × 9 dots.
6 × 7 dots ··· 13-digit display 6 × 7 dots.
6 × 8 dots ··· 13-digit display 6 × 8 dots.
6 × 9 dots ··· 13-digit display 6 × 9 dots.

・CGROM (Character generator ROM)
CGROM is the ROM that is used to generate the 240 kinds of 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240 × 45 bits. When a character code is written to DCRAM, the character pattern stored in the CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

・CGRAM (Character generator RAM)
CGRAM is the RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5 × 7, 5 × 8, or 5 × 9 dot matrix character patterns can be stored. CGRAM has a capacity of 16 × 45 bits.

・ALATCH (Additional data latch)
ALATCH is the latch that is used to store the ADATA display data for the accessory display. ALATCH has a capacity of 80 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM.

・SC (Scroll counter)
SC is the counter that is used to scroll the display in the left, right, up, or down directions in dot units. Since this function scrolls in dot units, it implements smooth scrolling.

Reset Function

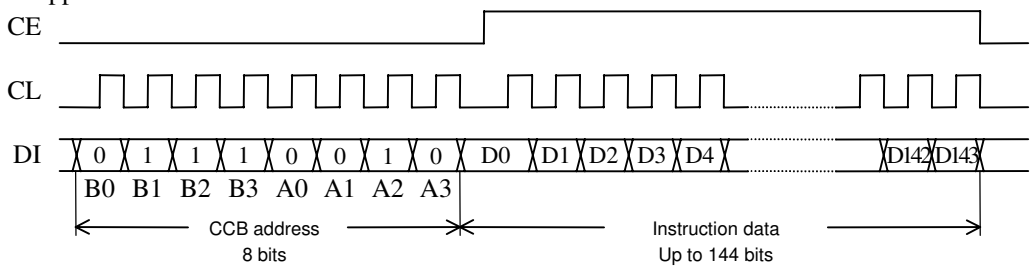
The LC75810E and LC75810T are reset when a low level is applied to the $\overline{RES}$ pin at power on and, in normal mode. On a reset the LC75810E and LC75810T create a display with all LCD panels turned off. However, after a reset applications must set the contents of DCRAM, ALATCH, and CGRAM before turning on display with a “display on/off control” instruction since the contents of these memories are undefined. That is, applications must execute the following instructions.

- Set display technique
- DCRAM data write
- ALATCH data write (If ALATCH is used.)
- CGRAM data write (IF CGRAM is used.)
- Set AC and SC addresses
- Set display contrast (If the display contrast adjustment circuit is used.)

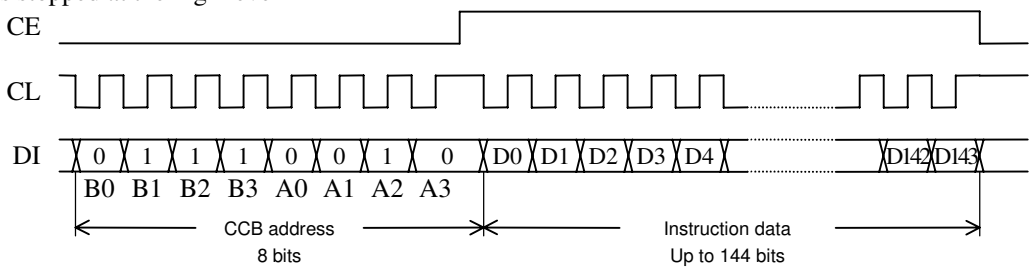
After executing the above instructions, applications must turn on the display with a “display on/off control” instruction. Note that when applications turn off in the normal mode, applications must turn off the display with a “display on/off control” instruction. (See the detailed instruction descriptions.)

Serial Data Transfer Format

• When CL is stopped at the low level



• When CL is stopped at the high level



・CCB address: 4EH

・D0 to D143: Instruction data
The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

Instruction	D0 D1 ··· D55	D56 D57 ··· D79	D80 D81 ··· D111	D112 D113 D114 D115 D116 D117 D118 D119	D120 D121 D122 D123 D124 D125 D126 D127	D128 D129 D130 D131 D132 D133 D134 D135	D136 D137 D138 D139	D140 D141 D142 D143	Execution time (∗4)
Set display technique						OZ1 OZ2 DW X X X X X	DT1 DT2 FC 0	0 0 0 1	0 µs
Display on/off control					DG1 DG2 DG3 DG4 DG5 DG6 DG7 DG8	DG9 DG10 DG11 DG12 DG13 DG14 DG15 DG16	M A SC BU	0 0 1 0	0 µs/27 µs (∗5)
Display scroll					HS0 HS1 HS2 X X X X X	VS0 VS1 VS2 VS3 X X X X	R/L D/U X 0	0 0 1 1	27 µs/162 µs (∗6)
Set AC and SC addresses				HA0 HA1 HA2 X X X X X	VA0 VA1 VA2 VA3 X X X X	DA0 DA1 DA2 DA3 DA4 DA5 X X	X X X 0	0 1 0 0	27 µs
DCRAM data write (∗7)					AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7	DA0 DA1 DA2 DA3 DA4 DA5 X X	IM1 IM2 X 0	0 1 0 1	27 µs/ti µs (∗8)
ALATCH data write		AD1 AD2 ··· AD24	AD25 AD26 ··· AD56	AD57 AD58 AD59 AD60 AD61 AD62 AD63 AD64	AD65 AD66 AD67 AD68 AD69 AD70 AD71 AD72	AD73 AD74 AD75 AD76 AD77 AD78 AD79 AD80	X X X 0	0 1 1 0	0 µs
CGRAM data write (∗9)			CD1 CD2 ··· CD32	CD33 CD34 CD35 CD36 CD37 CD38 CD39 CD40	CD41 CD42 CD43 CD44 CD45 X X X	CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7	WM X X 0	0 1 1 1	27 µs/40.5 µs (∗10)
Set display contrast						CT0 CT1 CT2 CT3 X X X X	CTC X X 0	1 0 0 0	0 µs

X: don't care

Notes ∗4: The execution times listed here apply when fosc = 300 kHz. The execution times differ when the oscillator frequency fosc differs.

Example: When fosc = 210 kHz

$$27\,\mu s \times \frac{300}{210} = 39\,\mu s \qquad 162\,\mu s \times \frac{300}{210} = 232\,\mu s \qquad ti\,\mu s \times \frac{300}{210} = ti \times 1.43\,\mu s \qquad 40.5\,\mu s \times \frac{300}{210} = 58\,\mu s$$

∗5: Note that when the power saving mode (BU = 1) is set, the execution time is 27 µs (when fosc = 300 kHz).

∗6: The execution time must be seen as being 162 µs (when fosc = 300 kHz) if another "display scroll" instruction is executed immediately after a preceding "display scroll" instruction.

∗7, ∗8: Note that the data format differs when a "DCRAM data write" instruction is executed in normal increment mode (IM1 = 1, IM2 = 0) or super-increment mode (IM1 = 0, IM2 = 1).
Also note that the execution time is ti µs (when fosc = 300 kHz) if a "DCRAM data write" instruction is executed in super-increment mode. (See detailed instruction descriptions.)

∗9, ∗10: Note that the data format differs when a "CGRAM data write" instruction is executed in double write mode (WM = 1). Also note that the execution time is 40.5 µs (when fosc = 300 kHz) if a "CGRAM data write" instruction is executed in double write mode. (See detailed instruction descriptions.)

Detailed Instruction Descriptions

• Set display technique ··· <Sets the display technique.>

Code															
D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
OZ1	OZ2	DW	X	X	X	X	X	DT1	DT2	FC	0	0	0	0	1

X:don't care

DT1, DT2: Set the display technique

DT1	DT2	Display technique	Output pins	
			S80/COM9	S79/COM10
0	0	1/8 duty, 1/4 bias drive	S80	S79
1	0	1/9 duty, 1/4 bias drive	COM9	S79
0	1	1/10 duty, 1/4 bias drive	COM9	COM10

∗11: Sn (n = 79, 80): Segment output
COMn (n = 9, 10): Common output

FC: Set the frame frequency of the common and segment output waveforms

FC	Frame frequency		
	1/8 duty, 1/4 bias drive f8[Hz]	1/9 duty, 1/4 bias drive f9[Hz]	1/10 duty, 1/4 bias drive f10[Hz]
0	$\frac{fosc}{3072}$	$\frac{fosc}{3456}$	$\frac{fosc}{3840}$
1	$\frac{fosc}{1536}$	$\frac{fosc}{1728}$	$\frac{fosc}{1920}$

OZ1, OZ2: Set the display structure

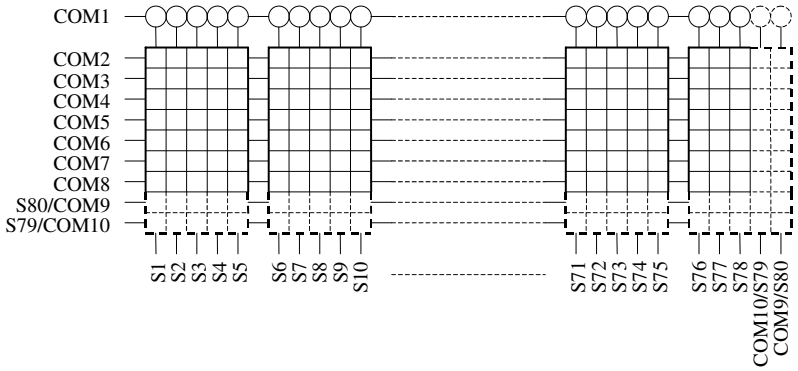
OZ1	OZ2	Display structure
0	0	64 digits × 1 line display structure
1	0	32 digits × 2 lines display structure
0	1	16 digits × 4 lines display structure

∗12: See block functions (DCRAM)

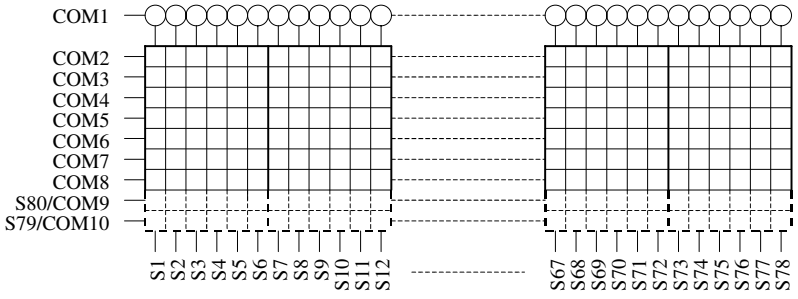
DW: Set the dot font width

DW	Dot font width	Number of display digits
0	5-dot font width	16 digits × 1 line (5 × 7 dots), 15 digits × 1 line (5 × 8 or 5 × 9 dots)
1	6-dot font width	13 digits × 1 line (6 × 7, 6 × 8, or 6 × 9 dots)

∗13: • 5-dot font width (5 × 7, 5 × 8, or 5 × 9 dots)



• 6-dot font width (6 × 7, 6 × 8, or 6 × 9 dots)



• Display on/off control ··· <Turns the display on or off.>

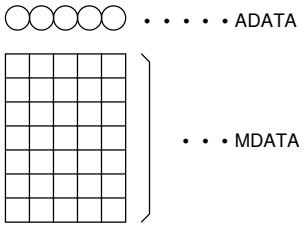
Code																								
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	DG14	DG15	DG16	M	A	SC	BU	0	0	1	0

M, A: Specifies the data to be turned on or off.

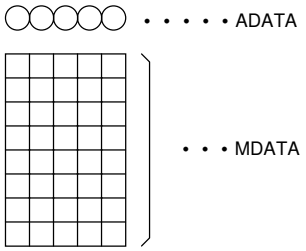
M	A	Display operating state
0	0	Both MDATA and ADATA are turned off. (The display is forcibly turned off, regardless of the DG1 to DG16 data.)
0	1	Only ADATA is turned on. (The ADATA of display digits specified by the DG1 to DG16 data are turned on.)
1	0	Only MDATA is turned on. (The MDATA of display digits specified by the DG1 to DG16 data are turned on.)
1	1	Both MDATA and ADATA are turned on. (The MDATA and ADATA of display digits specified by the DG1 to DG16 data are turned on.)

*14: MDATA, ADATA

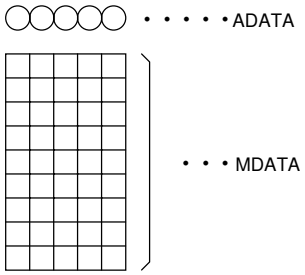
5 × 7 dot matrix



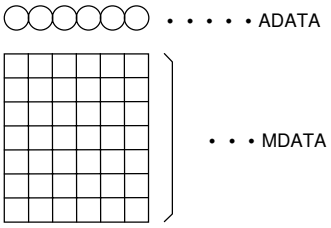
5 × 8 dot matrix



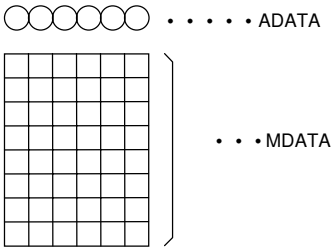
5 × 9 dot matrix



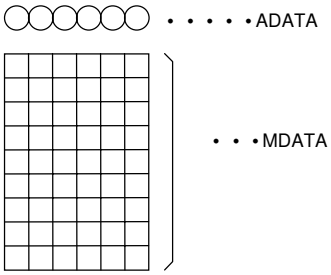
6 × 7 dot matrix



6 × 8 dot matrix



6 × 9 dot matrix



DG1 to DG16: Specifies the display digit.

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Display digit data	DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	DG14	DG15	DG16

For example, if DG1 to DG8 are 1, and DG9 to DG16 are 0, then display digits 1 to 8 will be turned on, and display digits 9 to 16 will be turned off (blanked).

SC: Controls the common and segment output pins.

SC	Common and segment output pin states
0	Output of LCD drive waveforms
1	Fixed at the V_{SS} level (all segments off)

Note *15: When SC is 1, the S1 to S80 and COM1 to COM10 output pins are set to the V_{SS} level, regardless of the M, A, and DG1 to DG16 data.

BU: Controls the normal mode and power saving mode.

BU	Mode
0	Normal mode
1	Power saving mode (In this mode, the OSC pin oscillator is stopped, and the common and segment pins are set to the V_{SS} level. In this mode, instructions other than the “display on/off control” and “set display contrast” instructions cannot be executed. Thus applications must set the IC to normal mode before executing any of the other instructions.)

• Display scroll ··· <Scrolls the display smoothly.>

Code																							
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
HS0	HS1	HS2	X	X	X	X	X	VS0	VS1	VS2	VS3	X	X	X	X	R/L	D/U	X	0	0	0	1	1

X: don't care

HS0 to HS2: Set the amount of smooth scrolling to be applied to MDATA in the left/right direction.

HS0	HS1	HS2	Amount of smooth scrolling to be applied to MDATA in the left/right direction
0	0	0	No shift in either the left or right direction
1	0	0	Shift 1 dot to the left or right. (The shift direction (left or right) is specified with the R/L data.)
0	1	0	Shift 2 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.)
1	1	0	Shift 3 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.)
0	0	1	Shift 4 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.)
1	0	1	Shift 5 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.)
0	1	1	Shift 6 dots to the left or right. (The shift direction (left or right) is specified with the R/L data.)

VS0 to VS3: Set the amount of smooth scrolling to be applied to MDATA in the up/down direction.

VS0	VS1	VS2	VS3	Amount of smooth scrolling to be applied to MDATA in the up/down direction
0	0	0	0	No shift in either the up or down direction
1	0	0	0	Shift 1 dot to the up or down. (The shift direction (up or down) is specified with the D/U data.)
0	1	0	0	Shift 2 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
1	1	0	0	Shift 3 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
0	0	1	0	Shift 4 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
1	0	1	0	Shift 5 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
0	1	1	0	Shift 6 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
1	1	1	0	Shift 7 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
0	0	0	1	Shift 8 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.)
1	0	0	1	Shift 9 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.) (∗16)
0	1	0	1	Shift 10 dots to the up or down. (The shift direction (up or down) is specified with the D/U data.) (∗17)

Notes: ∗16: This shift cannot be used when MDATA is 5 × 7 or 6 × 7 dots.
∗17: This shift cannot be used when MDATA is 5 × 7, 5 × 8, 6 × 7 or 6 × 8 dots.

R/L: Specifies the MDATA shift direction (left or right).

R/L	MDATA shift direction (left or right)
0	Shift left
1	Shift right

D/U: Specifies the MDATA shift direction (up or down).

D/U	MDATA shift direction (up or down)
0	Shift up
1	Shift down

∗18 Example of the "display scroll" instruction execution

Assume that a 32 digits × 2 lines display structure (OZ1 = 1, OZ2 = 0) has been set up with the "set display technique" instruction, and that the following data has been written to DCRAM with the "DCRAM data write" instruction.

Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
DCRAM data	First line	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	<	>	z	y	x	w
	Second line	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v

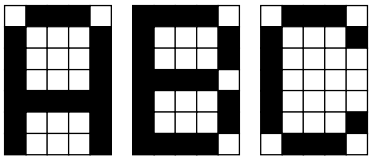
• Display state (1)

With no shifting in any direction, left, right, up, or down.

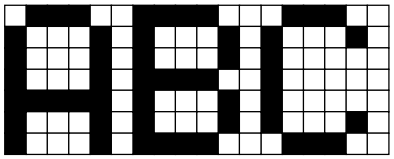
HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	0	0	0	0	0	0	X	X

X: don't care

(5 × 7 dot matrix)



(6 × 7 dot matrix)

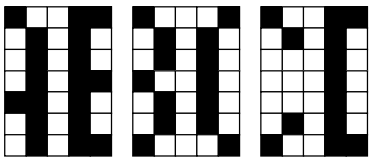


• Display state (2)

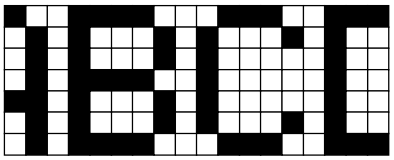
Shifted 3 dots to the left relative to display state (1)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
1	1	0	0	0	0	0	0	0

(5 × 7 dot matrix)



(6 × 7 dot matrix)



• Display state (3)

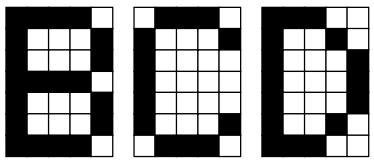
Shifted 6 dots to the left relative to display state (1)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	1	1	0	0	0	0	0	0

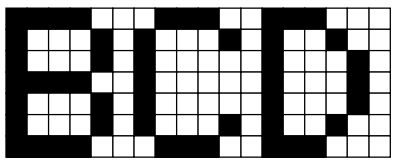
Shifted 3 dots to the left relative to display state (2)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
1	1	0	0	0	0	0	0	0

(5 × 7 dot matrix)



(6 × 7 dot matrix)

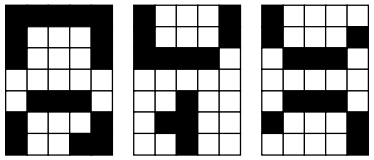


・Display state (4)

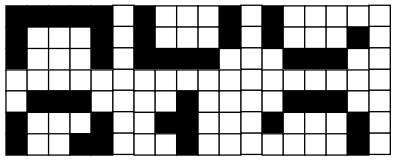
Shifted 4 dots to the up relative to display state (1)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	0	0	0	0	1	0	0	0

(5 × 7 dot matrix)



(6 × 7 dot matrix)



・Display state (5)

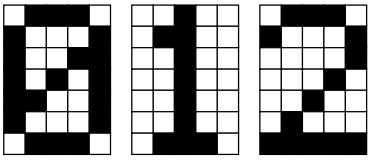
Shifted 8 dots to the up relative to display state (1)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	0	0	0	0	0	1	0	0

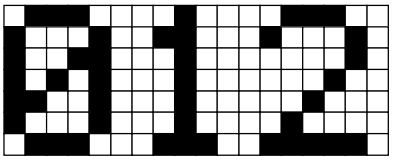
Shifted 4 dots to the up relative to display state (4)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	0	0	0	0	1	0	0	0

(5 × 7 dot matrix)



(6 × 7 dot matrix)

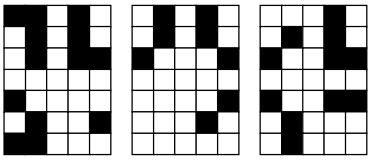


・Display state (6)

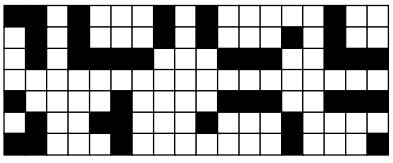
Shifted 3 dots to the left and 4 dots to the up relative to display state (1)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
1	1	0	0	0	1	0	0	0

(5 × 7 dot matrix)



(6 × 7 dot matrix)



• Display state (7)

Shifted 6 dots to the left and 8 dots to the up relative to display state (1)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	1	1	0	0	0	1	0	0

Shifted 8 dots to the up relative to display state (3)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	0	0	0	0	0	1	0	0

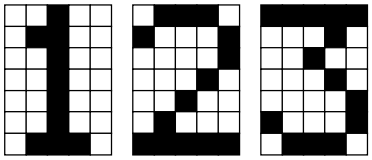
Shifted 6 dots to the left relative to display state (5)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
0	1	1	0	0	0	0	0	0

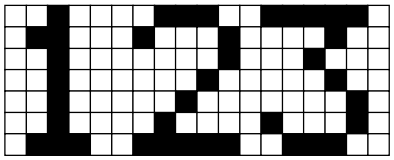
Shifted 3 dots to the left and 4 dots to the up relative to display state (6)

HS0	HS1	HS2	VS0	VS1	VS2	VS3	R/L	D/U
1	1	0	0	0	1	0	0	0

(5 × 7 dot matrix)



(6 × 7 dot matrix)



• Set AC and SC addresses ··· <Specifies the DCRAM address for AC and the dot address of the dot matrix character pattern for SC.>

Code															
D112	D113	D114	D115	D116	D117	D118	D119	D120	D121	D122	D123	D124	D125	D126	D127
HA0	HA1	HA2	X	X	X	X	X	VA0	VA1	VA2	VA3	X	X	X	X

Code																
D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143	
DA0	DA1	DA2	DA3	DA4	DA5	X	X	X	X	X	0	0	1	0	0	X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

HA0 to HA2: Dot address in the horizontal direction for the dot matrix character pattern

HA0	HA1	HA2

LSB ↑ Least significant bit

MSB ↑ Most significant bit

VA0 to VA3: Dot address in the vertical direction for the dot matrix character pattern

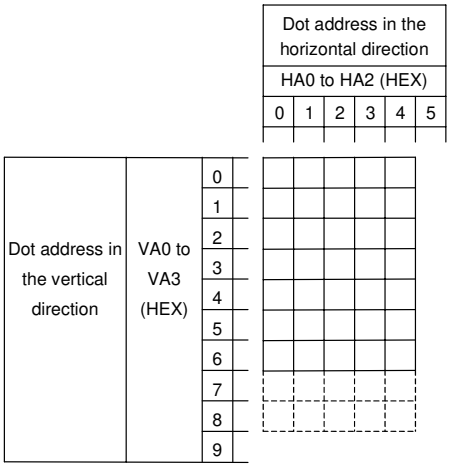
VA0	VA1	VA2	VA3

LSB ↑ Least significant bit

MSB ↑ Most significant bit

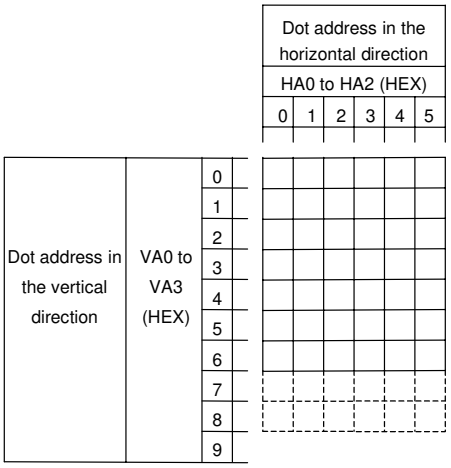
∗19 The figure below lists the correspondence between the data HA0 to HA2 which is dot address in the horizontal direction and the dot matrix character pattern, and the correspondence between the data VA0 to VA3 which is dot address in the vertical direction and the dot matrix character pattern.

• 5-dot font width: 5 × 7, 5 × 8, or 5 × 9 dots



- The area at HA0 to 2 = 5H is allocated to the space at the right of the dot matrix character pattern.
- The area at VA0 to 3 = 7H, for 5 × 7 dot characters, is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 8H is illegal for 5 × 7 dot characters. For 5 × 8 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 9H is illegal for 5 × 7 or 5 × 8 dot characters. For 5 × 9 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.

• 6-dot font width: 6 × 7, 6 × 8, or 6 × 9 dots



- The area at HA0 to 2 = 5H is allocated to the space at the right of the dot matrix character pattern.
- The area at VA0 to 3 = 7H, for 6 × 7 dot characters, is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 8H is illegal for 6 × 7 dot characters. For 6 × 8 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.
- The area at VA0 to 3 = 9H is illegal for 6 × 7 or 6 × 8 dot characters. For 6 × 9 dot characters, it is allocated to the space at the bottom of the dot matrix character pattern.

∗20: Example of the “set AC and SC addresses” instruction execution

Assume that a 32 digits × 2 lines display structure (OZ1 = 1, OZ2 = 0) has been set up with the “set display technique” instruction, and that the following data has been written to DCRAM with the “DCRAM data write” instruction.

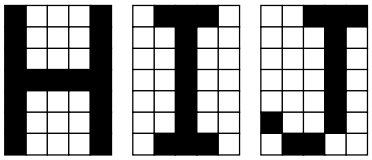
Display digit		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM data	First line (DCRAM address (hexadecimal))	A (00)	B (01)	C (02)	D (03)	E (04)	F (05)	G (06)	H (07)	I (08)	J (09)	K (0A)	L (0B)	M (0C)	N (0D)	O (0E)	P (0F)
	Second line (DCRAM address (hexadecimal))	0 (20)	1 (21)	2 (22)	3 (23)	4 (24)	5 (25)	6 (26)	7 (27)	8 (28)	9 (29)	a (2A)	b (2B)	c (2C)	d (2D)	e (2E)	f (2F)

Display digit		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
DCRAM data	First line (DCRAM address (hexadecimal))	Q (10)	R (11)	S (12)	T (13)	U (14)	V (15)	W (16)	X (17)	Y (18)	Z (19)	< (1A)	> (1B)	z (1C)	y (1D)	x (1E)	w (1F)
	Second line (DCRAM address (hexadecimal))	g (30)	h (31)	i (32)	j (33)	k (34)	l (35)	m (36)	n (37)	o (38)	p (39)	q (3A)	r (3B)	s (3C)	t (3D)	u (3E)	v (3F)

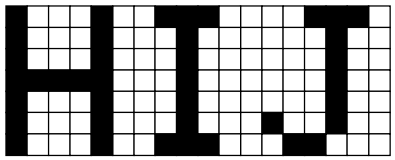
• When DA0 to 5 is set to 07H, HA0 to 2 is set to 0H, and VA0 to 3 is set to 0H.

HA0	HA1	HA2	VA0	VA1	VA2	VA3	DA0	DA1	DA2	DA3	DA4	DA5
0	0	0	0	0	0	0	1	1	1	0	0	0

(5 × 7 dot matrix)



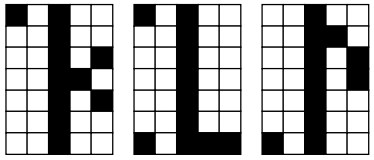
(6 × 7 dot matrix)



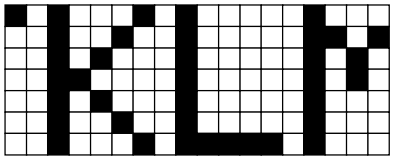
• When DA0 to 5 is set to 09H, HA0 to 2 is set to 4H, and VA0 to 3 is set to 0H.

HA0	HA1	HA2	VA0	VA1	VA2	VA3	DA0	DA1	DA2	DA3	DA4	DA5
0	0	1	0	0	0	0	1	0	0	1	0	0

(5 × 7 dot matrix)



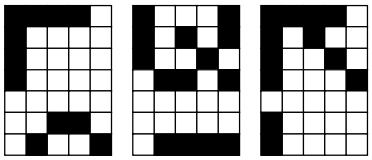
(6 × 7 dot matrix)



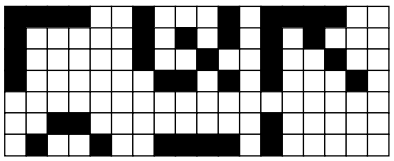
• When DA0 to 5 is set to 0FH, HA0 to 2 is set to 0H, and VA0 to 3 is set to 3H.

HA0	HA1	HA2	VA0	VA1	VA2	VA3	DA0	DA1	DA2	DA3	DA4	DA5
0	0	0	1	1	0	0	1	1	1	1	0	0

(5 × 7 dot matrix)



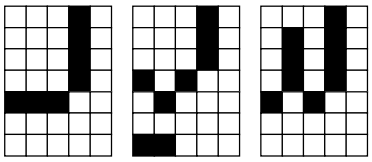
(6 × 7 dot matrix)



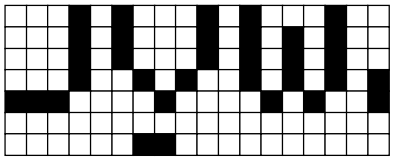
• When DA0 to 5 is set to 14H, HA0 to 2 is set to 1H, and VA0 to 3 is set to 2H.

HA0	HA1	HA2	VA0	VA1	VA2	VA3	DA0	DA1	DA2	DA3	DA4	DA5
1	0	0	0	1	0	0	0	0	1	0	1	0

(5 × 7 dot matrix)



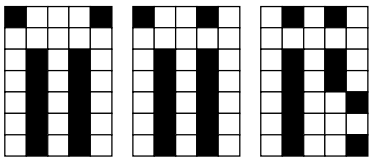
(6 × 7 dot matrix)



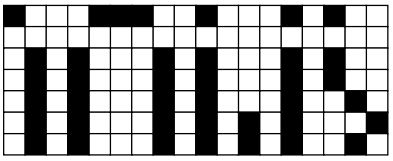
• When DA0 to 5 is set to 34H, HA0 to 2 is set to 3H, and VA0 to 3 is set to 6H.

HA0	HA1	HA2	VA0	VA1	VA2	VA3	DA0	DA1	DA2	DA3	DA4	DA5
1	1	0	0	1	1	0	0	0	1	0	1	1

(5 × 7 dot matrix)



(6 × 7 dot matrix)



• DCRAM data write ··· <Specifies the DCRAM address and stores data at that address.>

Code																							
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM1	IM2	X	0	0	1	0	1

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AC0 to AC7: DCRAM data (character code)

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

LSB ↑ Least significant bit

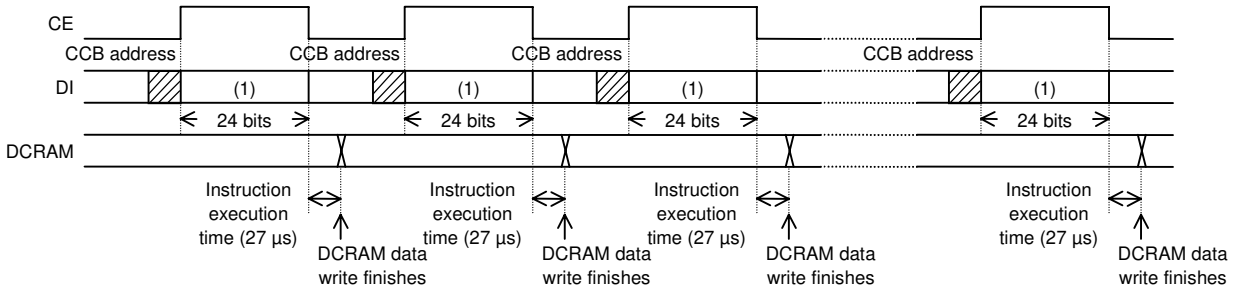
MSB ↑ Most significant bit

This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5 × 7, 5 × 8, or 5 × 9 dot matrix display data using CGROM or CGRAM.

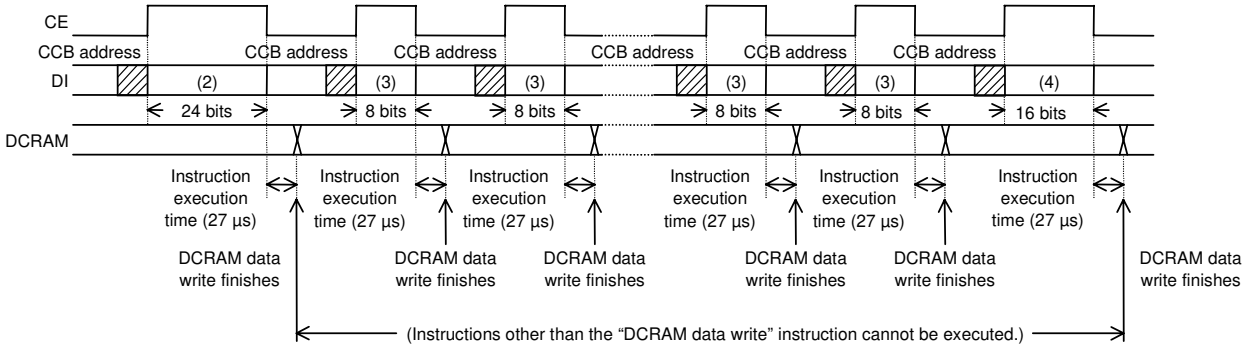
IM1 and IM2: Sets the method of writing data to DCRAM

IM1	IM2	DCRAM data write method
0	0	Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)
1	0	Normal increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.)
0	1	Super-increment mode DCRAM data write (Writes 2 to 16 characters of DCRAM data in a single operation.)

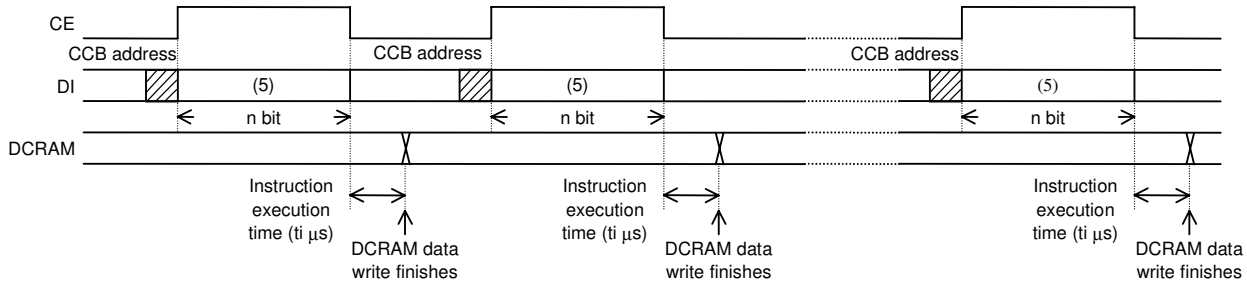
∗21 • DCRAM data write method when IM1 is 0 and IM2 is 0.



• DCRAM data write method when IM1 is 1 and IM2 is 0.
(Instructions other than the "DCRAM data write" instruction cannot be executed.)



• DCRAM data write method when IM1 is 0 and IM2 is 1.



$ti = 13.5\mu s \times (\frac{n}{8} - 1)$ (n = 8m + 16, m is an integer between 2 and 16 that is the number of characters written as DCRAM data.)

For example When n = 32 bits (m = 2): ti = 40.5 µs (when fosc = 300 kHz)
When n = 80 bits (m = 8): ti = 121.5 µs (when fosc = 300 kHz)
When n = 144 bits (m = 16): ti = 229.5 µs (when fosc = 300 kHz)

Note that the instruction execution time of 27 µs and ti values in µs apply when fosc = 300 kHz, and that these times will differ when the oscillator frequency fosc differs.

Data format (1) (24 bits)

Code																							
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	0	0	X	0	0	1	0	1

X: don't care

Data format (2) (24 bits)

Code																							
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	1	0	X	0	0	1	0	1

X: don't care

Data format (3) (8 bits)

Code							
D136	D137	D138	D139	D140	D141	D142	D143
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

Data format (4) (16 bits)

Code															
D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	0	0	X	0	0	1	0	1

X:don't care

Data format (5) (n bits)

Code																	
Dz	Dz+1	Dz+2	Dz+3	Dz+4	Dz+5	Dz+6	Dz+7	· · · · · · · · · · · · · · · · · · · ·	D112	D113	D114	D115	D116	D117	D118	D119	
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	· · · · · · · · · · · · · · · · · · · ·	$AC0_{m-1}$	$AC1_{m-1}$	$AC2_{m-1}$	$AC3_{m-1}$	$AC4_{m-1}$	$AC5_{m-1}$	$AC6_{m-1}$	$AC7_{m-1}$	

Code																							
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
$AC0_m$	$AC1_m$	$AC2_m$	$AC3_m$	$AC4_m$	$AC5_m$	$AC6_m$	$AC7_m$	$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	0	0	1	0	1

X: don't care

Here, n = 8m + 16, z = 128 - 8m (m is an integer between 2 and 16 that is the number of characters written as DCRAM data.)

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$) + 1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$) + 2	$AC0_3$ to $AC7_3$
⋮	⋮
($DA0_1$ to $DA5_1$) + (m – 3)	$AC0_{m-2}$ to $AC7_{m-2}$
($DA0_1$ to $DA5_1$) + (m – 2)	$AC0_{m-1}$ to $AC7_{m-1}$
($DA0_1$ to $DA5_1$) + (m – 1)	$AC0_m$ to $AC7_m$

Example 1: When n = 32 bits (m = 2: 2 characters DCRAM data write operation)

Code															
D112	D113	D114	D115	D116	D117	D118	D119	D120	D121	D122	D123	D124	D125	D126	D127
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	0	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$) + 1	$AC0_2$ to $AC7_2$

Example 2: When n = 80 bits (m = 8: 8 characters DCRAM data write operation)

Code															
D64	D65	D66	D67	D68	D69	D70	D71	D72	D73	D74	D75	D76	D77	D78	D79
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
$AC0_3$	$AC1_3$	$AC2_3$	$AC3_3$	$AC4_3$	$AC5_3$	$AC6_3$	$AC7_3$	$AC0_4$	$AC1_4$	$AC2_4$	$AC3_4$	$AC4_4$	$AC5_4$	$AC6_4$	$AC7_4$

Code															
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111
$AC0_5$	$AC1_5$	$AC2_5$	$AC3_5$	$AC4_5$	$AC5_5$	$AC6_5$	$AC7_5$	$AC0_6$	$AC1_6$	$AC2_6$	$AC3_6$	$AC4_6$	$AC5_6$	$AC6_6$	$AC7_6$

Code															
D112	D113	D114	D115	D116	D117	D118	D119	D120	D121	D122	D123	D124	D125	D126	D127
$AC0_7$	$AC1_7$	$AC2_7$	$AC3_7$	$AC4_7$	$AC5_7$	$AC6_7$	$AC7_7$	$AC0_8$	$AC1_8$	$AC2_8$	$AC3_8$	$AC4_8$	$AC5_8$	$AC6_8$	$AC7_8$

Code															
D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	0	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$) + 1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$) + 2	$AC0_3$ to $AC7_3$
($DA0_1$ to $DA5_1$) + 3	$AC0_4$ to $AC7_4$
($DA0_1$ to $DA5_1$) + 4	$AC0_5$ to $AC7_5$
($DA0_1$ to $DA5_1$) + 5	$AC0_6$ to $AC7_6$
($DA0_1$ to $DA5_1$) + 6	$AC0_7$ to $AC7_7$
($DA0_1$ to $DA5_1$) + 7	$AC0_8$ to $AC7_8$

Example 3: When n = 144 bits (m = 16: 16 characters DCRAM data write operation)

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
$AC0_0$	$AC1_0$	$AC2_0$	$AC3_0$	$AC4_0$	$AC5_0$	$AC6_0$	$AC7_0$	$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
$AC0_3$	$AC1_3$	$AC2_3$	$AC3_3$	$AC4_3$	$AC5_3$	$AC6_3$	$AC7_3$	$AC0_4$	$AC1_4$	$AC2_4$	$AC3_4$	$AC4_4$	$AC5_4$	$AC6_4$	$AC7_4$

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
$AC0_5$	$AC1_5$	$AC2_5$	$AC3_5$	$AC4_5$	$AC5_5$	$AC6_5$	$AC7_5$	$AC0_6$	$AC1_6$	$AC2_6$	$AC3_6$	$AC4_6$	$AC5_6$	$AC6_6$	$AC7_6$

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
$AC0_7$	$AC1_7$	$AC2_7$	$AC3_7$	$AC4_7$	$AC5_7$	$AC6_7$	$AC7_7$	$AC0_8$	$AC1_8$	$AC2_8$	$AC3_8$	$AC4_8$	$AC5_8$	$AC6_8$	$AC7_8$

Code															
D64	D65	D66	D67	D68	D69	D70	D71	D72	D73	D74	D75	D76	D77	D78	D79
$AC0_9$	$AC1_9$	$AC2_9$	$AC3_9$	$AC4_9$	$AC5_9$	$AC6_9$	$AC7_9$	$AC0_{10}$	$AC1_{10}$	$AC2_{10}$	$AC3_{10}$	$AC4_{10}$	$AC5_{10}$	$AC6_{10}$	$AC7_{10}$

Code															
D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
$AC0_{11}$	$AC1_{11}$	$AC2_{11}$	$AC3_{11}$	$AC4_{11}$	$AC5_{11}$	$AC6_{11}$	$AC7_{11}$	$AC0_{12}$	$AC1_{12}$	$AC2_{12}$	$AC3_{12}$	$AC4_{12}$	$AC5_{12}$	$AC6_{12}$	$AC7_{12}$

Code															
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111
$AC0_{13}$	$AC1_{13}$	$AC2_{13}$	$AC3_{13}$	$AC4_{13}$	$AC5_{13}$	$AC6_{13}$	$AC7_{13}$	$AC0_{14}$	$AC1_{14}$	$AC2_{14}$	$AC3_{14}$	$AC4_{14}$	$AC5_{14}$	$AC6_{14}$	$AC7_{14}$

Code															
D112	D113	D114	D115	D116	D117	D118	D119	D120	D121	D122	D123	D124	D125	D126	D127
$AC0_{15}$	$AC1_{15}$	$AC2_{15}$	$AC3_{15}$	$AC4_{15}$	$AC5_{15}$	$AC6_{15}$	$AC7_{15}$	$AC0_{16}$	$AC1_{16}$	$AC2_{16}$	$AC3_{16}$	$AC4_{16}$	$AC5_{16}$	$AC6_{16}$	$AC7_{16}$

Code															
D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	D138	D139	D140	D141	D142	D143
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	0	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$) + 1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$) + 2	$AC0_3$ to $AC7_3$
($DA0_1$ to $DA5_1$) + 3	$AC0_4$ to $AC7_4$
($DA0_1$ to $DA5_1$) + 4	$AC0_5$ to $AC7_5$
($DA0_1$ to $DA5_1$) + 5	$AC0_6$ to $AC7_6$
($DA0_1$ to $DA5_1$) + 6	$AC0_7$ to $AC7_7$
($DA0_1$ to $DA5_1$) + 7	$AC0_8$ to $AC7_8$

DCRAM address	DCRAM data
($DA0_1$ to $DA5_1$) + 8	$AC0_9$ to $AC7_9$
($DA0_1$ to $DA5_1$) + 9	$AC0_{10}$ to $AC7_{10}$
($DA0_1$ to $DA5_1$) + 10	$AC0_{11}$ to $AC7_{11}$
($DA0_1$ to $DA5_1$) + 11	$AC0_{12}$ to $AC7_{12}$
($DA0_1$ to $DA5_1$) + 12	$AC0_{13}$ to $AC7_{13}$
($DA0_1$ to $DA5_1$) + 13	$AC0_{14}$ to $AC7_{14}$
($DA0_1$ to $DA5_1$) + 14	$AC0_{15}$ to $AC7_{15}$
($DA0_1$ to $DA5_1$) + 15	$AC0_{16}$ to $AC7_{16}$

• ALATCH data write ····· <Write data to the ALATCH>

Code															
D56	D57	D58	D59	D60	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70	D71
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16

Code															
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87
AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26	AD27	AD28	AD29	AD30	AD31	AD32

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
AD33	AD34	AD35	AD36	AD37	AD38	AD39	AD40	AD41	AD42	AD43	AD44	AD45	AD46	AD47	AD48

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD49	AD50	AD51	AD52	AD53	AD54	AD55	AD56	AD57	AD58	AD59	AD60	AD61	AD62	AD63	AD64

Code															
D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135
AD65	AD66	AD67	AD68	AD69	AD70	AD71	AD72	AD73	AD74	AD75	AD76	AD77	AD78	AD79	AD80

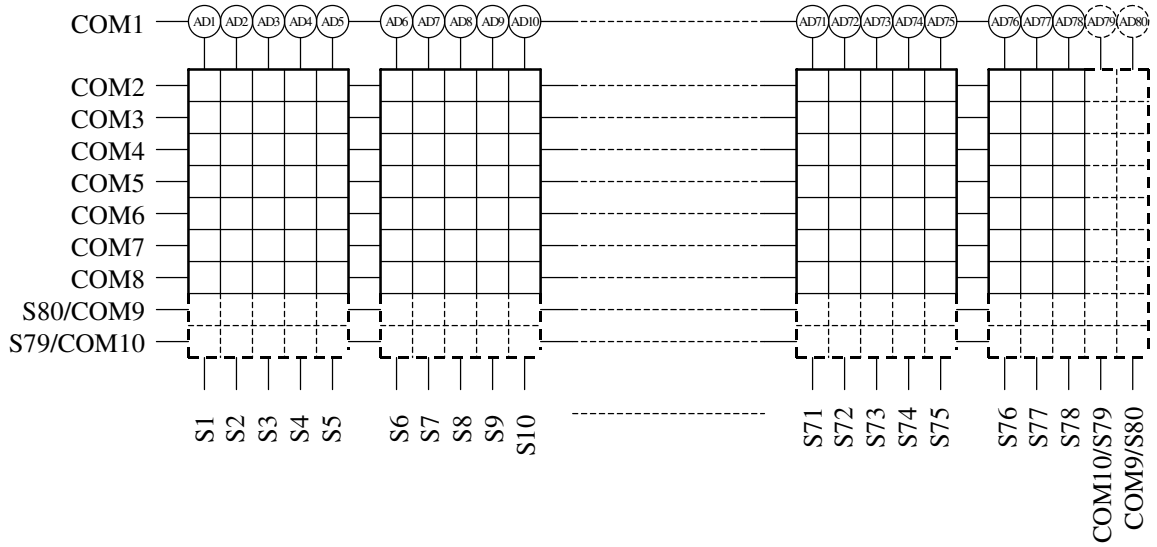
Code							
D136	D137	D138	D139	D140	D141	D142	D143
X	X	X	0	0	1	1	0

X: don't care

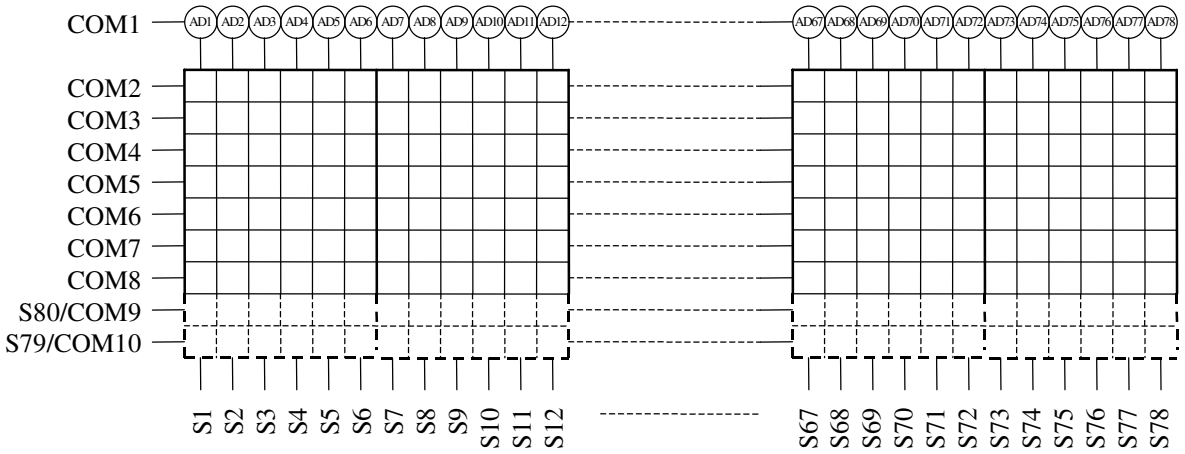
AD1 to AD80: ADATA display data

In addition to the 5 × 7, 5 × 8, 5 × 9, 6 × 7, 6 × 8, or 6 × 9 dot matrix display data (MDATA), the LC75810E/T also supports an accessory display of 5 or 6 segments (ADATA) at each display digit, and allows arbitrary data to be displayed directly without going through CGROM or CGRAM. The figure below shows the correspondence between that data and the display. When ADn = 1 (where n is an integer between 1 and 80), the segment corresponding to that data will be turned on.

5-dot font width (5 × 7, 5 × 8, or 5 × 9 dots)



6-dot font width (6 × 7, 6 × 8, or 6 × 9 dots)



Correspondence between ADATA and the output pins

ADATA	Corresponding output pin
AD1	S1
AD2	S2
AD3	S3
AD4	S4
AD5	S5
AD6	S6
AD7	S7
AD8	S8
AD9	S9
AD10	S10
AD11	S11
AD12	S12
AD13	S13
AD14	S14
AD15	S15
AD16	S16
AD17	S17
AD18	S18
AD19	S19
AD20	S20
AD21	S21
AD22	S22
AD23	S23
AD24	S24
AD25	S25
AD26	S26
AD27	S27
AD28	S28
AD29	S29
AD30	S30

ADATA	Corresponding output pin
AD31	S31
AD32	S32
AD33	S33
AD34	S34
AD35	S35
AD36	S36
AD37	S37
AD38	S38
AD39	S39
AD40	S40
AD41	S41
AD42	S42
AD43	S43
AD44	S44
AD45	S45
AD46	S46
AD47	S47
AD48	S48
AD49	S49
AD50	S50
AD51	S51
AD52	S52
AD53	S53
AD54	S54
AD55	S55
AD56	S56
AD57	S57
AD58	S58
AD59	S59
AD60	S60

ADATA	Corresponding output pin
AD61	S61
AD62	S62
AD63	S63
AD64	S64
AD65	S65
AD66	S66
AD67	S67
AD68	S68
AD69	S69
AD70	S70
AD71	S71
AD72	S72
AD73	S73
AD74	S74
AD75	S75
AD76	S76
AD77	S77
AD78	S78
AD79	S79
AD80	S80