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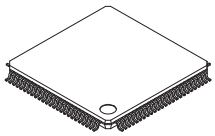
LC75812PT

1/8, 1/9-Duty Dot Matrix LCD Controller / Driver with Key Input Function

ON Semiconductor®

www.onsemi.com



TQFP100 14x14 / TQFP100

Overview

The LC75812PT is 1/8, 1/9 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75812PT also provide on-chip character display ROM and RAM to allow display systems to be implemented easily. These products also provide up to 3 general-purpose output ports and incorporate a key scan circuit that accepts input from up to 35 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 35 keys
  (A key scan is performed only when a key is pressed.)
- Controls and drives a 5×7 or 5×8 dot matrix LCD.
- Supports accessory display segment drive (up to 65 segments)
- Display technique: 1/8 duty 1/4 bias drive (5×7 dots)
  1/9 duty 1/4 bias drive (5×8 dots)
- Display digits: 13 digits×1 line (5×7 dots), 12 digits×1 line (5×8 dots)
- Display control memory
  - CGROM: 240 characters (5×7 or 5×8 dots)
  - CGRAM: 16 characters (5×7 or 5×8 dots)
  - ADRAM: 13×5 bits
  - DCRAM: 52×8 bits
- Instruction function
  - Display on/off control
  - Display shift function
- Sleep mode can be used to reduce current drain.
- Built-in display contrast adjustment circuit
- Switching between key scan output and general-purpose output ports can be controlled with instructions.
- PWM output for adjusting the LED backlight brightness
- The frame frequency of the common and segment output waveforms can be controlled by instructions.
- Serial data control of switching between the RC oscillator operating mode and external clock operating mode.
- Independent LCD driver block power supply V_{LCD}
- A voltage detection type reset circuit is provided to initialize the IC and prevent incorrect display.
- The $\overline{INH}$ pin is provided. This pin turns off the display, disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 55 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +4.2	V
	V_{LCD} max	V_{LCD}	−0.3 to +11.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +4.2	V
		CE, CL, DI, $\overline{INH}$ V_{DD}=2.7 to 3.6V	−0.3 to +6.5	
	$V_{IN}2$	OSC, KI1 to KI5, TEST	−0.3 to V_{DD} +0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, $V_{LCD}4$	−0.3 to V_{LCD} +0.3	
Output voltage	$V_{OUT}1$	DO	-0.3 to +6.5	V
	$V_{OUT}2$	OSC, KS1 to KS7, P1 to P3	−0.3 to V_{DD} +0.3	
	$V_{OUT}3$	$V_{LCD}0$, S1 to S65, COM1 to COM9	−0.3 to V_{LCD} +0.3	
Output current	$I_{OUT}1$	S1 to S65	300	μA
	$I_{OUT}2$	COM1 to COM9	3	mA
	$I_{OUT}3$	KS1 to KS7	1	
	$I_{OUT}4$	P1 to P3	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range at Ta = −40°C to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		3.6	V
	V_{LCD}	V_{LCD} When the display contrast adjustment circuit is used.	7.0		10.0	
		V_{LCD} When the display contrast adjustment circuit is not used.	4.5		10.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	$V_{LCD}4$ +4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4 ($V_{LCD}0$−$V_{LCD}4$)	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4 ($V_{LCD}0$−$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4 ($V_{LCD}0$−$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}4$	$V_{LCD}4$	0		1.5	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8V_{DD}		3.6	V
		CE, CL, DI, $\overline{INH}$ V_{DD} = 2.7 to 3.6 V	0.8V_{DD}		5.5	
	$V_{IH}2$	OSC external clock operating mode	0.8V_{DD}		V_{DD}	
	$V_{IH}3$	KI1 to KI5	0.6V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$, KI1 to KI5	0		0.2V_{DD}	V
	$V_{IL}2$	OSC external clock operating mode	0		0.2V_{DD}	

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Output pull-up voltage	V_{OUP}	DO	0		5.5	V
Recommended external resistor for RC oscillation	Rosc	OSC RC oscillator operating mode		10		kΩ
Recommended external capacitor for RC oscillation	Cosc	OSC RC oscillator operating mode		470		pF
Guaranteed range of RC oscillation	fosc	OSC RC oscillator operating mode	150	300	600	kHz
External clock operating frequency	f_{CK}	OSC external clock operating mode [Figure 4]	100	300	600	kHz
External clock duty cycle	D_{CK}	OSC external clock operating mode [Figure 4]	30	50	70	%
Data setup time	tds	CL, DI [Figure 2],[Figure 3]	160			ns
Data hold time	tdh	CL, DI [Figure 2],[Figure 3]	160			ns
CE wait time	tcp	CE, CL [Figure 2],[Figure 3]	160			ns
CE setup time	tcs	CE, CL [Figure 2],[Figure 3]	160			ns
CE hold time	tch	CE, CL [Figure 2],[Figure 3]	160			ns
High level clock pulse width	tϕH	CL [Figure 2],[Figure 3]	160			ns
Low level clock pulse width	tϕL	CL [Figure 2],[Figure 3]	160			ns
DO output delay time	tdc	DO R_{PU} = 4.7 kΩ C_L = 10 pF *1 [Figure 2],[Figure 3]			1.5	μs
DO rise time	tdr	DO R_{PU} = 4.7 kΩ C_L = 10 pF *1 [Figure 2],[Figure 3]			1.5	μs

Note: *1. Since the DO pin is an open-drain output, these times depend on the values of the pull-up resistor R_{PU} and the load capacitance C_L.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

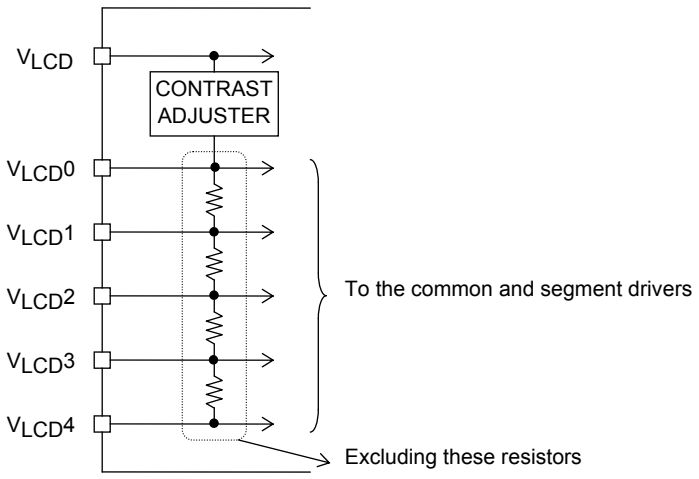
Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$, KI1 to KI5			$0.1V_{DD}$		V
Power-down detection voltage	V_{DET}			2.0	2.2	2.4	V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 3.6 V			5.0	μA
			V_I = 5.5 V V_{DD} = 2.7 to 3.6 V			5.0	
	$I_{IH}2$	OSC	$V_I = V_{DD}$ external clock operating mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0 V	–5.0			μA
	$I_{IL}2$	OSC	V_I = 0 V external clock operating mode	–5.0			
Input floating voltage	V_{IF}	KI1 to KI5				$0.05V_{DD}$	V
Pull-down resistance	R_{PD}	KI1 to KI5	V_{DD} = 3.3 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO	V_O = 5.5 V			6.0	μA
Output high level voltage	$V_{OH}1$	S1 to S65	I_O = –20 μA	$V_{LCD}0$–0.6			V
	$V_{OH}2$	COM1 to COM9	I_O = –100 μA	$V_{LCD}0$–0.6			
	$V_{OH}3$	KS1 to KS7	I_O = –250 μA	V_{DD}–0.8	V_{DD}–0.4	V_{DD}–0.1	
	$V_{OH}4$	P1 to P3	I_O = –1 mA	V_{DD}–0.9			
Output low level voltage	$V_{OL}1$	S1 to S65	I_O = 20 μA			$V_{LCD}4$+0.6	V
	$V_{OL}2$	COM1 to COM9	I_O = 100 μA			$V_{LCD}4$+0.6	
	$V_{OL}3$	KS1 to KS7	I_O = 12.5 μA	0.1	0.4	1.2	
	$V_{OL}4$	P1 to P3	I_O = 1 mA			0.9	
	$V_{OL}5$	DO	I_O = 1 mA		0.1	0.3	

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Output middle level voltage *2	$V_{MID}1$	S1 to S65	I_O = ±20 μA	2/4 ($V_{LCD}0$ −$V_{LCD}4$) −0.6		2/4 ($V_{LCD}0$ −$V_{LCD}4$) +0.6	V
	$V_{MID}2$	COM1 to COM9	I_O = ±100 μA	3/4 ($V_{LCD}0$ −$V_{LCD}4$) −0.6		3/4 ($V_{LCD}0$ −$V_{LCD}4$) +0.6	
	$V_{MID}3$	COM1 to COM9	I_O = ±100 μA	1/4 ($V_{LCD}0$ −$V_{LCD}4$) −0.6		1/4 ($V_{LCD}0$ −$V_{LCD}4$) +0.6	
Oscillator frequency	fosc	OSC	Rosc = 10 kΩ, Cosc = 470 pF	210	300	390	kHz
Current drain	$I_{DD}1$	V_{DD}	sleep mode			100	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 3.6 V, output open, fosc = 300 kHz		500	1000	
	$I_{LCD}1$	V_{LCD}	sleep mode			15	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 10.0 V, output open, fosc = 300 kHz, When the display contrast adjustment circuit is used.		450	900	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 10.0 V, output open, fosc = 300 kHz, When the display contrast adjustment circuit is not used.		200	400	

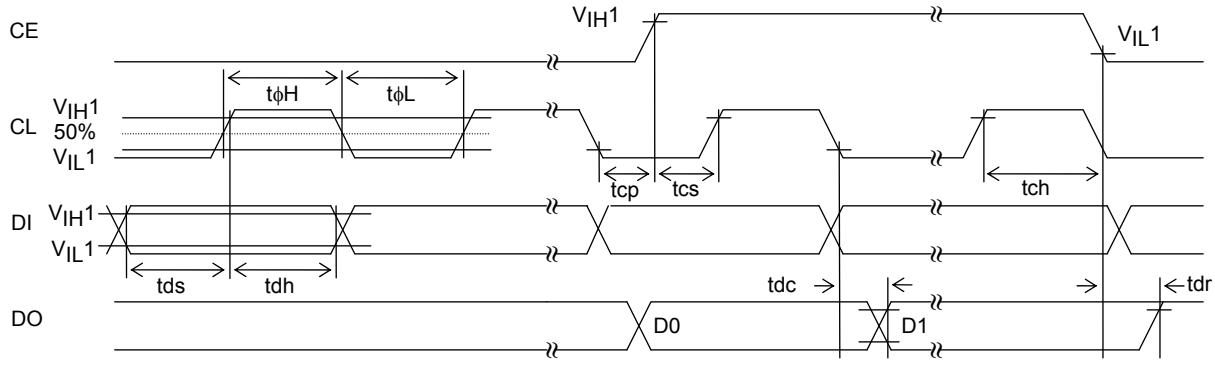
Note: *2. Excluding the bias voltage generation divider resistor built into the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (See Figure 1.)



[Figure 1]

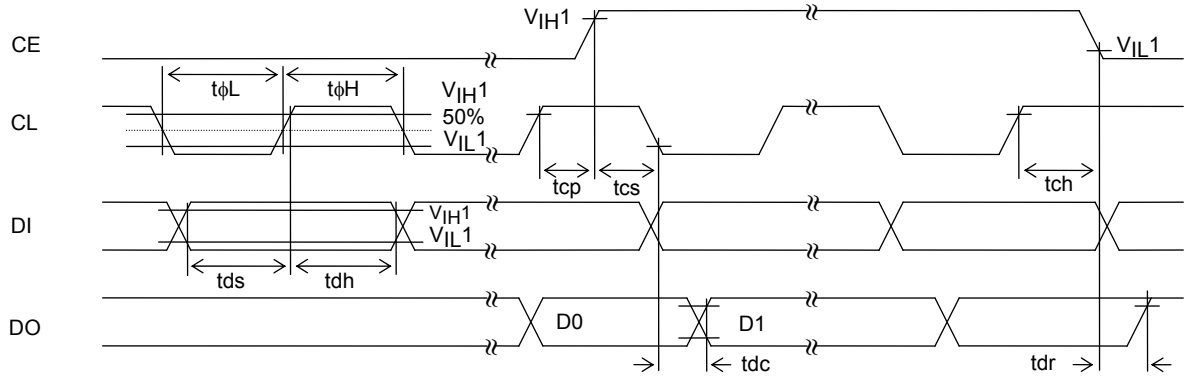
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(1) When CL is stopped at the low level



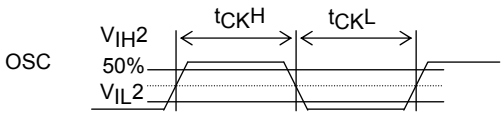
[Figure 2]

(2) When CL is stopped at the high level



[Figure 3]

(3) OSC pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \text{ [kHz]}$$

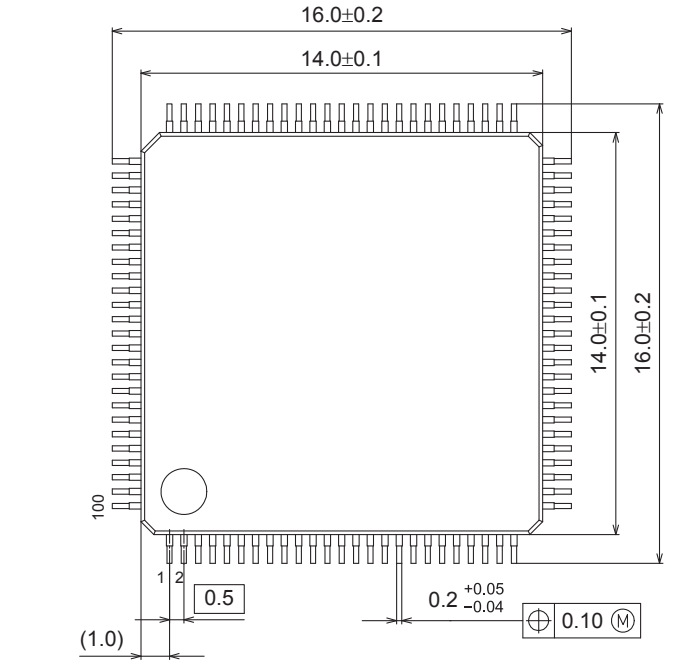
$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100[\%]$$

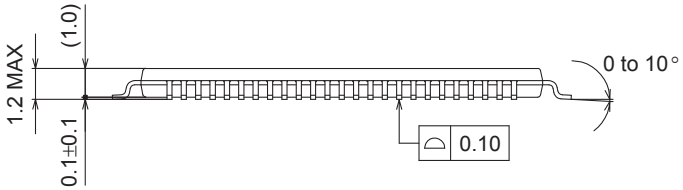
[Figure 4]

Package Dimensions

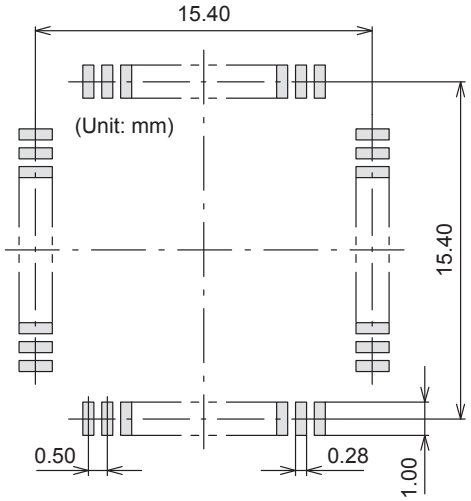
unit : mm

TQFP100 14x14 / TQFP100
CASE 932AY
ISSUE A

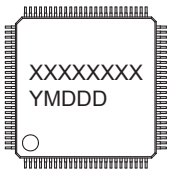




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



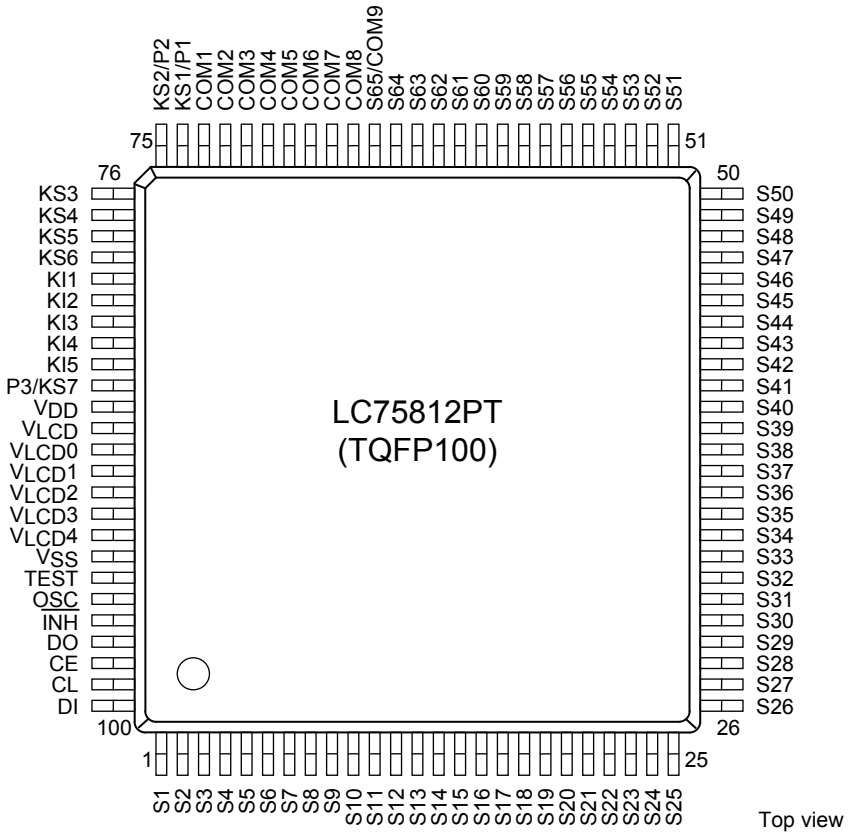
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

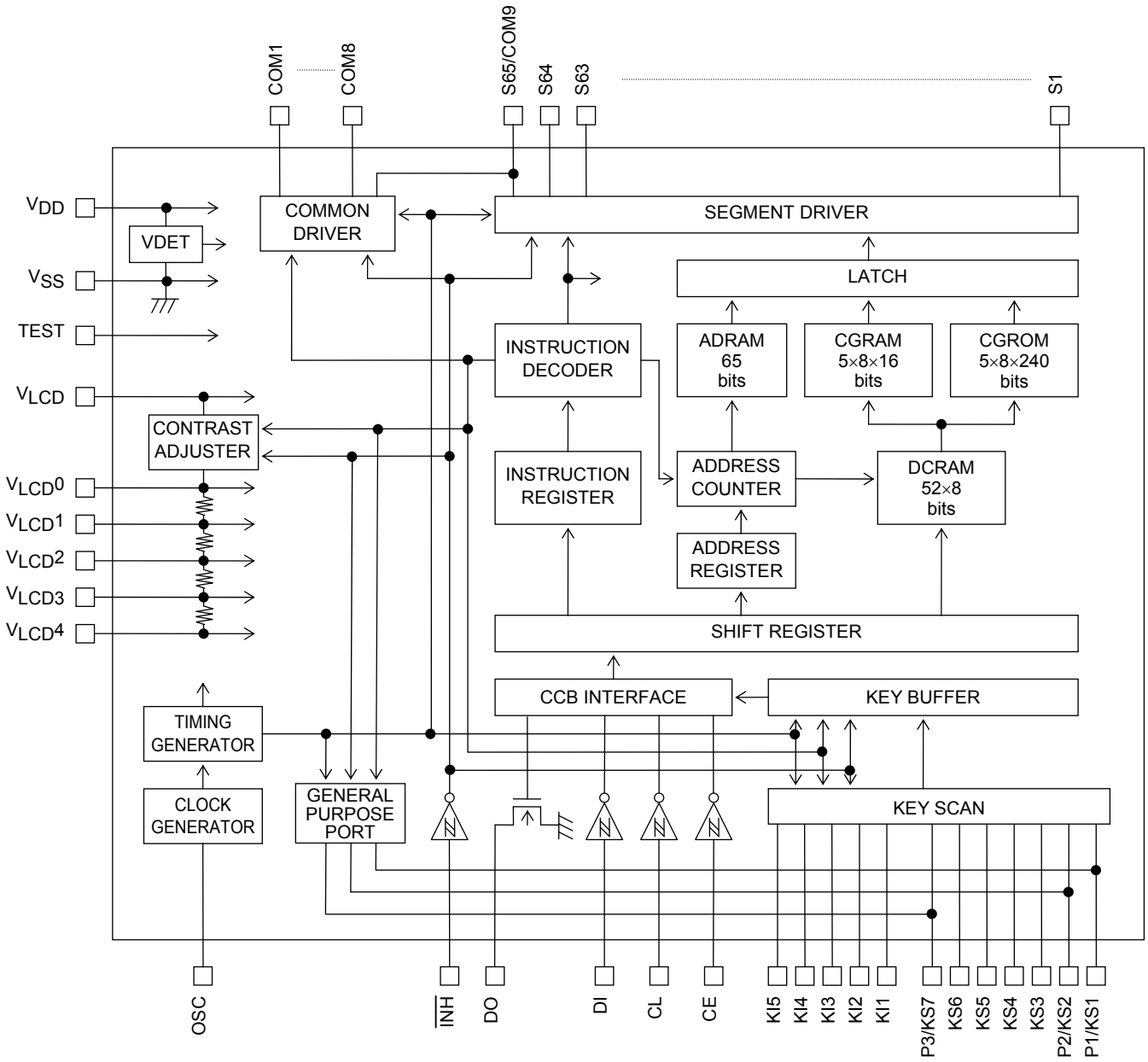
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignments



Top view

Block Diagram



Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1 to S64 S65/COM9	1 to 64 65	Segment driver outputs. S65/COM9 can be used as common driver output pin under the "set display technique" instruction.	-	O	OPEN
COM1 to COM8	73 to 66	Common driver outputs.	-	O	OPEN
KS1/P1 KS2/P2 KS3 to KS6 KS7/P3	74 75 76 to 79 85	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. KS1/P1, KS2/P2, and KS7/P3 can be used as general-purpose output ports under the "set key scan output port/general-purpose output port state" instruction.	-	O	OPEN
KI1 to KI5	80 to 84	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
OSC	95	Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can also be used as the external clock input pin with the "set display technique" instruction.	-	I/O	V_{DD}
CE	98	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	H	I	GND
CL	99		↑	I	
DI	100		-	I	
DO	97		-	O	OPEN
$\overline{INH}$	96	Input that turns the display off, disables key scanning, and forces the general-purpose output ports low. • When $\overline{INH}$ is low (V_{SS}): • Display off S1 to S64="L" ($V_{LCD}4$) S65/COM9="L" ($V_{LCD}4$) COM1 to COM8="L" ($V_{LCD}4$) • General-purpose output ports P1 to P3=low (V_{SS}) • Key scanning disabled: KS1 to KS7=low (V_{SS}) • All the key data is reset to low. • When $\overline{INH}$ is high (V_{DD}): • Display on • The state of the pins as key scan output pins or general-purpose output ports can be set with the "set key scan output port/general-purpose output port state" instruction. • Key scanning is enabled. However, serial data can be transferred when the $\overline{INH}$ pin is low.	L	I	V_{DD}
TEST	94	This pin must be connected to ground.	-	I	-
$V_{LCD}0$	88	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	-	O	OPEN
$V_{LCD}1$	89	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 (V_{LCD} - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}2$	90	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN

Continued on next page.

Continued from preceding page.

Pin	Pin No.	Function	Active	I/O	Handling when unused
$V_{LCD}3$	91	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}4$	92	LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V, and $V_{LCD}4$ must be in the range 0V to 1.5V, inclusive.	-	I	GND
V_{DD}	86	Logic block power supply connection. Provide a voltage of between 2.7 to 3.6V.	-	-	-
V_{LCD}	87	LCD driver block power supply connection. Provide a voltage of between 7.0 to 10.0V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 to 10.0V when the circuit is not used.	-	-	-
V_{SS}	93	Power supply connection. Connect to ground.	-	-	-

Block Functions

- AC (address counter)
  AC is a counter that provides the addresses used for DCRAM and ADRAM.
  The address is automatically modified internally, and the LCD display state is retained.

- DCRAM (data control RAM)
  DCRAM is RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to 5×7 or 5×8 dot matrix character patterns using CGROM or CGRAM.) DCRAM has a capacity of 52×8 bits, and can hold 52 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

- When the DCRAM address loaded into AC is 00H.

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
DCRAM address (hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C

However, when the display shift is performed by specifying MDATA, the DCRAM address shifts as shown below.

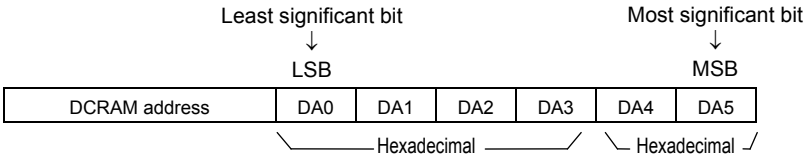
Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
DCRAM address (hexadecimal)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D

(shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
DCRAM address (hexadecimal)	33	00	01	02	03	04	05	06	07	08	09	0A	0B

(shift right)

Note: *3. The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is 2EH.

DA0	DA1	DA2	DA3	DA4	DA5
0	1	1	1	0	1

Note: *4. 5×7 dots ····· 13th digit display 5×7 dots
5×8 dots ····· 13th digit display 4×8 dots

• ADRAM (Additional data RAM)
ADRAM is RAM that is used to store the ADATA display data. ADRAM has a capacity of 13×5 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM. The table below lists the correspondence between the 4-bit ADRAM address loaded into AC and the display position on the LCD panel.

• When the ADRAM address loaded into AC is 0H. (Number of digit displayed: 13)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
ADRAM address (hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C

However, when the display shift is performed by specifying ADATA, the ADRAM address shifts as shown below.

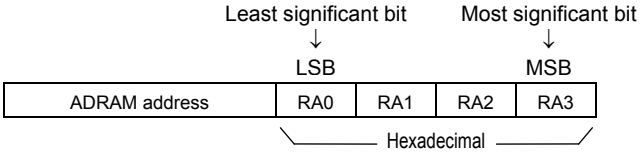
Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
ADRAM address (hexadecimal)	1	2	3	4	5	6	7	8	9	A	B	C	0

(shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
ADRAM address (hexadecimal)	C	0	1	2	3	4	5	6	7	8	9	A	B

(shift right)

Note: *5. The ADRAM address is expressed in hexadecimal.



Example: When the ADRAM address is AH.

RA0	RA1	RA2	RA3
0	1	0	1

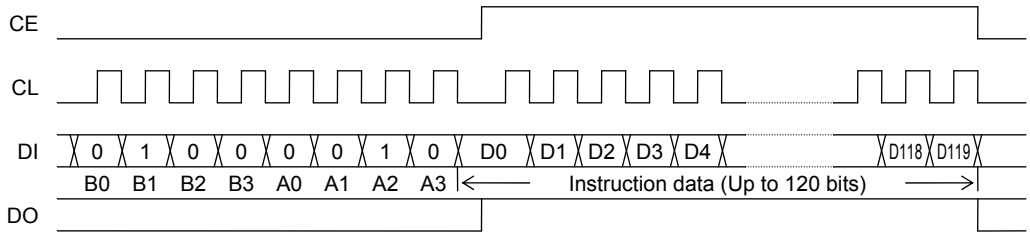
Note: *6. 5×7 dots ····· 13th digit display 5 dots
5×8 dots ····· 13th digit display 4 dots

• CGROM (Character generator ROM)
CGROM is ROM that is used to generate the 240 kinds of 5×7 or 5×8 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240×40 bits. When a character code is written to DCRAM, the character pattern stored in CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

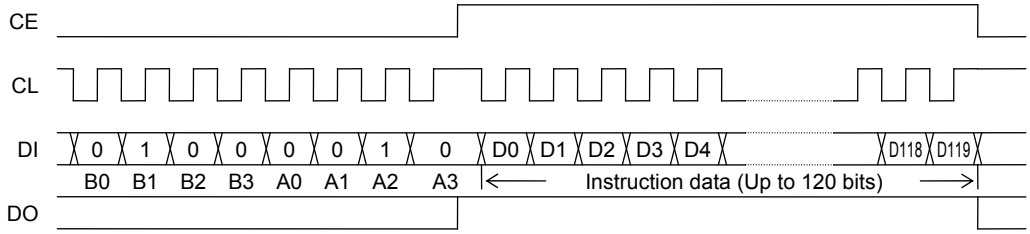
• CGRAM (Character generator RAM)
CGRAM is RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5×7 or 5×8 dot matrix character patterns can be stored. CGRAM has a capacity of 16×40 bits.

Serial Data Input

(1) When CL is stopped at the low level



(2) When CL is stopped at the high level



- B0 to B3, A0 to A3: CCB address 42H
- D0 to D119: Instruction data

The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

Instruction	D0…D56…D71	D72...D77 D78 D79	D80...D85 D86 D87	D88...D93 D94 D95	D96 D97 D98 D99 D100 D101 D102 D103	D104 D105 D106 D107 D108 D109 D110 D111	D112 D113 D114 D115	D116 D117 D118 D119	Execution time *11
Set display technique *7							DT FC0 FC1 OC	0 0 0 1	0μs/ 108μs *7
Display on/off control					DG1 DG2 DG3 DG4 DG5 DG6 DG7 DG8	DG9 DG10 DG11 DG12 DG13 X X X	M A SC SP	0 0 1 0	0μs/27μs *8
Display shift							M A R/L X	0 0 1 1	27μs
Set AC address						DA0 DA1 DA2 DA3 DA4 DA5 X X	RA0 RA1 RA2 RA3	0 1 0 0	27μs
DCRAM data write *9					AC0 AC1 AC2 AC3 AC4 AC5 AC6 AC7	DA0 DA1 DA2 DA3 DA4 DA5 X X	IM1 IM2 X X	0 1 0 1	27μs/tiμs *9
ADRAM data write *10					AD1 AD2 AD3 AD4 AD5 X X X	RA0 RA1 RA2 RA3 X X X X	IM1 IM2 X X	0 1 1 0	27μs/tiμs *10
CGRAM data write	... CD1...CD16	CD17 ... CD24	CD25 ... CD32	CD33 ... CD40	X X X X X X X X	CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7	X X X X	0 1 1 1	27μs
Set display contrast						CT0 CT1 CT2 CT3 X X X X	CTC X X X	1 0 0 0	0μs
Set key scan output port/ general-purpose output port state		W10...W15 W20 W21	W22...W25...W33	W34 W35 PC10...PC31	PC32 PF0 PF1 PF2 PF3 KC1 KC2 KC3	KC4 KC5 KC6 KC7 KP1 KP2 KP3 X	X X X X	1 0 0 1	0μs

X: don't care

Notes:
*7. Be sure to execute the "set display technique" instruction first after power-on (V_{DET}-based system reset). Note that the execution time of this first instruction is 108μs (fosc=300kHz, f_{CK}=300kHz).
*8.When the sleep mode (SP = 1) is set, the execution time is 27μs (when fosc = 300kHz, f_{CK} = 300kHz).
*9. The data format differs when the DCRAM data write instruction is executed in the normal increment mode (IM1=1, IM2=0) or in the super increment mode (IM1=0, IM2=1). Note that the execution time for the DCRAM data write instruction executed in the super increment mode is tiμs (fosc=300kHz, f_{CK}=300kHz). (See the detailed descriptions.)
*10. The data format differs when the ADRAM data write instruction is executed in the normal increment mode (IM1=1, IM2=0) or in the super increment mode (IM1=0, IM2=1). Note that the execution time for the ADRAM data write instruction executed in the super increment mode is tiμs (fosc=300kHz, f_{CK}=300kHz). (See the detailed descriptions.)
*11. The execution times listed here apply when fosc=300kHz, f_{CK}=300kHz. The execution times differ when the oscillator frequency fosc or the external clock frequency f_{CK} differs.
Example: When fosc = 210kHz, f_{CK} = 210kHz

$$27\mu s\times\frac{300}{210}=39\mu s,\ 108\mu s\times\frac{300}{210}=155\mu s,\ ti\mu s\times\frac{300}{210}=ti\times1.43\mu s$$

Detailed Instruction Descriptions

• Set display technique ... <Sets the display technique>

(Display technique)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
DT	FC0	FC1	OC	0	0	0	1

X: don't care

Note: Be sure to execute the "set display technique" instruction first after power-on (V_{DET}-based system reset).

DT: Sets the display technique

DT	Display technique	Output pins
		S65/COM9
0	1/8 duty, 1/4 bias drive	S65
1	1/9 duty, 1/4 bias drive	COM9

Note: *12. S65: Segment output
COM9: Common output

FC0, FC1: Sets the frame frequency of the common and segment output waveforms

FC0	FC1	Frame frequency	
		1/8 duty, 1/4 bias drive f8[Hz]	1/9 duty, 1/4 bias drive f9[Hz]
0	0	fosc/3072, f_{CK}/3072	fosc/3456, f_{CK}/3456
1	0	fosc/1536, f_{CK}/1536	fosc/1728, f_{CK}/1728
0	1	fosc/768, f_{CK}/768	fosc/864, f_{CK}/864

OC: Sets the RC oscillator operating mode and external clock operating mode.

OC	OSC pin function
0	RC oscillator operating mode
1	External clock operating mode

Note: *13. When selecting the RC oscillator operating mode, be sure to connect an external resistor Rosc and an external capacitor Cosc to the OSC pin.

• Display on/off control ... <Turns the display on or off>

(Display ON/OFF control)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	X	X	X	M	A	SC	SP	0	0	1	0

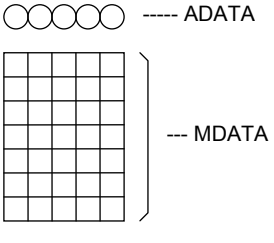
X: don't care

M, A: Specifies the data to be turned on or off

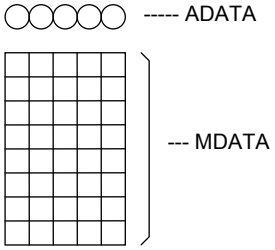
M	A	Display operating state
0	0	Both MDATA and ADATA are turned off (The display is forcibly turned off regardless of the DG1 to DG13 data.)
0	1	Only ADATA is turned on (The ADATA of display digits specified by the DG1 to DG13 data are turned on.)
1	0	Only MDATA is turned on (The MDATA of display digits specified by the DG1 to DG13 data are turned on.)
1	1	Both MDATA and ADATA are turned on (The MDATA and ADATA of display digits specified by the DG1 to DG13 data are turned on.)

Note: *14. MDATA, ADATA

5×7 dot matrix display



5×8 dot matrix display



DG1 to DG13: Specifies the display digit

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13
Display digit data	DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13

For example, if DG1 to DG7 are 1, and DG8 to DG13 are 0, then display digits 1 to 7 will be turned on, and display digits 8 to 13 will be turned off (blanked).

SC: Controls the common and segment output pins

SC	Common and segment output pin states
0	Output of LCD drive waveforms
1	Fixed at the $V_{LCD}4$ level (all segments off)

Note: *15. When SC is 1, the S1 to S65 and COM1 to COM9 output pins are set to the $V_{LCD}4$ level, regardless of the M, A, and DG1 to DG13 data.

SP: Controls the normal mode and sleep mode

SP	Mode
0	Normal mode
1	Sleep mode The common and segment pins go to the $V_{LCD}4$ level and the oscillator on the OSC pin is stopped (although it operates during key scan operations) in RC oscillator operating mode (OC="0") and reception of the external clock is stopped (external clock is received during key scan operations) in external clock operating mode (OC="1"), to reduce current drain. Although the "display on/off control", "set display contrast" and "set key scan output port/general-purpose output port state" (disallowed to set pins P1 to P3 for PWM signal output and pin P3 for clock signal output) instructions can be executed in this mode, applications must return the IC to normal mode to execute any of the other instruction setting. When the IC is in external clock operating mode, be sure to stop the external clock input after the lapse of the instruction execution time (27μs: f_{CK}=300kHz).

• Display shift ... <Shifts the display>
(Display shift)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
M	A	R/L	X	0	0	1	1

X: don't care

M, A: Specifies the data to be shifted

M	A	Shift operating state
0	0	Neither MDATA nor ADATA is shifted
0	1	Only ADATA is shifted
1	0	Only MDATA is shifted
1	1	Both MDATA and ADATA are shifted

R/L: Specifies the shift direction

R/L	Shift direction
0	Shift left
1	Shift right

• Set AC address... <Specifies the DCRAM and ADRAM address for AC>
(Set AC)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
DA0	DA1	DA2	DA3	DA4	DA5	X	X	RA0	RA1	RA2	RA3	0	1	0	0

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

RA0 to RA3: ADRAM address

RA0	RA1	RA2	RA3

LSB ↑ Least significant bit

MSB ↑ Most significant bit

This instruction loads the 6-bit DCRAM address DA0 to DA5 and the 4-bit ADRAM address RA0 to RA3 into the AC.

• DCRAM data write ... <Specifies the DCRAM address and stores data at that address>
(Write data to DCRAM)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM1	IM2	X	X	0	1	0	1

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AC0 to AC7: DCRAM data (character code)

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

LSB ↑ Least significant bit

MSB ↑ Most significant bit

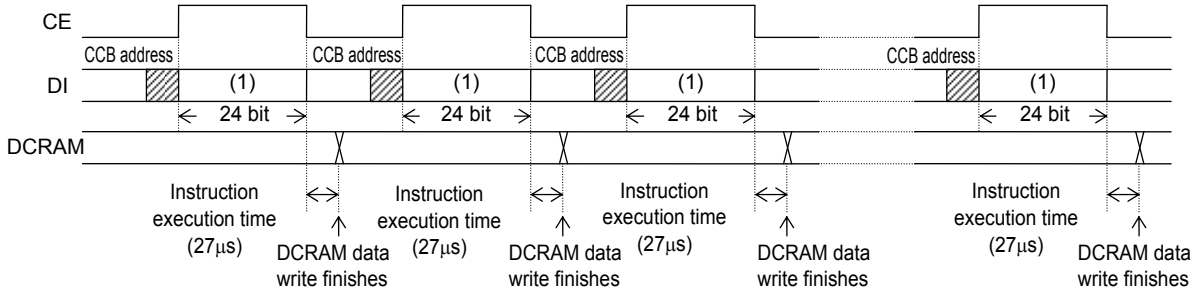
This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5×7 or 5×8 dot matrix display data using CGROM or CGRAM.

IM1, IM2: Sets the method of writing data to DCRAM

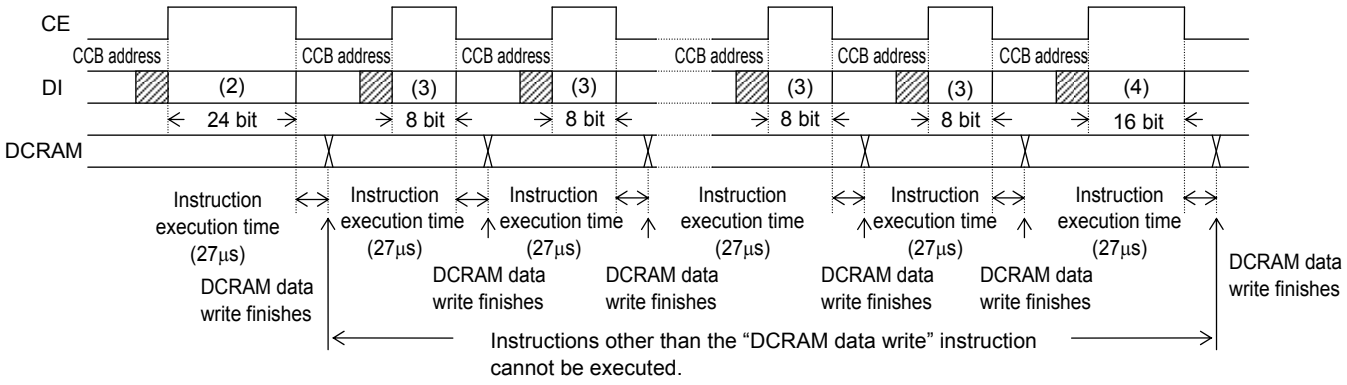
IM1	IM2	DCRAM data write method
0	0	Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)
1	0	Normal increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.)
0	1	Super increment mode DCRAM data write (Writes 2 to 13 characters of DCRAM data in single operation.)

Notes: *16.

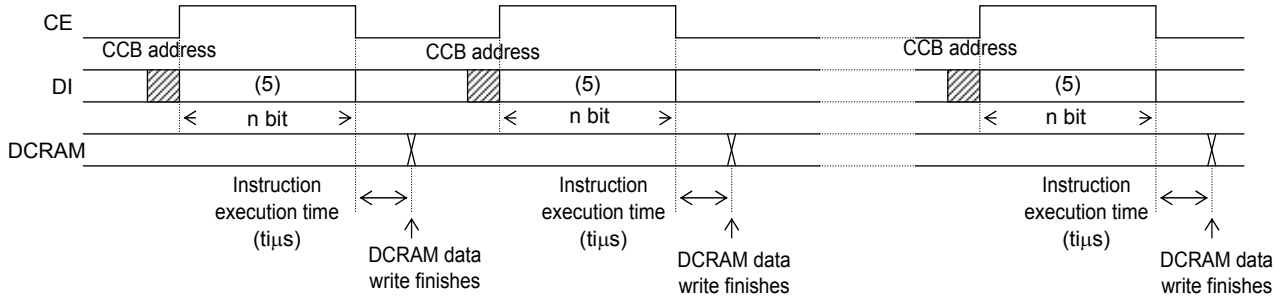
• DCRAM data write method when IM1 = 0, IM2 = 0



• DCRAM data write method when IM1 = 1, IM2 = 0
(Instructions other than the "DCRAM data write" instruction cannot be executed.)



• DCRAM data write method when IM1 = 0, IM2 = 1



$ti=13.5\mu s\times(\frac{n}{8}-1)$
(n=8m+16, m is an integer between 2 and 13 that is the number of characters written as DCRAM data.)
For example

When n= 32 bits (m=2): ti= 40.5μs (fosc=300kHz, f_{CK}=300kHz)
When n= 80 bits (m=8) : ti=121.5μs (fosc=300kHz, f_{CK}=300kHz)
When n=120 bits (m=13): ti=189.0μs (fosc=300kHz, f_{CK}=300kHz)

Note that the instruction execution time of 27μs and ti values in μs apply when fosc=300kHz and f_{CK}=300kHz, and that these execution times will differ when the CR oscillator frequency fosc and external clock frequency f_{CK} differ.

Data format at (1) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	0	0	X	X	0	1	0	1

X: don’t care

Data format at (2) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	1	0	X	X	0	1	0	1

X: don’t care

Data format at (3) (8 bits)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

Data format at (4) (16 bits)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	0	0	X	X	0	1	0	1

Data format at (5) (n bit)

Code																		
Dz	Dz+1	Dz+2	Dz+3	Dz+4	Dz+5	Dz+6	Dz+7	•••••••••••••••••••••••••••							D88	D89	D90	D91	D92	D93	D94	D95
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	•••••••••••••••••••••••••••							$AC0_{m-1}$	$AC1_{m-1}$	$AC2_{m-1}$	$AC3_{m-1}$	$AC4_{m-1}$	$AC5_{m-1}$	$AC6_{m-1}$	$AC7_{m-1}$

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$AC0_m$	$AC1_m$	$AC2_m$	$AC3_m$	$AC4_m$	$AC5_m$	$AC6_m$	$AC7_m$	$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	X	0	1	0	1

X: don’t care

Here, n=8m+16, z=104-8m (m is an integer between 2 and 13 that is the number of characters written as DCRAM data.)

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$)+2	$AC0_3$ to $AC7_3$
⋮	⋮
($DA0_1$ to $DA5_1$)+(m-3)	$AC0_{m-2}$ to $AC7_{m-2}$
($DA0_1$ to $DA5_1$)+(m-2)	$AC0_{m-1}$ to $AC7_{m-1}$
($DA0_1$ to $DA5_1$)+(m-1)	$AC0_m$ to $AC7_m$

Example 1: When n=32 bits (m=2: 2 characters DCRAM data write operation)

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	X	0	1	0	1

X: don’t care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$

Example 2: When n=80 bits (m=8: 8 characters DCRAM data write operation)

Code															
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D56	D57	D58	D59	D60	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70	D71
$AC0_3$	$AC1_3$	$AC2_3$	$AC3_3$	$AC4_3$	$AC5_3$	$AC6_3$	$AC7_3$	$AC0_4$	$AC1_4$	$AC2_4$	$AC3_4$	$AC4_4$	$AC5_4$	$AC6_4$	$AC7_4$

Code															
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87
$AC0_5$	$AC1_5$	$AC2_5$	$AC3_5$	$AC4_5$	$AC5_5$	$AC6_5$	$AC7_5$	$AC0_6$	$AC1_6$	$AC2_6$	$AC3_6$	$AC4_6$	$AC5_6$	$AC6_6$	$AC7_6$

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AC0_7$	$AC1_7$	$AC2_7$	$AC3_7$	$AC4_7$	$AC5_7$	$AC6_7$	$AC7_7$	$AC0_8$	$AC1_8$	$AC2_8$	$AC3_8$	$AC4_8$	$AC5_8$	$AC6_8$	$AC7_8$

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X	0	1	X	X	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$)+2	$AC0_3$ to $AC7_3$
($DA0_1$ to $DA5_1$)+3	$AC0_4$ to $AC7_4$
($DA0_1$ to $DA5_1$)+4	$AC0_5$ to $AC7_5$
($DA0_1$ to $DA5_1$)+5	$AC0_6$ to $AC7_6$
($DA0_1$ to $DA5_1$)+6	$AC0_7$ to $AC7_7$
($DA0_1$ to $DA5_1$)+7	$AC0_8$ to $AC7_8$

Example 3: When n=120 bits (m=13: 13 characters DCRAM data write operation)

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
$AC0_1$	$AC1_1$	$AC2_1$	$AC3_1$	$AC4_1$	$AC5_1$	$AC6_1$	$AC7_1$	$AC0_2$	$AC1_2$	$AC2_2$	$AC3_2$	$AC4_2$	$AC5_2$	$AC6_2$	$AC7_2$

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
$AC0_3$	$AC1_3$	$AC2_3$	$AC3_3$	$AC4_3$	$AC5_3$	$AC6_3$	$AC7_3$	$AC0_4$	$AC1_4$	$AC2_4$	$AC3_4$	$AC4_4$	$AC5_4$	$AC6_4$	$AC7_4$

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
$AC0_5$	$AC1_5$	$AC2_5$	$AC3_5$	$AC4_5$	$AC5_5$	$AC6_5$	$AC7_5$	$AC0_6$	$AC1_6$	$AC2_6$	$AC3_6$	$AC4_6$	$AC5_6$	$AC6_6$	$AC7_6$

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
$AC0_7$	$AC1_7$	$AC2_7$	$AC3_7$	$AC4_7$	$AC5_7$	$AC6_7$	$AC7_7$	$AC0_8$	$AC1_8$	$AC2_8$	$AC3_8$	$AC4_8$	$AC5_8$	$AC6_8$	$AC7_8$

Code															
D64	D65	D66	D67	D68	D69	D70	D71	D72	D73	D74	D75	D76	D77	D78	D79
$AC0_9$	$AC1_9$	$AC2_9$	$AC3_9$	$AC4_9$	$AC5_9$	$AC6_9$	$AC7_9$	$AC0_{10}$	$AC1_{10}$	$AC2_{10}$	$AC3_{10}$	$AC4_{10}$	$AC5_{10}$	$AC6_{10}$	$AC7_{10}$

Code															
D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
$AC0_{11}$	$AC1_{11}$	$AC2_{11}$	$AC3_{11}$	$AC4_{11}$	$AC5_{11}$	$AC6_{11}$	$AC7_{11}$	$AC0_{12}$	$AC1_{12}$	$AC2_{12}$	$AC3_{12}$	$AC4_{12}$	$AC5_{12}$	$AC6_{12}$	$AC7_{12}$

Code															
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111
$AC0_{13}$	$AC1_{13}$	$AC2_{13}$	$AC3_{13}$	$AC4_{13}$	$AC5_{13}$	$AC6_{13}$	$AC7_{13}$	$DA0_1$	$DA1_1$	$DA2_1$	$DA3_1$	$DA4_1$	$DA5_1$	X	X

Code								
D112	D113	D114	D115	D116	D117	D118	D119
0	1	X	X	0	1	0	1

X: don't care

Correspondence between the DCRAM address and the DCRAM data

DCRAM address	DCRAM data
$DA0_1$ to $DA5_1$	$AC0_1$ to $AC7_1$
($DA0_1$ to $DA5_1$)+1	$AC0_2$ to $AC7_2$
($DA0_1$ to $DA5_1$)+2	$AC0_3$ to $AC7_3$
($DA0_1$ to $DA5_1$)+3	$AC0_4$ to $AC7_4$
($DA0_1$ to $DA5_1$)+4	$AC0_5$ to $AC7_5$
($DA0_1$ to $DA5_1$)+5	$AC0_6$ to $AC7_6$
($DA0_1$ to $DA5_1$)+6	$AC0_7$ to $AC7_7$

DCRAM address	DCRAM data
($DA0_1$ to $DA5_1$)+7	$AC0_8$ to $AC7_8$
($DA0_1$ to $DA5_1$)+8	$AC0_9$ to $AC7_9$
($DA0_1$ to $DA5_1$)+9	$AC0_{10}$ to $AC7_{10}$
($DA0_1$ to $DA5_1$)+10	$AC0_{11}$ to $AC7_{11}$
($DA0_1$ to $DA5_1$)+11	$AC0_{12}$ to $AC7_{12}$
($DA0_1$ to $DA5_1$)+12	$AC0_{13}$ to $AC7_{13}$

• ADRAM data write ... <Specifies the ADRAM address and stores data at that address>
(Write data to ADRAM)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM1	IM2	X	X	0	1	1	0

X: don't care

RA0 to RA3:ADRAM address

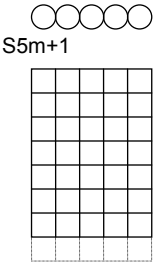
RA0	RA1	RA2	RA3

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AD1 to AD5: ADATA display data

In addition to the 5×7 or 5×8 dot matrix display data (MDATA), this IC supports direct display of the five accessory display segments provided in each digit as ADATA. This display function does not use CGROM or CGRAM. The figure below shows the correspondence between the data and the display. When ADn = 1(where n is an integer between 1 and 5) the segment corresponding to that data will be turned on.



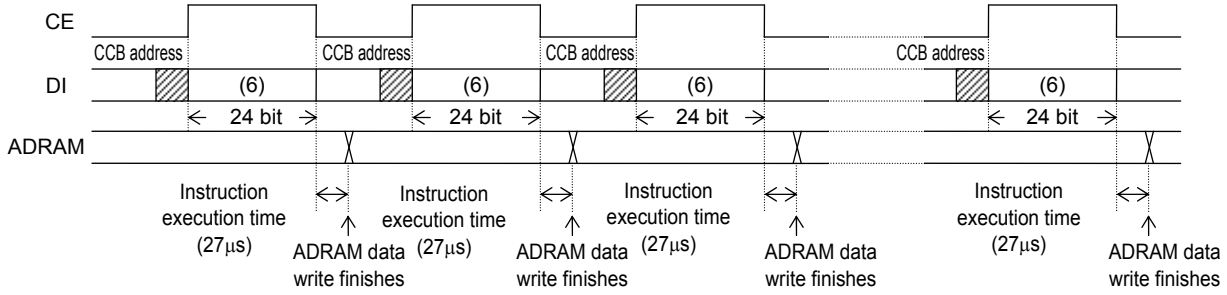
ADATA	Corresponding output pin
AD1	S5m+1 (m is an integer between 0 and 12)
AD2	S5m+2
AD3	S5m+3
AD4	S5m+4
AD5	S5m+5

IM1, IM2: Sets the method of writing data to ADRAM

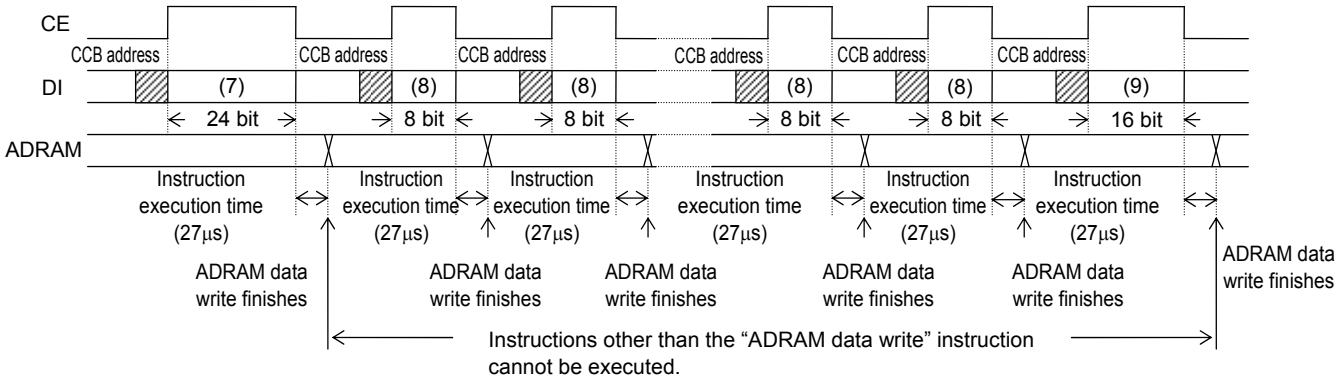
IM1	IM2	ADRAM data write method
0	0	Normal ADRAM data write (Specifies the ADRAM address and writes the ADRAM data.)
1	0	Nomal increment mode ADRAM data write (Increments the ADRAM address by +1 each time data is written to ADRAM.)
0	1	Super increment mode ADRAM data write (Writes 2 to 13 digits of ADRAM data in single operation.)

Notes: *17.

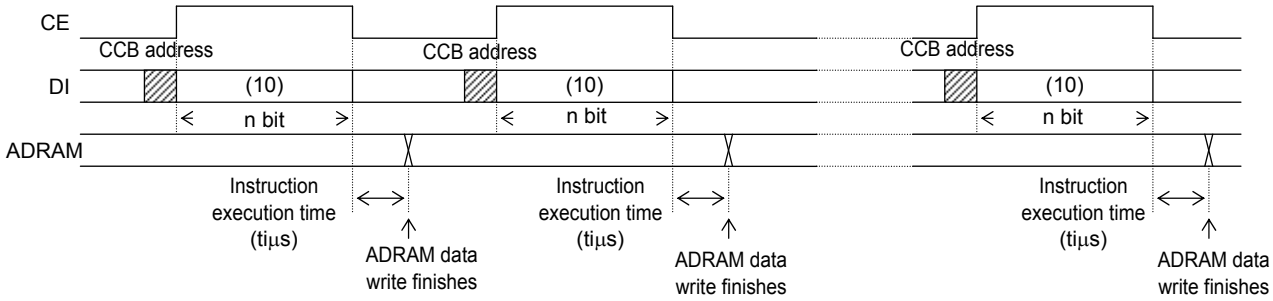
• ADRAM data write method when IM1 = 0, IM2 = 0



• ADRAM data write method when IM1 = 1, IM2 = 0
(Instructions other than the "ADRAM data write" instruction cannot be executed.)



• ADRAM data write method when IM1 = 0, IM2 = 1



$ti=13.5\mu s\times(\frac{n}{8}-1)$
(n=8m+16, m is an integer between 2 and 13 that is the number of characters written as ADRAM data.)
For example

When n= 32 bits (m=2): ti= 40.5μs (fosc=300kHz, f_{CK}=300kHz)
When n= 80 bits (m=8): ti=121.5μs (fosc=300kHz, f_{CK}=300kHz)
When n=120 bits (m=13): ti=189.0μs (fosc=300kHz, f_{CK}=300kHz)

Note that the instruction execution time of 27μs and ti values in μs apply when fosc=300kHz and f_{CK}=300kHz, and that these execution times will differ when the CR oscillator frequency fosc and external clock frequency f_{CK} differ.

Data format at (6) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	0	0	X	X	0	1	1	0

X: don't care

Data format at (7) (24 bits)

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	1	0	X	X	0	1	1	0

X: don't care

Data format at (8) (8 bits)

Code							
D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X

Data format at (9) (16 bits)

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
AD1	AD2	AD3	AD4	AD5	X	X	X	0	0	X	X	0	1	1	0

X: don't care

Data format at (10) (n bit)

Code																		
Dz	Dz+1	Dz+2	Dz+3	Dz+4	Dz+5	Dz+6	Dz+7	•••••••••••••••••••••••••••••	D88	D89	D90	D91	D92	D93	D94	D95
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	•••••••••••••••••••••••••••••	$AD1_{m-1}$	$AD2_{m-1}$	$AD3_{m-1}$	$AD4_{m-1}$	$AD5_{m-1}$	X	X	X

Code																							
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$AD1_m$	$AD2_m$	$AD3_m$	$AD4_m$	$AD5_m$	X	X	X	$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X	0	1	X	X	0	1	1	0

X: don't care

Here, n=8m+16, z=104-8m
(m is an integer between 2 and 13 that is the number of characters written as ADRAM data.)

Correspondence between the ADRAM address and theADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$
($RA0_1$ to $RA3_1$)+2	$AD1_3$ to $AD5_3$
⋮	⋮
($RA0_1$ to $RA3_1$)+(m-3)	$AD1_{m-2}$ to $AD5_{m-2}$
($RA0_1$ to $RA3_1$)+(m-2)	$AD1_{m-1}$ to $AD5_{m-1}$
($RA0_1$ to $RA3_1$)+(m-1)	$AD1_m$ to $AD5_m$

Example 1: When n=32 bits (m=2: 2 characters ADRAM data write operation)

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	$AD1_2$	$AD2_2$	$AD3_3$	$AD4_4$	$AD5_5$	X	X	X

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X	0	1	X	X	0	1	1	0

X: don’t care

Correspondence between the ADRAM address and the ADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$

Example 2: When n=80 bits (m=8: 8 characters ADRAM data write operation)

Code															
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	$AD1_2$	$AD2_2$	$AD3_2$	$AD4_2$	$AD5_2$	X	X	X

Code															
D56	D57	D58	D59	D60	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70	D71
$AD1_3$	$AD2_3$	$AD3_3$	$AD4_3$	$AD5_3$	X	X	X	$AD1_4$	$AD2_4$	$AD3_4$	$AD4_4$	$AD5_4$	X	X	X

Code															
D72	D73	D74	D75	D76	D77	D78	D79	D80	D81	D82	D83	D84	D85	D86	D87
$AD1_5$	$AD2_5$	$AD3_5$	$AD4_5$	$AD5_5$	X	X	X	$AD1_6$	$AD2_6$	$AD3_6$	$AD4_6$	$AD5_6$	X	X	X

Code															
D88	D89	D90	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100	D101	D102	D103
$AD1_7$	$AD2_7$	$AD3_7$	$AD4_7$	$AD5_7$	X	X	X	$AD1_8$	$AD2_8$	$AD3_8$	$AD4_8$	$AD5_8$	X	X	X

Code															
D104	D105	D106	D107	D108	D109	D110	D111	D112	D113	D114	D115	D116	D117	D118	D119
$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X	0	1	X	X	0	1	1	0

X: don't care

Correspondence between the ADRAM address and the ADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$
($RA0_1$ to $RA3_1$)+2	$AD1_3$ to $AD5_3$
($RA0_1$ to $RA3_1$)+3	$AD1_4$ to $AD5_4$
($RA0_1$ to $RA3_1$)+4	$AD1_5$ to $AD5_5$
($RA0_1$ to $RA3_1$)+5	$AD1_6$ to $AD5_6$
($RA0_1$ to $RA3_1$)+6	$AD1_7$ to $AD5_7$
($RA0_1$ to $RA3_1$)+7	$AD1_8$ to $AD5_8$

Example 3: When n=120 bits (m=13: 13 characters ADRAM data write operation)

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
$AD1_1$	$AD2_1$	$AD3_1$	$AD4_1$	$AD5_1$	X	X	X	$AD1_2$	$AD2_2$	$AD3_2$	$AD4_2$	$AD5_2$	X	X	X

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
$AD1_3$	$AD2_3$	$AD3_3$	$AD4_3$	$AD5_3$	X	X	X	$AD1_4$	$AD2_4$	$AD3_4$	$AD4_4$	$AD5_4$	X	X	X

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
$AD1_5$	$AD2_5$	$AD3_5$	$AD4_5$	$AD5_5$	X	X	X	$AD1_6$	$AD2_6$	$AD3_6$	$AD4_6$	$AD5_6$	X	X	X

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
$AD1_7$	$AD2_7$	$AD3_7$	$AD4_7$	$AD5_7$	X	X	X	$AD1_8$	$AD2_8$	$AD3_8$	$AD4_8$	$AD5_8$	X	X	X

Code															
D64	D65	D66	D67	D68	D69	D70	D71	D72	D73	D74	D75	D76	D77	D78	D79
$AD1_9$	$AD2_9$	$AD3_9$	$AD4_9$	$AD5_9$	X	X	X	$AD1_{10}$	$AD2_{10}$	$AD3_{10}$	$AD4_{10}$	$AD5_{10}$	X	X	X

Code															
D80	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90	D91	D92	D93	D94	D95
$AD1_{11}$	$AD2_{11}$	$AD3_{11}$	$AD4_{11}$	$AD5_{11}$	X	X	X	$AD1_{12}$	$AD2_{12}$	$AD3_{12}$	$AD4_{12}$	$AD5_{12}$	X	X	X

Code															
D96	D97	D98	D99	D100	D101	D102	D103	D104	D105	D106	D107	D108	D109	D110	D111
$AD1_{13}$	$AD2_{13}$	$AD3_{13}$	$AD4_{13}$	$AD5_{13}$	X	X	X	$RA0_1$	$RA1_1$	$RA2_1$	$RA3_1$	X	X	X	X

Code							
D112	D113	D114	D115	D116	D117	D118	D119
0	1	X	X	0	1	1	0

X: don't care

Correspondence between the ADRAM address and the ADRAM data

ADRAM address	ADRAM data
$RA0_1$ to $RA3_1$	$AD1_1$ to $AD5_1$
($RA0_1$ to $RA3_1$)+1	$AD1_2$ to $AD5_2$
($RA0_1$ to $RA3_1$)+2	$AD1_3$ to $AD5_3$
($RA0_1$ to $RA3_1$)+3	$AD1_4$ to $AD5_4$
($RA0_1$ to $RA3_1$)+4	$AD1_5$ to $AD5_5$
($RA0_1$ to $RA3_1$)+5	$AD1_6$ to $AD5_6$
($RA0_1$ to $RA3_1$)+6	$AD1_7$ to $AD5_7$

ADRAM address	ADRAM data
($RA0_1$ to $RA3_1$)+7	$AD1_8$ to $AD5_8$
($RA0_1$ to $RA3_1$)+8	$AD1_9$ to $AD5_9$
($RA0_1$ to $RA35_1$)+9	$AD1_{10}$ to $AD5_{10}$
($RA0_1$ to $RA3_1$)+10	$AD1_{11}$ to $AD5_{11}$
($RA0_1$ to $RA3_1$)+11	$AD1_{12}$ to $AD5_{12}$
($RA0_1$ to $RA3_1$)+12	$AD1_{13}$ to $AD5_{13}$