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LC75818PT

1/8 to 1/10-Duty Dot Matrix LCD Controller & Driver with Key Input Function

ON Semiconductor®

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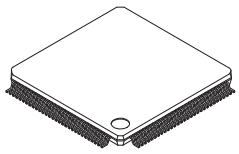

TQFP120 14x14 / TQFP120

Overview

The LC75818PT is 1/8 to 1/10 duty dot matrix LCD display controllers/drivers that support the display of characters, numbers, and symbols. In addition to generating dot matrix LCD drive signals based on data transferred serially from a microcontroller, the LC75818PT also provide on-chip character display ROM and RAM to allow display systems to be implemented easily. These products also provide up to 4 general-purpose output ports and incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 30 keys
  (A key scan is performed only when a key is pressed.)
- Controls and drives a 5×7, 5×8, or 5×9 dot matrix LCD.
- Supports accessory display segment drive (up to 80 segments)
- Display technique: 1/8 duty 1/4 bias drive (5×7 dots)
  1/9 duty 1/4 bias drive (5×8 dots)
  1/10 duty 1/4 bias drive (5×9 dots)
- Display digits: 16 digits×1 line (5×7 dots, 5×8 dots, 5×9 dots)
- Display control memory
  CGROM: 240 characters (5×7, 5×8, or 5×9 dots)
  CGRAM: 16 characters (5×7, 5×8, or 5×9 dots)
  ADRAM: 16×5 bits
  DCRAM: 64×8 bits
- Instruction function
  Display on/off control
  Display shift function
- Sleep mode can be used to reduce current drain.
- Built-in display contrast adjustment circuit
- The frame frequency of the common and segment output waveforms can be controlled by instructions.
- Serial data I/O supports CCB* format communication with the system controller.
- Independent LCD driver block power supply V_{LCD}
- A voltage detection type reset circuit is provided to initialize the IC and prevent incorrect display.
- The $\overline{INH}$ pin is provided. This pin turns off the display, disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 44 of this data sheet.

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +4.2	V
	V_{LCD} max	V_{LCD}	−0.3 to +11.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +4.2	V
		CE, CL, DI, $\overline{INH}$ V_{DD}=2.7 to 3.6V	−0.3 to +6.5	
	$V_{IN}2$	OSC, KI1 to KI5, TEST	−0.3 to V_{DD} +0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, $V_{LCD}4$	−0.3 to V_{LCD} +0.3	
Output voltage	$V_{OUT}1$	DO	−0.3 to +6.5	V
	$V_{OUT}2$	OSC, KS1 to KS6, P1 to P4	−0.3 to V_{DD} +0.3	
	$V_{OUT}3$	$V_{LCD}0$, S1 to S80, COM1 to COM10	−0.3 to V_{LCD} +0.3	
Output current	$I_{OUT}1$	S1 to S80	300	μA
	$I_{OUT}2$	COM1 to COM10	3	mA
	$I_{OUT}3$	KS1 to KS6	1	
	$I_{OUT}4$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range at Ta = −40°C to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		3.6	V
	V_{LCD}	V_{LCD} When the display contrast adjustment circuit is used.	7.0		10.0	
		V_{LCD} When the display contrast adjustment circuit is not used.	4.5		10.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	$V_{LCD}4$ +4.5		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		3/4 ($V_{LCD}0$ −$V_{LCD}4$)	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		2/4 ($V_{LCD}0$ −$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}3$	$V_{LCD}3$		1/4 ($V_{LCD}0$ −$V_{LCD}4$)	$V_{LCD}0$	
	$V_{LCD}4$	$V_{LCD}4$	0		1.5	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8V_{DD}		3.6	V
		CE, CL, DI, $\overline{INH}$ V_{DD} = 2.7 to 3.6 V	0.8V_{DD}		5.5	
	$V_{IH}2$	OSC external clock operating mode	0.8V_{DD}		V_{DD}	
	$V_{IH}3$	KI1 to KI5	0.6V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$, KI1 to KI5	0		0.2V_{DD}	V
	$V_{IL}2$	OSC external clock operating mode	0		0.2V_{DD}	
Output pull-up voltage	V_{OUP}	DO	0		5.5	V

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Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Recommended external resistor for RC oscillation	Rosc	OSC RC oscillator operating mode		10		kΩ
Recommended external capacitor for RC oscillation	Cosc	OSC RC oscillator operating mode		470		pF
Guaranteed range of RC oscillation	fosc	OSC RC oscillator operating mode	150	300	600	kHz
External clock operating frequency	f_{CK}	OSC external clock operating mode [Figure 4]	100	300	600	kHz
External clock duty cycle	D_{CK}	OSC external clock operating mode [Figure 4]	30	50	70	%
Data setup time	tds	CL, DI [Figure 2],[Figure 3]	160			ns
Data hold time	tdh	CL, DI [Figure 2],[Figure 3]	160			ns
CE wait time	tcp	CE, CL [Figure 2],[Figure 3]	160			ns
CE setup time	tcs	CE, CL [Figure 2],[Figure 3]	160			ns
CE hold time	tch	CE, CL [Figure 2],[Figure 3]	160			ns
High level clock pulse width	tφH	CL [Figure 2],[Figure 3]	160			ns
Low level clock pulse width	tφL	CL [Figure 2],[Figure 3]	160			ns
DO output delay time	tdc	DO R_{PU}=4.7kΩ C_L=10pF *1[Figure 2],[Figure 3]			1.5	μs
DO rise time	tdr	DO R_{PU}=4.7kΩ C_L=10pF *1[Figure 2],[Figure 3]			1.5	μs

Note: *1. Since the DO pin is an open-drain output, these times depend on the values of the pull-up resistor R_{PU} and the load capacitance C_L.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

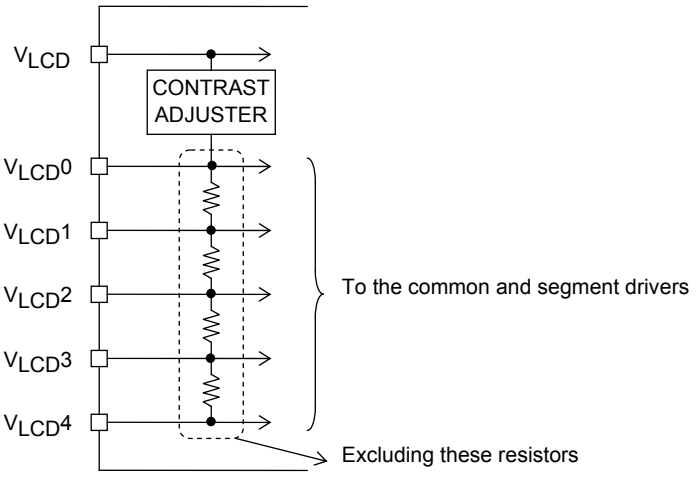
Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$, KI1 to KI5			$0.1V_{DD}$		V
Power-down detection voltage	V_{DET}			2.0	2.2	2.4	V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 3.6 V			5.0	μA
			V_I = 5.5 V V_{DD} = 2.7 to 3.6 V			5.0	
	$I_{IH}2$	OSC	$V_I = V_{DD}$ external clock operating mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0 V	-5.0			μA
	$I_{IL}2$	OSC	V_I = 0 V external clock operating mode	-5.0			
Input floating voltage	V_{IF}	KI1 to KI5				$0.05V_{DD}$	V
Pull-down resistance	R_{PD}	KI1 to KI5	V_{DD} = 3.3 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO	V_O = 5.5 V			6.0	μA
Output high level voltage	$V_{OH}1$	S1 to S80	I_O = –20 μA	$V_{LCD}O$ –0.6			V
	$V_{OH}2$	COM1 to COM10	I_O = –100 μA	$V_{LCD}O$ –0.6			
	$V_{OH}3$	KS1 to KS6	I_O = –250 μA	V_{DD} –0.8	V_{DD} –0.4	V_{DD} –0.1	
	$V_{OH}4$	P1 to P4	I_O = –1 mA	V_{DD} –0.9			
Output low level voltage	$V_{OL}1$	S1 to S80	I_O = 20 μA			$V_{LCD}4$ +0.6	V
	$V_{OL}2$	COM1 to COM10	I_O = 100 μA			$V_{LCD}4$ +0.6	
	$V_{OL}3$	KS1 to KS6	I_O = 12.5 μA	0.1	0.4	1.2	
	$V_{OL}4$	P1 to P4	I_O = 1 mA			0.9	
	$V_{OL}5$	DO	I_O = 1 mA		0.1	0.3	

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Output middle level voltage *2	$V_{MID}1$	S1 to S80	I_O = ±20 μA	2/4 ($V_{LCD}0$ – $V_{LCD}4$) –0.6		2/4 ($V_{LCD}0$ – $V_{LCD}4$) +0.6	V
	$V_{MID}2$	COM1 to COM10	I_O = ±100 μA	3/4 ($V_{LCD}0$ – $V_{LCD}4$) –0.6		3/4 ($V_{LCD}0$ – $V_{LCD}4$) +0.6	
	$V_{MID}3$	COM1 to COM10	I_O = ±100 μA	1/4 ($V_{LCD}0$ – $V_{LCD}4$) –0.6		1/4 ($V_{LCD}0$ – $V_{LCD}4$) +0.6	
Oscillator frequency	fosc	OSC	Rosc = 10 kΩ Cosc = 470 pF	210	300	390	kHz
Current drain	$I_{DD}1$	V_{DD}	sleep mode			100	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 3.6 V output open fosc = 300 kHz		500	1000	
	$I_{LCD}1$	V_{LCD}	sleep mode			15	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 10.0 V output open fosc = 300 kHz When the display contrast adjustment circuit is used.		450	900	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 10.0 V output open fosc = 300 kHz When the display contrast adjustment circuit is not used.		200	400	

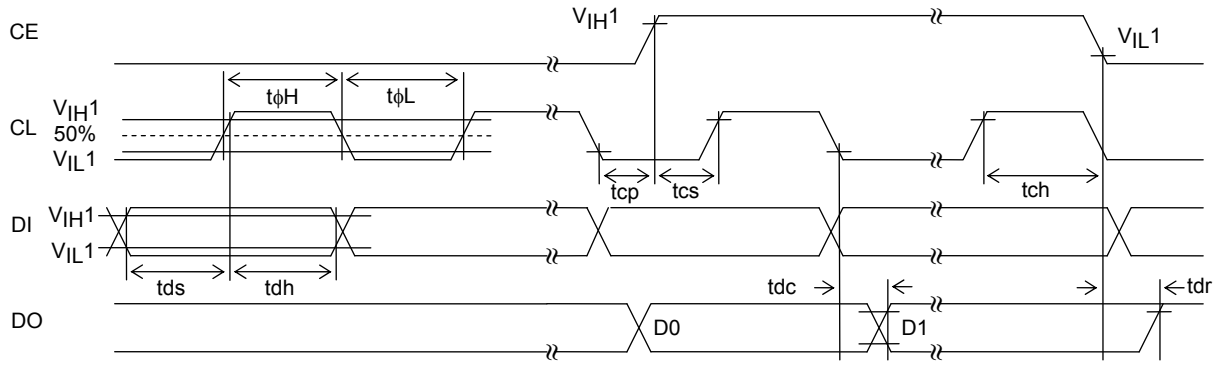
Note: *2. Excluding the bias voltage generation divider resistor built into the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, $V_{LCD}3$, and $V_{LCD}4$. (See Figure 1.)



[Figure 1]

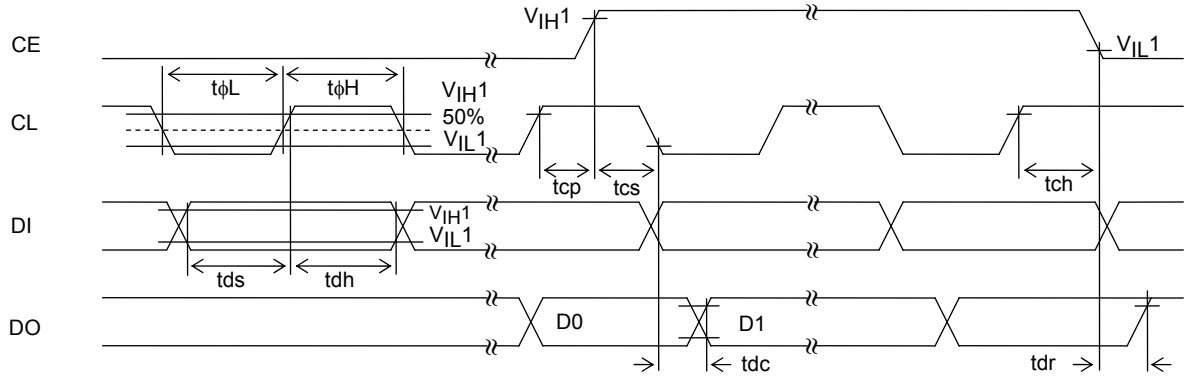
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(1) When CL is stopped at the low level



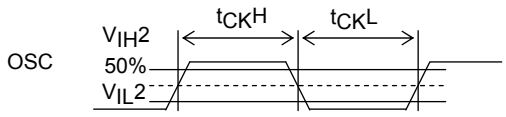
[Figure 2]

(2) When CL is stopped at the high level



[Figure 3]

(3) OSC pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \text{ [kHz]}$$

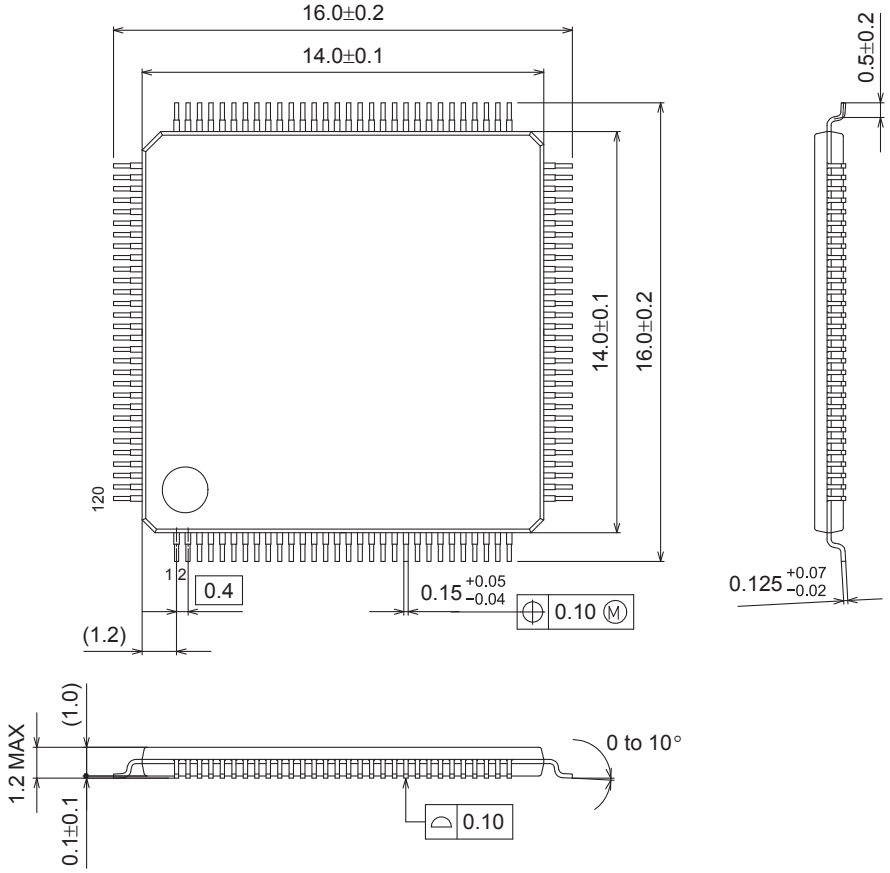
$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100[\%]$$

[Figure 4]

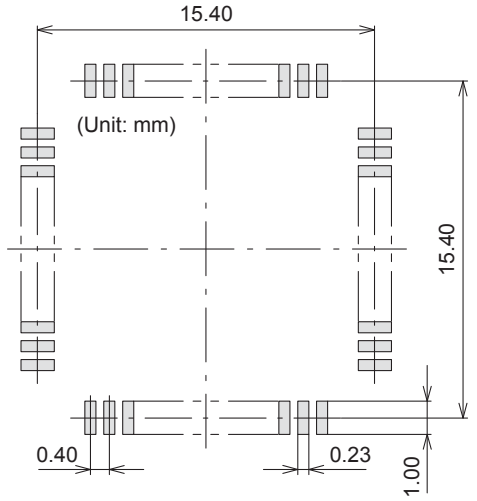
Package Dimensions

unit : mm

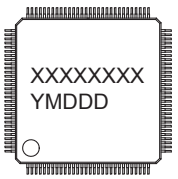
TQFP120 14x14 / TQFP120
CASE 932AZ
ISSUE A



SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



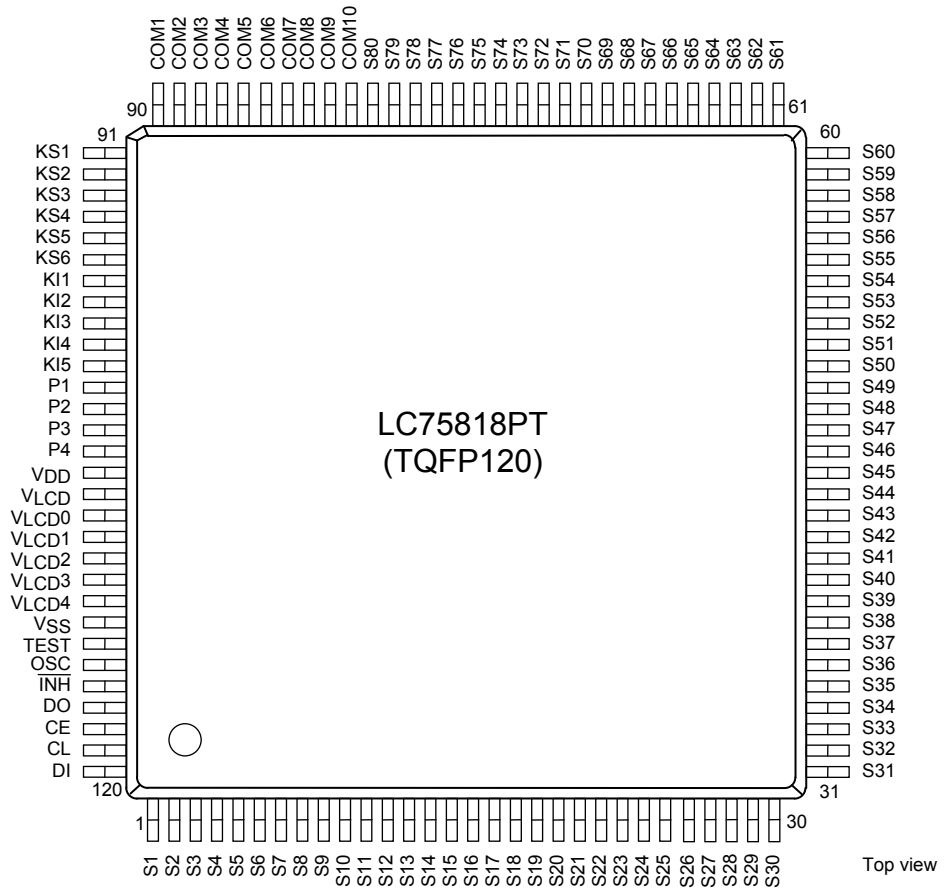
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

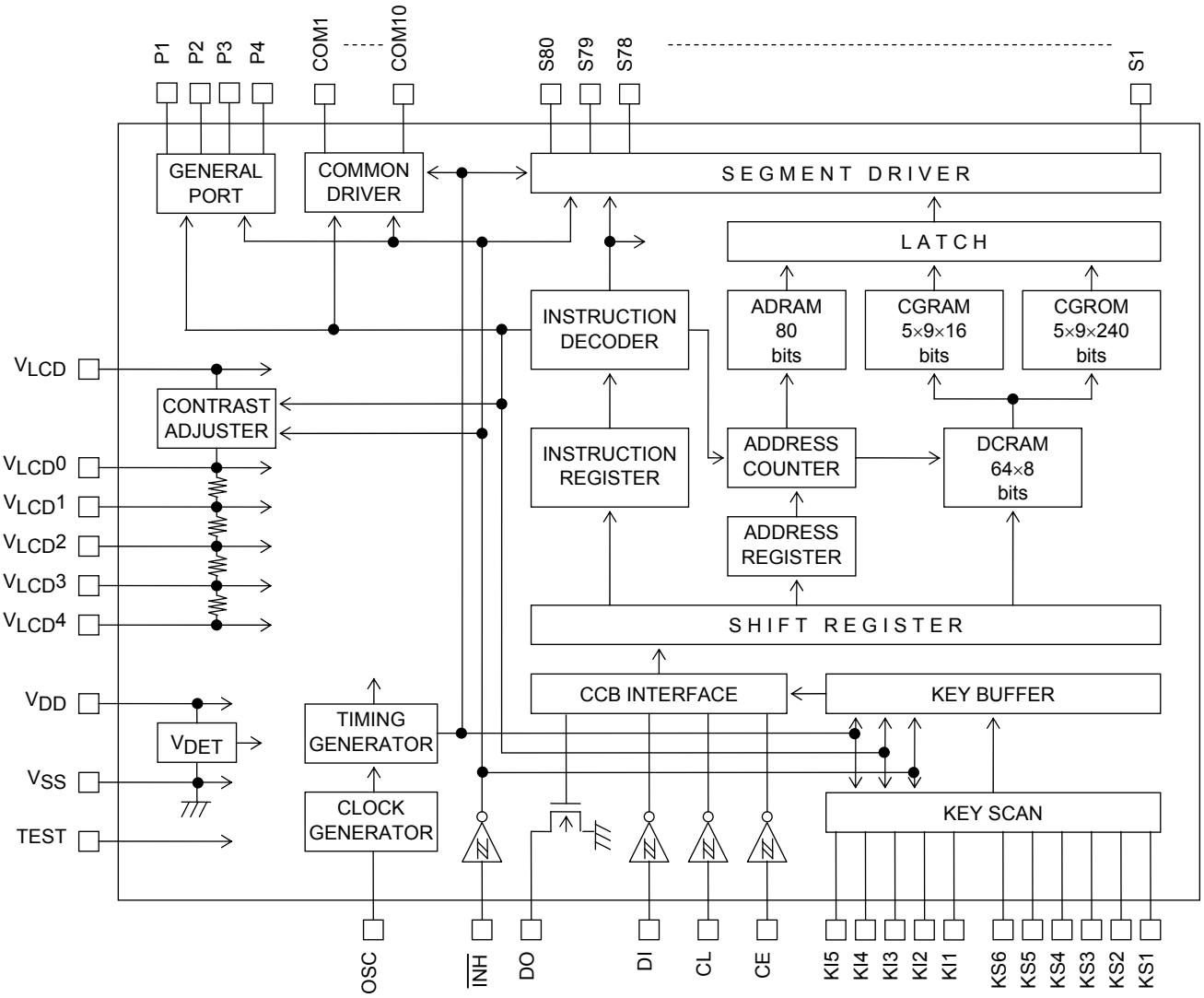
NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignments



Block Diagram



Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1 to S80	1 to 80	Segment driver outputs.	-	O	OPEN
COM1 to COM10	90 to 81	Common driver outputs.	-	O	OPEN
KS1 to KS6	91 to 96	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix.	-	O	OPEN
KI1 to KI5	97 to 101	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
P1 to P4	102 to 105	General-purpose outputs. P4 can be used as a clock output port with the "set key scan output port/general-purpose output port state" instruction.	-	O	OPEN
OSC	115	Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can also be used as the external clock input pin with the "set display technique" instruction.	-	I/O	V_{DD}
CE	118	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	H	I	GND
CL	119		↑	I	
DI	120		-	I	
DO	117		-	O	OPEN
$\overline{INH}$	116	Input that turns the display off, disables key scanning, and forces the general-purpose output ports low. • When $\overline{INH}$ is low (V_{SS}): • Display off S1 to S80="L" ($V_{LCD}4$) COM1 to COM10="L" ($V_{LCD}4$) • General-purpose output ports P1 to P4=low (V_{SS}) • Key scanning disabled: KS1 to KS6=low (V_{SS}) • All the key data is reset to low. • When $\overline{INH}$ is high (V_{DD}): • Display on • The state of the pins as key scan output pins or general-purpose output ports can be set with the "set key scan output port/general-purpose output port state" instruction. • Key scanning is enabled. However, serial data can be transferred when the $\overline{INH}$ pin is low.	L	I	V_{DD}
TEST	114	This pin must be connected to ground.	-	I	-
$V_{LCD}0$	108	LCD drive 4/4 bias voltage (high level) supply pin. The level on this pin can be changed by the display contrast adjustment circuit. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V. Also, external power must not be applied to this pin since the pin circuit includes the display contrast adjustment circuit.	-	O	OPEN
$V_{LCD}1$	109	LCD drive 3/4 bias voltage (middle level) supply pin. This pin can be used to supply the 3/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}2$	110	LCD drive 2/4 bias voltage (middle level) supply pin. This pin can be used to supply the 2/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN

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Pin	Pin No.	Function	Active	I/O	Handling when unused
$V_{LCD}3$	111	LCD drive 1/4 bias voltage (middle level) supply pin. This pin can be used to supply the 1/4 ($V_{LCD}0$ - $V_{LCD}4$) voltage level externally.	-	I	OPEN
$V_{LCD}4$	112	LCD drive 0/4 bias voltage (low level) supply pin. Fine adjustment of the display contrast can be implemented by connecting an external variable resistor to this pin. However, ($V_{LCD}0$ - $V_{LCD}4$) must be greater than or equal to 4.5V, and $V_{LCD}4$ must be in the range 0V to 1.5V, inclusive.	-	I	GND
V_{DD}	106	Logic block power supply connection. Provide a voltage of between 2.7to 3.6V.	-	-	-
V_{LCD}	107	LCD driver block power supply connection. Provide a voltage of between 7.0 to 10.0V when the display contrast adjustment circuit is used and provide a voltage of between 4.5 to 10.0V when the circuit is not used.	-	-	-
V_{SS}	113	Power supply connection. Connect to ground.	-	-	-

Block Functions

- AC (address counter)
  AC is a counter that provides the addresses used for DCRAM and ADRAM.
  The address is automatically modified internally, and the LCD display state is retained.

- DCRAM (data control RAM)
  DCRAM is RAM that is used to store display data expressed as 8-bit character codes. (These character codes are converted to 5×7, 5×8, or 5×9 dot matrix character patterns using CGROM or CGRAM.) DCRAM has a capacity of 64×8 bits, and can hold 64 characters. The table below lists the correspondence between the 6-bit DCRAM address loaded into AC and the display position on the LCD panel.

- When the DCRAM address loaded into AC is 00H.

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (hexadecimal)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

However, when the display shift is performed by specifying MDATA, the DCRAM address shifts as shown below.

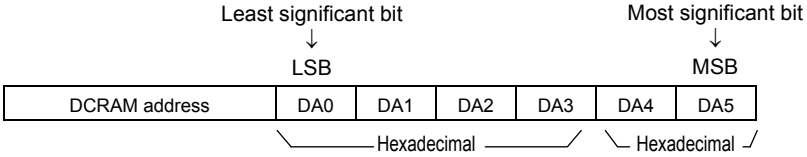
Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (hexadecimal)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

(shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DCRAM address (hexadecimal)	3F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

(shift right)

Note: *3. The DCRAM address is expressed in hexadecimal.



Example: When the DCRAM address is 2EH.

DA0	DA1	DA2	DA3	DA4	DA5
0	1	1	1	0	1

• ADRAM (Additional data RAM)

ADRAM is RAM that is used to store the ADATA display data. ADRAM has a capacity of 16×5 bits, and the stored display data is displayed directly without the use of CGROM or CGRAM. The table below lists the correspondence between the 4-bit ADRAM address loaded into AC and the display position on the LCD panel.

• When the ADRAM address loaded into AC is 0H. (Number of digit displayed: 16)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ADRAM address (hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

However, when the display shift is performed by specifying ADATA, the ADRAM address shifts as shown below.

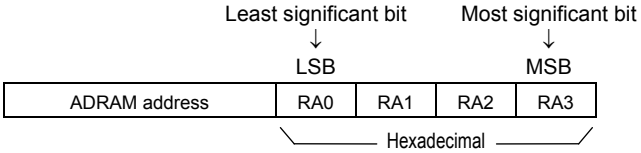
Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ADRAM address (hexadecimal)	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0

(shift left)

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ADRAM address (hexadecimal)	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E

(shift right)

Note: *4. The ADRAM address is expressed in hexadecimal.



Example: When the ADRAM address is AH.

RA0	RA1	RA2	RA3
0	1	0	1

• CGROM (Character generator ROM)

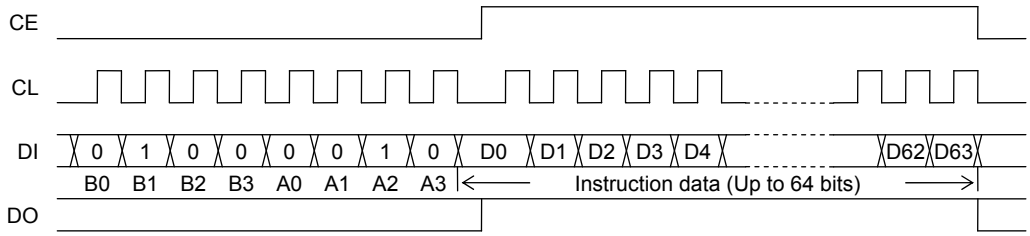
CGROM is ROM that is used to generate the 240 kinds of 5×7, 5×8, or 5×9 dot matrix character patterns from the 8-bit character codes. CGROM has a capacity of 240×45 bits. When a character code is written to DCRAM, the character pattern stored in CGROM corresponding to the character code is displayed at the position on the LCD corresponding to the DCRAM address loaded into AC.

• CGRAM (Character generator RAM)

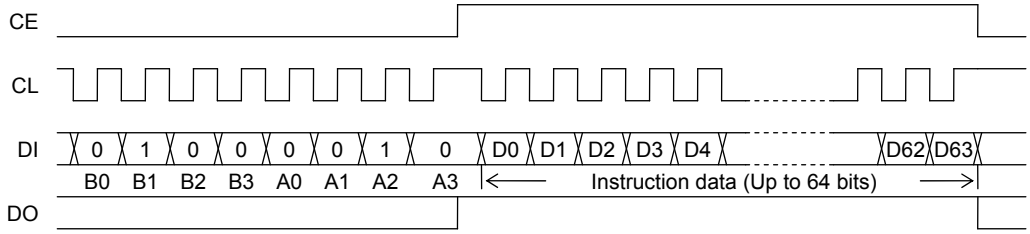
CGRAM is RAM to which user programs can freely write arbitrary character patterns. Up to 16 kinds of 5×7, 5×8, or 5×9 dot matrix character patterns can be stored. CGRAM has a capacity of 16×45 bits.

Serial Data Input

(1) When CL is stopped at the low level



(2) When CL is stopped at the high level



- B0 to B3, A0 to A3: CCB address 42H
- D0 to D63: Instruction data

The data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When transferring instruction data from the microcontroller, applications must assure that the time from the transfer of one set of instruction data until the next instruction data transfer is significantly longer than the instruction execution time.

Instruction Table

Instruction	D0	D1... D39	D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63	Execution time *8
Set display technique *5																			DT1	DT2	FC	OC	0	0	0	1	0μs/108μs *5
Display on/off control			DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	DG14	DG15	DG16	M	A	SC	SP	0	0	1	0	0μs/27μs *9
Display shift																			M	A	R/L	X	0	0	1	1	27μs
Set AC address											DA0	DA1	DA2	DA3	DA4	DA5	X	X	RA0	RA1	RA2	RA3	0	1	0	0	27μs
DCRAM data write *6			AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1	27μs
ADRAM data write *7			AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM	X	X	X	0	1	1	0	27μs
CGRAM data write	CD1	CD2...CD40	CD41	CD42	CD43	CD44	CD45	X	X	X	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	0	1	1	1	27μs
Set display contrast											CT0	CT1	CT2	CT3	X	X	X	X	CTC	X	X	X	1	0	0	0	0μs
Set key scan output port/ general-purpose output port state											KC1	KC2	KC3	KC4	KC5	KC6	PC40	PC41	PC1	PC2	PC3	X	1	0	0	1	0μs

X: don't care

Notes: *5. Be sure to execute the "set display technique" instruction first after power-on (V_{DET}-based system reset). Note that the execution time of this first instruction is 108μs (fosc=300kHz, f_{CK}=300kHz).

*6. The data format differs when the "DCRAM data write" instruction is executed in the increment mode (IM = 1). (See detailed instruction descriptions .)

*7. The data format differs when the "ADRAM data write" instruction is executed in the increment mode (IM = 1). (See detailed instruction descriptions.)

*8. The execution times listed here apply when fosc=300kHz, f_{CK}=300kHz. The execution times differ when the oscillator frequency fosc or the external clock frequency f_{CK} differs.

Example: When fosc = 210kHz, f_{CK} = 210kHz

$$27\mu s \times \frac{300}{210} = 39\mu s,\ 108\mu s \times \frac{300}{210} = 155\mu s$$

*9.When the sleep mode (SP = 1) is set, the execution time is 27μs (when fosc = 300kHz, f_{CK} = 300kHz).

Detailed Instruction Descriptions

• Set display technique ... <Sets the display technique>

(Display technique)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
DT1	DT2	FC	0C	0	0	0	1

X: don't care

Note: Be sure to execute the "set display technique" instruction first after power-on (V_{DET}-based system reset).

DT1, DT2: Sets the display technique

DT1	DT2	Display technique	Output pins	
			COM9	COM10
0	0	1/8 duty, 1/4 bias drive	V_{LCD}4 level	V_{LCD}4 level
1	0	1/9 duty, 1/4 bias drive	COM9	V_{LCD}4 level
0	1	1/10 duty, 1/4 bias drive	COM9	COM10

Note: *10. COMn (n=9,10): Common output

FC: Sets the frame frequency of the common and segment output waveforms

FC	Frame frequency		
	1/8 duty, 1/4 bias drive f8[Hz]	1/9 duty, 1/4 bias drive f9[Hz]	1/10 duty, 1/4 bias drive f10[Hz]
0	fosc/3072, f_{CK}/3072	fosc/3456, f_{CK}/3456	fosc/3840, f_{CK}/3840
1	fosc/1536, f_{CK}/1536	fosc/1728, f_{CK}/1728	fosc/1920, f_{CK}/1920

OC: Sets the RC oscillator operating mode and external clock operating mode.

OC	OSC pin function
0	RC oscillator operating mode
1	External clock operating mode

Note: *11. When selecting the RC oscillator operating mode, be sure to connect an external resistor Rosc and an external capacitor Cosc to the OSC pin.

• Display on/off control ... <Turns the display on or off>

(Display ON/OFF control)

Code																									
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	DG14	DG15	DG16	M	A	SC	SP	0	0	1	0

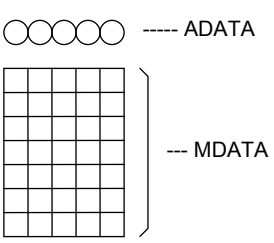
X: don't care

M, A: Specifies the data to be turned on or off

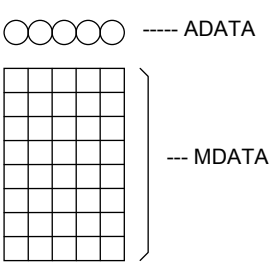
M	A	Display operating state
0	0	Both MDATA and ADATA are turned off (The display is forcibly turned off regardless of the DG1 to DG16 data.)
0	1	Only ADATA is turned on (The ADATA of display digits specified by the DG1 to DG16 data are turned on.)
1	0	Only MDATA is turned on (The MDATA of display digits specified by the DG1 to DG16 data are turned on.)
1	1	Both MDATA and ADATA are turned on (The MDATA and ADATA of display digits specified by the DG1 to DG16 data are turned on.)

Note: *12. MDATA, ADATA

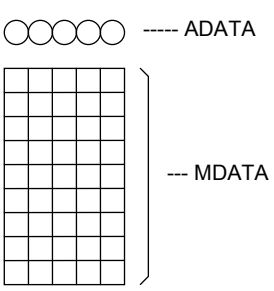
5×7 dot matrix display



5×8 dot matrix display



5×9 dot matrix display



DG1 to DG16: Specifies the display digit

Display digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Display digit data	DG1	DG2	DG3	DG4	DG5	DG6	DG7	DG8	DG9	DG10	DG11	DG12	DG13	DG14	DG15	DG16

For example, if DG1 to DG7 are 1, and DG8 to DG16 are 0, then display digits 1 to 7 will be turned on, and display digits 8 to 16 will be turned off (blanked).

SC: Controls the common and segment output pins

SC	Common and segment output pin states
0	Output of LCD drive waveforms
1	Fixed at the $V_{LCD}4$ level (all segments off)

Note: *13. When SC is 1, the S1 to S80 and COM1 to COM10 output pins are set to the $V_{LCD}4$ level, regardless of the M, A, and DG1 to DG16 data.

SP: Controls the normal mode and sleep mode

SP	Mode
0	Normal mode
1	Sleep mode The common and segment pins go to the $V_{LCD}4$ level and the oscillator on the OSC pin is stopped (although it operates during key scan operations) in RC oscillator operating mode (OC="0") and reception of the external clock is stopped (external clock is received during key scan operations) in external clock operating mode (OC="1"), to reduce current drain. Although the "display on/off control", "set display contrast" and "set key scan output port/general-purpose output port state" (disallowed to set the clock output at the P4 pin) instructions can be executed in this mode, applications must return the IC to normal mode to execute any of the other instruction setting. When the IC is in external clock operating mode, be sure to stop the external clock input after the lapse of the instruction execution time (27μs: f_{CK}=300kHz).

• Display shift ... <Shifts the display>
(Display shift)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
M	A	R/L	X	0	0	1	1

X: don't care

M, A: Specifies the data to be shifted

M	A	Shift operating state
0	0	Neither MDATA nor ADATA is shifted
0	1	Only ADATA is shifted
1	0	Only MDATA is shifted
1	1	Both MDATA and ADATA are shifted

R/L: Specifies the shift direction

R/L	Shift direction
0	Shift left
1	Shift right

• Set AC address... <Specifies the DCRAM and ADRAM address for AC>
(Set AC)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
DA0	DA1	DA2	DA3	DA4	DA5	X	X	RA0	RA1	RA2	RA3	0	1	0	0

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

RA0 to RA3: ADRAM address

RA0	RA1	RA2	RA3

LSB ↑ Least significant bit

MSB ↑ Most significant bit

This instruction loads the 6-bit DCRAM address DA0 to DA5 and the 4-bit ADRAM address RA0 to RA3 into the AC.

• DCRAM data write ... <Specifies the DCRAM address and stores data at that address>
(Write data to DCRAM)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1

X: don't care

DA0 to DA5: DCRAM address

DA0	DA1	DA2	DA3	DA4	DA5

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AC0 to AC7: DCRAM data (character code)

AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

LSB ↑ Least significant bit

MSB ↑ Most significant bit

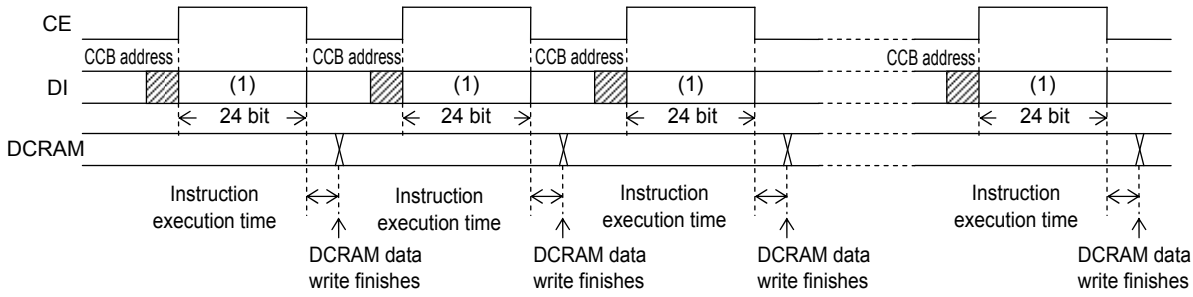
This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code, and is converted to a 5×7, 5× 8, or 5×9 dot matrix display data using CGROM or CGRAM.

IM: Sets the method of writing data to DCRAM

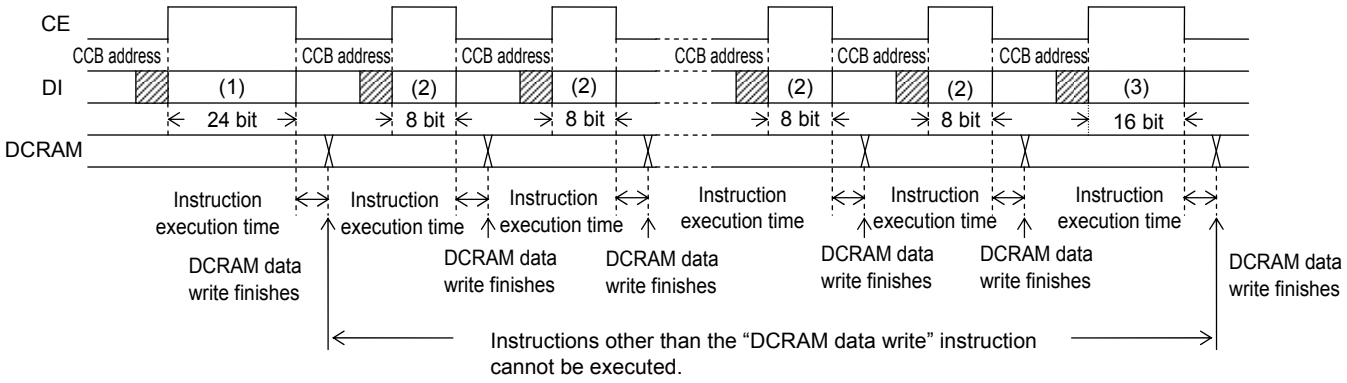
IM	DCRAM data write method
0	Normal DCRAM data write (Specifies the DCRAM address and writes the DCRAM data.)
1	Increment mode DCRAM data write (Increments the DCRAM address by +1 each time data is written to DCRAM.)

Notes: *14.

• DCRAM data write method when IM = 0



• DCRAM data write method when IM = 1
(Instructions other than the “DCRAM data write” instruction cannot be executed.)



Data format at (1) (24 bits)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	DA0	DA1	DA2	DA3	DA4	DA5	X	X	IM	X	X	X	0	1	0	1

X: don’t care

Data format at (2) (8 bits)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7

Data format at (3) (16 bits)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	0	X	X	X	0	1	0	1

X: don’t care

• ADRAM data write ... <Specifies the ADRAM address and stores data at that address>
(Write data to ADRAM)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM	X	X	X	0	1	1	0

X: don’t care

RA0 to RA3:ADRAM address

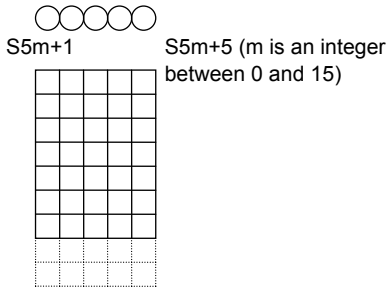
RA0	RA1	RA2	RA3

LSB ↑ Least significant bit

MSB ↑ Most significant bit

AD1 to AD5: ADATA display data

In addition to the 5×7, 5×8, or 5×9 dot matrix display data (MDATA), this IC supports direct display of the five accessory display segments provided in each digit as ADATA. This display function does not use CGROM or CGRAM. The figure below shows the correspondence between the data and the display. When ADn = 1(where n is an integer between 1 and 5) the segment corresponding to that data will be turned on.



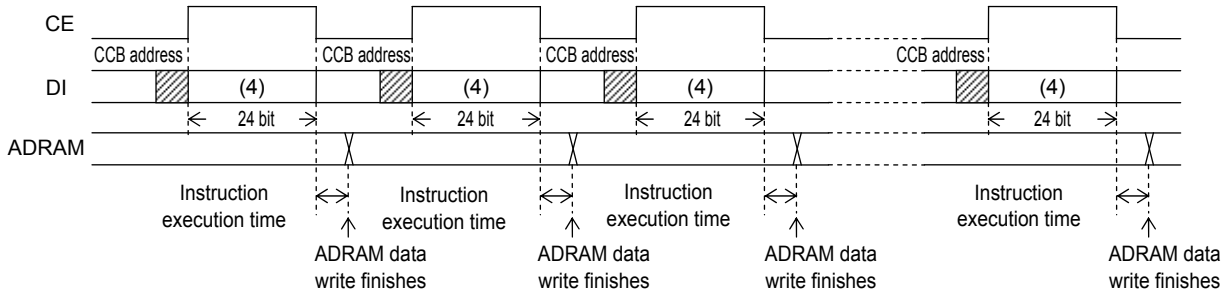
ADATA	Corresponding output pin
AD1	S5m+1 (m is an integer between 0 and 15)
AD2	S5m+2
AD3	S5m+3
AD4	S5m+4
AD5	S5m+5

IM: Sets the method of writing data to ADRAM

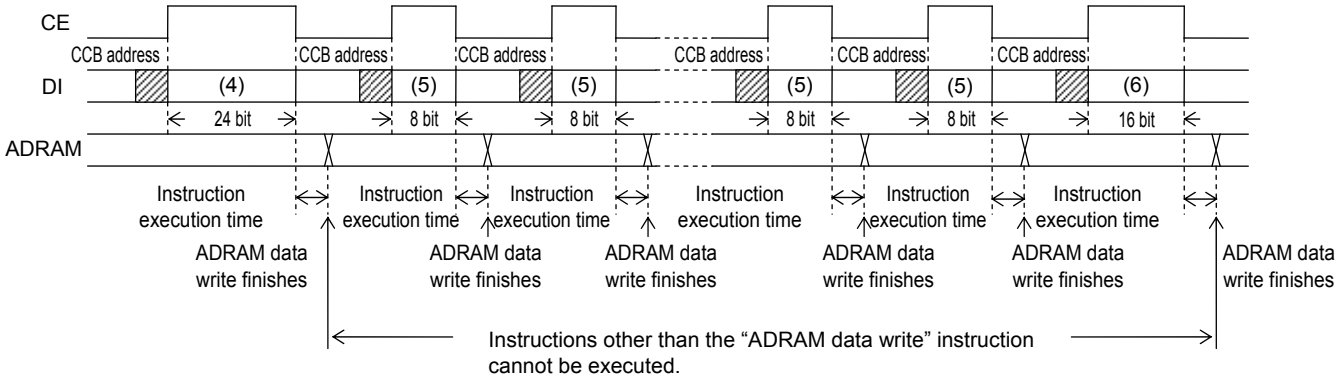
IM	ADRAM data write method
0	Normal ADRAM data write (Specifies the ADRAM address and writes the ADRAM data.)
1	Increment mode ADRAM data write (Increments the ADRAM address by +1 each time data is written to ADRAM.)

Notes: *15.

• ADRAM data write method when IM = 0



• ADRAM data write method when IM = 1
(Instructions other than the “ADRAM data write” instruction cannot be executed.)



Data format at (4) (24 bits)

Code																							
D40	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	RA0	RA1	RA2	RA3	X	X	X	X	IM	X	X	X	0	1	1	0

X: don't care

Data format at (5) (8 bits)

Code							
D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X

X: don't care

Data format at (6) (16 bits)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
AD1	AD2	AD3	AD4	AD5	X	X	X	0	X	X	X	0	1	1	0

X: don't care

• CGRAM data write ... <Specifies the CGRAM address and stores data at that address>
(Write data to CGRAM)

Code															
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
CD1	CD2	CD3	CD4	CD5	CD6	CD7	CD8	CD9	CD10	CD11	CD12	CD13	CD14	CD15	CD16

Code															
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
CD17	CD18	CD19	CD20	CD21	CD22	CD23	CD24	CD25	CD26	CD27	CD28	CD29	CD30	CD31	CD32

Code															
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
CD33	CD34	CD35	CD36	CD37	CD38	CD39	CD40	CD41	CD42	CD43	CD44	CD45	X	X	X

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	0	1	1	1

X: don't care

CA0 to CA7: CGRAM address

CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
LSB							MSB
↑							↑
Least significant bit							Most significant bit

CD1 to CD45: CGRAM data (5×7, 5×8, or 5×9 dot matrix display data)
The bit CDn (where n is an integer between 1 and 45) corresponds to the 5×7, 5×8, or 5×9 dot matrix display data.
The figure below shows that correspondence. When CDn is 1 the dots which correspond to that data will be turned on.

CD1	CD2	CD3	CD4	CD5
CD6	CD7	CD8	CD9	CD10
CD11	CD12	CD13	CD14	CD15
CD16	CD17	CD18	CD19	CD20
CD21	CD22	CD23	CD24	CD25
CD26	CD27	CD28	CD29	CD30
CD31	CD32	CD33	CD34	CD35
CD36	CD37	CD38	CD39	CD40
CD41	CD42	CD43	CD44	CD45

Note: *16. CD1 to CD35: 5×7 dot matrix display data
CD1 to CD40: 5×8 dot matrix display data
CD1 to CD45: 5×9 dot matrix display data

• Set display contrast… <Sets the display contrast>

(Set display contrast)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
CT0	CT1	CT2	CT3	X	X	X	X	CTC	X	X	X	1	0	0	0

X: don't care

CT0 to CT3: Sets the display contrast (11 steps)

CT0	CT1	CT2	CT3	LCD drive 4/4 bias voltage supply $V_{LCD}0$ level
0	0	0	0	$0.94V_{LCD}=V_{LCD}-(0.03V_{LCD}\times2)$
1	0	0	0	$0.91V_{LCD}=V_{LCD}-(0.03V_{LCD}\times3)$
0	1	0	0	$0.88V_{LCD}=V_{LCD}-(0.03V_{LCD}\times4)$
1	1	0	0	$0.85V_{LCD}=V_{LCD}-(0.03V_{LCD}\times5)$
0	0	1	0	$0.82V_{LCD}=V_{LCD}-(0.03V_{LCD}\times6)$
1	0	1	0	$0.79V_{LCD}=V_{LCD}-(0.03V_{LCD}\times7)$
0	1	1	0	$0.76V_{LCD}=V_{LCD}-(0.03V_{LCD}\times8)$
1	1	1	0	$0.73V_{LCD}=V_{LCD}-(0.03V_{LCD}\times9)$
0	0	0	1	$0.70V_{LCD}=V_{LCD}-(0.03V_{LCD}\times10)$
1	0	0	1	$0.67V_{LCD}=V_{LCD}-(0.03V_{LCD}\times11)$
0	1	0	1	$0.64V_{LCD}=V_{LCD}-(0.03V_{LCD}\times12)$

CTC: Sets the display contrast adjustment circuit state

CTC	Display contrast adjustment circuit state
0	The display contrast adjustment circuit is disabled, and the $V_{LCD}0$ pin level is forced to the V_{LCD} level.
1	The display contrast adjustment circuit operates, and the display contrast is adjusted.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it is also possible to apply fine adjustments to the contrast by connecting an external variable resistor to the $V_{LCD}4$ pin and modifying the $V_{LCD}4$ pin voltage. However, the following conditions must be met: $V_{LCD}0$-$V_{LCD}4\geq 4.5V$, and $1.5V\geq V_{LCD}4 \geq 0V$.

• Set key scan output port/general-purpose output port state

... <Sets the key scan output port and general-purpose output port states>

(Key scan output port and General-purpose output port control)

Code															
D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
KC1	KC2	KC3	KC4	KC5	KC6	PC40	PC41	PC1	PC2	PC3	X	1	0	0	1

X:don't care

KC1 to KC6: Sets the key scan output pin KS1 to KS6 state

Output pin	KS1	KS2	KS3	KS4	KS5	KS6
Key scan output state setting data	KC1	KC2	KC3	KC4	KC5	KC6

When KC1 to KC3 are set to 1 and KC4 to KC6 are set to 0, in the key scan standby state, the KS1 to KS3 output pins will output the high level (V_{DD}) and KS4 to KS6 will output the low level (V_{SS}).

Note that key scan output signals are not output from output pins that are set to the low level.

PC1, PC2, PC3: Sets the general-purpose output port P1, P2, P3 state

Output pin	P1	P2	P3
General-purpose output port state setting	PC1	PC2	PC3

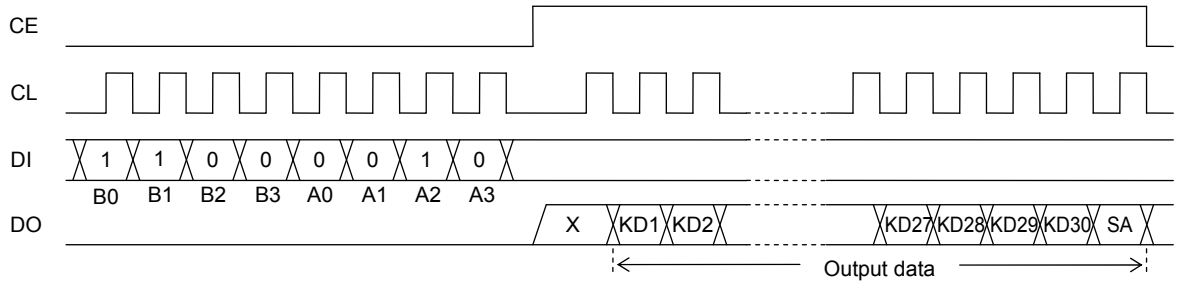
When PC1 is set to 1 and PC2 to PC3 are set to 0, P1 output pin will output the high levels (V_{DD}) and P2 to P3 will output the low levels (V_{SS}).

PC40, PC41: Sets the general-purpose output port P4 state

PC40	PC41	Output pin (P4) state
0	0	"L"(V_{SS})
1	0	"H"(V_{DD})
0	1	Clock signal output (fosc/2, f_{CK}/2)
1	1	Clock signal output (fosc/8, f_{CK}/8)

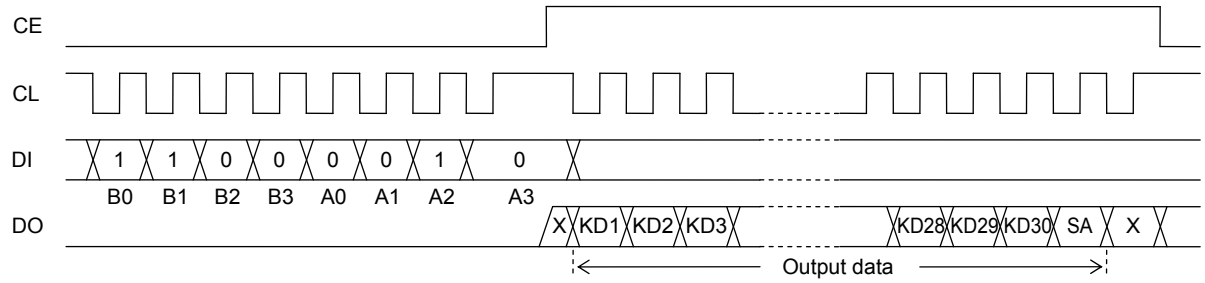
Serial Data Output

(1) When CL is stopped at the low level



X: don't care

(2) When CL is stopped at the high level



X: don't care

- B0 to B3, A0 to A3: CCB address 43H
- KD1 to KD30: Key data
- SA: Sleep acknowledge data

Note: *17. If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data(SA) will be invalid.

Output Data

(1) KD1 to KD30: Key data

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

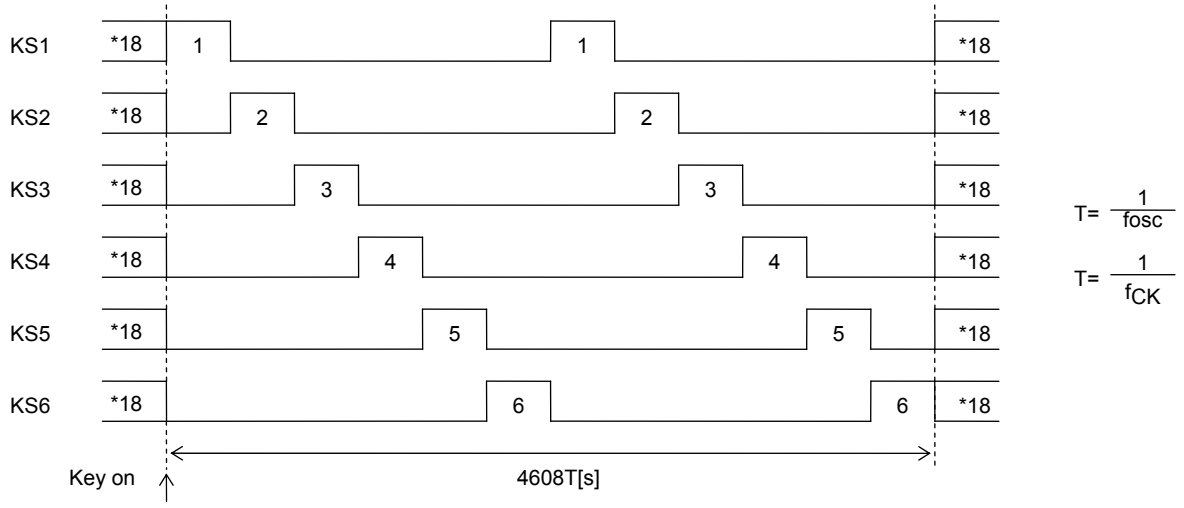
(2) SA : Sleep acknowledge data

This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in Sleep mode and 0 in normal mode.

Key Scan Operation Functions

(1) Key scan timing

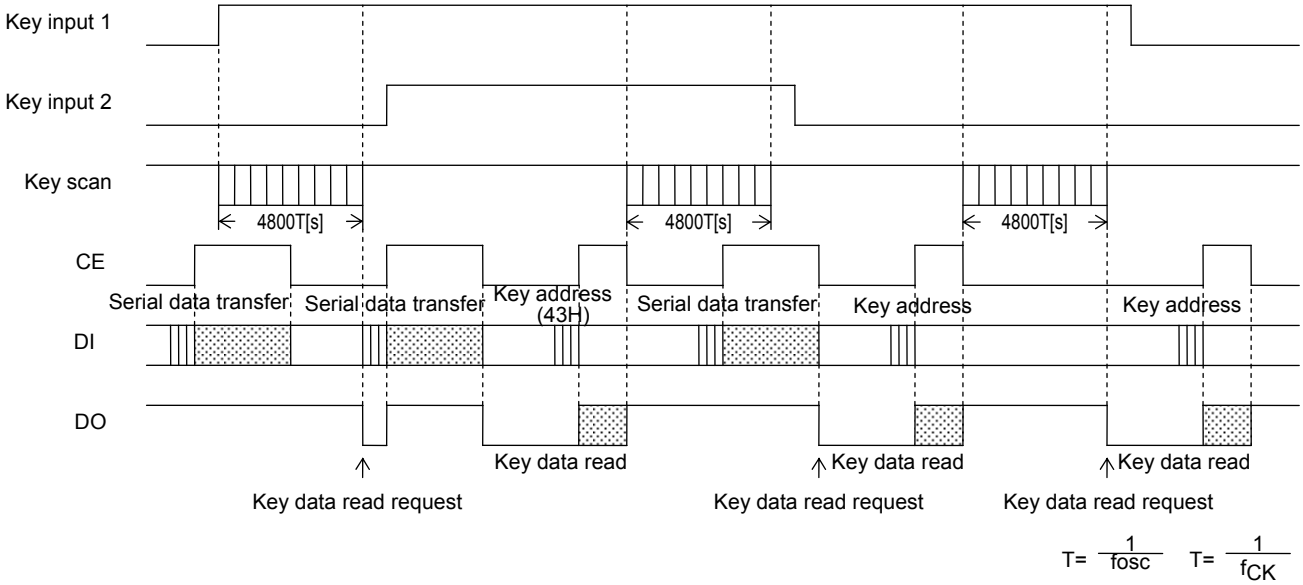
The key scan period is 2304T(s). To reliably determine the on/off state of the keys, the LC75818PT scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 4800T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the LC75818PT cannot detect a key press shorter than 4800T(s).



Note: *18. Not that the high/low states of these pins are determined by the "set key scan output port/general-purpose output port state" instruction, and that key scan output signals are not output from pins that are set to low.

(2) In normal mode

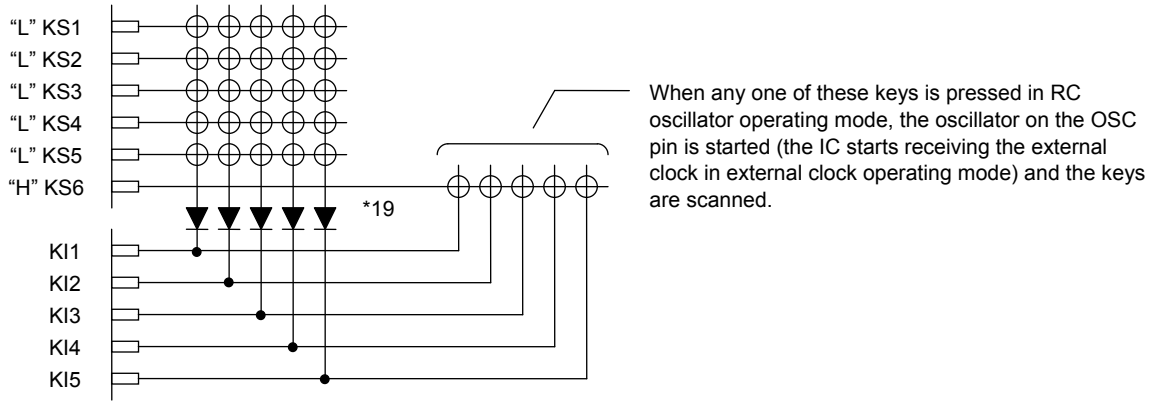
- The pins KS1 to KS6 are set to high or low with the "set key scan output port/general-purpose output port state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where T=1/fosc, T=1/f_{CK}) the LC75818PT outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75818PT performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ).



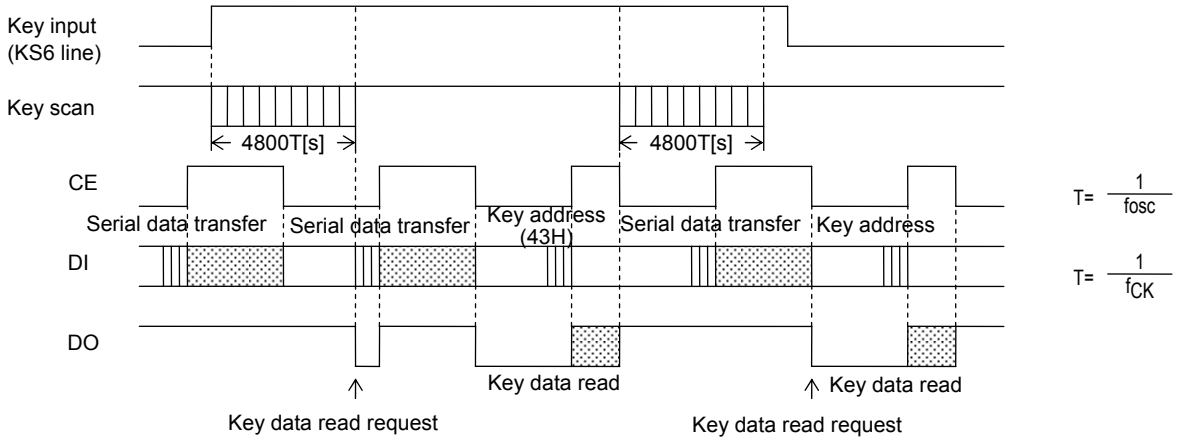
(3) In sleep mode

- The pins KS1 to KS6 are set to high or low with the "set key scan output port/general-purpose output port state" instruction.
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed in the RC oscillator operating mode, the oscillator on the OSC pin is started (the IC starts receiving the external clock in external clock operating mode) and a key scan is performed . Keys are scanned until all keys released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than 4800T(s) (Where T=1/fosc, T=1/f_{CK}) the LC75818PT outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75818PT performs another key scan. However, this dose not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ).
- Sleep mode key scan example

Example: When a "display on/off control (SP=1)" instruction and a "set key scan output port/general-purpose output port state (KC1 to KC5= 0, KC6=1)" instruction are executed. (i.e. sleep mode with only KS6 high.)



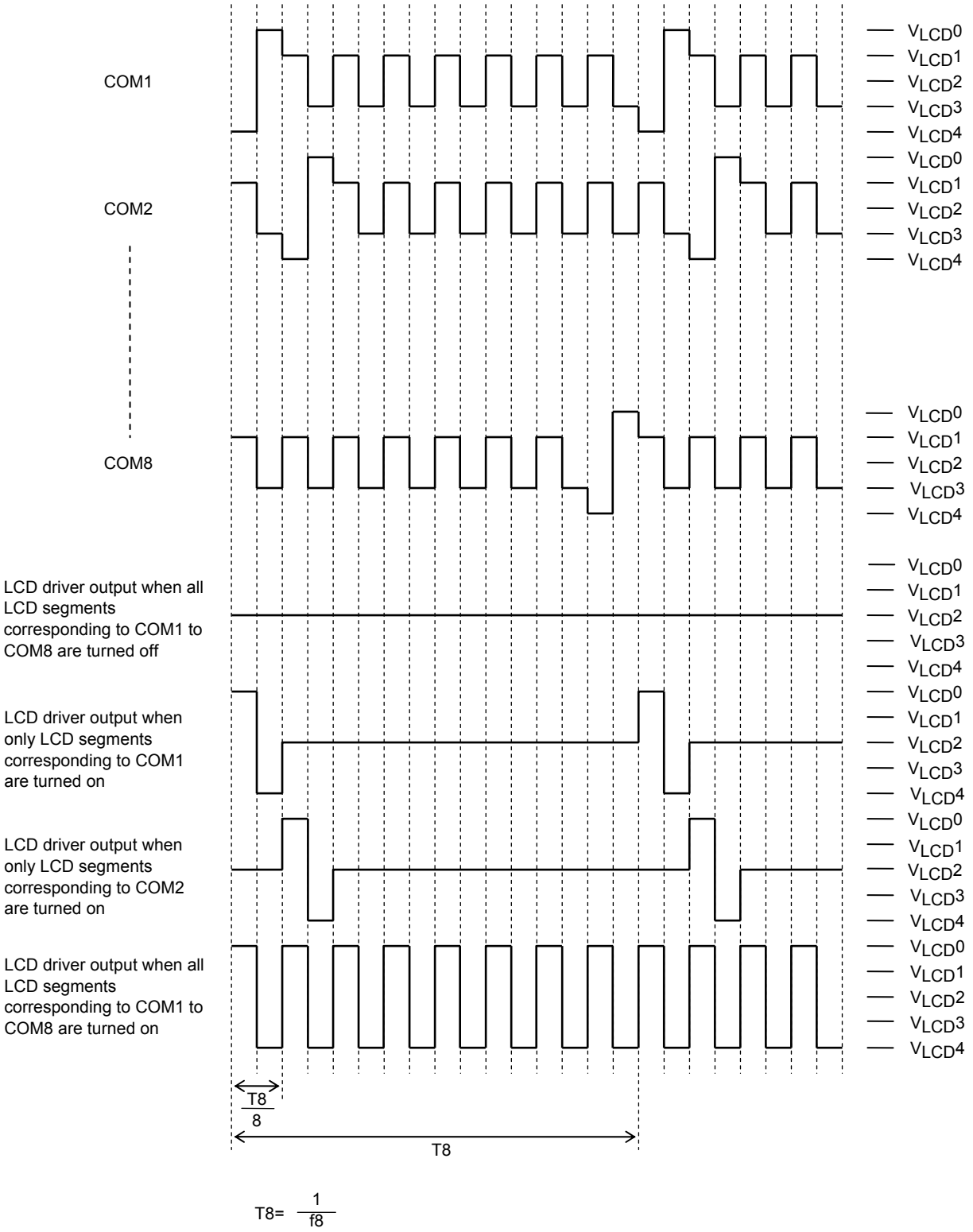
Note: *19. These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example.
That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



Multiple Key Presses

Although the LC75818PT is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed.
Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/8 Duty, 1/4 Bias Drive Technique

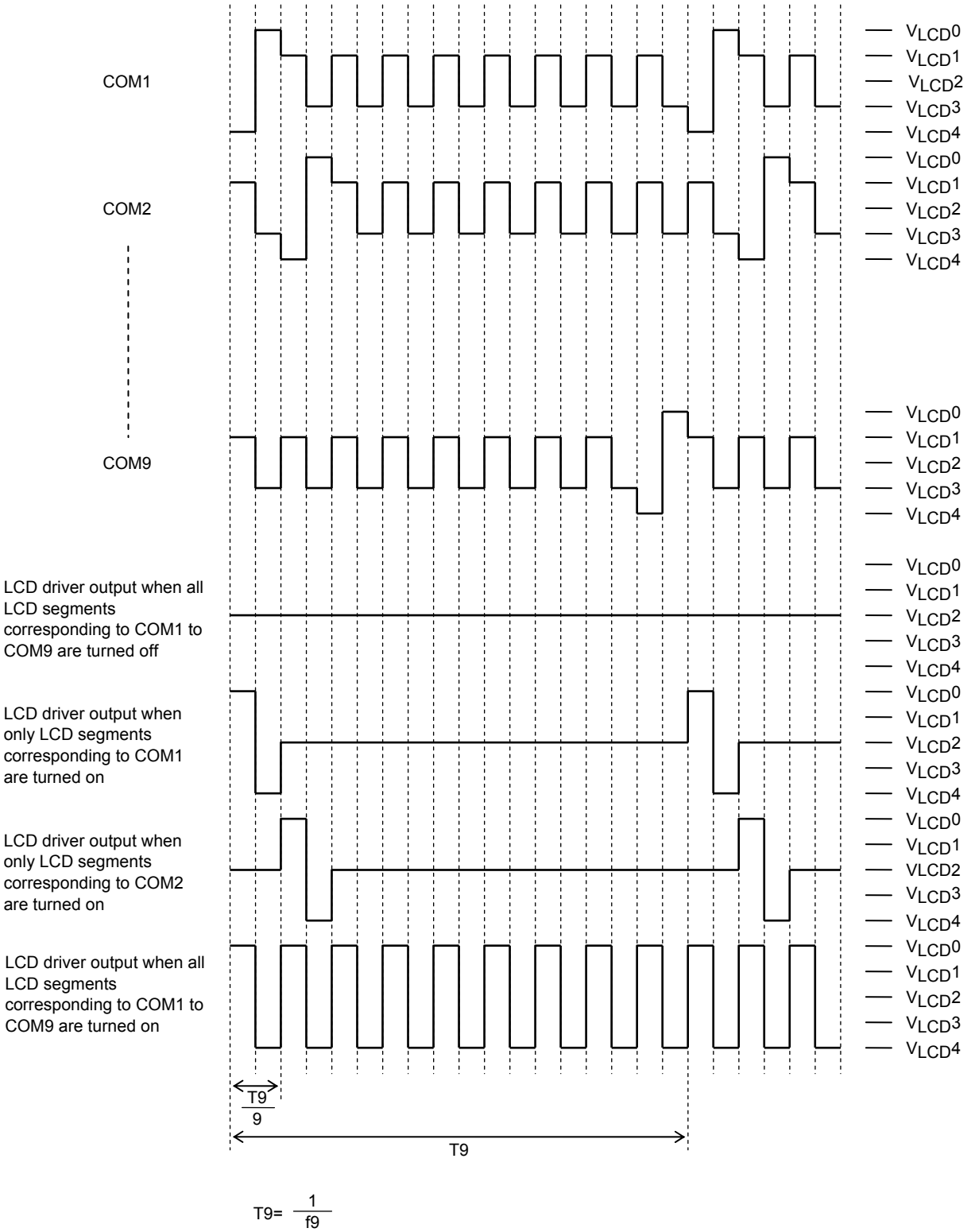


$$T8 = \frac{1}{f8}$$

When a "set display technique" instruction with FC = 0 is executed: $f8 = \frac{fosc}{3072}$, $f8 = \frac{f_{CK}}{3072}$

When a "set display technique" instruction with FC = 1 is executed: $f8 = \frac{fosc}{1536}$, $f8 = \frac{f_{CK}}{1536}$

1/9 Duty, 1/4 Bias Drive Technique



$$T9 = \frac{1}{f9}$$

When a "set display technique" instruction with FC = 0 is executed: $f9 = \frac{fosc}{3456}$, $f9 = \frac{f_{CK}}{3456}$

When a "set display technique" instruction with FC = 1 is executed: $f9 = \frac{fosc}{1728}$, $f9 = \frac{f_{CK}}{1728}$