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LC75843UGAGEVB

LC75843UGA LCD Driver IC Evaluation Board User's Manual

ON Semiconductor®

http://onsemi.com

EVAL BOARD USER'S MANUAL

Overview

The LC75843UGAGEVB is an evaluation board for operation check of 1/1 to 1/4 duty general-purpose LCD driver IC (LC75843UGA). This evaluation board has a power supply circuit, a controller circuit, an LCD driver IC circuit, an LCD panel circuit, an LED circuit. Therefore, this evaluation board can facilitate the operation check (state setting and waveform monitor, etc.) of the LCD driver IC. In addition, this evaluation board can automatically demonstrate.

Features

- This Evaluation Board is Equipped with a Controller, and the Control of the LCD Driver IC is Possible by Serial Communication (CCB* Format)
- The 1/4 Duty LCD Panel is Implemented
- Capable of the LED Control by the General-purpose Port of the LCD Driver IC (Capable of the LED Brightness Adjustment by the PWM Control)
- Capable of Waveform Monitor of All Common Outputs, All Segment Outputs and All General-purpose Port Outputs
- This Evaluation Board can Separate the Signal between Each Circuit Block. Therefore the External Input to an LCD Driver IC is Possible
- This Evaluation Board has the Demonstration Mode which Automatically Performs LCD Display and LED Control by Controller Control
- This Evaluation Board is Pb-free and RoHS Compliant

*CCB® is ON Semiconductor's original format. All addresses are managed by ON Semiconductor for this format.

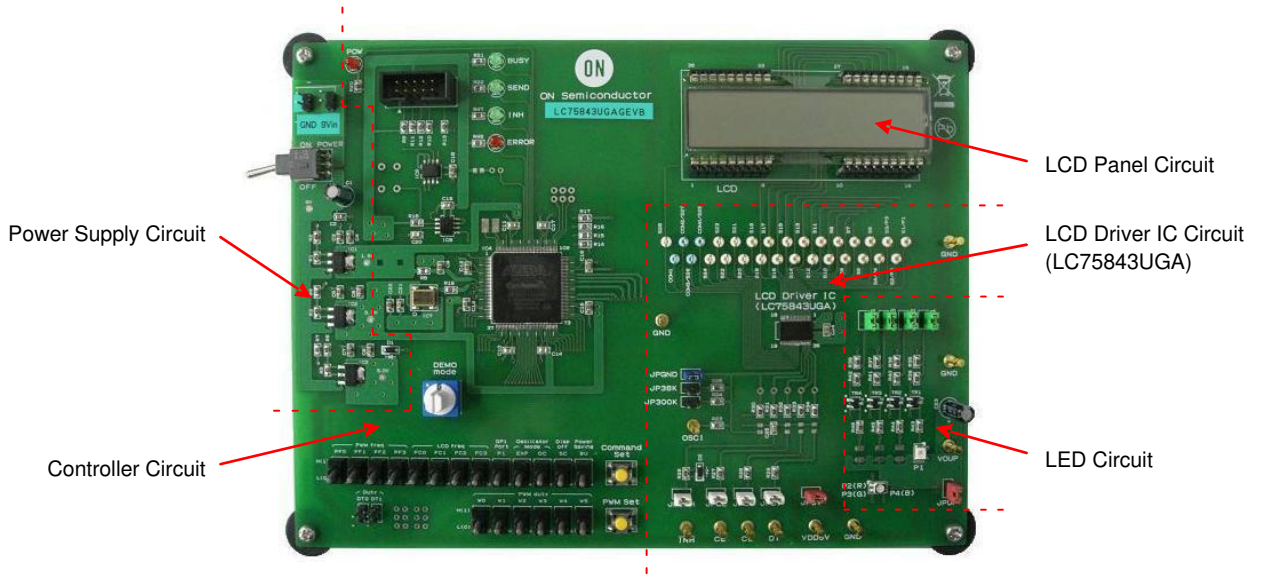


Figure 1. Appearance of LCD Driver IC Evaluation Board (LC75843UGAGEVB)

SPECIFICATIONS

Table 1. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value/Ratings			Unit
			Min	Typ	Max	
Specifications of LCD Driver IC Evaluation Board (LC75843UGAGEVB)						
Main Power Supply Voltage	9Vin		7.0	9.0	12.0	V
Pull-up Power Supply Voltage for LED	VOUP	When the jump socket of the JPUP is removed and an external power supply is inputted from VOUP pin.	4.5	5.0	6.3	V
Main Power Supply Current	I_{DD9V}	9Vin = 9.0 V, When the switch of the P1 is set to H(1) and moving the “All ON test (DEMO mode = “1”)” mode. (This condition is a maximum current flow)	–	125	–	mA
Board Size			200 mm × 150 mm, t = 1.6 mm			
Board Material			Glass Epoxy (FR4), 2-levels, Copper Foil 35 μm			
Specifications of LCD Driver IC (LC75843UGA)						
Power Supply Voltage	V_{DD}	When the jump socket of the JP5V is removed and an external power supply is inputted from VDD5V pin.	4.5	–	6.3	V
Input High Level Voltage	V_{IH1}	When the jump sockets of the JPINH, JPCE, JPCL and JPDI are removed and an external signal is inputted from CE, CL, DI and $\overline{INH}$ pins.	0.4 V_{DD}	–	6.3	V
	V_{IH2}	When the jump sockets of the JPGND, JP38K and JP300K are removed and an external clock is inputted from OSCI pin.	0.4 V_{DD}	–	6.3	V
Input Low Level Voltage	V_{IL1}	When the jump sockets of the JPINH, JPCE, JPCL and JPDI are removed and an external signal is inputted from CE, CL, DI and $\overline{INH}$ pins.	0	–	0.2 V_{DD}	V
	V_{IL2}	When the jump sockets of the JPGND, JP38K and JP300K are removed and an external clock is inputted from OSCI pin.	0	–	0.2 V_{DD}	V
CCB Serial Clock Operating Frequency	f_{CL}	When the jump socket of the JPCL is removed and an external signal is inputted from CL pin.	–	–	3.125	MHz
External Clock Operating Frequency	f_{CK}	When the jump sockets of the JPGND, JP38K and JP300K are removed and an external clock is inputted from OSCI pin.	10	300	600	kHz
External Clock Duty Cycle	D_{CK}	When the jump sockets of the JPGND, JP38K and JP300K are removed and an external clock is inputted from OSCI pin.	30	50	70	%

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTE: We have a case to change these specifications without a notice for improvement.

BLOCK DIAGRAM

The following figure shows the block diagram of the LC75843UGAGEVB.

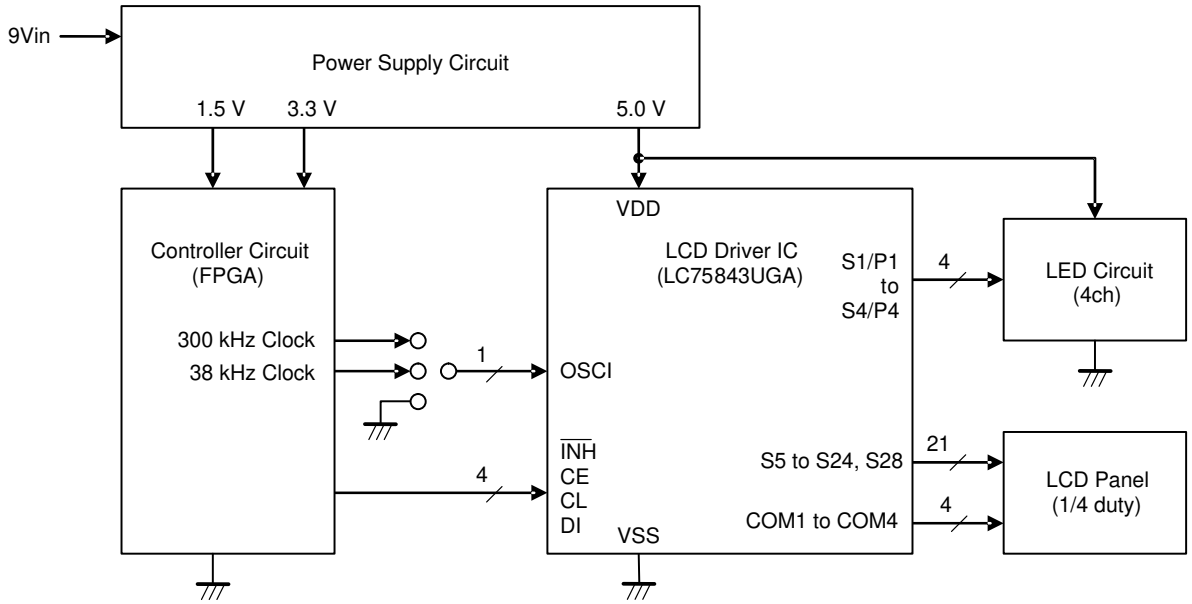


Figure 2. Block Diagram of LCD Driver IC Evaluation Board (LC75843UGAGEVB)

TEST PROCEDURE

When the All Circuits in the LC75843UGAGEVB Board Are Used

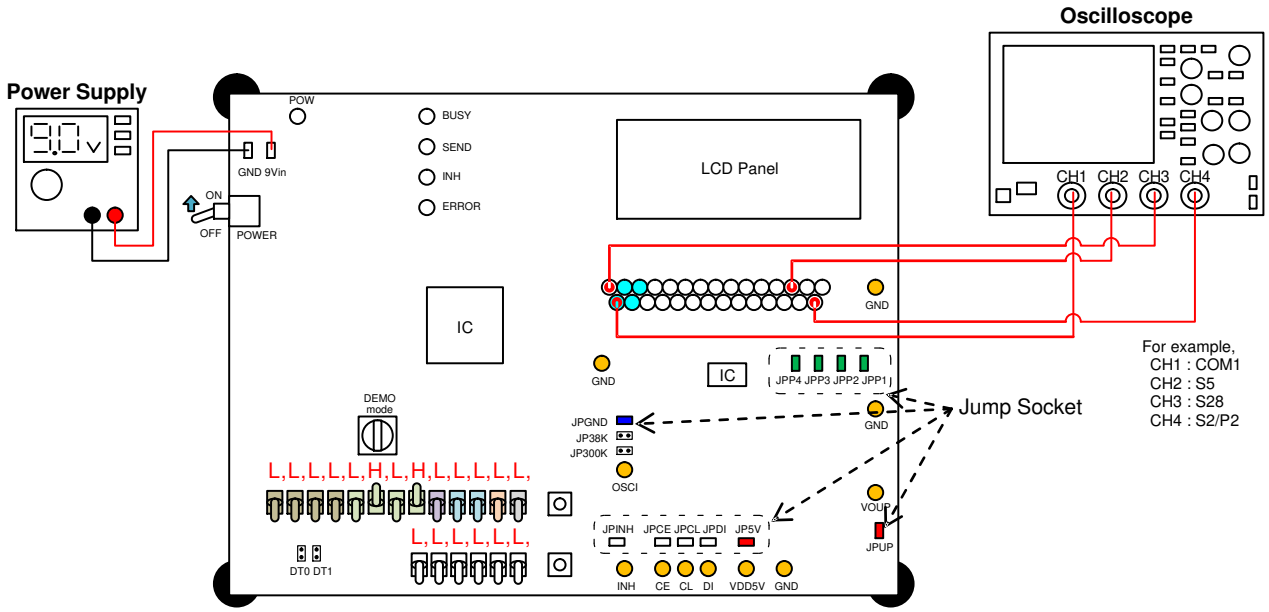


Figure 3. The Test Constitution when the All Circuits in the LC75843UGAGEVB Board Are Used

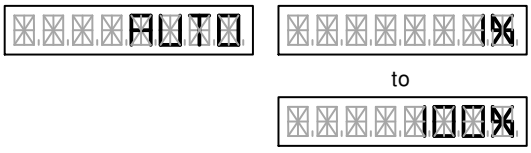
1. Connect the test setup as shown in Figure 3.
2. Insert the jump sockets of the JP5V, JPGND, JPINH, JPCE, JPCL, JPDI, JPUP, JPP1, JPP2, JPP3 and JPP4, and remove the jump sockets of the DT0, DT1, JP38K and JP300K.
3. The power supply of the evaluation board is turned on by moving “POWER” switch to the “ON” position. (The red LED monitor of the “POW” is turned on)
4. An automatic demonstration mode is selected by moving “DEMO mode” switch to the “9” position.
5. Set the following switches. About the setting contents details of the switch, refer to “Explanation of the Switches of Setting the Control Data”.

Switches	Functions	Contents Which Are Set
PF0 to PF3	PWM output waveform frame frequency select.	The PWM output waveform frame frequency is 195 [Hz] by moving “PF0, PF1, PF2, PF3” switch to the “L(0), L(0), L(0), L(0)” position.
FC0 to FC3	Common/Segment output waveform frame frequency select.	The common/segment output waveform frame frequency is 97 [Hz] by moving “FC0, FC1, FC2, FC3” switch to the “L(0), H(1), L(0), H(1)” position.
P1	General-purpose output port (S1/P1) function select.	L(0) : Low level output mode
EXF	External clock operating frequency mode select at OC = H(1).	L(0) : 300 kHz input operating mode
OC	Fundamental clock operating mode select.	L(0) : Internal oscillator clock operating mode
SC	Display on/off select.	L(0) : Normal display mode
BU	Power saving mode select.	L(0) : Normal mode
W0 to W5	PWM output waveform duty select.	When switch of the “DEMO mode” is set to “9”, duty of the PWM output waveform is automatically set, therefore switches of the “W0 to W5” are set to “L(0), L(0), L(0), L(0), L(0), L(0)” position.

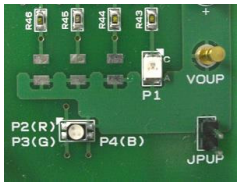
6. The CCB serial data are transferred from a controller circuit to LCD driver IC by pushing the “Command Set” switch. (The green LED monitor of the “BUSY” and “INH” are turned on)
7. The customer can confirm the movement of the LCD display and LED brightness adjustment by the automatic demonstration. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port outputs (P1 to P4).

For example, when the DEMO mode is “9”

- The green LED monitor of the “SEND” flashes quickly.
- The customer can confirm that a “AUTO” characters and a PWM duty value are displayed to LCD.



- The customer can confirm that LEDs from P1 to P4 change brightly gradually.



When the External Power Supply Is Used

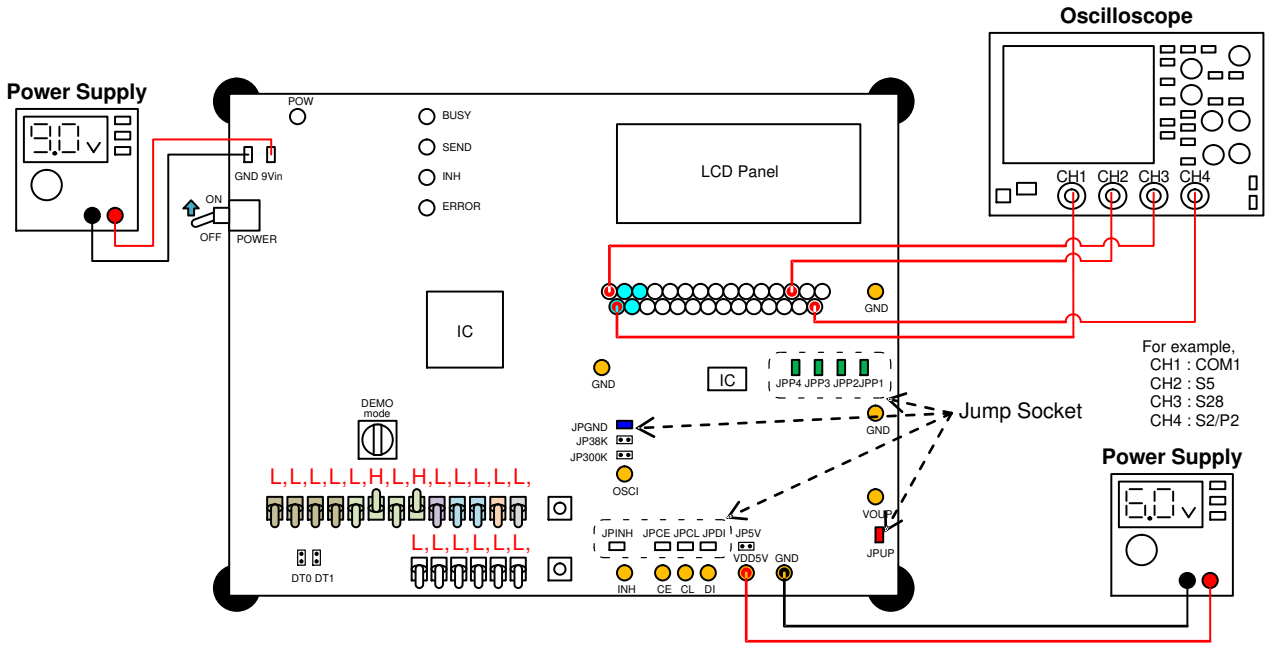


Figure 4. The Test Constitution when the External Power Supply Is Used

1. Connect the test setup as shown in Figure 4.
2. Insert the jump sockets of the JPGND, JPINH, JPCE, JPCL, JPDI, JPUP, JPP1, JPP2, JPP3 and JPP4, and remove the jump sockets of the DT0, DT1, JP38K, JP300K and JP5V.
3. The power supply of the evaluation board is turned on by moving “POWER” switch to the “ON” position. (The red LED monitor of the “POW” is turned on)
4. Supply the voltage of the external power supply to “VDD5V” pin. The following specification shows the allowable operating ranges of LC75843UGA.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage for LC75843UGA	V_{DD}	4.5	–	6.3	V

5. An automatic demonstration mode is selected by moving “DEMO mode” switch to the “9” position.
6. Set the following switches. About the setting contents details of the switch, refer to “Explanation of the Switches of Setting the Control Data”.

Switches	Functions	Contents Which Are Set
PF0 to PF3	PWM output waveform frame frequency select.	The PWM output waveform frame frequency is 195 [Hz] by moving “PF0, PF1, PF2, PF3” switch to the “L(0), L(0), L(0), L(0)” position.
FC0 to FC3	Common/Segment output waveform frame frequency select.	The common/segment output waveform frame frequency is 97 [Hz] by moving “FC0, FC1, FC2, FC3” switch to the “L(0), H(1), L(0), H(1)” position.
P1	General-purpose output port (S1/P1) function select.	L(0) : Low level output mode
EXF	External clock operating frequency mode select at OC = H(1).	L(0) : 300kHz input operating mode
OC	Fundamental clock operating mode select.	L(0) : Internal oscillator clock operating mode
SC	Display on/off select.	L(0) : Normal display mode
BU	Power saving mode select.	L(0) : Normal mode
W0 to W5	PWM output waveform duty select.	When switch of the “DEMO mode” is set to “9”, duty of the PWM output waveform is automatically set, therefore switches of the “W0 to W5” are set to “L(0), L(0), L(0), L(0), L(0), L(0)” position.

7. The CCB serial data are transferred from a controller circuit to LCD driver IC by pushing the “Command Set” switch. (The green LED monitor of the “BUSY” and “INH” are turned on)
8. The customer can confirm the movement of the LCD display and LED brightness adjustment by the automatic demonstration. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port outputs (P1 to P4). (The green LED monitor of the “SEND” flashes quickly)

When the Customer’s Original Controller Board Is Used

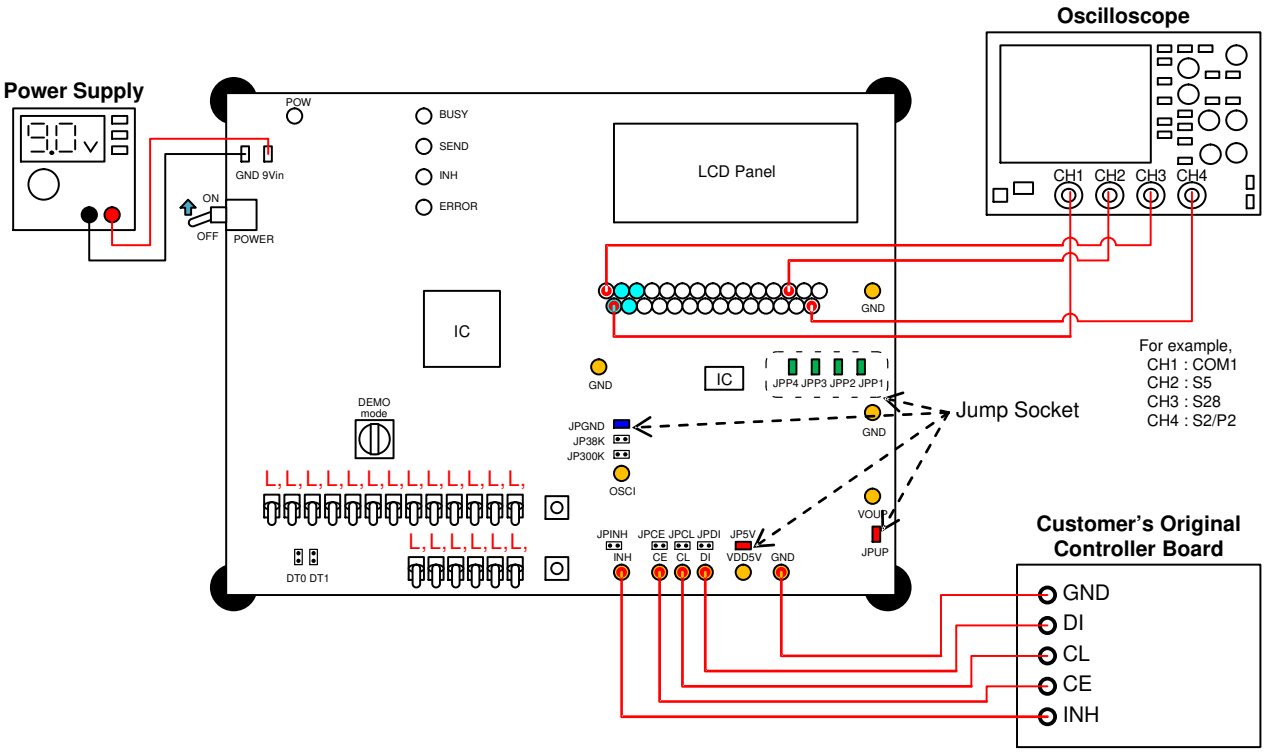


Figure 5. The Test Constitution when the Customer’s Original Controller Board Is Used

1. Connect the test setup as shown in Figure 5.
2. Insert the jump sockets of the JP5V, JPGND, JPUP, JPP1, JPP2, JPP3 and JPP4, and remove the jump sockets of the DT0, DT1, JP38K, JP300K, JPINH, JPCE, JPCL and JPDI.
3. The switch does not need to set because the switch on the evaluation board are not used.
4. The power supply of the evaluation board is turned on by moving “POWER” switch to the “ON” position. (The red LED monitor of the “POW” is turned on)
5. The CCB serial data are transferred from a customer’s original controller board to LCD driver IC. The following specification shows the allowable operating ranges of LC75843UGA.

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level Voltage	V_{IH1}	0.4 V_{DD}	–	6.3	V
Input Low Level Voltage	V_{IL1}	0	–	0.2 V_{DD}	V
CCB Serial Clock Operating Frequency	f_{CL}	–	–	3.125	MHz

6. Confirm a result of LCD display and the LED display controlled by the customer’s original controller board. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port outputs (P1 to P4).

When the LCD Display Is Driven by the External Clock Input

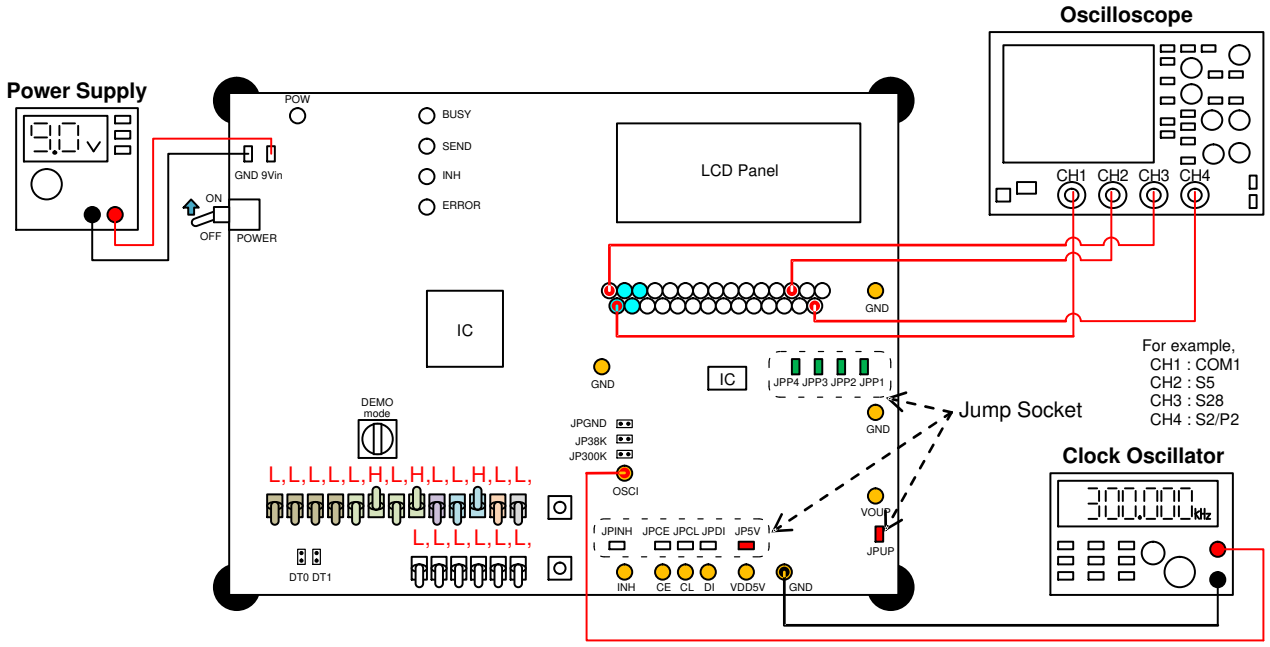


Figure 6. The Test Constitution when the LCD Display Is Driven by the External Clock Input

When the LCD Display Is Driven by the Clock Oscillator

1. Connect the test setup as shown in Figure 6.
2. Insert the jump sockets of the JP5V, JPINH, JPCE, JPCL, JPDI, JPUP, JPP1, JPP2, JPP3 and JPP4, and remove the jump sockets of the DT0, DT1, JPGND, JP38K and JP300K.
3. The power supply of the evaluation board is turned on by moving “POWER” switch to the “ON” position. (The red LED monitor of the “POW” is turned on)
4. An automatic demonstration mode is selected by moving “DEMO mode” switch to the “9” position.
5. Set the following switches. About the setting contents details of the switch, refer to “Explanation of the Switches of Setting the Control Data”.

Switches	Functions	Contents Which Are Set
PF0 to PF3	PWM output waveform frame frequency select.	The PWM output waveform frame frequency is 195 [Hz] by moving “PF0, PF1, PF2, PF3” switch to the “L(0), L(0), L(0), L(0)” position.
FC0 to FC3	Common/Segment output waveform frame frequency select.	The common/segment output waveform frame frequency is 97 [Hz] by moving “FC0, FC1, FC2, FC3” switch to the “L(0), H(1), L(0), H(1)” position.
P1	General-purpose output port (S1/P1) function select.	L(0) : Low level output mode
EXF	External clock operating frequency mode select at OC = H(1).	L(0) : 300kHz input operating mode
OC	Fundamental clock operating mode select.	H(1) : External clock operating mode
SC	Display on/off select.	L(0) : Normal display mode
BU	Power saving mode select.	L(0) : Normal mode
W0 to W5	PWM output waveform duty select.	When switch of the “DEMO mode” is set to “9”, duty of the PWM output waveform is automatically set, therefore switches of the “W0 to W5” are set to “L(0), L(0), L(0), L(0), L(0), L(0)” position.

6. Supply the external clock to “OSCI” pin.
   The following specification shows the allowable operating ranges of LC75843UGA.

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level Voltage	V_{IH2}	0.4 V_{DD}	–	6.3	V
Input Low Level Voltage	V_{IL2}	0	–	0.2 V_{DD}	V
External Clock Operating Frequency	f_{CK}	10	300	600	kHz
External Clock Duty Cycle	D_{CK}	30	50	70	%

7. The CCB serial data are transferred from a controller circuit to LCD driver IC by pushing the “Command Set” switch. (The green LED monitor of the “BUSY” and “INH” are turned on)
8. The customer can confirm the movement of the LCD display and LED brightness adjustment by the automatic demonstration. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port outputs (P1 to P4).

When the LCD Display Is Driven by the 300 [kHz] External Clock Input

1. The LCD display is turned off by pushing the switch of “Command Set” and “PWM Set” at the same time more than two seconds. (The green LED monitor of the “BUSY” and “INH” are turned off)
2. Insert the jump socket of the JP300K, and remove the jump sockets of the JPGND and JP38K. The 301.205 [MHz] (50 MHz × 166 clock) clock output by the controller is input into an LCD driver IC by inserting a jump socket of the JP300K.
3. Move “OC” switch to the “H(1)” position and “EXF” switch to the “L(0)” position.
4. The CCB serial data are transferred from a controller circuit to LCD driver IC by pushing the “Command Set” switch. (The green LED monitor of the “BUSY” and “INH” are turned on)
5. The customer can confirm the movement of the LCD display and LED brightness adjustment by the automatic demonstration. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port outputs (P1 to P4).

When the LCD Display Is Driven by the 38 [kHz] External Clock Input

1. The LCD display is turned off by pushing the switch of “Command Set” and “PWM Set” at the same time more than two seconds. (The green LED monitor of the “BUSY” and “INH” are turned off)
2. Insert the jump socket of the JP38K, and remove the jump sockets of the JPGND and JP300K. The 37.994 [MHz] (50 MHz × 1316 clock) clock output by the controller is input into an LCD driver IC by inserting a jump socket of the JP38K.
3. Move “OC” switch to the “H(1)” position and “EXF” switch to the “H(1)” position.

4. The CCB serial data are transferred from a controller circuit to LCD driver IC by pushing the “Command Set” switch. (The green LED monitor of the “BUSY” and “INH” are turned on)
5. The customer can confirm the movement of the LCD display and LED brightness adjustment by the automatic demonstration. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port outputs (P1 to P4).

When the LCD Display Is Driven Using the LCD Driver IC in All Customer Original Environment

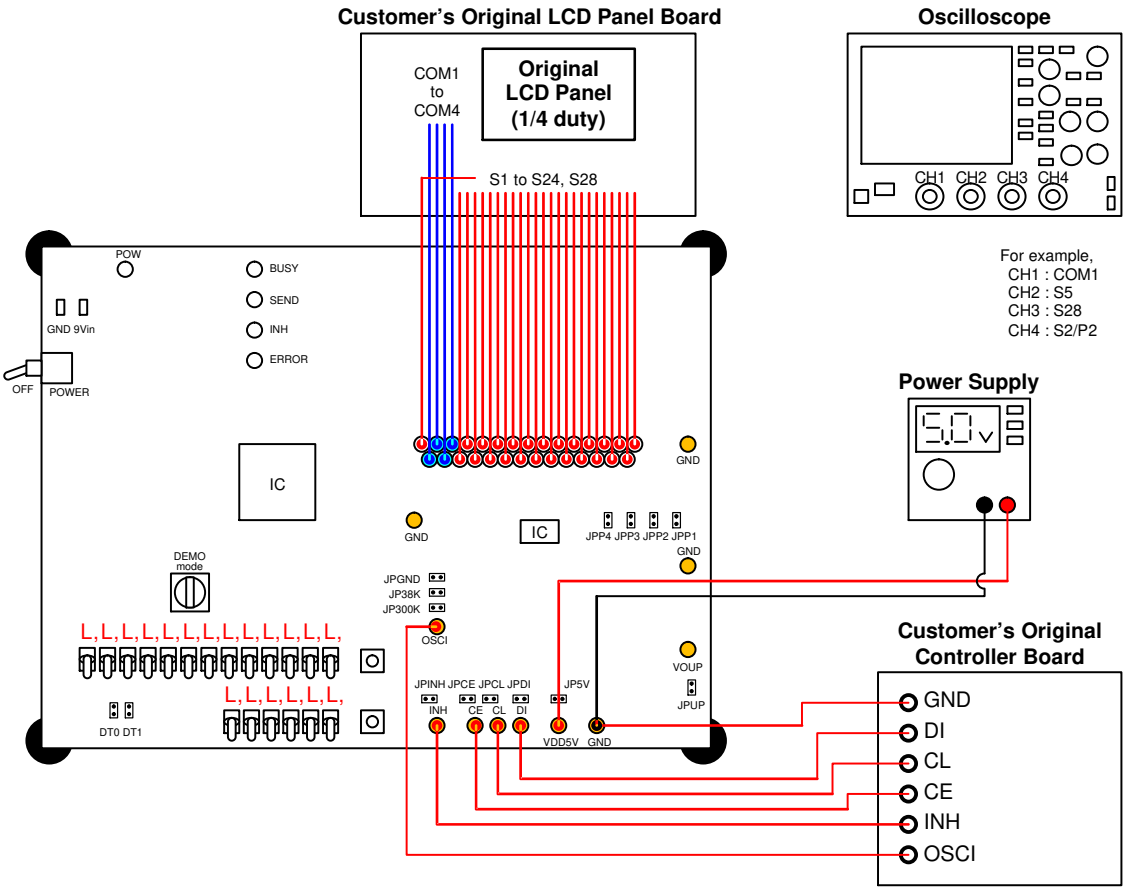
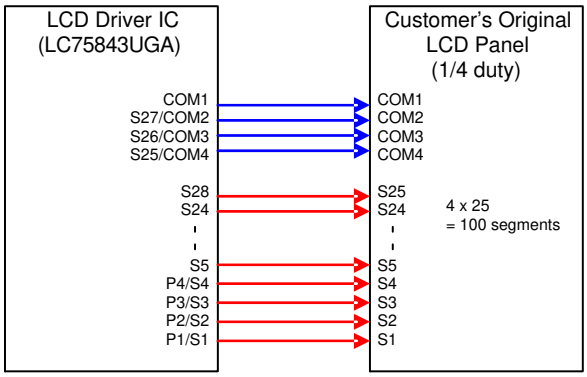


Figure 7. The Test Constitution when the LCD Display Is Driven Using the LCD Driver IC in All Customer Original Environment.

When the Customer's Original LCD Panel of the 1/4 Duty Is Used

When a customer uses the “Customer's original LCD panel”, because the segment allotments of the LCD panel are different the control by the “Customer's original controller board” is necessary. When 1/4 duty drive mode, LC75843UGA can drive the LCD up to 100 segments.



1. Connect the test setup shown in Figure 7.
2. Remove the all jump sockets of the JP5V, JPGND, JP38K, JP300K, DT0, DT1, JPINH, JPCE, JPCL, JPDI, JPUP, JPP1, JPP2, JPP3 and JPP4. However, when the controller circuit in the evaluation board is used, remove the jump sockets of the DT0 and DT1. The switch does not need to set because the switch on the evaluation board are not used.
3. Supply the voltage of the external power supply to "VDD5V" pin.
   The following specification shows the allowable operating ranges of LC75843UGA.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage for LC75843UGA	V_{DD}	4.5	–	6.3	V

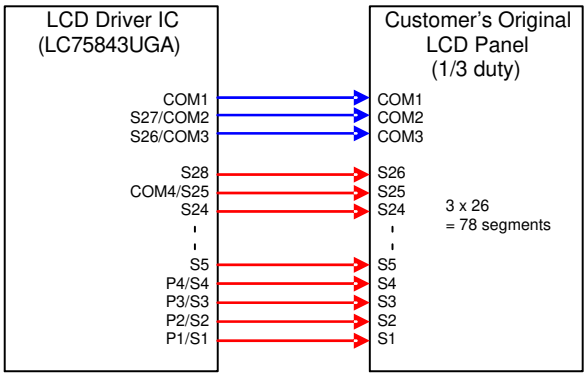
4. Supply the external clock to "OSCI" pin, and the CCB serial data are transferred from a customer's original controller board to LCD driver IC.
   The following specification shows the allowable operating ranges of LC75843UGA.

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level Voltage	V_{IH1}	0.4 V_{DD}	–	6.3	V
Input High Level Voltage	V_{IH2}	0.4 V_{DD}	–	6.3	V
Input Low Level Voltage	V_{IL1}	0	–	0.2 V_{DD}	V
Input Low Level Voltage	V_{IL2}	0	–	0.2 V_{DD}	V
CCB Serial Clock Operating Frequency	f_{CL}	–	–	3.125	MHz
External Clock Operating Frequency	f_{CK}	10	300	600	kHz
External Clock Duty Cycle	D_{CK}	30	50	70	%

5. Confirm a result of LCD display and the LED display controlled by the customer's original controller board. Then, the customer can confirm the waveform of the common outputs (COM1 to COM4), segment outputs (S5 to S24, S28) and general-purpose port and segment outputs (S1/P1 to S4/P4).

When the Customer's Original LCD Panel of the 1/3 Duty Is Used

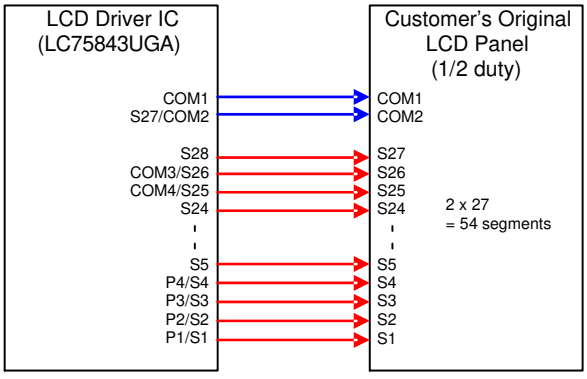
When a customer uses the "Customer's original LCD panel", because the segment allotments of the LCD panel are different the control by the "Customer's original controller board" is necessary. When 1/3 duty drive mode, LC75843UGA can drive the LCD up to 78 segments.



1. Connect the test setup shown in Figure 7. However, an LCD panel of the 1/3 duty is used.
2. Remove the all jump sockets (JP5V, JPGND, JP38K, JP300K, DT0, DT1, JPINH, JPCE, JPCL, JPDI, JPUP and JPP1 to JPP4). However, when the controller circuit in the evaluation board is used, insert the "DT0" jump socket and remove the "DT1" jump socket. The switch does not need to set because the switch on the evaluation board are not used.

When the Customer's Original LCD Panel of the 1/2 Duty Is Used

When a customer uses the "Customer's original LCD panel", because the segment allotments of the LCD panel are different the control by the "Customer's original controller board" is necessary. When 1/2 duty drive mode, LC75843UGA can drive the LCD up to 54 segments.

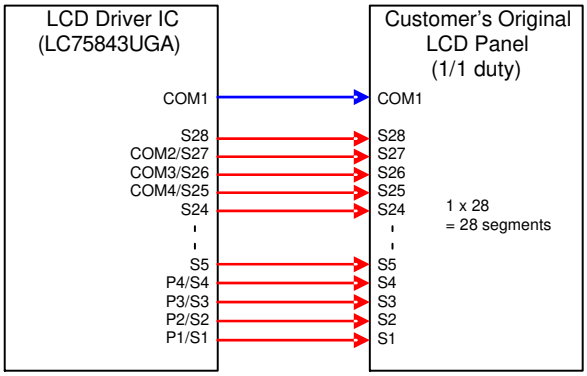


1. Connect the test setup shown in Figure 7. However, an LCD panel of the 1/2 duty is used.
2. Remove the all jump sockets of the JP5V, JPGND, JP38K, JP300K, DT0, DT1, JPINH, JPCE, JPCL, JPDI, JPUP, JPP1, JPP2, JPP3 and JPP4. However,

when the controller circuit in the evaluation board is used, insert the jump socket of the DT1 and remove the jump socket of the DT0. The switch does not need to set because the switch on the evaluation board are not used.

When the Customer's Original LCD Panel of the Static (1/1 Duty) Is Used

When a customer uses the "Customer's original LCD panel", because the segment allotments of the LCD panel are different the control by the "Customer's original controller board" is necessary. When static (1/1 duty) drive mode, LC75843UGA can drive the LCD up to 28 segments.



1. Connect the test setup shown in Figure 7. However, an LCD panel of the static (1/1 duty) is used.
2. Remove the all jump sockets of the JP5V, JPGND, JP38K, JP300K, DT0, DT1, JPINH, JPCE, JPCL, JPDI, JPUP, JPP1, JPP2, JPP3 and JPP4. However, when the controller circuit in the evaluation board is used, insert the jump sockets of the DT0 and DT1. The switch does not need to set because the switch on the evaluation board are not used.

SCHEMATIC

Power Supply Circuit

The power supply circuit of this evaluation board generates three kinds of voltage by a linear regulator IC (LM317) from the power supply voltage of 9 V inputted. The +1.5 V power supply circuit is a power supply for FPGA core, the +3.3 V power supply circuit is a power supply for FPGA I/O and peripheral IC circuits, and the +5.0 V power supply circuit is a power supply for LCD driver IC. The linear regulator IC (LM317) can adjust the output voltage from 1.2 V to 37 V by an external resistor.

The calculating formula of the output voltage:
$VOUT = 1.25 \times (1 + R2 / R1) + IADJ \times R2$ [V]

For example,
+1.5 V Power Supply Circuit:
$VOUT1 = 1.25 \times (1 + 51 / 240) + 50\ \mu A \times 51 = 1.518$ V

+3.3 V Power Supply Circuit:
$VOUT2 = 1.25 \times (1 + 390 / 240) + 50\ \mu A \times 390 = 3.301$ V

+5.0 V Power Supply Circuit:
$VOUT3 = 1.25 \times (1 + (360+620) / 330) + 50\ \mu A \times (360 + 620) = 5.011$ V

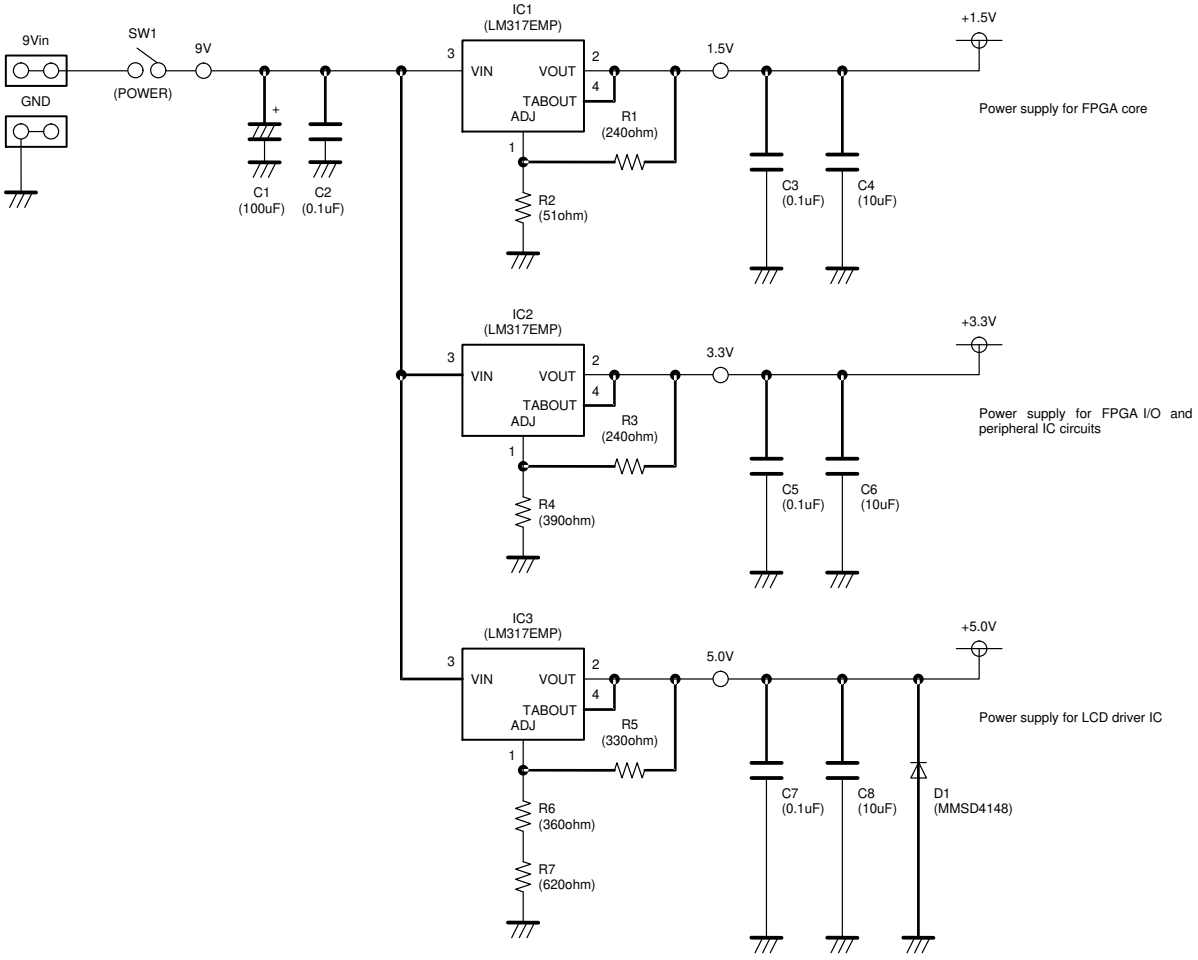


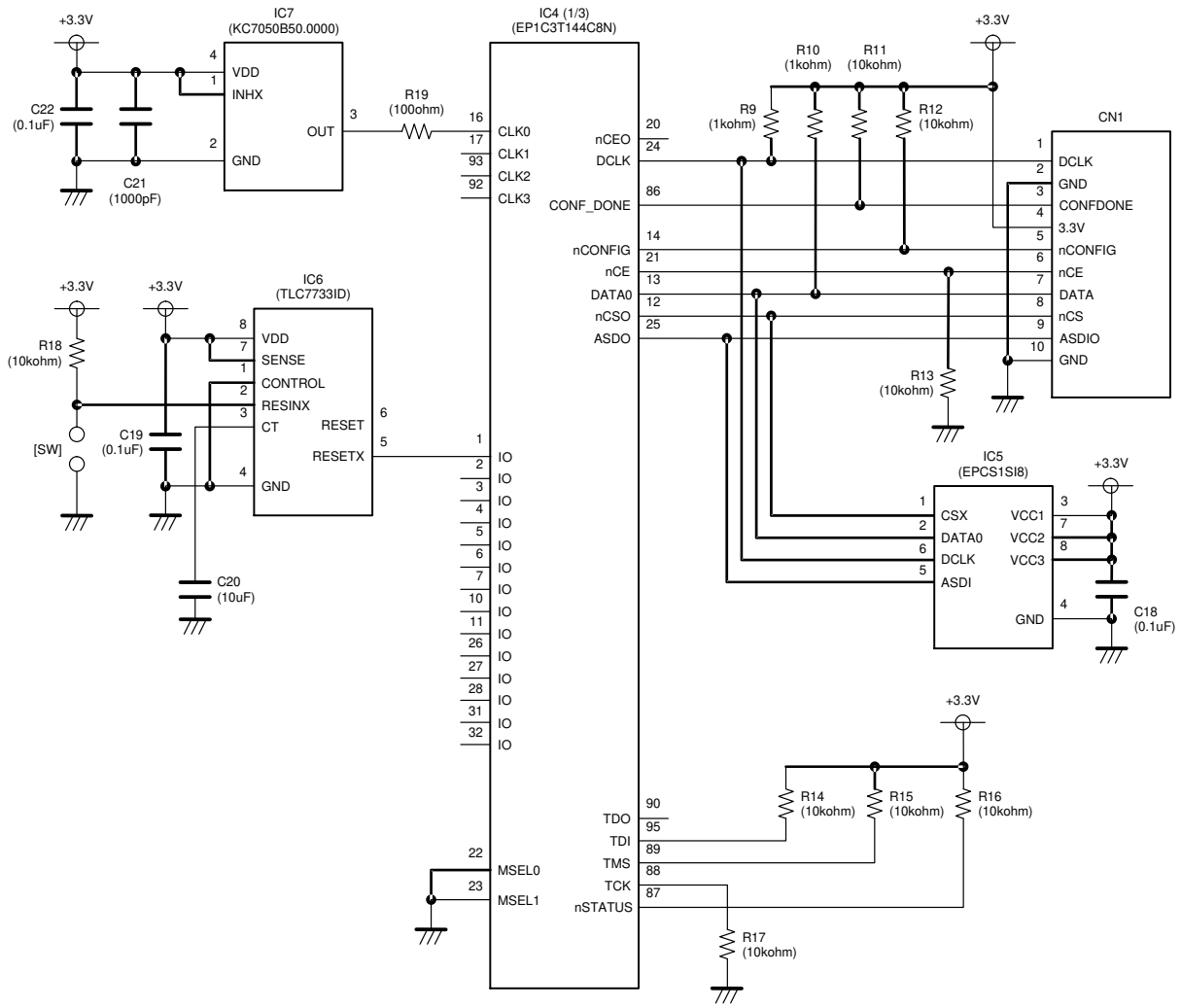
Figure 8. Schematic of Power Supply Circuit

Controller Circuit

The controller circuit of this evaluation board controls LCD driver IC (LC75843UGA) by CCB format serial data (3 V interface) using FPGA. The crystal oscillator circuit (50 [MHz]), power-on reset circuit, configuration ROM circuit, connector for configuration, switch for condition setting, LED monitor circuit and LCD driver IC interface are connected to FPGA.

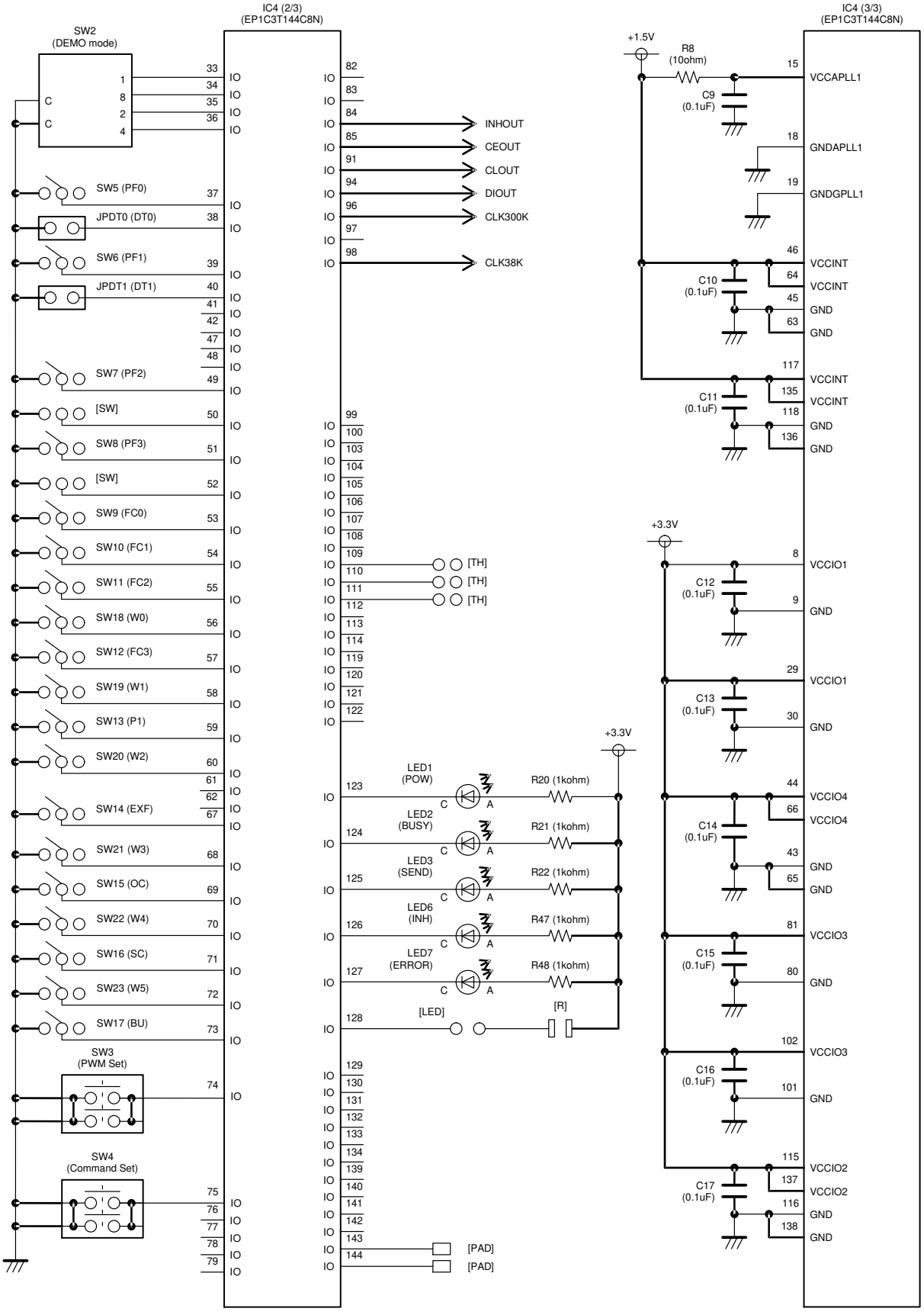
The LCD driver IC (LC75843UGA) has various control data for condition setting. Serial data are transferred when push SW4 (Command Set) after having set toggle switches from SW5 to SW23. In addition, PWM data from SW18 to SW23 are set by pushing SW3 (PWM Set) depending on a demonstration mode. Furthermore, the LCD display data for various display and the general-purpose port data for LED control are generated by a demonstration mode chosen by SW2 (DEMO mode). The internal pull-up resistor function of the input pins of FPGA are set to active.

The customer can confirm the operating conditions of the internal circuit of an FPGA by an LED monitor (POW, BUSY, SEND, INH, ERROR).



NOTE: The part with a square bracket is not implemented on a board. ([SW])

Figure 9. Schematic of Controller Circuit (1/2)



NOTE: The part with a square bracket is not implemented on a board. ([SW], [LED], [R], [TH], [PAD])

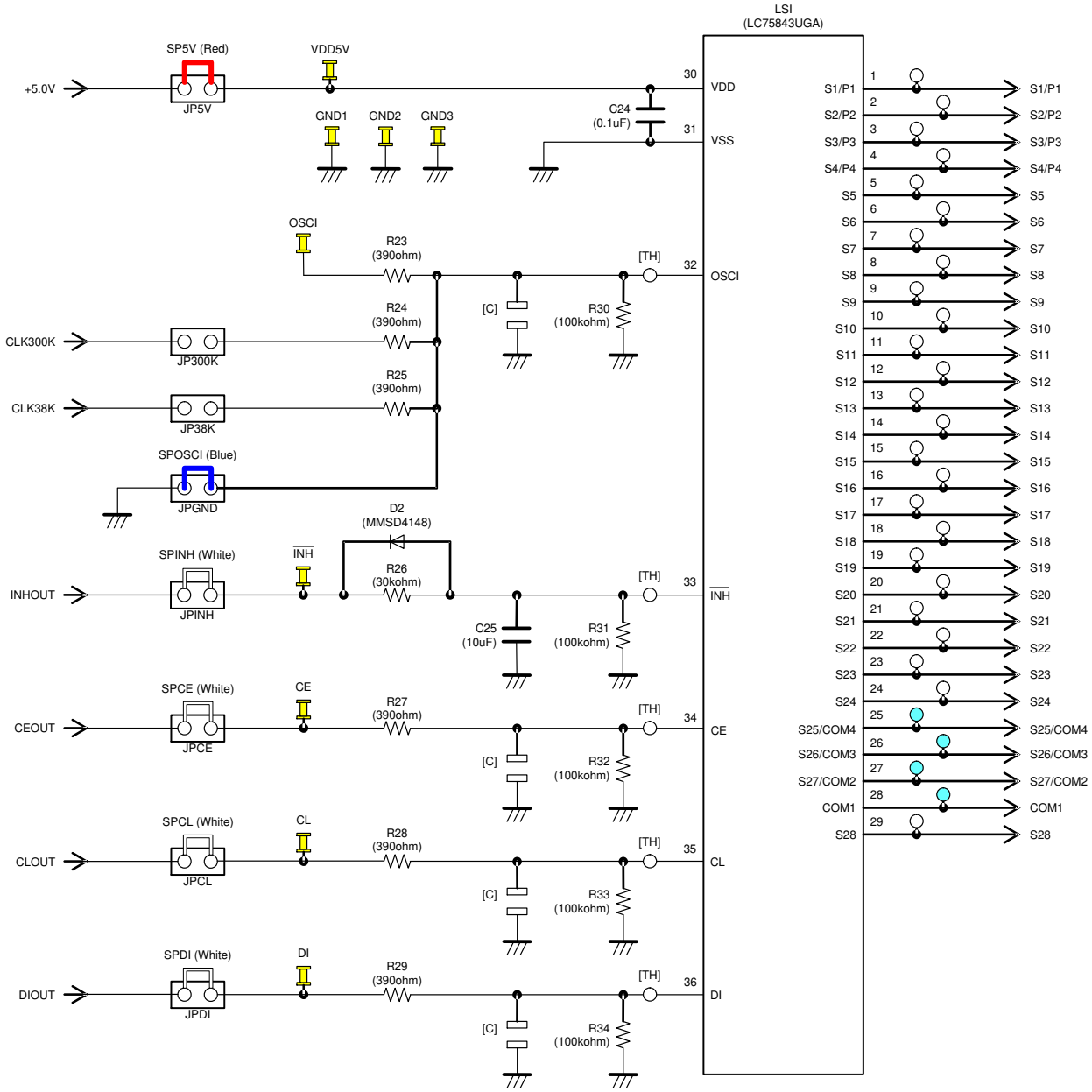
Figure 10. Schematic of Controller Circuit (2/2)

LCD Driver IC Circuit

The LCD driver circuit of this evaluation board uses LC75843UGA. The power supply and the control signal supplied from the controller circuit can separate it by removing a jump socket. Thereby, the customer can supply a power supply and a control signal from the external.

The power supply of the LCD driver IC is supplied +5 V voltage by the power supply circuit of this evaluation board. When customer evaluate the voltage other than +5 V, remove the jump socket of the JP5V, and supply power supply to “VDD5V” pin. Insert only one jump socket in a socket pin of the JPGND, JP38K or JP300K for OSCI signal by setting of control data of the LCD driver IC. When OC is set to L(0), insert the jump socket of the JPGND. When OC is set to H(1) and EXF is set to L(0), insert the jump socket of the JP300K. When OC is set to H(1) and EXF is set to H(1), insert the jump socket of the JP38K.

The resistors from R23 to R29 are the dumping resistance for waveform shaping. In addition, when waveform shaping is more necessary, connect a condenser (for example, from 100 to 1000 pF) to [C]. The resistors from R30 to R34 are pull-down resistor to protect a circuit when a jump socket was removed.



NOTE: The part with a square bracket is not implemented on a board. ([C], [TH])

Figure 11. Schematic of LCD Driver IC Circuit

LCD Panel Circuit

The LCD panel circuit of this evaluation board uses a socket pin, and LCD panel made in varitronix is inserted there. The specifications of the LCD panel are four common pins, 32 segment pins, twisted nematic (TN) type, reflection type, alphanumeric character display and 70.00 mm × 25.00 mm × 2.80 mm.

Four common output signals and 21 segment output signals of the LCD driver IC are connected to an LCD panel. Because S28 output is connected to twelve segments of the LCD panel, the customer can confirm the waveform of big load. About the segment allotment of the LCD panel, refer to “LCD Panel Segment Allotment”.

When customer evaluate the display system using the customer’s original LCD panel, remove an inserted LCD panel, and connect a customer’s original LCD panel.

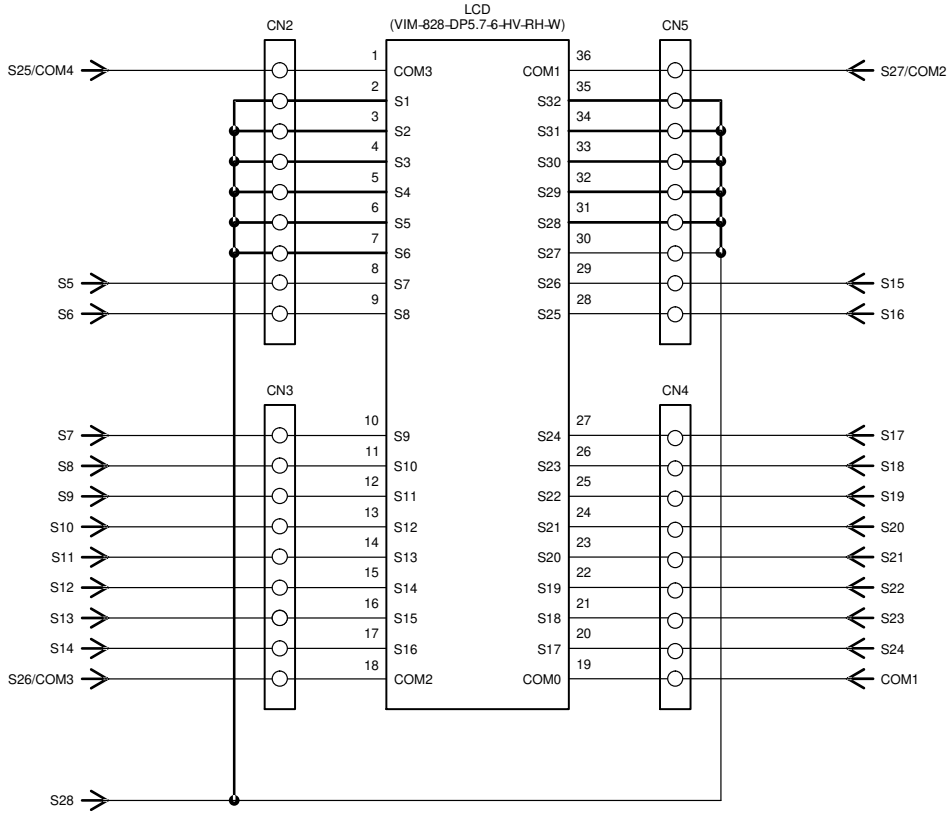


Figure 12. Schematic of LCD Panel Circuit

LED Circuit

The LED circuit of this evaluation board uses a single color LED and three color (RGB) LED. The LED is controlled by the general-purpose port output of LCD driver IC (LC75843UGA). The general-purpose port output has up to four, and brightness adjustment (64 steps) is possible by PWM output function of up to 3-channel.

The pull-up power supply of the LED is supplied +5 V voltage by the power supply circuit of this evaluation board. When customer evaluate the voltage other than +5 V, remove the jump socket of the JPUP, and supply pull-up power supply to “VOUP” pin.

When customer uses general-purpose port outputs (S1/P1 to S4/P4) of LCD driver IC (LC75843UGA) as a segment output, remove the jump sockets from JPP1 to JPP4. The resistors from R35 to R38 are pull-down resistor to protect a circuit when a jump socket was removed.

The calculating formula of the LED current:
IF = (VOUP – VF – Vsat) / R [A]

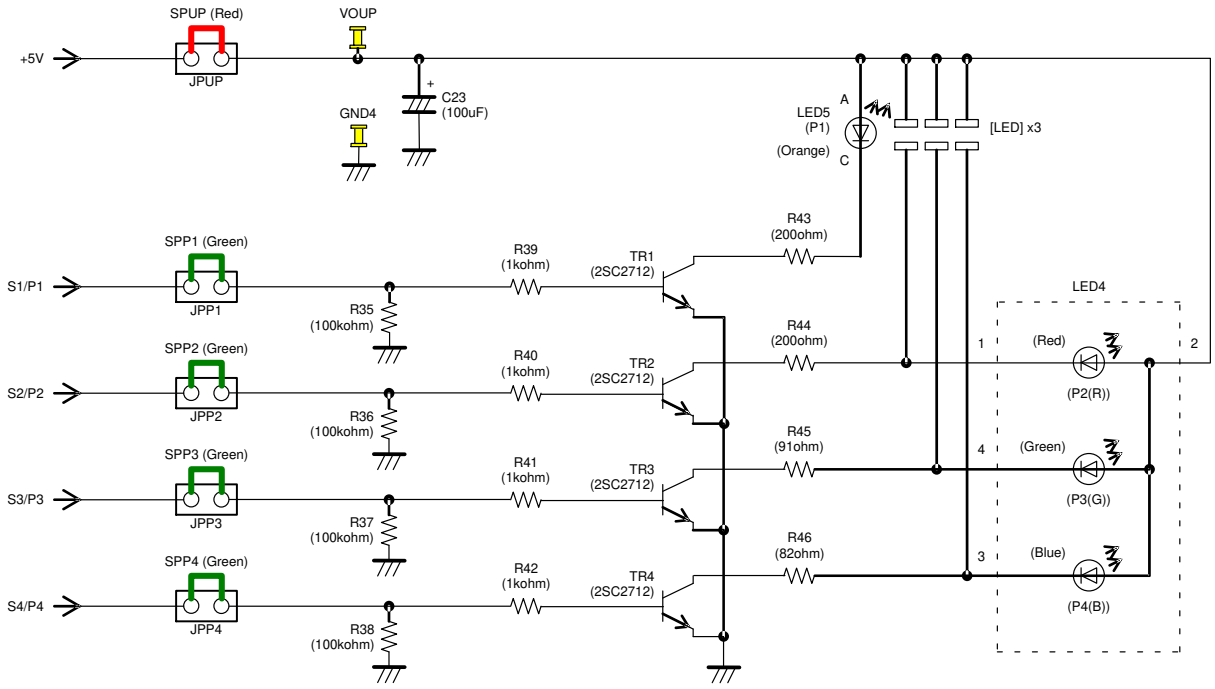
For example,

LED5 (P1): IF1 = (5 – 1.9 – 0.1) / 200 = 15.0 mA

LED4 (P2(R)): IF2 = (5 – 2.0 – 0.1) / 200 = 14.5 mA

LED4 (P3(G)): IF3 = (5 – 3.5 – 0.1) / 91 = 15.4 mA

LED4 (P4(B)): IF4 = (5 – 3.6 – 0.1) / 82 = 15.8 mA



NOTE: The part with a square bracket is not implemented on a board. ([LED])

Figure 13. Schematic of LED Circuit

PIN FUNCTIONS

Table 2. PIN FUNCTIONS OF LC75843UGA EVALUATION BOARD (LC75843UGAGEVB)

Pin Name	Functions	I/O	Control Jump Socket
VDD5V	Power supply pin for LCD driver IC (LC75843UGA). When supply the power supply voltage from the external, remove the jump socket of the JP5V. When the power supply circuit in the evaluation board is used, the +5.0 [V] voltage is outputted.	I/O	JP5V 
VOUP	Pull-up power supply pin for LED. When supply the pull-up power supply voltage from the external, remove the jump socket of the JPUP. When the power supply circuit in the evaluation board is used, the +5.0 [V] voltage is outputted.	I/O	JPUP 
GND	Ground pin. Must be connected to ground of all external equipments.	–	– 
OSCI	External clock input pin. When OC is set to L(0), insert the jump socket of the JPGND. When OC is set to H(1) and EXF is set to L(0), insert the jump socket of the JP300K. When OC is set to H(1) and EXF is set to H(1), insert the jump socket of the JP38K.	I/O	JPGND, JP38K, JP300K 
$\overline{\text{INH}}$	Display forced off control input pin. When input the $\overline{\text{INH}}$ signal from the external, remove the jump socket of the JPINH.	I/O	JPINH 
CE	Chip enable signal input pin of the CCB format. When input the CE signal from the external, remove the jump socket of the JPCE.	I/O	JPCE 
CL	Synchronization clock signal input pin of the CCB format. When input the CL signal from the external, remove the jump socket of the JPCL.	I/O	JPCL 
DI	Serial data signal input pin of the CCB format. When input the DI signal from the external, remove the jump socket of the JPDI.	I/O	JPDI 
S1/P1 to S4/P4	Segment outputs or general-purpose port outputs pin. The pins from S1/P1 to S4/P4 can be used as a general-purpose port output by setting of CCB serial data. When the general-purpose port output is used for a segment function in the evaluation environment of the customer's original, remove the jump sockets from JPP1 to JPP4.	O	JPP1 to JPP4 
S5 to S24, S28	Segment output pins.	O	–
COM1	Common output pin.	O	–
COM2/S27, COM3/S26, COM4/S25	Common output or segment output pins. The pins from COM2/S27 to COM4/S25 can be used as a segment output by setting of CCB serial data.	O	–

SETTING METHOD OF THE SWITCH

“DEMO Mode” Rotary Switch

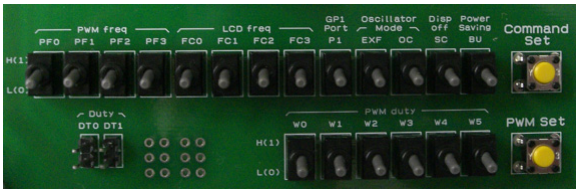
This evaluation board has the demonstration mode which automatically performs LCD display and LED control by controller control. The customer can select various demonstration contents by the “DEMO mode” rotary switch. The following tables shows the setting contents of the “DEMO mode” rotary switch.

When the jump sockets of the DT0 and DT1 were set for the setting that was not 1/4 duty drive, the “DEMO mode” can use only a mode of “0”, “1”, “4” and “5”. In addition, when “DEMO mode” was set to “2”, “3”, “6”, “7”, “8” and “9”, the controller is ignored without operating.

Table 3. SETTING CONTENTS OF THE “DEMO MODE” ROTARY SWITCH

“DEMO Mode” Rotary Switch	Demonstration Item	LCD Display Contents	LED Control Contents
0	All OFF Test	All segments are off.	All LED turn off the light.
1	All ON Test	All segments are on.	All LED turn on the light. (100% brightness)
2	LCD Display Test (1)	The LCD displays a “01234”.	All LED turn off the light.
3	LCD Display Test (2)	The LCD displays a “AbcdE”.	All LED turn off the light.
4	Segment Test	The segment of the LCD displays on in turn.	LED does on in turn.
5	Common Test	LCD segment corresponding to same COM are all on.	When COM1 is on, LED turn on the light.
6	LED (PWM) Test (1)	The LCD displays a “PWM_1” and a PWM duty value.	Any PWM duty are selected by the switches from W0 to W5. (LED1 to LED3 can set same duty)
7	LED (PWM) Test (2)	The LCD displays a “PWM_2” and a PWM channel number.	Any PWM duty are selected by the switches from W0 to W5. (LED1 to LED3 can set each duty)
8	Demonstration (1)	LCD number display count ups every second.	LED does on in turn every second.
9	Demonstration (2)	The LCD displays a “AUTO” and a PWM duty value.	PWM duty changes every 100 ms

Toggle Switch and Push Switch Allotment



The LCD driver IC (LC75843UGA) has various control data for condition setting. Serial data are transferred when push SW4 (Command Set) after having set toggle switches from SW5 (PF0) to SW23 (W5). In addition, PWM data from SW18 (W0) to SW23 (W5) are set by pushing SW3 (PWM Set) depending on a demonstration mode.

Table 4. SETTING CONTENTS OF THE TOGGLE SWITCH

Parts Symbol	Silk Characters	Functions	Control Data of the LCD Driver IC (LC75843UGA)
SW5	PF0	The switches for setting of the PWM output waveform frame frequency	PF0
SW6	PF1		PF1
SW7	PF2		PF2
SW8	PF3		PF3
SW9	FC0	The switches for setting of the common/segment output waveform frame frequency	FC0
SW10	FC1		FC1
SW11	FC2		FC2
SW12	FC3		FC3
SW13	P1	The switch for setting of the general-purpose output port (S1/P1) function	D1, PS10, PS11
SW14	EXF	The switch for setting of the external clock operating frequency	EXF
SW15	OC	The switch for setting of the internal oscillator operating mode/external clock operating mode	OC
SW16	SC	The switch for setting of the on/off state of the segments	SC
SW17	BU	The switch for setting of the normal mode/power-saving mode	BU
SW18 to SW23	W0 to W5	The switches for setting of the PWM data of the PWM output	W0 to W5
JPDT0, JPDT1	DT0, DT1	The sockets for setting of the LCD drive scheme (1/1 to 1/4 duty drive)	DT0, DT1

EXPLANATION OF THE SWITCHES OF SETTING THE CONTROL DATA

The Switches for Setting of the PWM Output Waveform Frame Frequency (PF0 to PF3)

Table 5. EXPLANATION OF THE PF0 TO PF3 TOGGLE SWITCH

Switches				Internal Oscillator Operating Mode (f_{osc} = 300 [kHz] typ.) (OC = "L(0)")	300 [kHz] External Clock Operating Mode (OC = "H(1)", EXF = "L(0)")	38 [kHz] External Clock Operating Mode (OC = "H(1)", EXF = "H(1)")
PF0	PF1	PF2	PF3			
L(0)	L(0)	L(0)	L(0)	195 [Hz]	195 [Hz]	When OC = "1" and EXF = "1" were set to the LCD driver IC, because the LCD driver IC cannot use PWM output function, this setting is ignored.
H(1)	L(0)	L(0)	L(0)	213 [Hz]	213 [Hz]	
L(0)	H(1)	L(0)	L(0)	234 [Hz]	234 [Hz]	
H(1)	H(1)	L(0)	L(0)	260 [Hz]	260 [Hz]	
L(0)	L(0)	H(1)	L(0)	293 [Hz]	293 [Hz]	
H(1)	L(0)	H(1)	L(0)	335 [Hz]	335 [Hz]	
L(0)	H(1)	H(1)	L(0)	390 [Hz]	390 [Hz]	
H(1)	H(1)	H(1)	L(0)	469 [Hz]	469 [Hz]	
L(0)	L(0)	L(0)	H(1)	586 [Hz]	586 [Hz]	
H(1)	L(0)	L(0)	H(1)	781 [Hz]	781 [Hz]	
L(0)	H(1)	L(0)	H(1)	1171 [Hz]	1171 [Hz]	
H(1)	H(1)	L(0)	H(1)	335 [Hz]	335 [Hz]	
L(0)	L(0)	H(1)	H(1)			
H(1)	L(0)	H(1)	H(1)			
L(0)	H(1)	H(1)	H(1)			
H(1)	H(1)	H(1)	H(1)			

The Switches for Setting of the Common/Segment Output Waveform Frame Frequency (FC0 to FC3)

Table 6. EXPLANATION OF THE FC0 TO FC3 TOGGLE SWITCH

Switches				Internal Oscillator Operating Mode (f_{osc} = 300 [kHz] typ.) (OC = "L(0)")	300 [kHz] External Clock Operating Mode (OC = "H(1)", EXF = "L(0)")	38 [kHz] External Clock Operating Mode (OC = "H(1)", EXF = "H(1)")
FC0	FC1	FC2	FC3			
L(0)	L(0)	L(0)	L(0)	49 [Hz]	49 [Hz]	49 [Hz]
L(0)	L(0)	L(0)	H(1)	56 [Hz]	56 [Hz]	56 [Hz]
L(0)	L(0)	H(1)	L(0)	65 [Hz]	65 [Hz]	66 [Hz]
L(0)	L(0)	H(1)	H(1)	78 [Hz]	78 [Hz]	79 [Hz]
L(0)	H(1)	L(0)	L(0)	87 [Hz]	87 [Hz]	88 [Hz]
L(0)	H(1)	L(0)	H(1)	97 [Hz]	97 [Hz]	99 [Hz]
L(0)	H(1)	H(1)	L(0)	111 [Hz]	111 [Hz]	113 [Hz]
L(0)	H(1)	H(1)	H(1)	130 [Hz]	130 [Hz]	132 [Hz]
H(1)	L(0)	L(0)	L(0)	142 [Hz]	142 [Hz]	144 [Hz]
H(1)	L(0)	L(0)	H(1)	156 [Hz]	156 [Hz]	158 [Hz]
H(1)	L(0)	H(1)	L(0)	173 [Hz]	173 [Hz]	176 [Hz]
H(1)	L(0)	H(1)	H(1)	195 [Hz]	195 [Hz]	198 [Hz]
H(1)	H(1)	L(0)	L(0)	223 [Hz]	223 [Hz]	226 [Hz]
H(1)	H(1)	L(0)	H(1)	260 [Hz]	260 [Hz]	264 [Hz]
H(1)	H(1)	H(1)	L(0)	312 [Hz]	312 [Hz]	316 [Hz]
H(1)	H(1)	H(1)	H(1)	390 [Hz]	390 [Hz]	396 [Hz]

The Switch for Setting of the General-purpose Output Port (S1/P1) Function (P1)

Table 7. EXPLANATION OF THE P1 TOGGLE SWITCH

Switch	Control Data of the LCD Driver IC (LC75843UGA)			
P1	D1	PS10	PS10	Operating Contents
L(0)	0	0	0	The LED(P1) is Turned Off
H(1)	1	0	0	The LED(P1) is Turned On

The Switch for Setting of the Internal Oscillator Operating Mode/External Clock Operating Mode (OC and EXF)

Table 8. EXPLANATION OF THE OC AND EXF TOGGLE SWITCH

Switches			
OC	EXF	Clock Operating Mode	Control Jump Socket
L(0)	L(0)	Internal Oscillator Operating Mode	Insert the Jump Socket of the JPGND
L(0)	H(1)		
H(1)	L(0)	300 [kHz] External Clock Operating Mode	Insert the Jump Socket of the JP300K
H(1)	H(1)	38 [kHz] External Clock Operating Mode	insert the Jump Socket of the JP38K

The Switch for Setting of the On/Off State of the Segments (SC)

Table 9. EXPLANATION OF THE SC TOGGLE SWITCH

Switch	
SC	Operating Contents
L(0)	Normal Display
H(1)	All Segments are OFF Waveform Drive

The Switch for Setting of the Normal Mode/Power-saving Mode (BU)

Table 10. EXPLANATION OF THE BU TOGGLE SWITCH

Switch	
BU	Operating Contents
L(0)	Normal Mode
H(1)	Power Saving Mode

The Switches for Setting of the PWM Data of the PWM Output (W0 to W5)

Table 11. EXPLANATION OF THE W0 TO W5 TOGGLE SWITCH

Switches						
W0	W1	W2	W3	W4	W5	PWM Duty of the General-purpose Port Output
L(0)	L(0)	L(0)	L(0)	L(0)	L(0)	1/64 (1.56%)
H(1)	L(0)	L(0)	L(0)	L(0)	L(0)	2/64 (3.12%)
L(0)	H(1)	L(0)	L(0)	L(0)	L(0)	3/64 (4.69%)
H(1)	H(1)	L(0)	L(0)	L(0)	L(0)	4/64 (6.25%)
L(0)	L(0)	H(1)	L(0)	L(0)	L(0)	5/64 (7.81%)
H(1)	L(0)	H(1)	L(0)	L(0)	L(0)	6/64 (9.38%)
L(0)	H(1)	H(1)	L(0)	L(0)	L(0)	7/64 (10.94%)
H(1)	H(1)	H(1)	L(0)	L(0)	L(0)	8/64 (12.50%)
L(0)	L(0)	L(0)	H(1)	L(0)	L(0)	9/64 (14.06%)
H(1)	L(0)	L(0)	H(1)	L(0)	L(0)	10/64 (15.62%)
L(0)	H(1)	L(0)	H(1)	L(0)	L(0)	11/64 (17.19%)
H(1)	H(1)	L(0)	H(1)	L(0)	L(0)	12/64 (18.75%)
L(0)	L(0)	H(1)	H(1)	L(0)	L(0)	13/64 (20.31%)
H(1)	L(0)	H(1)	H(1)	L(0)	L(0)	14/64 (21.87%)
L(0)	H(1)	H(1)	H(1)	L(0)	L(0)	15/64 (23.44%)
H(1)	H(1)	H(1)	H(1)	L(0)	L(0)	16/64 (25.00%)
L(0)	L(0)	L(0)	L(0)	H(1)	L(0)	17/64 (26.56%)
H(1)	L(0)	L(0)	L(0)	H(1)	L(0)	18/64 (28.12%)
L(0)	H(1)	L(0)	L(0)	H(1)	L(0)	19/64 (29.69%)
H(1)	H(1)	L(0)	L(0)	H(1)	L(0)	20/64 (31.25%)
L(0)	L(0)	H(1)	L(0)	H(1)	L(0)	21/64 (32.81%)
H(1)	L(0)	H(1)	L(0)	H(1)	L(0)	22/64 (34.37%)
L(0)	H(1)	H(1)	L(0)	H(1)	L(0)	23/64 (35.94%)
H(1)	H(1)	H(1)	L(0)	H(1)	L(0)	24/64 (37.50%)
L(0)	L(0)	L(0)	H(1)	H(1)	L(0)	25/64 (39.06%)
H(1)	L(0)	L(0)	H(1)	H(1)	L(0)	26/64 (40.62%)
L(0)	H(1)	L(0)	H(1)	H(1)	L(0)	27/64 (42.19%)
H(1)	H(1)	L(0)	H(1)	H(1)	L(0)	28/64 (43.75%)
L(0)	L(0)	H(1)	H(1)	H(1)	L(0)	29/64 (45.31%)
H(1)	L(0)	H(1)	H(1)	H(1)	L(0)	30/64 (46.87%)
L(0)	H(1)	H(1)	H(1)	H(1)	L(0)	31/64 (48.44%)
H(1)	H(1)	H(1)	H(1)	H(1)	L(0)	32/64 (50.00%)
L(0)	L(0)	L(0)	L(0)	L(0)	H(1)	33/64 (51.56%)
H(1)	L(0)	L(0)	L(0)	L(0)	H(1)	34/64 (53.12%)
L(0)	H(1)	L(0)	L(0)	L(0)	H(1)	35/64 (54.69%)
H(1)	H(1)	L(0)	L(0)	L(0)	H(1)	36/64 (56.25%)
L(0)	L(0)	H(1)	L(0)	L(0)	H(1)	37/64 (57.81%)
H(1)	L(0)	H(1)	L(0)	L(0)	H(1)	38/64 (59.37%)
L(0)	H(1)	H(1)	L(0)	L(0)	H(1)	39/64 (60.94%)
H(1)	H(1)	H(1)	L(0)	L(0)	H(1)	40/64 (62.50%)

Table 11. EXPLANATION OF THE W0 TO W5 TOGGLE SWITCH (continued)

Switches						
W0	**W1**	**W2**	**W3**	**W4**	**W5**	**PWM Duty of the General-purpose Port Output**
L(0)	L(0)	L(0)	H(1)	L(0)	H(1)	41/64 (64.06%)
H(1)	L(0)	L(0)	H(1)	L(0)	H(1)	42/64 (65.62%)
L(0)	H(1)	L(0)	H(1)	L(0)	H(1)	43/64 (67.19%)
H(1)	H(1)	L(0)	H(1)	L(0)	H(1)	44/64 (68.75%)
L(0)	L(0)	H(1)	H(1)	L(0)	H(1)	45/64 (70.31%)
H(1)	L(0)	H(1)	H(1)	L(0)	H(1)	46/64 (71.87%)
L(0)	H(1)	H(1)	H(1)	L(0)	H(1)	47/64 (73.44%)
H(1)	H(1)	H(1)	H(1)	L(0)	H(1)	48/64 (75.00%)
L(0)	L(0)	L(0)	L(0)	H(1)	H(1)	49/64 (76.56%)
H(1)	L(0)	L(0)	L(0)	H(1)	H(1)	50/64 (78.12%)
L(0)	H(1)	L(0)	L(0)	H(1)	H(1)	51/64 (79.69%)
H(1)	H(1)	L(0)	L(0)	H(1)	H(1)	52/64 (81.25%)
L(0)	L(0)	H(1)	L(0)	H(1)	H(1)	53/64 (82.81%)
H(1)	L(0)	H(1)	L(0)	H(1)	H(1)	54/64 (84.37%)
L(0)	H(1)	H(1)	L(0)	H(1)	H(1)	55/64 (85.94%)
H(1)	H(1)	H(1)	L(0)	H(1)	H(1)	56/64 (87.50%)
L(0)	L(0)	L(0)	H(1)	H(1)	H(1)	57/64 (89.06%)
H(1)	L(0)	L(0)	H(1)	H(1)	H(1)	58/64 (90.62%)
L(0)	H(1)	L(0)	H(1)	H(1)	H(1)	59/64 (92.19%)
H(1)	H(1)	L(0)	H(1)	H(1)	H(1)	60/64 (93.75%)
L(0)	L(0)	H(1)	H(1)	H(1)	H(1)	61/64 (95.31%)
H(1)	L(0)	H(1)	H(1)	H(1)	H(1)	62/64 (96.87%)
L(0)	H(1)	H(1)	H(1)	H(1)	H(1)	63/64 (98.44%)
H(1)	H(1)	H(1)	H(1)	H(1)	H(1)	64/64 (100.00%)

EXPLANATION OF THE JUMP SOCKETS OF SETTING THE CONTROL DATA

The Sockets for Setting of the LCD Drive Scheme (1/1 to 1/4 Duty Drive) (DT0 and DT1)

When a customer uses the “Customer’s original LCD panel”, because the segment allotments of the LCD panel are different the control by the “Customer’s original controller board” is necessary.

When the controller circuit in the evaluation board and the 1/4 duty LCD panel are used, remove the jump sockets of the DT0 and DT1.

When the controller circuit in the evaluation board and the 1/3 duty LCD panel are used, insert the jump socket of the DT0 and remove the jump socket of the DT1.

When the controller circuit in the evaluation board and the 1/2 duty LCD panel are used, insert the jump socket of the DT1 and remove the jump socket of the DT0.

When the controller circuit in the evaluation board and the static (1/1 duty) LCD panel are used, insert the jump sockets of the DT0 and DT1.

When the jump sockets of the DT0 and DT1 were set for the setting that was not 1/4 duty drive, the “DEMO mode” can use only a mode of “0”, “1”, “4” and “5”. In addition, when “DEMO mode” was set to “2”, “3”, “6”, “7”, “8” and “9”, the controller is ignored without operating, and the LED of the “ERROR” is turned on.

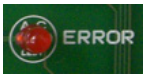
Table 12. EXPLANATION OF THE DT0 AND DT1 JUMP SOCKETS

Jump Sockets		Control Data of the LCD Driver IC (LC75843UGA)		Operating Contents
DT0	DT1	DT0	DT1	
Remove	Remove	0	0	1/4 Duty Drive Scheme
Insert	Remove	1	0	1/3 Duty Drive Scheme
Remove	Insert	0	1	1/2 Duty Drive Scheme
Insert	Insert	1	1	Static (1/1 Duty) Drive Scheme

EXPLANATION OF THE LED MONITOR OF THE CONTROLLER CIRCUIT

The LED monitor circuit is connected to FPGA. The customer can confirm the operating conditions of the internal circuit of an FPGA by an LED monitor of the POW, BUSY, SEND, INH and ERROR.

Table 13. EXPLANATION OF THE LED MONITOR

Symbol	Functions
POW 	LED monitor for main power supply ON/OFF. The power supply is supplied by moving “POWER” switch to the “ON” position, and the LED of the “POW” is turned on when FPGA operated normally.
BUSY 	LED monitor for during the demonstration. The automatic demonstration mode is selected by moving “DEMO mode” switch to the “8” or “9” positions, and the LED of the “BUSY” is turned on when a demonstration is started.
SEND 	LED monitor for CCB serial data transfer. The LED of the “SEND” is turned on when the CCB serial data are transferred by a demonstration or pushing the switches of the “Command Set” or “PWM Set”.
INH 	LED monitor for INH signal state. The LED of the “INH” is turned on when INH output is outputted to high level.
ERROR 	LED monitor for the setting state error of the switches. The LED of the “ERROR” is turned on, when the setting of the switch of the “DEMO mode” and the setting of the jump socket of the “Duty” included an error. At the time of error, the CCB serial data are not transferred even if pushing the switches of the “Command Set” or “PWM Set”.