Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ordering number : EN4828A

CMOS LSI

# LC75852E, 75852W

## Asynchronous Silicon Gate 1/2 Duty LCD Driver with On-Chip Key Input Function

An ON Semiconductor Company

## Overview

The LC75852E and LC75852W are 1/2 duty dynamic LCD display drivers. In addition to being able to directly drive LCD panels with up to 90 segments, they can also control up to four general-purpose output ports. These products also include a key scan circuit which allows them to accept input from keypads with up to 30 keys. This allows end product front panel wiring to be simplified.

## Features

- Up to 30 key inputs (Key scan is only performed when a key is pressed.)
- 1/2 duty – 1/2 bias (up to 90 segments)
- Sleep mode and the all segments off function can be controlled from serial data.
- Segment output port/general-purpose output port usage can be controlled from serial data.
- Serial data I/O supports CCB format communication with the system controller.
- High generality since display data is displayed directly without decoder intervention
- Reset pin that can establish the initial state.

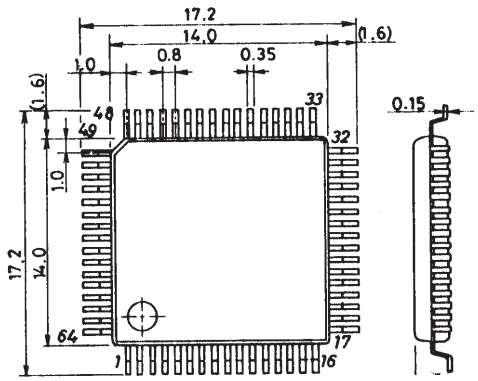
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

## Package Dimensions

unit: mm

**3159-QFP64E**

[LC75852E]

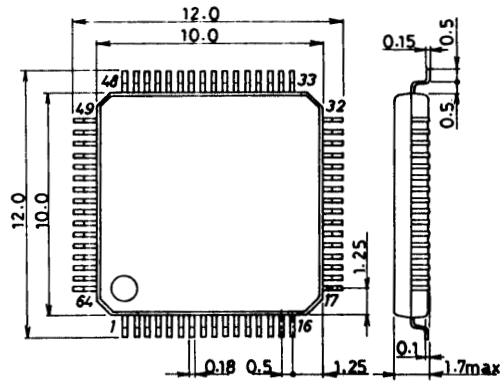



SANYO: QIP64E

unit: mm

**3190-SQFP64**

[LC75852W]




SANYO: SQFP64

## Specifications

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | OSC, CE, CL, DI, $\overline{RES}$, KI1 to KI5 | –0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage | $V_{OUT}$ | OSC, DO, S1 to S45, COM1, COM2, KS1 to KS6, P1 to P4 | –0.3 to $V_{DD}$ + 0.3 | V |
| Output current | $I_{OUT}1$ | S1 to S45 | 100 | µA |
| | $I_{OUT}2$ | COM1, COM2, KS1 to KS6 | 1 | mA |
| | $I_{OUT}3$ | P1 to P4 | 5 | mA |
| Allowable power dissipation | Pd max | Ta = 85°C | 200 | mW |
| Operating temperature | Topr | | –40 to +85 | °C |
| Storage temperature | Tstg | | –55 to +125 | °C |

## Allowable Operating Ranges at Ta = –40 to +85°C, $V_{SS}$ = 0 V

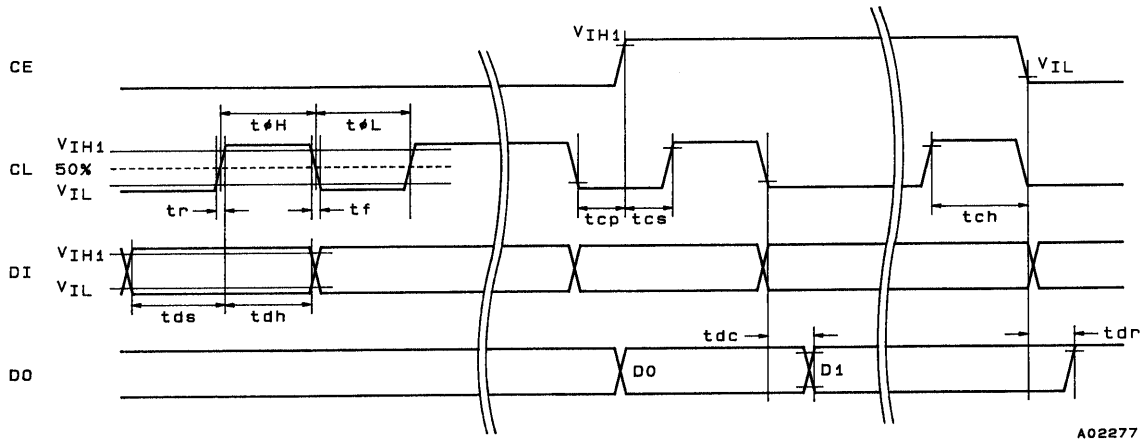
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 4.5 | | 6.0 | V |
| Input high-level voltage | $V_{IH}1$ | CE, CL, DI, $\overline{RES}$ | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH}2$ | KI1 to KI5 | 0.6 $V_{DD}$ | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}$ | CE, CL, DI, $\overline{RES}$, KI1 to KI5 | 0 | | 0.2 $V_{DD}$ | V |
| Recommended external resistance | $R_{OSC}$ | OSC | | 62 | | kΩ |
| Recommended external capacitance | $C_{OSC}$ | OSC | | 680 | | pF |
| Guaranteed oscillator range | $f_{OSC}$ | OSC | 25 | 50 | 100 | kHz |
| Data setup time | $t_{ds}$ | CL, DI: Figure 1 | 160 | | | ns |
| Data hold time | $t_{dh}$ | CL, DI: Figure 1 | 160 | | | ns |
| CE wait time | $t_{cp}$ | CE, CL: Figure 1 | 160 | | | ns |
| CE setup time | $t_{cs}$ | CE, CL: Figure 1 | 160 | | | ns |
| CE hold time | $t_{ch}$ | CE, CL: Figure 1 | 160 | | | ns |
| High-level clock pulse width | $t_{øH}$ | CL: Figure 1 | 160 | | | ns |
| Low-level clock pulse width | $t_{øL}$ | CL: Figure 1 | 160 | | | ns |
| Rise time | $t_r$ | CE, CL, DI: Figure 1 | | 160 | | ns |
| Fall time | $t_f$ | CE, CL, DI: Figure 1 | | 160 | | ns |
| DO output delay time | $t_{dc}$ | DO, $R_{PU}$ = 4.7 kΩ, $C_L$ = 10 pF*: Figure 1 | | | 1.5 | µs |
| DO rise time | $t_{dr}$ | DO, $R_{PU}$ = 4.7 kΩ, $C_L$ = 10 pF*: Figure 1 | | | 1.5 | µs |
| $\overline{RES}$ switching time | t2 | Figure 2 | 10 | | | µs |

Note: * Since DO is an open-drain output, these values differ depending on the pull-up resistor $R_{PU}$ and the load capacitance $C_L$.

## Electrical Characteristics in the Allowable Operating Ranges

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Hysteresis | $V_H$ | CE, CL, DI, $\overline{RES}$, KI1 to KI5 | | 0.1 $V_{DD}$ | | V |
| Input high-level current | $I_{IH}$ | CE, CL, DI, $\overline{RES}$: $V_I$ = 6.0 V | | | 5.0 | µA |
| Input low-level current | $I_{IL}$ | CE, CL, DI, $\overline{RES}$: $V_I$ = 0 V | –5.0 | | | µA |
| Input floating voltage | $V_{IF}$ | KI1 to KI5 | | | 0.05 $V_{DD}$ | V |
| Pull-down resistance | $R_{PD}$ | KI1 to KI5: $V_{DD}$ = 5.0 V | 50 | 100 | 250 | kΩ |
| Output off leakage current | $I_{OFFH}$ | DO: $V_O$ = 6.0 V | | | 6.0 | µA |
| Output high-level voltage | $V_{OH}1$ | KS1 to KS6: $I_O$ = –1 mA | $V_{DD}$ – 1.0 | | | V |
| | $V_{OH}2$ | P1 to P4: $I_O$ = –1 mA | $V_{DD}$ – 1.0 | | | V |
| | $V_{OH}3$ | S1 to S45: $I_O$ = –10 µA | $V_{DD}$ – 1.0 | | | V |
| | $V_{OH}4$ | COM1, COM2: $I_O$ = –100 µA | $V_{DD}$ – 0.6 | | | V |
| Output low-level voltage | $V_{OL}1$ | KS1 to KS6: $I_O$ = 50 µA | 0.4 | 1.0 | 3.0 | V |
| | $V_{OL}2$ | P1 to P4: $I_O$ = 1 mA | | | 1.0 | V |
| | $V_{OL}3$ | S1 to S45: $I_O$ = 10 µA | | | 1.0 | V |
| | $V_{OL}4$ | COM1, COM2: $I_O$ = 100 µA | | | 0.6 | V |
| | $V_{OL}5$ | DO: $I_O$ = 1 mA | | 0.1 | 0.5 | V |
| Output middle-level voltage | $V_{MID}1$ | COM1, COM2: $V_{DD}$ = 6.0 V, $I_O$ = ±100 µA | 2.4 | 3.0 | 3.6 | V |
| | $V_{MID}2$ | COM1, COM2: $V_{DD}$ = 4.5 V, $I_O$ = ±100 µA | 1.65 | 2.25 | 2.85 | V |
| Current drain | $I_{DD}1$ | Sleep mode, Ta = 25°C | | | 5 | µA |
| | $I_{DD}2$ | $V_{DD}$ = 6.0 V, output open, Ta = 25°C, $f_{OSC}$ = 50 kHz | | 1.4 | 2.5 | mA |

1. When stopped with CL at the low level




2. When stopped with CL at the high level

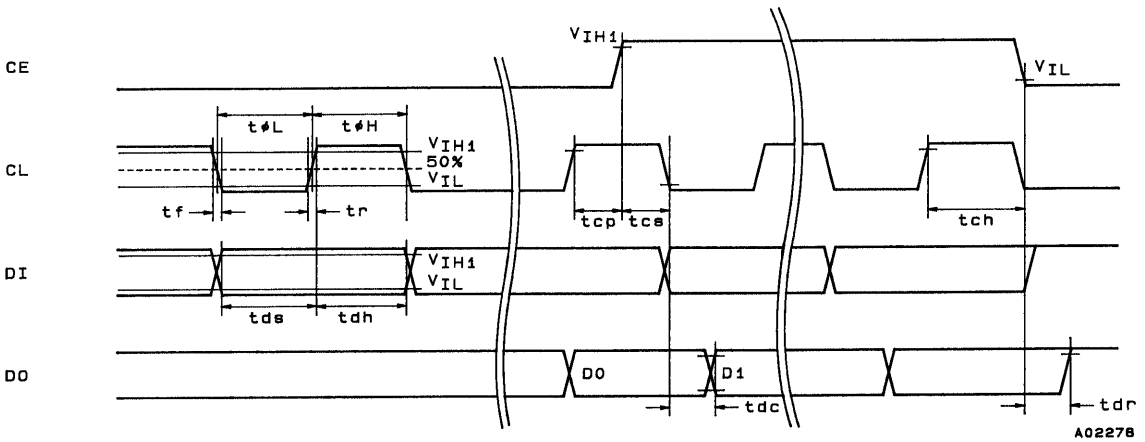
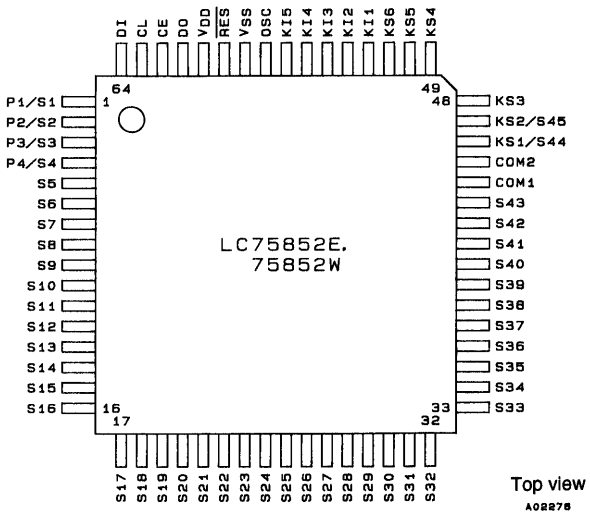
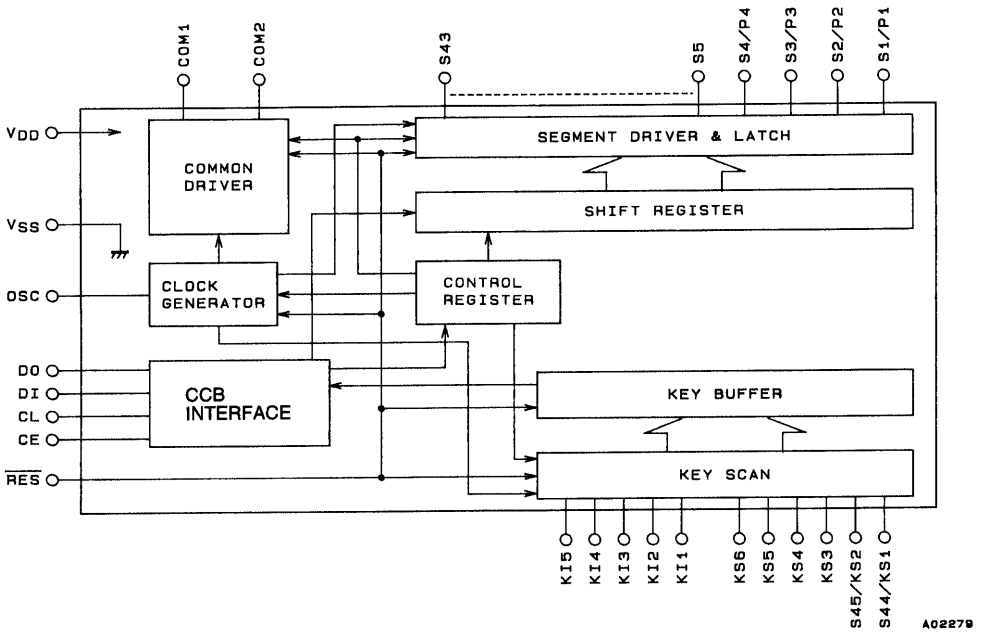



**Figure 1**

## Pin Assignment



## Block Diagram

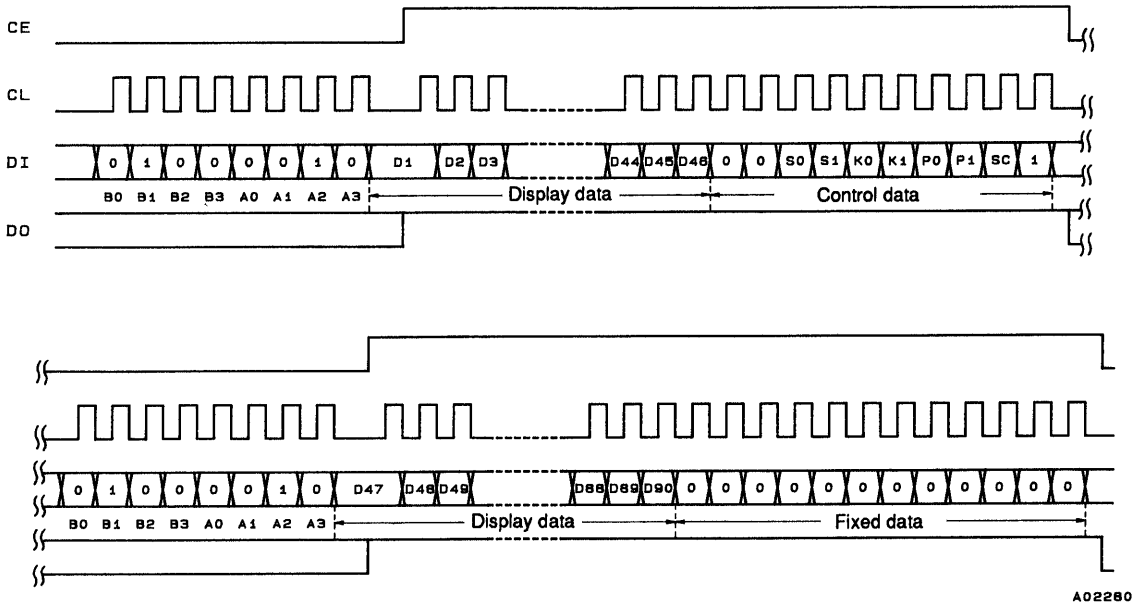



## Pin Functions

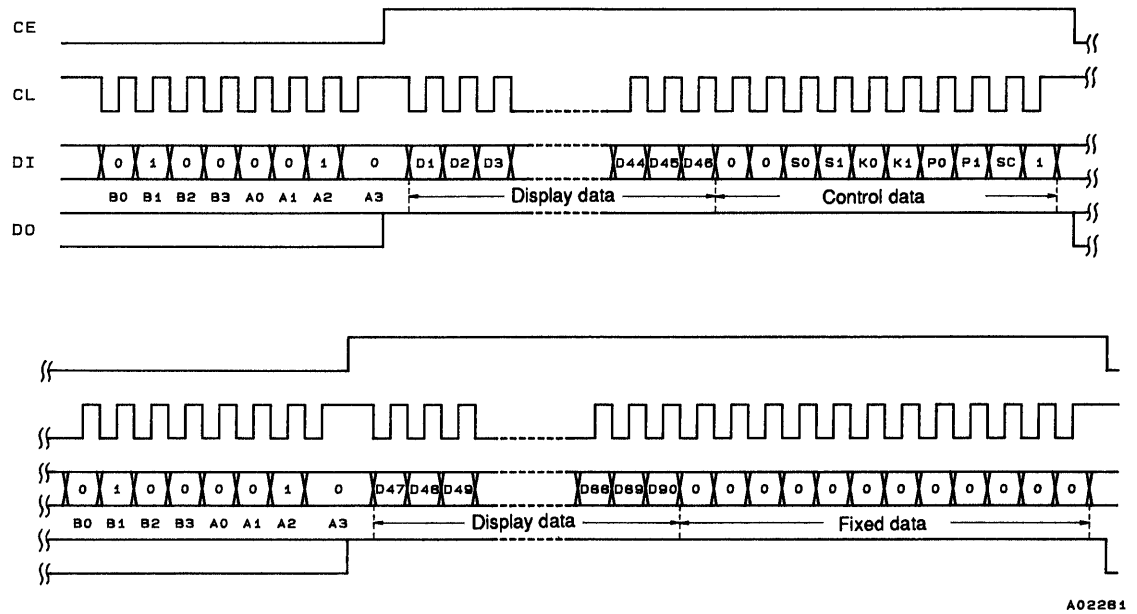
| Pin | Pin No. | Function | Active | I/O | Handling when unused |
|---|---|---|---|---|---|
| S1/P1 to S4/P4<br>S5 to S43 | 1 to 4<br>5 to 43 | Segment outputs: Used to output the display data that is transmitted over the serial data input. Pins S1/P1 to S4/P4 can be used as general-purpose outputs according to control data specification. | — | O | Open |
| COM1<br>COM2 | 44<br>45 | Common driver outputs. The frame frequency $f_O$ is ($f_{OSC}$/512) Hz. | — | O | Open |
| KS1/S44,<br>KS2/S45,<br>KS3 to KS6 | 46<br>47<br>48 to 51 | Key scan outputs. When a key matrix is formed, normally a diode will be attached to the key scan timing line to prevent shorts. However, since the output transistor impedance is an unbalanced CMOS output, it will not be damaged if shorted. Pins KS1/S44 and KS2/S45 can be used as segment outputs according to control data specification. | — | O | Open |
| KI1 to KI5 | 52 to 56 | Key scan inputs: Pins with a built-in pull-down resistor. | H | I | GND |
| OSC | 57 | Oscillator connection: Oscillator circuit can be formed by connecting the pin to a resistor and a capacitor. | — | I/O | $V_{DD}$ |
| CE | 62 | Serial data interface: Connected to the controller. Since DO is an open-drain output, it requires a pull-up resistor.<br>CE: Chip enable<br>CL: Synchronization clock<br>DI: Transfer data<br>DO: Output data | H | I | GND |
| CL | 63 | | ↑ | I | |
| DI | 64 | | — | I | |
| DO | 61 | | — | O | Open |
| $\overline{RES}$ | 59 | Reset input that re-initializes the LSI internal states. During a reset, the display segments are turned off forcibly regardless of the internal display data. All internal key data is reset to low and the key scan operation is disabled. However, serial data can be input during a reset. | L | I | GND |
| $V_{DD}$ | 60 | Power supply connection. A supply voltage of between 4.5 and 6.0 V must be provided. | — | — | — |
| $V_{SS}$ | 58 | Power supply ground connection. Must be connected to GND. | — | — | — |

## Serial Data Input

1. When stopped with CL at the low level




2. When stopped with CL at the high level




CCB address.....[42H]
D1 to D90.....Display data
S0, S1 .....Sleep control data
K0, K1 .....Key scan output/segment output selection data
P0, P1 .....Segment output port/general-purpose output port selection data
SC .....Segment on/off control data

## Control Data Functions

1. S0, S1 .....Sleep control data
   This control data switches the LSI between normal mode and sleep mode. It also sets the key scan output standby states for pins KS1 to KS6.

| Control data | | Mode | Oscillator | Segment outputs Common outputs | Key scan standby mode output pin states | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S0 | S1 | | | | KS1 | KS2 | KS3 | KS4 | KS5 | KS6 |
| 0 | 0 | Normal | Oscillator | Operation | H | H | H | H | H | H |
| 0 | 1 | Sleep | Stopped | L | L | L | L | L | L | H |
| 1 | 0 | Sleep | Stopped | L | L | L | L | L | H | H |
| 1 | 1 | Sleep | Stopped | L | H | H | H | H | H | H |

Note: The KS1/S44 and KS2/S45 output pins are set to the key scan output state.

2. K0, K1.....Key scan output/segment output selection data
   This control data switches the KS1/S44 and KS2/S45 output pins between the key scan output and segment output functions.

| Control data | | Output pin states | | Maximum number of key inputs |
|---|---|---|---|---|
| K0 | K1 | KS1/S44 | KS2/S45 | |
| 0 | 0 | KS1 | KS2 | 30 |
| 0 | 1 | S44 | KS2 | 25 |
| 1 | X | S44 | S45 | 20 |

X: don't care

3. P0, P1 .....Segment output port/general-purpose output port selection data
   This control data switches the S1/P1 to S4/P4 output pins between the segment output port and the general-purpose output port functions.

| Control data | | Output pin states | | | |
|---|---|---|---|---|---|
| P0 | P1 | S1/P1 | S2/P2 | S3/P3 | S4/P4 |
| 0 | 0 | S1 | S2 | S3 | S4 |
| 0 | 1 | P1 | P2 | S3 | S4 |
| 1 | 0 | P1 | P2 | P3 | S4 |
| 1 | 1 | P1 | P2 | P3 | P4 |

The table below lists the correspondence between the display data and the output pins when the general-purpose output port function is selected.

| Output pin | Corresponding display data |
|---|---|
| S1/P1 | D1 |
| S2/P2 | D3 |
| S3/P3 | D5 |
| S4/P4 | D7 |

For example, if the output pin S4/P4 is set for use as a general-purpose output port, the output pin S4/P4 will output a high level when the display data D7 is 1.

4. SC.....Segment on/off control data
   This control data controls the segment on/off states.

| SC | Display state |
|---|---|
| 0 | On |
| 1 | Off |

## Display Data and Output Pin Correspondences

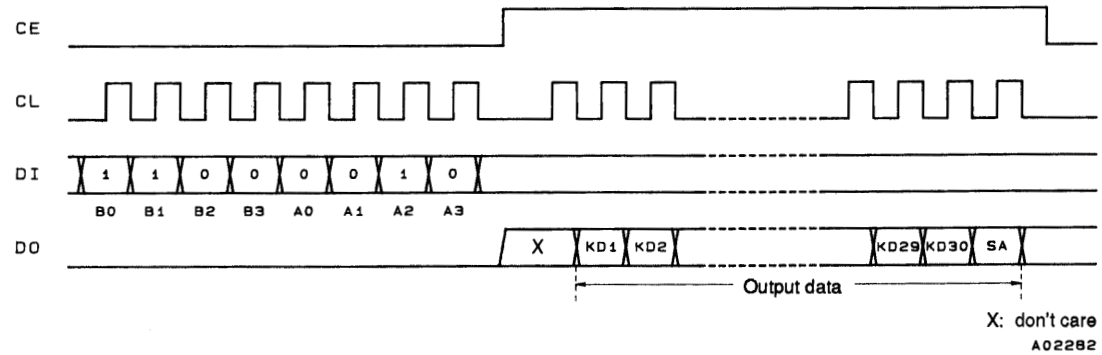
| Output pin | COM1 | COM2 |
|---|---|---|
| S1/P1 | D1 | D2 |
| S2/P2 | D3 | D4 |
| S3/P3 | D5 | D6 |
| S4/P4 | D7 | D8 |
| S5 | D9 | D10 |
| S6 | D11 | D12 |
| S7 | D13 | D14 |
| S8 | D15 | D16 |
| S9 | D17 | D18 |
| S10 | D19 | D20 |
| S11 | D21 | D22 |
| S12 | D23 | D24 |
| S13 | D25 | D26 |
| S14 | D27 | D28 |
| S15 | D29 | D30 |
| S16 | D31 | D32 |
| S17 | D33 | D34 |
| S18 | D35 | D36 |
| S19 | D37 | D38 |
| S20 | D39 | D40 |
| S21 | D41 | D42 |
| S22 | D43 | D44 |
| S23 | D45 | D46 |
| S24 | D47 | D48 |
| S25 | D49 | D50 |
| S26 | D51 | D52 |
| S27 | D53 | D54 |
| S28 | D55 | D56 |
| S29 | D57 | D58 |
| S30 | D59 | D60 |
| S31 | D61 | D62 |
| S32 | D63 | D64 |
| S33 | D65 | D66 |
| S34 | D67 | D68 |
| S35 | D69 | D70 |
| S36 | D71 | D72 |
| S37 | D73 | D74 |
| S38 | D75 | D76 |
| S39 | D77 | D78 |
| S40 | D79 | D80 |
| S41 | D81 | D82 |
| S42 | D83 | D84 |
| S43 | D85 | D86 |
| KS1/S44 | D87 | D88 |
| KS2/S45 | D89 | D90 |

For example, the output states of output pin S11 are listed in the table below.

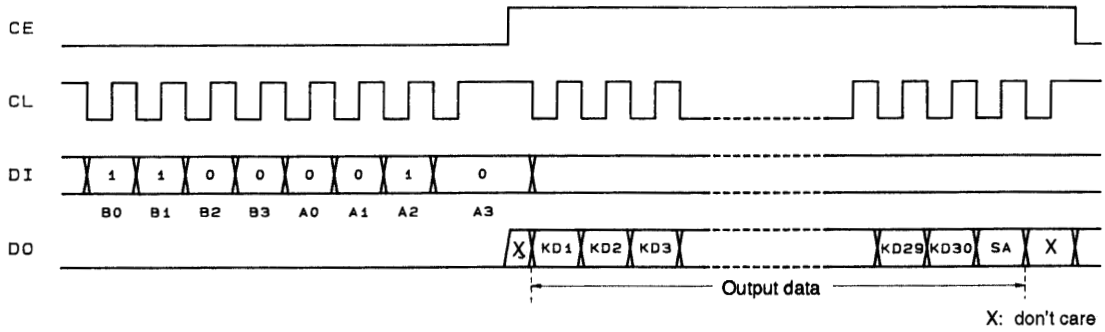
| Display data | | Output pin state |
|---|---|---|
| D21 | D22 | S11 |
| 0 | 0 | Segment off for both COM1 and COM2 |
| 0 | 1 | Segment on for COM2 |
| 1 | 0 | Segment on for COM1 |
| 1 | 1 | Segments on for both COM1 and COM2 |

## Serial Data Output

1. When stopped with CL at the low level




2. When stopped with CL at the high level




CCB address.....[43H]
KD1 to KD30 .....Key data
SA .....Sleep acknowledge data

Note: If key data is read when DO is high, the key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

## Output Data

1. KD1 to KD30.....Key data
   When a key matrix with up to 30 keys is formed using the KS1 to KS6 output pins and the KI1 to KI5 input pins, the key data corresponding to a given key will be 1 if that key is pressed. The table below lists that correspondence.

| Item | KI1 | KI2 | KI3 | KI4 | KI5 |
|---|---|---|---|---|---|
| KS1/S44 | KD1 | KD2 | KD3 | KD4 | KD5 |
| KS2/S45 | KD6 | KD7 | KD8 | KD9 | KD10 |
| KS3 | KD11 | KD12 | KD13 | KD14 | KD15 |
| KS4 | KD16 | KD17 | KD18 | KD19 | KD20 |
| KS5 | KD21 | KD22 | KD23 | KD24 | KD25 |
| KS6 | KD26 | KD27 | KD28 | KD29 | KD30 |

   When the output pins KS1/S44 and KS2/S45 are selected for segment output by the control data K0 and K1, the key data items KD1 to KD10 will be 0.

2. SA .....Sleep acknowledge data
   This output data is set according to the state when the key was pressed. If the LSI was in sleep mode, SA will be 1, and if the LSI was in normal mode, SA will be 0.

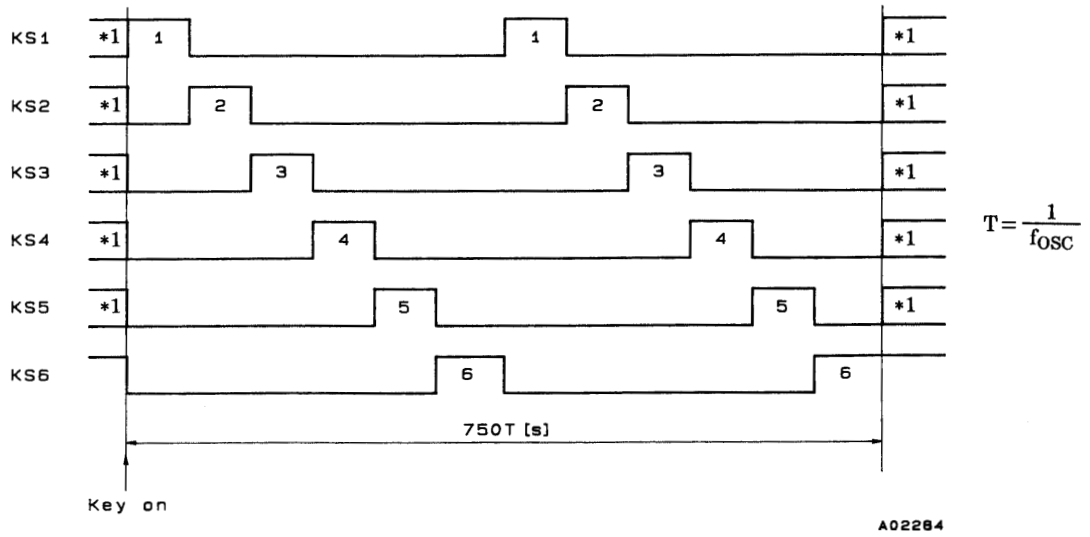
## Sleep Mode

When S0 or S1 in the control data is set to 1, the oscillator at the OSC pin will stop (it will restart if a key is pressed) and the segment and common outputs will all go to the low level. This reduces the LSI power dissipation. However, the S1/P1 to S4/P4 output pins can be used as general-purpose output ports even in sleep mode if selected for such use by the P0 and P1 control data bits.

## Key Scan Operation

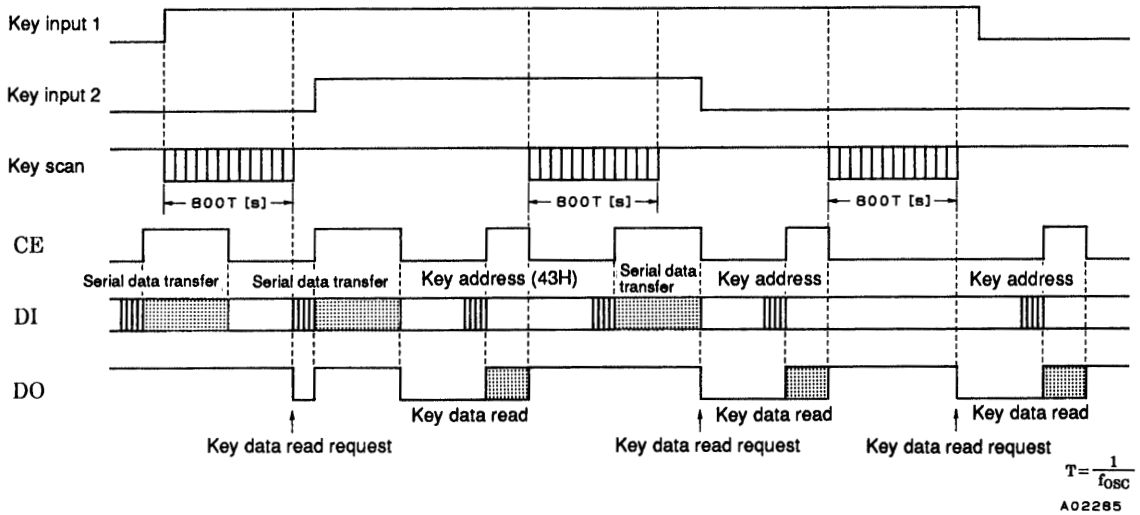
1. Key Scan Timing

   The key scan period is 375T [s]. The key scan is performed twice to reliably determine the key on/off states, and the LSI detects key data agreement. When the key data agrees, the LSI determines that a key has been pressed, and outputs a key read request (by setting DO low) 800T [s] after the key scan started. If a key is pressed again without the key data agreeing, a key scan is performed once more. Thus key on/off operations shorter than 800T [s] cannot be detected.



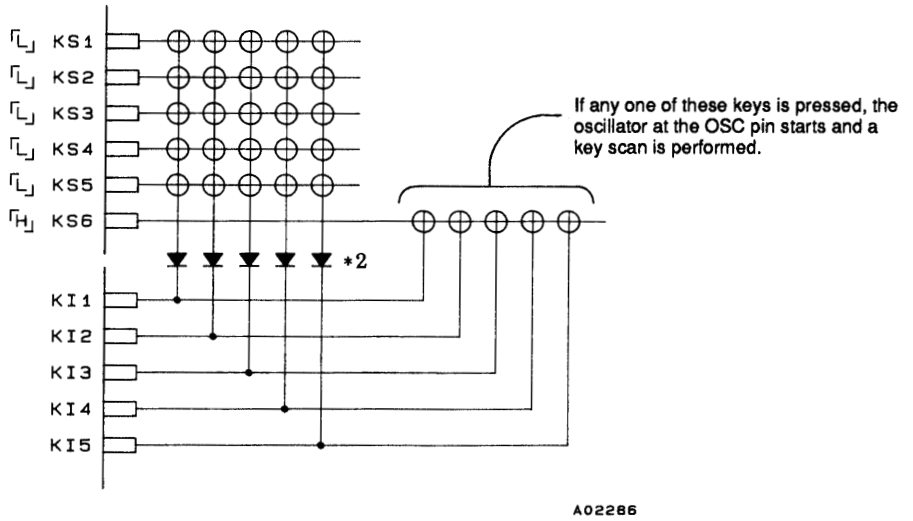

*1 The high or low states of these signals in sleep mode are determined by the S0 and S1 control data bits.

2. Key Scan during Normal Mode
   - The pins KS1 to KS6 are set high.
   - A key scan starts if any key is pressed, and the scan continues until all keys have been released. Multiple key presses can be recognized by determining if multiple key data bits have been set.
   - When a key has been pressed for 800T [s] (where $T = 1/f_{OSC}$) or longer, a key data read request (DO is set to low) is output to the controller. The controller acknowledges this request and reads the key data. However, DO will go high when CE is high during a serial data transfer.
   - After the controller has finished reading the key data, the LSI clears the key data read request (by setting DO high) and performs another key scan. Note that since DO is an open drain output, a pull-up resistor of between 1 and 10 kΩ is required.

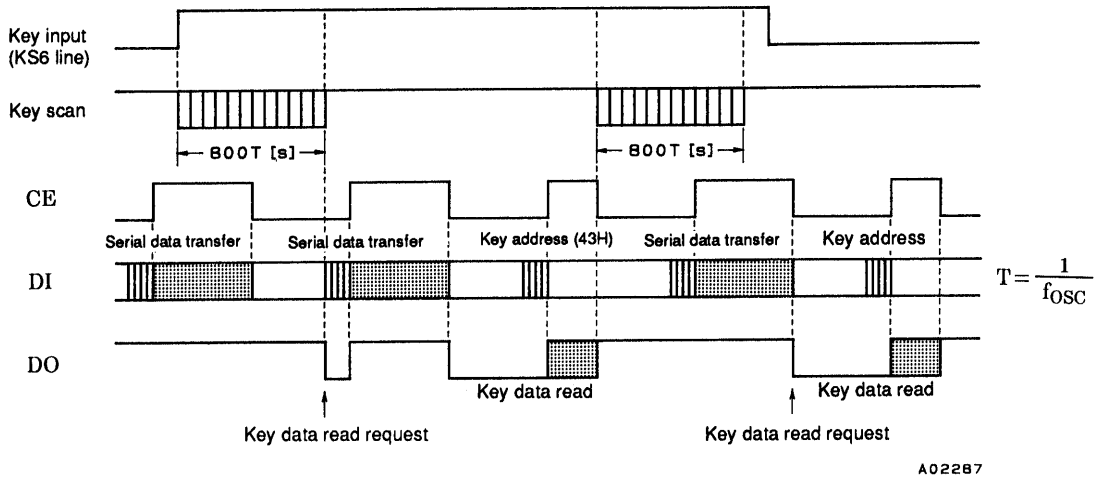


3. Key Scan during Sleep Mode
   - The pins KS1 to KS6 are set high or low according to the S0 and S1 control data bits. (See the description of the control data function for details.)
   - If a key for a line corresponding to one of the pins KS1 to KS6 which is high is pressed, the oscillator at the OSC pin starts and a key scan is performed. The key scan continues until all keys have been released. Multiple key presses can be recognized by determining if multiple key data bits have been set.
   - When a key has been pressed for 800T [s] (where $T = 1/f_{OSC}$) or longer, a key data read request (DO is set to low) is output to the controller. The controller acknowledges this request and reads the key data. However, DO will go high when CE is high during a serial data transfer.
   - After the controller has finished reading the key data, the LSI clears the key data read request (by setting DO high) and performs another key scan. Note that since DO is an open drain output, a pull-up resistor of between 1 and 10 kΩ is required.
   - Key scan example in sleep mode

   Example: Here S0 = 0 and S1 = 1 (This is a sleep in which only KS6 is high.)



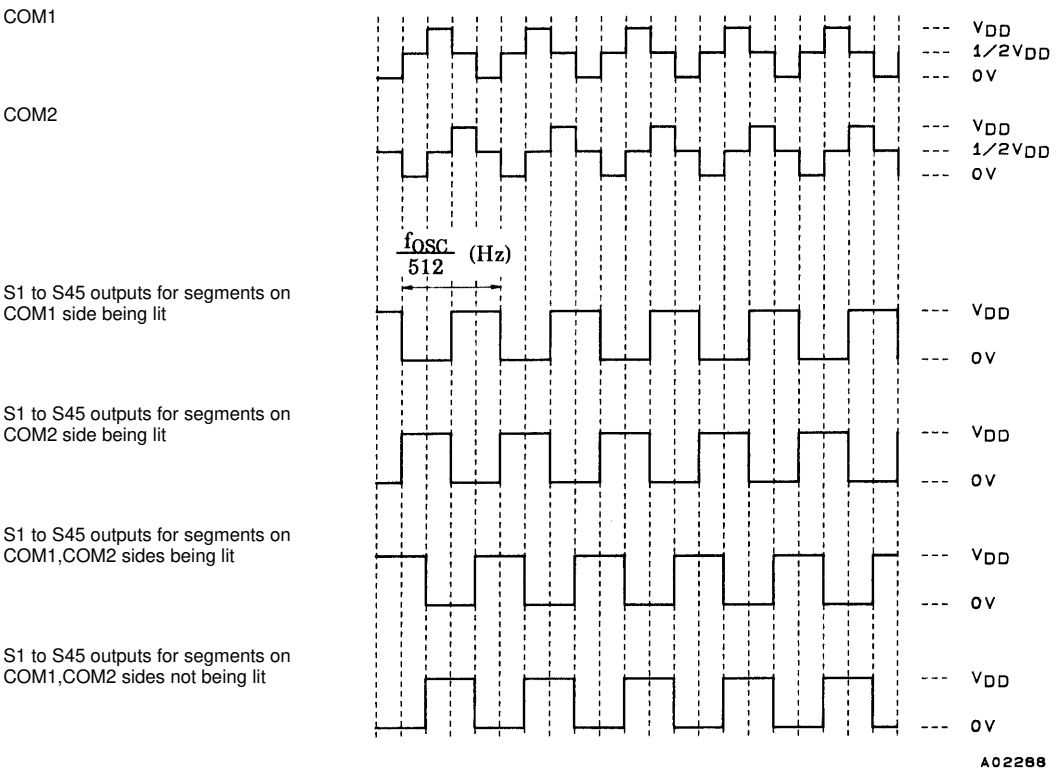

*2: These diodes are required to reliably recognize events in which three or more of the keys on the KS6 line are pressed at the same time.




## Multiple Key Presses

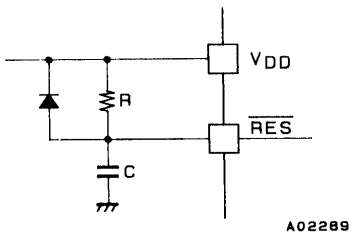
Without the insertion of additional diodes, the LC75852 supports key scan for double key presses in general, triple key presses of keys on the lines for input pins KI1 to KI5, and multiple key presses of keys on the lines for the output pins KS1 to KS6. However, if multiple key presses in excess of these limits occur, the LC75852 may recognize keys that were not pressed as having been pressed. Therefore, series diodes must be connected to each key.

## 1/2 Duty - 1/2 Bias LCD Drive Scheme




## $\overline{\text{RES}}$ and the Display Controller

Since the LSI internal data (D1 to D90 and the control data) is undefined when power is first applied, the output pins S1/P1 to S4/P4, S5 to S43, COM1, COM2, KS1/S44 and KS2/S45 should be held low by setting the $\overline{\text{RES}}$ pin low at the same time as power is applied. Then, meaningless displays at power on can be prevented by transferring data from the controller and setting $\overline{\text{RES}}$ high when that transfer has completed.



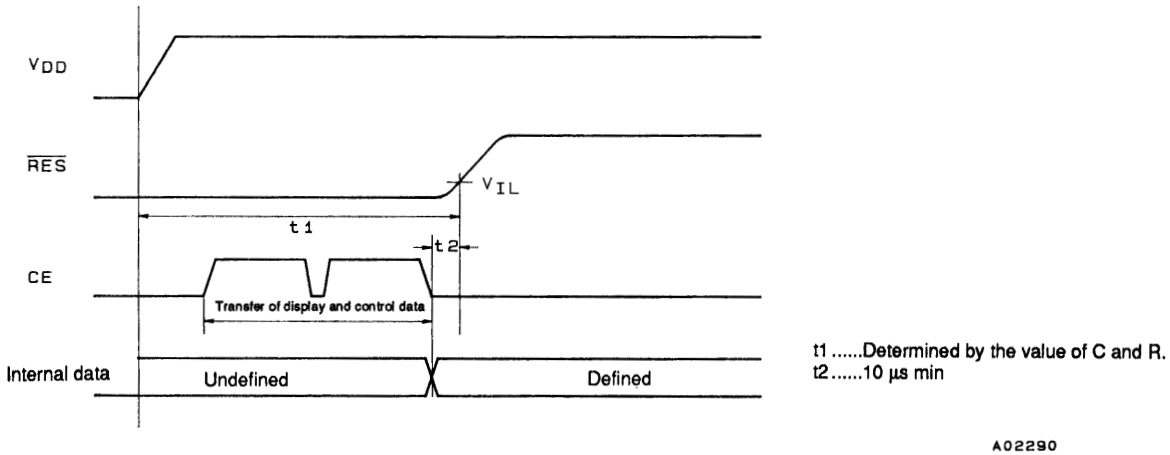




**Figure 2**

## Internal Block States during the Reset Period (when $\overline{RES}$ is low)

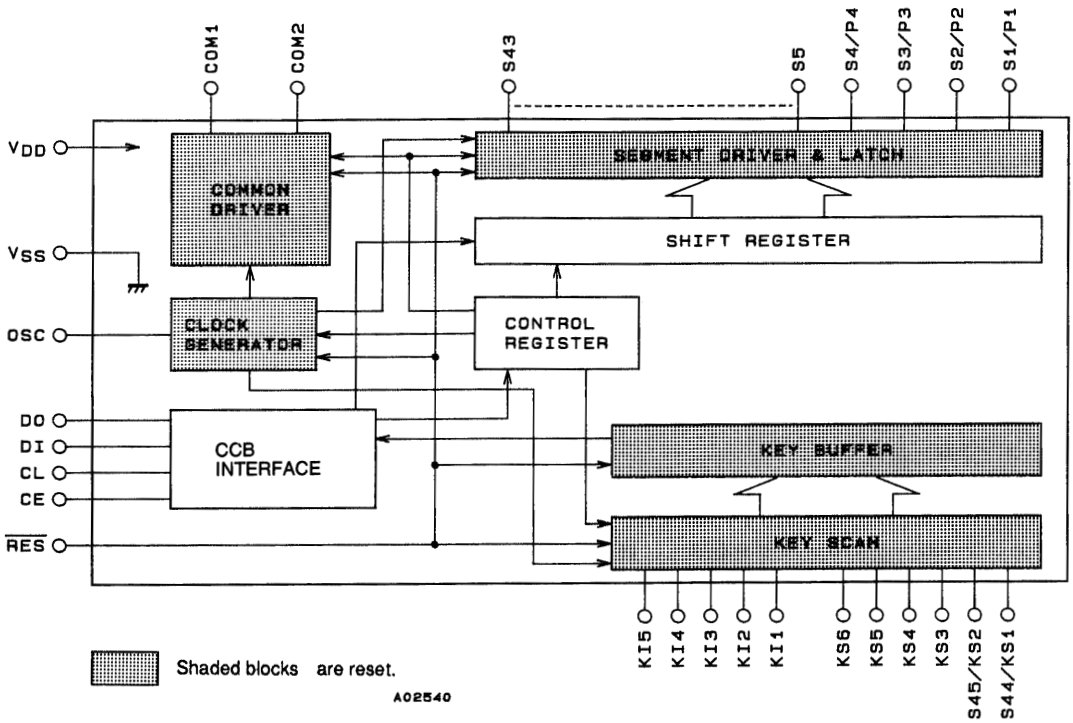
1. CLOCK GENERATOR
   Reset is applied and the basic clock stops. However, the state of the OSC pin (the normal or sleep state) is determined after the control data S0 and S1 has been sent.

2. COMMON DRIVER, SEGMENT DRIVER & LATCH
   Reset is applied and the display is turned off. However, display data can be input to the LATCH.

3. KEY SCAN
   Reset is applied and at the same time as the internal states are set to their initial states, the key scan operation is disabled.

4. KEY BUFFER
   Reset is applied and all the key data is set to the low level.

5. CCB INTERFACE, CONTROL REGISTER, SHIFT REGISTER
   To allow serial data transfers, reset is not applied to these circuits.



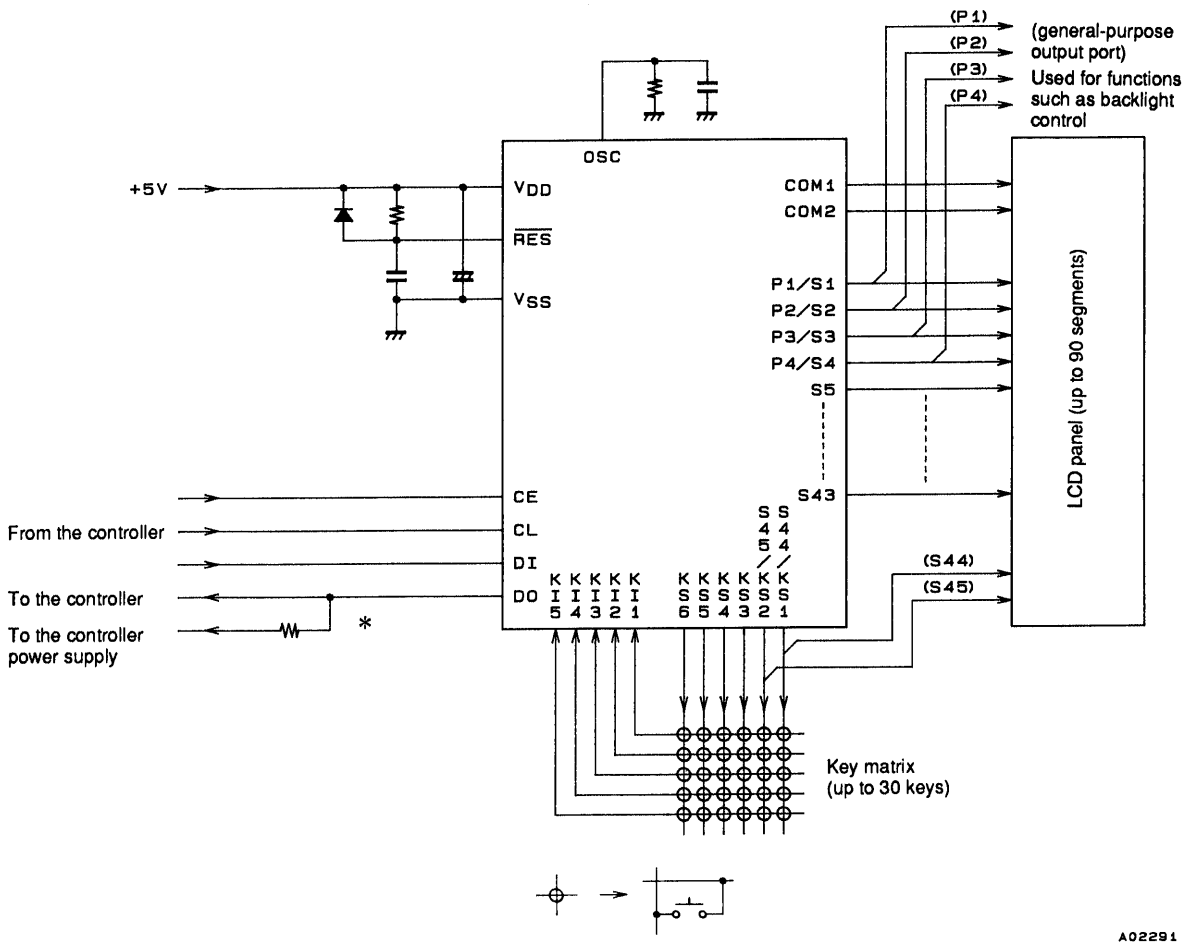

## Output Pin States during the Reset Period (when $\overline{RES}$ is low)

| Output pin | State during reset |
|---|---|
| S1/P1 to S4/P4 | L*3 |
| S5 to S43 | L |
| COM1, COM2 | L |
| KS1/S44, KS2/S45 | L*3 |
| KS3 to KS5 | X*4 |
| KS6 | H |
| DO | H*5 |

X: don't care

Note: 3. These output pins are forcibly set to the segment output mode and held low.
4. Immediately following power on, these output pins are undefined until the control data S0 and S1 has been sent.
5. Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10 kΩ is required. This pin is held high during the reset period even if key data is read.

## Sample Application Circuit



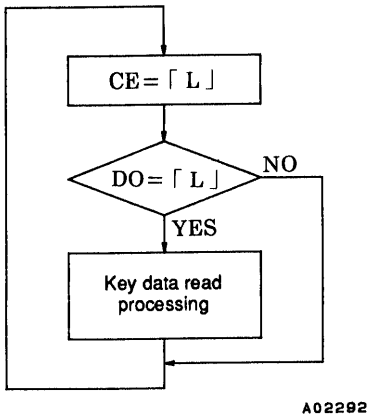

Note: * Since DO is an open-drain output, a pull-up resistor is required. Select a value (between 1 and 10 kΩ) that is appropriate for the capacitance of the external wiring so that the waveforms are not distorted.

## Notes on Controller Display Data Transfer

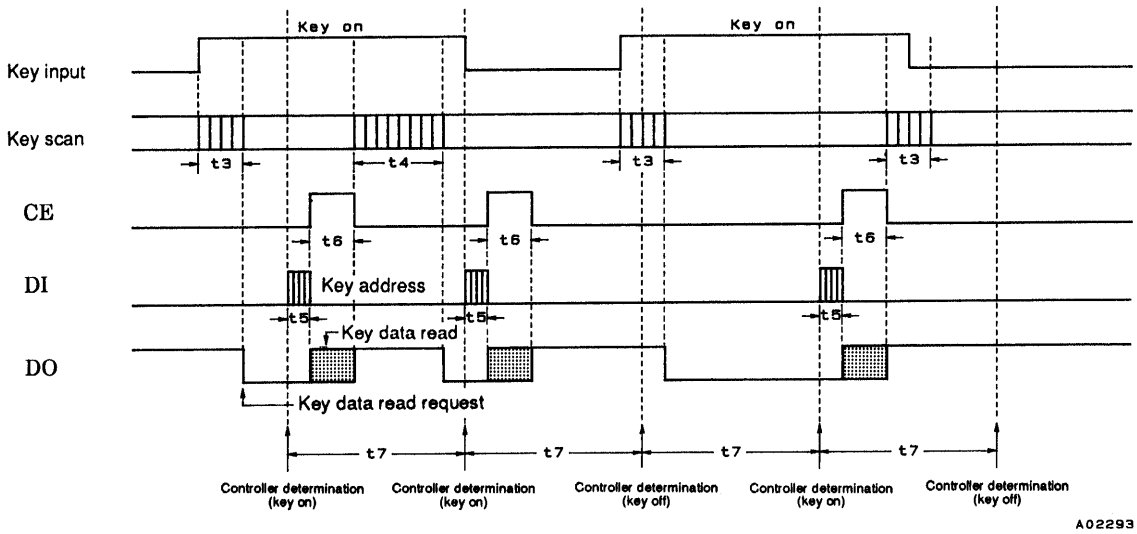
The LC75852 transfers the display data (D1 to D90) in two operations. To assure visual display quality, all the display data should be sent within a 30 ms or shorter period.

## Notes on Controller Key Data Read Techniques

1. Controller key data reading under timer control
   - Flowchart




   - Timing Chart




t3 .....Key scan execution time (800T [s]) when the key scan data for two key scans agrees
t4 .....Key scan execution time (1600T [s]) when the key scan data for two key scans does not agree and a key scan is executed again
t5 .....Key address (43H) transfer time
t6 .....Key data read time

$T = \frac{1}{f_{osc}}$

   - Description

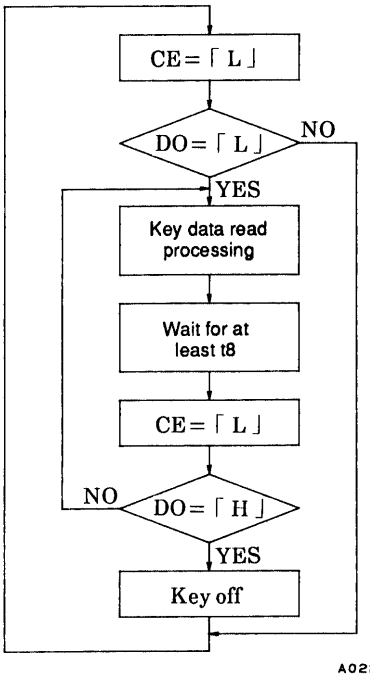
     When determining key on/off and reading key data, the controller must confirm the state of DO output when CE is low for each period t7. When DO is low, the controller recognizes that a key has been pressed and reads the key data.

     During this operation t7 must obey the following condition:

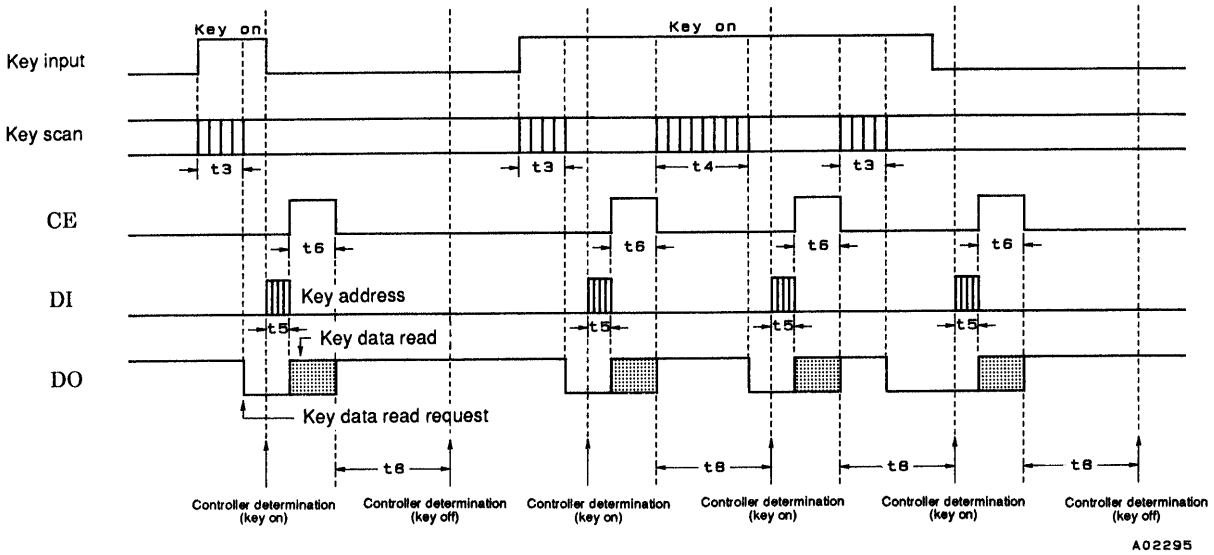
     $t7 > t5 + t6 + t4$

     If key data is read when DO is high, the key data (KD1 to KD30) and the sleep acknowledge data (SA) will be invalid.

2. Controller key data reading under interrupt control
   - Flowchart




   - Timing Chart




t3 .....Key scan execution time (800T [s]) when the key scan data for two key scans agrees
t4 .....Key scan execution time (1600T [s]) when the key scan data for two key scans does not agree and a key scan is executed again
t5 .....Key address (43H) transfer time
t6 .....Key data read time

$T = \frac{1}{f_{OSC}}$

- Description

  When determining key on/off and reading key data, the controller must confirm the state of DO output when CE is low. When DO is low, the controller recognizes that a key has been pressed and reads the key data. After the time t8, the next key on/off determination and reading key data must be confirmed by the state of DO output when CE is low. During this operation t8 must obey the following condition:

  t8 > t4

  If key data is read when DO is high, the key data (KD1 to KD30) and the sleep acknowledge data (SA) will be invalid.