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Preliminary

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS IC

LC75897PW — 1/3, 1/4-Duty General-Purpose LCD Display Driver

Overview

The LC75897PW is 1/3 duty and 1/4 duty general-purpose LCD display driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75897PW can drive an LCD with up to 512 segments directly. The LC75897PW can also control up to 8 general-purpose output ports. The LC75897PW has a built-in of up to three PWM output port channels, which enables to adjust the brightness of the RGB LED backlight.

Features

- Switching between 1/3 duty and 1/4 duty drive techniques under serial data control.
- Switching between 1/2 bias and 1/3 bias drive techniques under serial data control.
- Up to 387 segments for 1/3 duty drive and 512 segments for 1/4 duty drive can be displayed.
- Switching between the segment, general-purpose, PWM, and clock output ports can be controlled using serial data (up to 8 general-purpose output ports, up to 3-channel PWM output ports, and one clock output port).
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function.
- Serial data control of the frame frequency for common and segment output waveforms.
- Serial data control of switching between the RC oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without decoder intervention.
- Built-in display contrast adjustment circuit
- Independent V_{LCD} for the LCD driver block
- The $\overline{INH}$ pin can force the display to the off state.
- RC oscillator circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	-0.3 to +7.0	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	-0.3 to +7.0	V
	$V_{IN}2$	OSC	-0.3 to V_{DD}+0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$	-0.3 to V_{LCD}+0.3	
Output voltage	$V_{OUT}1$	OSC	-0.3 to V_{DD}+0.3	V
	$V_{OUT}2$	$V_{LCD}0$, S1 to S129, COM1 to COM4, P1 to P8	-0.3 to V_{LCD}+0.3	
Output current	$I_{OUT}1$	S1 to S129	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P8	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}, $V_{LCD}0$ = 0.70V_{LCD} to 0.95V_{LCD}	4.0		6.0	
		V_{LCD}, $V_{LCD}0$ = V_{LCD}	2.7		6.0	
Output voltage	$V_{LCD}0$	$V_{LCD}0$	2.7		V_{LCD}	V
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3$V_{LCD}0$	$V_{LCD}0$	V
	$V_{LCD}2$	$V_{LCD}2$		1/3$V_{LCD}0$	$V_{LCD}0$	
Input high-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.8V_{DD}		6.0	V
	$V_{IH}2$	OSC external clock operating mode	0.7V_{DD}		V_{DD}	
Input low-level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSC external clock operating mode	0		0.3V_{DD}	
Recommended external resistor for RC oscillation	R_{OSC}	OSC RC oscillator operating mode		10		kΩ
Recommended external capacitor for RC oscillation	C_{OSC}	OSC RC oscillator operating mode		470		pF
Guaranteed range of RC oscillation	f_{OSC}	OSC RC oscillator operating mode	150	300	600	kHz
External clock operating frequency	f_{CK}	OSC external clock operating mode [Figure 4]	150	300	600	kHz
External clock duty cycle	D_{CK}	OSC external clock operating mode [Figure 4]	30	50	70	%
Data setup time	tds	CL,DI [Figure 2],[Figure 3]	160			ns
Data hold time	tdh	CL,DI [Figure 2],[Figure 3]	160			ns
CE wait time	tcp	CE,CL [Figure 2],[Figure 3]	160			ns
CE setup time	tcs	CE,CL [Figure 2],[Figure 3]	160			ns
CE hold time	tch	CE,CL [Figure 2],[Figure 3]	160			ns
High-level clock pulse width	tϕH	CL [Figure 2],[Figure 3]	160			ns
Low-level clock pulse width	tϕL	CL [Figure 2],[Figure 3]	160			ns
Rise time	tr	CE, CL, DI [Figure 2],[Figure 3]		160		ns
Fall time	tf	CE, CL, DI [Figure 2],[Figure 3]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure 5],[Figure 6]	10			μs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.1V_{DD}$		V
Input high-level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 6.0V			5.0	µA
	$I_{IH}2$	OSC	$V_I = V_{DD}$ External clock operating mode			5.0	
Input low-level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0V	-5.0			µA
	$I_{IL}2$	OSC	V_I = 0V External clock operating mode	-5.0			
Output high-level voltage	$V_{OH}1$	S1 to S129	I_O = -20µA	$V_{LCD}0$-0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = -100µA	$V_{LCD}0$-0.9			
	$V_{OH}3$	P1 to P8	I_O = -1mA	V_{LCD}-0.9			
Output low-level voltage	$V_{OL}1$	S1 to S129	I_O = 20µA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O = 100µA			0.9	
	$V_{OL}3$	P1 to to P8	I_O = 1mA			0.9	
Output middle-level voltage *1	$V_{MID}1$	COM1 to COM4	1/2 bias, I_O = ±100µA	$1/2V_{LCD}0$ -0.9		$1/2V_{LCD}0$ +0.9	V
	$V_{MID}2$	S1 to S129	1/3 bias, I_O = ±20µA	$2/3V_{LCD}0$ -0.9		$2/3V_{LCD}0$ +0.9	
	$V_{MID}3$	S1 to S129	1/3 bias, I_O = ±20µA	$1/3V_{LCD}0$ -0.9		$1/3V_{LCD}0$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias, I_O = ±100µA	$2/3V_{LCD}0$ -0.9		$2/3V_{LCD}0$ +0.9	
	$V_{MID}5$	COM1 to COM4	1/3 bias, I_O = ±100µA	$1/3V_{LCD}0$ -0.9		$1/3V_{LCD}0$ +0.9	
Oscillator frequency	f_{OSC}	OSC	RC oscillator operating mode R_{OSC} = 10kΩ C_{OSC} = 470pF	210	300	390	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			10	µA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.0V, output open, f_{OSC} = 300kHz		700	1400	
	$I_{LCD}1$	V_{LCD}	Power-saving mode			15	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 6.0V, output open, 1/2 bias, f_{OSC} = 300kHz, $V_{LCD}0 = 0.70V_{LCD}$ to $0.95V_{LCD}$		600	1200	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 6.0V, output open, 1/2 bias, f_{OSC} = 300kHz, $V_{LCD}0 = V_{LCD}$		500	1000	
	$I_{LCD}4$	V_{LCD}	V_{LCD} = 6.0V, output open, 1/3 bias, f_{OSC} = 300kHz, $V_{LCD}0 = 0.70V_{LCD}$ to $0.95V_{LCD}$		450	900	
	$I_{LCD}5$	V_{LCD}	V_{LCD} = 6.0V, output open, 1/3 bias, f_{OSC} = 300kHz, $V_{LCD}0 = V_{LCD}$		350	700	

Note: *1 Excluding the bias voltage generation divider resistors built in the $V_{LCD}0$, $V_{LCD}1$, $V_{LCD}2$, and V_{SS}. (See Figure 1.)

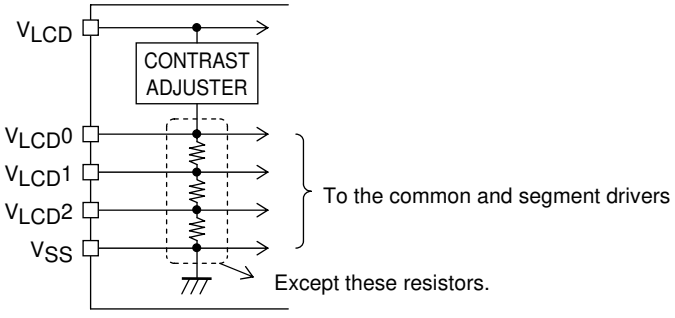


Figure 1

1. When CL is stopped at the low level

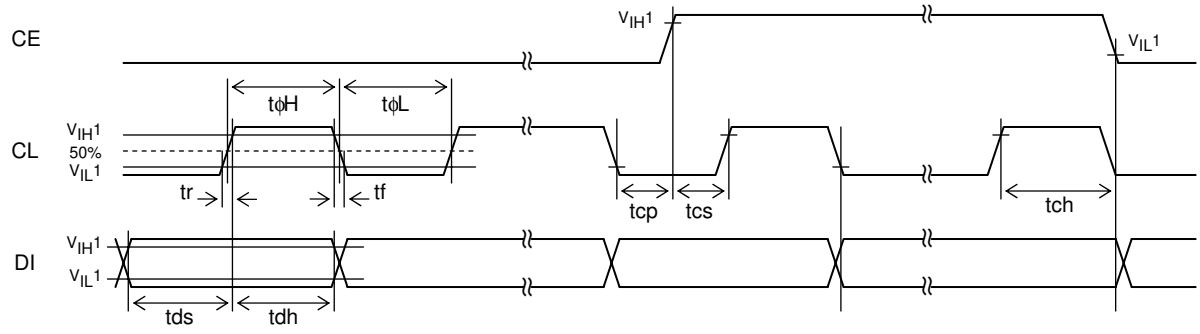


Figure 2

2. When CL is stopped at the high level

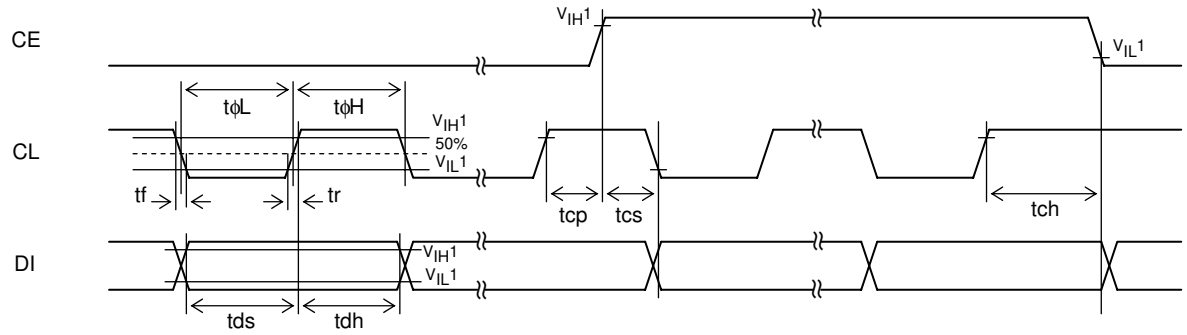
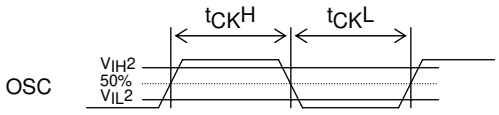


Figure 3

3. OSC pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \quad [kHz]$$

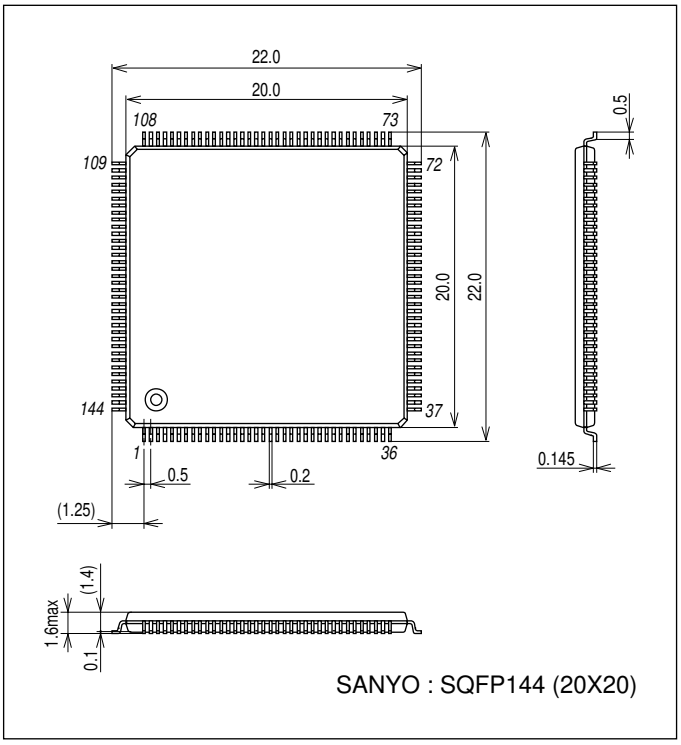
$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

Figure 4

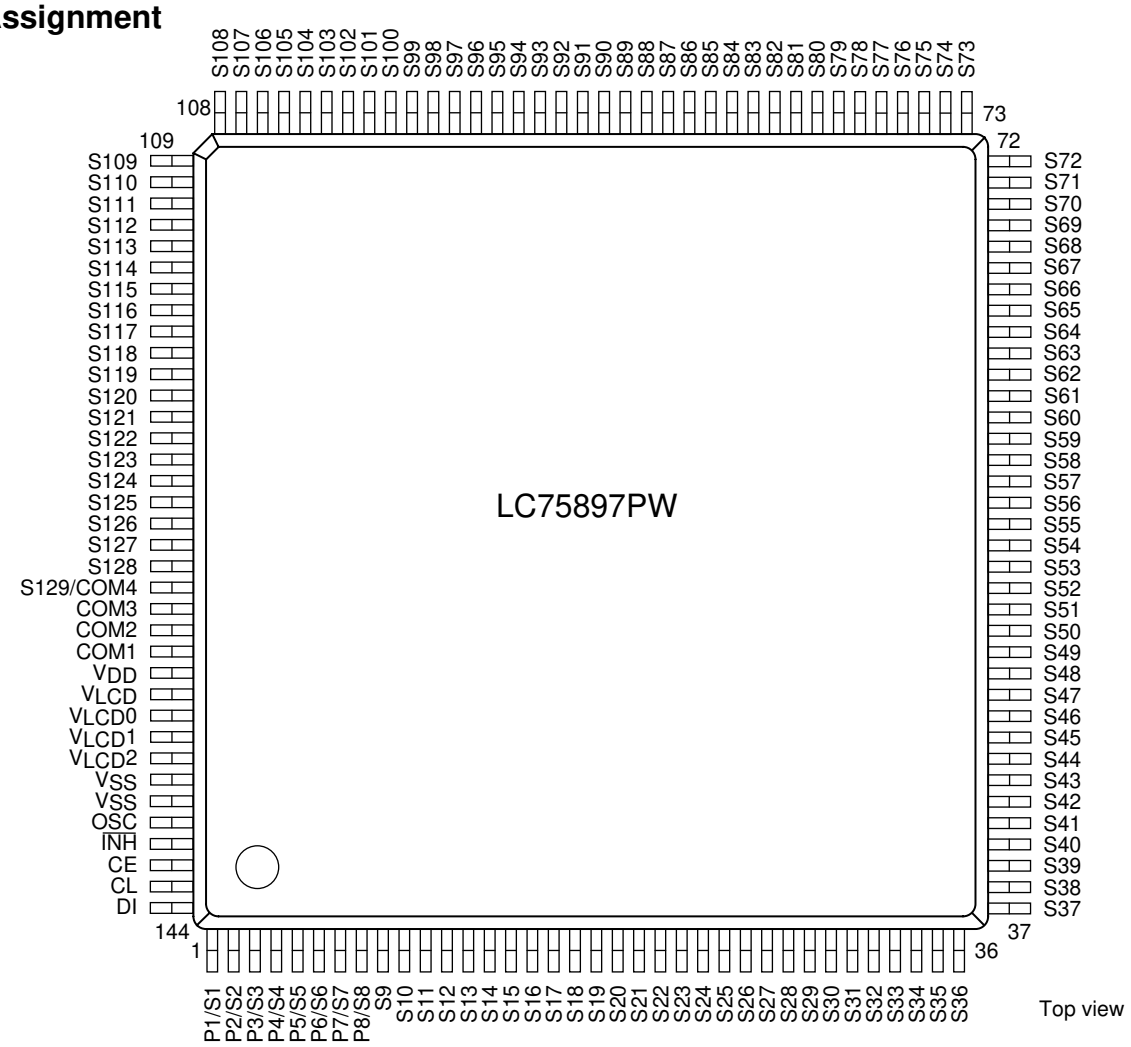
Package Dimensions

unit : mm (typ)

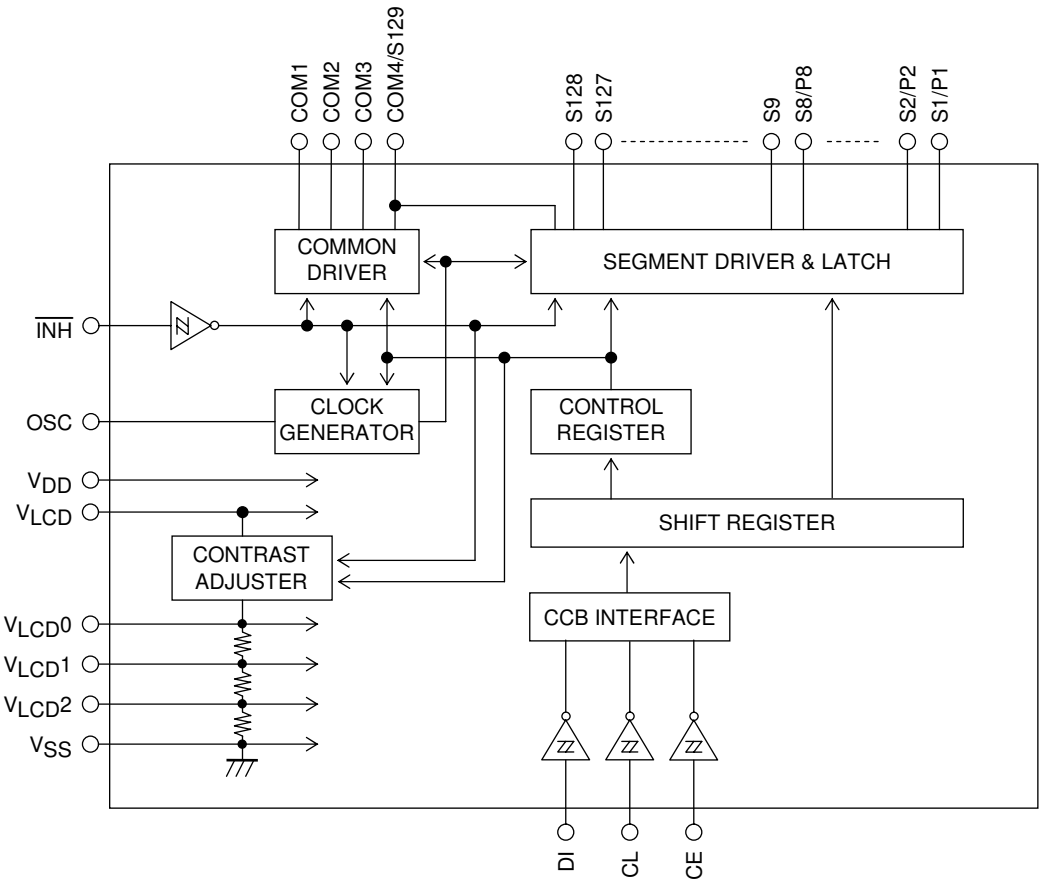
3214A



Pin Assignment



Block Diagram



Pin Functions

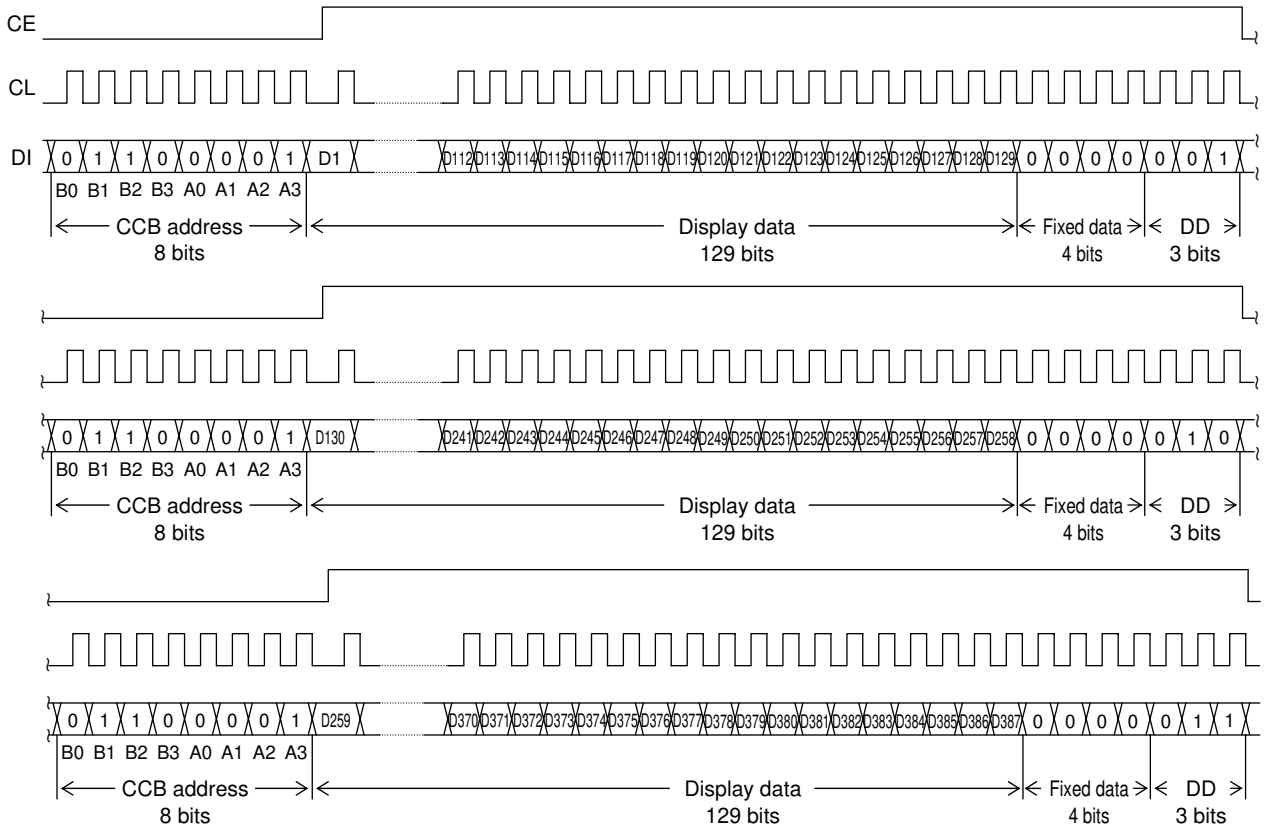
Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S8/P8 S9 to S128	1 to 8 9 to 128	Segment outputs for displaying the display data transferred by serial data input. Also, by the control data, S1/P1 to S3/P3 can be used as a general-purpose output port or PWM output port, while S4/P4 can be used as a general-purpose output port or clock output port and S5/P5 to S8/P8 can be used as a general-purpose output port.	-	O	OPEN
COM1 to COM3 COM4/S129	132 to 130 129	Common driver outputs. The frame frequency is fo [Hz]. The COM4/S129 pin can be used as a segment output in 1/3 duty.	-	O	OPEN
OSC	140	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can also be used as the external clock input pin as controlled by control data.	-	I/O	V_{DD}
CE CL DI	142 143 144	Serial data transfer inputs. These pins are connected to the control microprocessor. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ -	I I I	GND
$\overline{INH}$	141	Display off control input • $\overline{INH}$ = low (V_{SS}) ...Off S1/P1 to S8/P8 = low (V_{SS}) (These pins are forcibly set to the segment output port function and fixed at the V_{SS} level.) S9 to S128 = low (V_{SS}) COM1 to COM3 = low (V_{SS}) COM4/S129 = low (V_{SS}) OSC = "Z" (high impedance) RC oscillation stopped External clock input inhibited Display contrast adjustment circuit stopped • $\overline{INH}$ = high (V_{DD}) ...On RC oscillation enabled (RC oscillator operating mode) Enables external clock input (external clock operating mode). Display contrast adjustment circuit enabled Note that serial data transfers can be performed when the display is forced off by this pin.	L	I	GND
$V_{LCD}0$	135	LCD drive 3/3 bias voltage (high level) supply. This level can be modified using the display contrast adjustment circuit. However, note that $V_{LCD}0$ must be greater than or equal to 2.7V. Also, since this IC provides the built-in display contrast adjustment circuit, applications must not attempt to provide this level from external circuits.	-	O	OPEN
$V_{LCD}1$	136	LCD drive 2/3 bias voltage (middle level) supply. It is possible to supply the $2/3V_{LCD}0$ voltage to this pin externally. This pin must be shorted to $V_{LCD}2$ if 1/2 bias is used.	-	I	OPEN
$V_{LCD}2$	137	LCD drive 1/3 bias voltage (middle level) supply. It is possible to supply the $1/3V_{LCD}0$ voltage to this pin externally. This pin must be shorted to $V_{LCD}1$ if 1/2 bias is used.	-	I	OPEN
V_{DD}	133	Logic block power supply. Provide a voltage in the range 2.7 to 6.0V.	-	-	-
V_{LCD}	134	LCD driver block power supply. When $V_{LCD}0$ is between $0.70V_{LCD}$ and $0.95V_{LCD}$, supply a voltage in the range 4.0 to 6.0V. When $V_{LCD}0$ and V_{LCD} will be equal, supply a voltage in the range 2.7 to 6.0V.	-	-	-
V_{SS}	138,139	Ground pin. Connect to ground.	-	-	-

Serial Data Transfer Formats

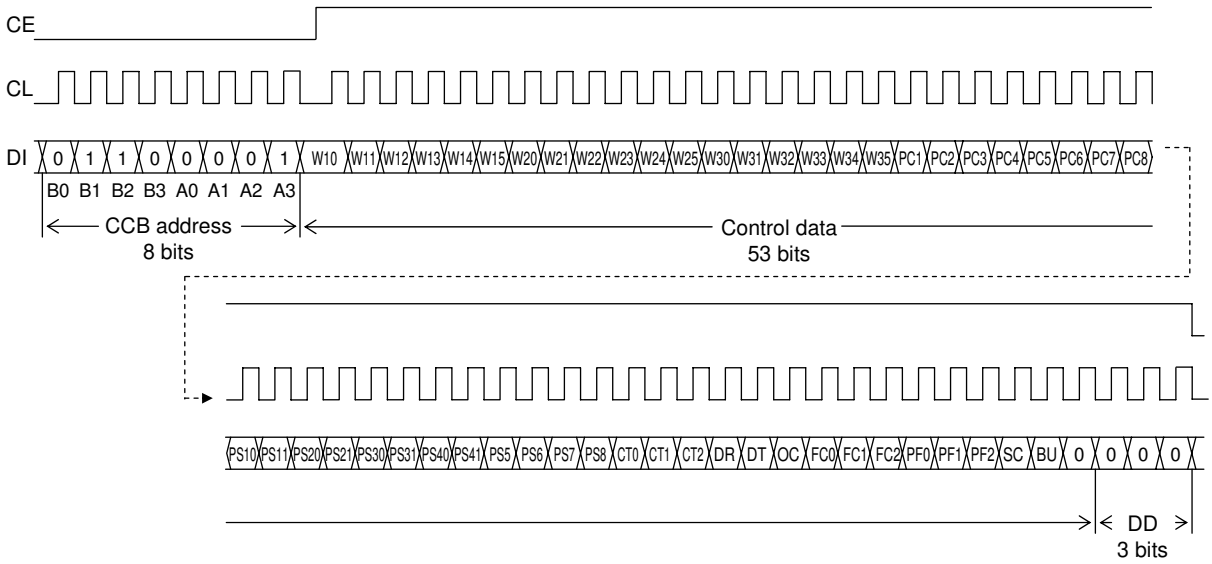
(1) 1/3 duty

1. When CL is stopped at the low level

• When the display data is transferred

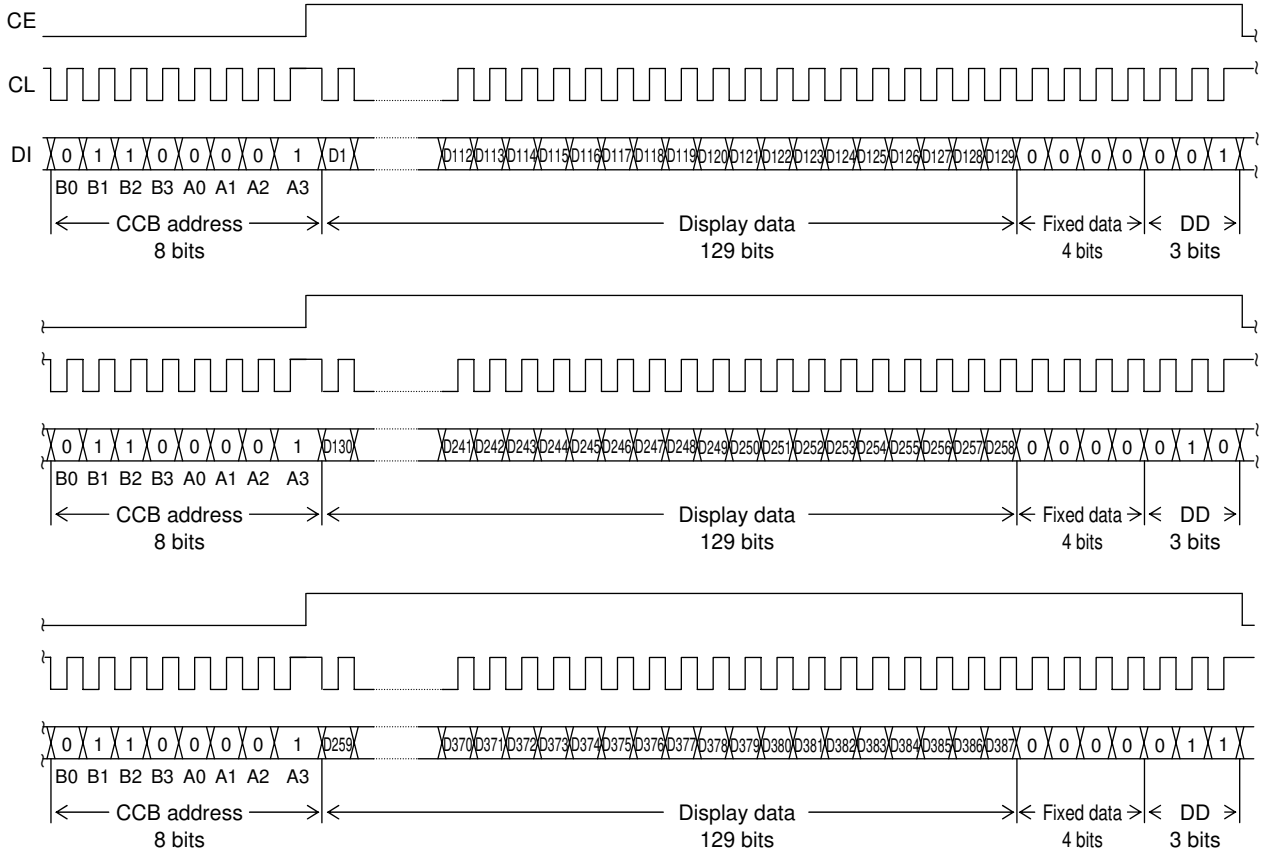


• When the control data is transferred

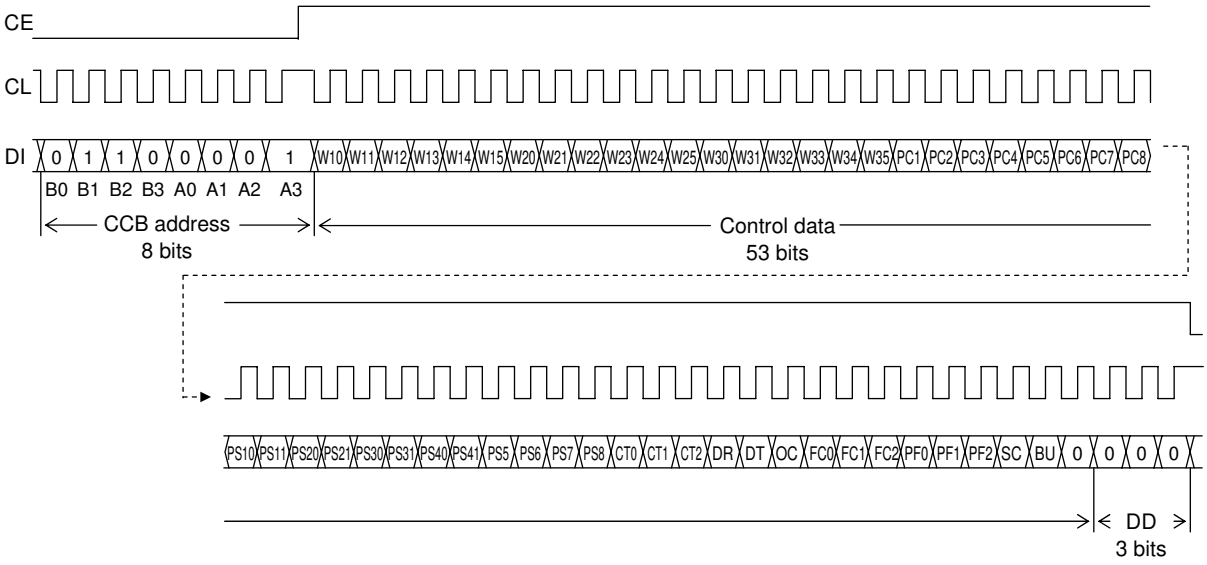


Note: DD is the direction data.

2. When CL is stopped at the high level
   - When the display data is transferred



• When the control data is transferred



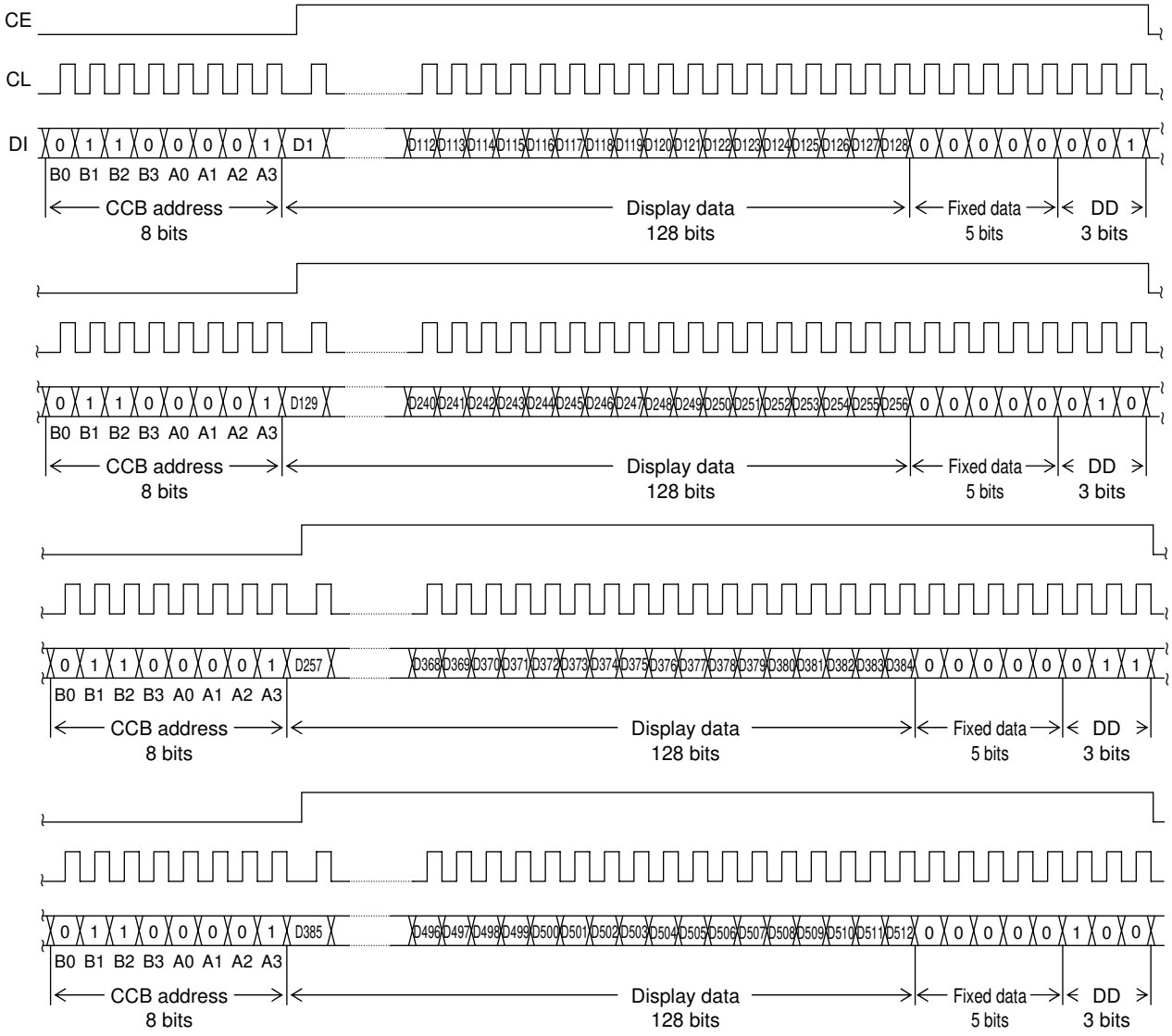
Note: DD is the direction data.

- CCB address ..... "86H"
- D1 to D387 ..... Display data
- W10 to W15, W20 to W25, W30 to W35
  ..... PWM data at PWM output ports
- PC1 to PC8 ..... General-purpose output port state setting control data
- PS10, PS11, PS20, PS21, PS30, PS31, PS40, PS41, PS5 to PS8
  ..... Segment output port/general-purpose output port/PWM output port/clock output port switching control data
- CT0 to CT2 ..... Display contrast setting control data
- DR ..... 1/2 bias drive or 1/3 bias drive switching control data
- DT ..... 1/3 duty drive or 1/4 duty drive switching control data
- OC ..... RC oscillator operating mode/external clock operating mode switching control data
- FC0 to FC2 ..... Common and segment output waveforms frame frequency setting control data
- PF0 to PF2 ..... PWM output waveforms frame frequency setting control data
- SC ..... Segments on/off control data
- BU ..... Normal mode/power-saving mode control data

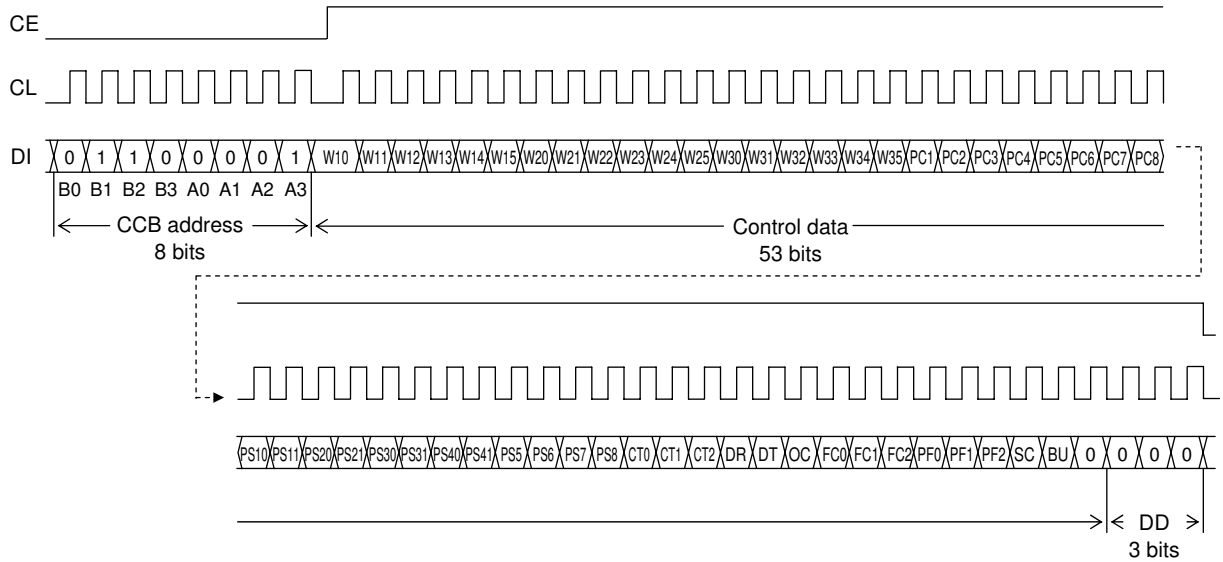
(2) 1/4 duty

1. When CL is stopped at the low level

• When the display data is transferred

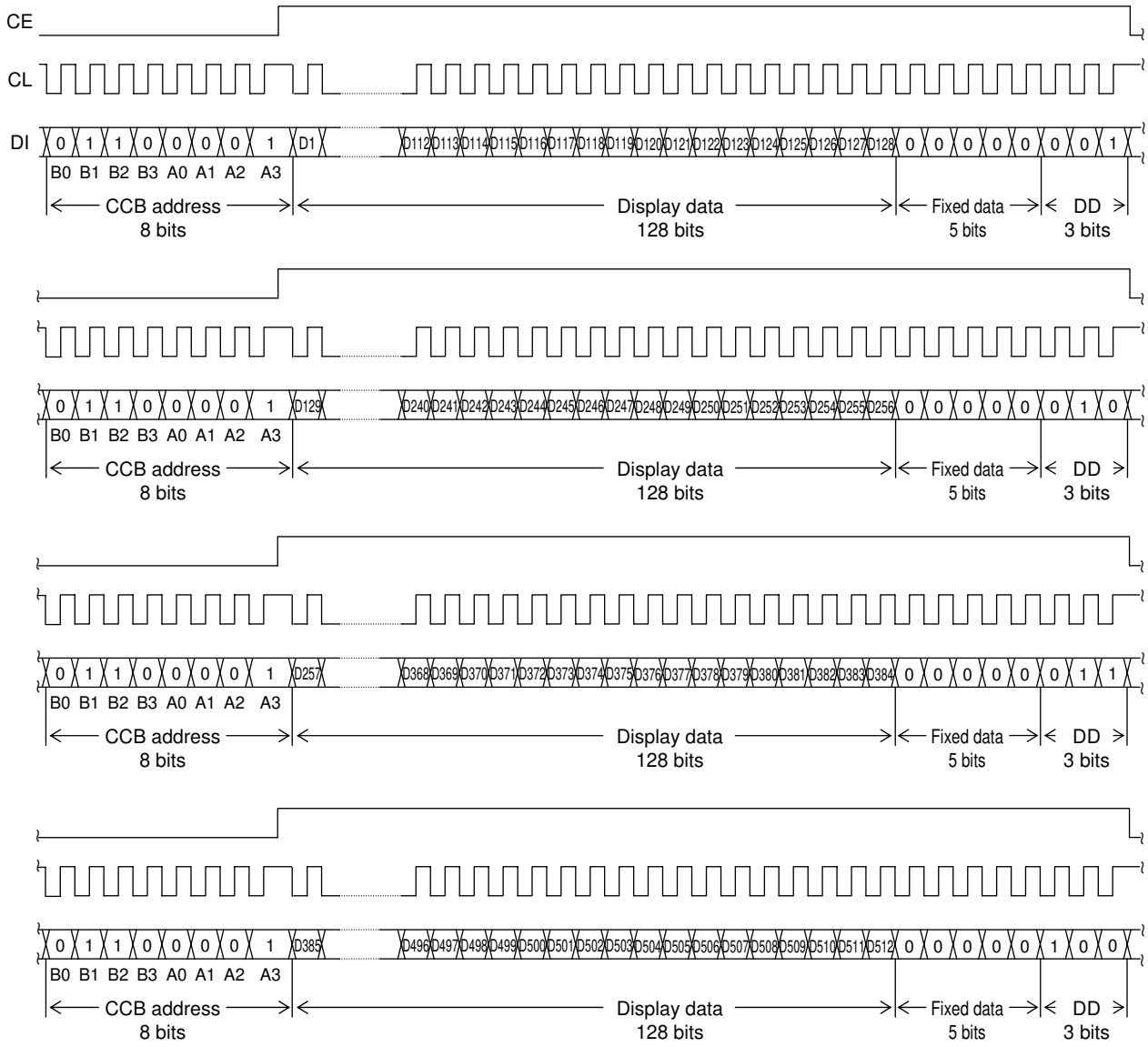


• When the control data is transferred

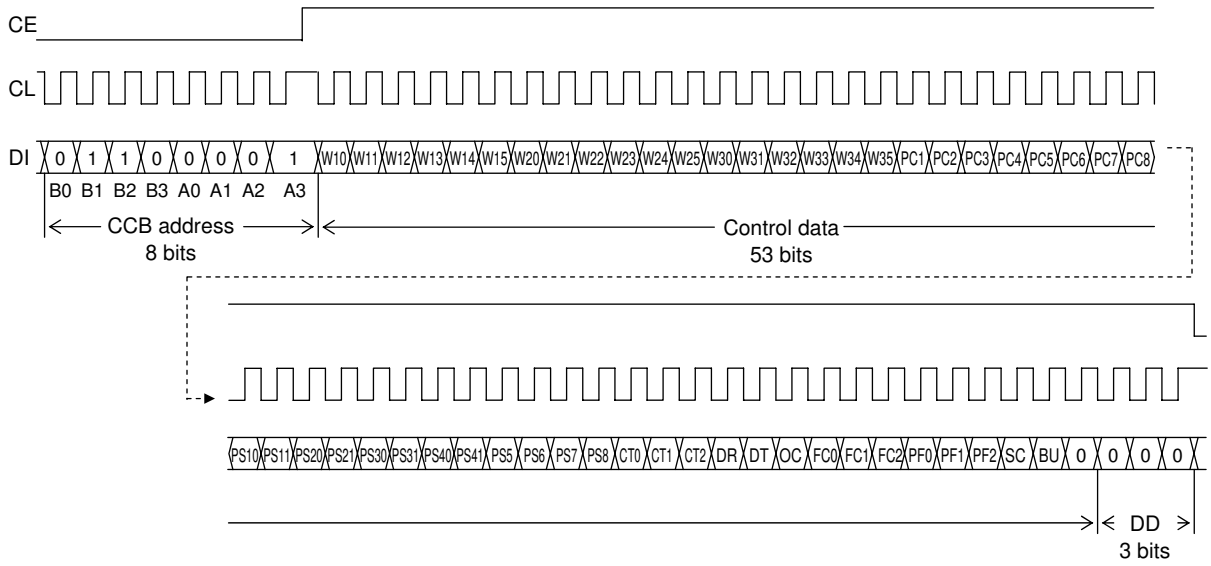


Note: DD is the direction data.

2. When CL is stopped at the high level
   • When the display data is transferred



• When the control data is transferred



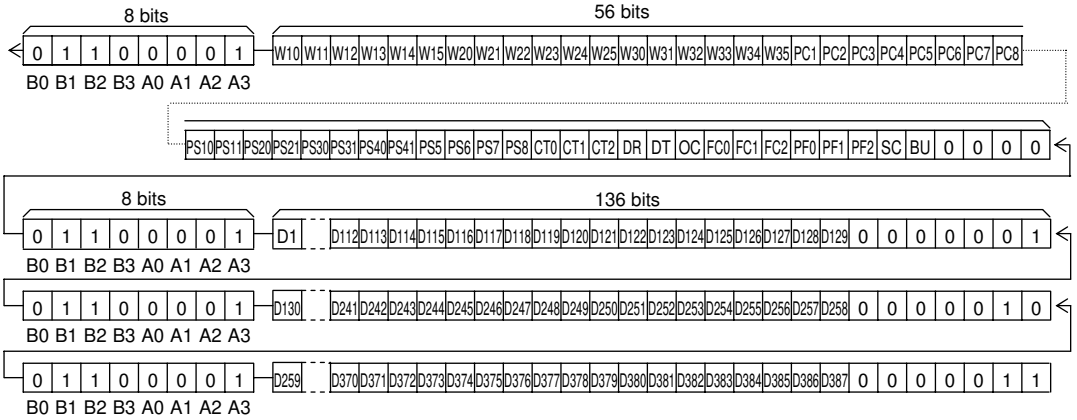
Note: DD is the direction data.

• CCB address ..... "86H"
• D1 to D512 ..... Display data
• W10 to W15, W20 to W25, W30 to W35
..... PWM data at PWM output ports
• PC1 to PC8 ..... General-purpose output port state setting control data
• PS10, PS11, PS20, PS21, PS30, PS31, PS40, PS41, PS5 to PS8
..... Segment output port/general-purpose output port/PWM output port/clock output port switching control data
• CT0 to CT2 ..... Display contrast setting control data
• DR ..... 1/2 bias drive or 1/3 bias drive switching control data
• DT ..... 1/3 duty drive or 1/4 duty drive switching control data
• OC ..... RC oscillator operating mode/external clock operating mode switching control data
• FC0 to FC2 ..... Common and segment output waveforms frame frequency setting control data
• PF0 to PF2 ..... PWM output waveforms frame frequency setting control data
• SC ..... Segments on/off control data
• BU ..... Normal mode/power-saving mode control data

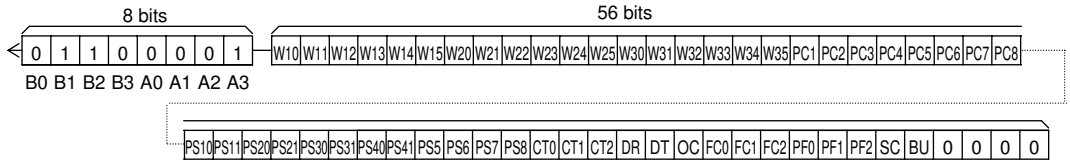
Serial Data Transfer Example

(1) 1/3 duty

- When 259 or more segments are used
  All 496 bits of serial data (including CCB addresses) must be sent.

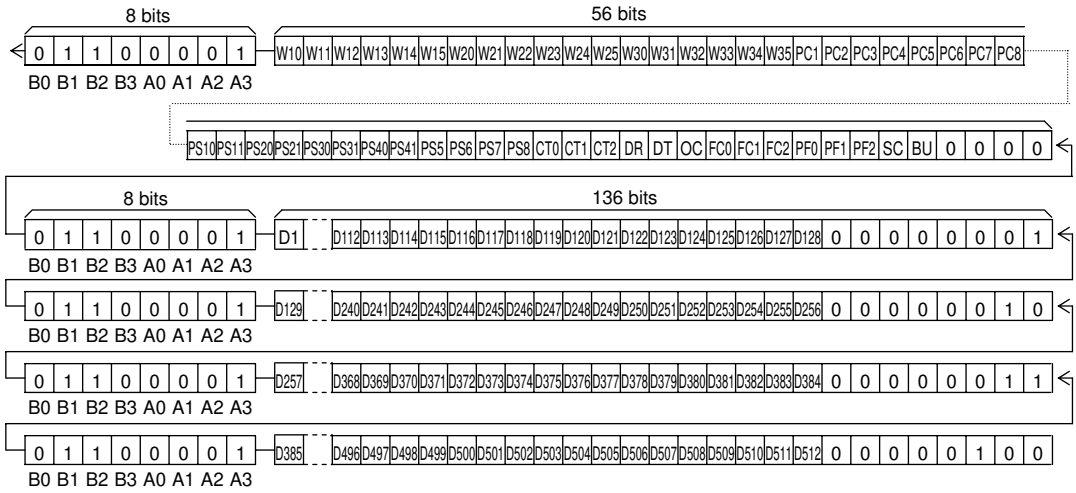


- When fewer than 259 segments are used
  Either 208 or 352 bits (including CCB addresses) of serial data may be sent, depending on the number of segments used. However, the serial data shown below (control data) must be sent.

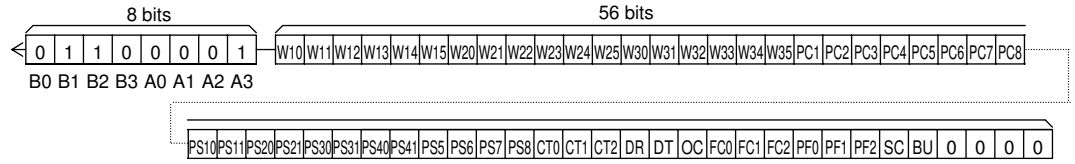


(2) 1/4 duty

- When 385 or more segments are used
  All 640 bits of serial data (including CCB addresses) must be sent.



- When fewer than 385 segments are used
  Either 208, 352 or 496 bits (including CCB addresses) of serial data may be sent, depending on the number of segments used. However, the serial data shown below (control data) must be sent.



Control Data Functions

(1) W10 to W15, W20 to W25, W30 to W35: PWM data at PWM output ports

This control data determines the pulse width of the PWM at PWM output ports P1/S1 to P3/S3.

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output port Pn
0	0	0	0	0	0	(1/64)×Tp
1	0	0	0	0	0	(2/64)×Tp
0	1	0	0	0	0	(3/64)×Tp
1	1	0	0	0	0	(4/64)×Tp
0	0	1	0	0	0	(5/64)×Tp
1	0	1	0	0	0	(6/64)×Tp
0	1	1	0	0	0	(7/64)×Tp
1	1	1	0	0	0	(8/64)×Tp
0	0	0	1	0	0	(9/64)×Tp
1	0	0	1	0	0	(10/64)×Tp
0	1	0	1	0	0	(11/64)×Tp
1	1	0	1	0	0	(12/64)×Tp
0	0	1	1	0	0	(13/64)×Tp
1	0	1	1	0	0	(14/64)×Tp
0	1	1	1	0	0	(15/64)×Tp
1	1	1	1	0	0	(16/64)×Tp
0	0	0	0	1	0	(17/64)×Tp
1	0	0	0	1	0	(18/64)×Tp
0	1	0	0	1	0	(19/64)×Tp
1	1	0	0	1	0	(20/64)×Tp
0	0	1	0	1	0	(21/64)×Tp
1	0	1	0	1	0	(22/64)×Tp
0	1	1	0	1	0	(23/64)×Tp
1	1	1	0	1	0	(24/64)×Tp
0	0	0	1	1	0	(25/64)×Tp
1	0	0	1	1	0	(26/64)×Tp
0	1	0	1	1	0	(27/64)×Tp
1	1	0	1	1	0	(28/64)×Tp
0	0	1	1	1	0	(29/64)×Tp
1	0	1	1	1	0	(30/64)×Tp
0	1	1	1	1	0	(31/64)×Tp
1	1	1	1	1	0	(32/64)×Tp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output port Pn
0	0	0	0	0	1	(33/64)×Tp
1	0	0	0	0	1	(34/64)×Tp
0	1	0	0	0	1	(35/64)×Tp
1	1	0	0	0	1	(36/64)×Tp
0	0	1	0	0	1	(37/64)×Tp
1	0	1	0	0	1	(38/64)×Tp
0	1	1	0	0	1	(39/64)×Tp
1	1	1	0	0	1	(40/64)×Tp
0	0	0	1	0	1	(41/64)×Tp
1	0	0	1	0	1	(42/64)×Tp
0	1	0	1	0	1	(43/64)×Tp
1	1	0	1	0	1	(44/64)×Tp
0	0	1	1	0	1	(45/64)×Tp
1	0	1	1	0	1	(46/64)×Tp
0	1	1	1	0	1	(47/64)×Tp
1	1	1	1	0	1	(48/64)×Tp
0	0	0	0	1	1	(49/64)×Tp
1	0	0	0	1	1	(50/64)×Tp
0	1	0	0	1	1	(51/64)×Tp
1	1	0	0	1	1	(52/64)×Tp
0	0	1	0	1	1	(53/64)×Tp
1	0	1	0	1	1	(54/64)×Tp
0	1	1	0	1	1	(55/64)×Tp
1	1	1	0	1	1	(56/64)×Tp
0	0	0	1	1	1	(57/64)×Tp
1	0	0	1	1	1	(58/64)×Tp
0	1	0	1	1	1	(59/64)×Tp
1	1	0	1	1	1	(60/64)×Tp
0	0	1	1	1	1	(61/64)×Tp
1	0	1	1	1	1	(62/64)×Tp
0	1	1	1	1	1	(63/64)×Tp
1	1	1	1	1	1	(64/64)×Tp

Note: Wn0 to Wn5 (n = 1 to 3): PWM data at output pins S1/P1 to S3/P3

$$Tp = \frac{1}{fp}$$

(2) PC1 to PC8: General-purpose output port state setting control data

This control data is used to set the high/low state of general-purpose output ports P1 to P8.

Output pins	P1	P2	P3	P4	P5	P6	P7	P8
Control data	PC1	PC2	PC3	PC4	PC5	PC6	PC7	PC8

Note: PCn = 1: The output pin Pn is set high (V_{LCD}) (n = 1 to 8).

PCn = 0: The output pin Pn is set low (V_{SS}) (n = 1 to 8).

For example, if output pins S4/P4 and S5/P5 are selected as general-purpose output ports, setting PC4 to 1 and PC5 to 0 causes the output pin P4 to be set high (V_{LCD}) and P5 to be set low (V_{SS}).

(3) PS10, PS11, PS20, PS21, PS30, PS31, PS40, PS41, PS5 to PS8: Segment output port/general-purpose output port/PWM output port/clock output port switching control data
This control data is used to set the state of output pins S1/P1 to S8/P8.

PS10 and PS11: Output pin (S1/P1) state settings

PS10	PS11	Output pin (S1/P1) state
0	0	Segment output port (S1)
1	0	General-purpose output port (P1)
0	1	PWM output port (P1)

PS20 and PS21: Output pin (S2/P2) state settings

PS20	PS21	Output pin (S2/P2) state
0	0	Segment output port (S2)
1	0	General-purpose output port (P2)
0	1	PWM output port (P2)

PS30 and PS31: Output pin (S3/P3) state settings

PS30	PS31	Output pin (S3/P3) state
0	0	Segment output port (S3)
1	0	General-purpose output port (P3)
0	1	PWM output port (P3)

PS40 and PS41: Output pin (S4/P4) state settings

PS40	PS41	Output pin (S4/P4) state
0	0	Segment output port (S4)
1	0	General-purpose output port (P4)
0	1	Clock output port (P4) (clock frequency fosc/2, $f_{CK}/2$)
1	1	Clock output port (P4) (clock frequency fosc/8, $f_{CK}/8$)

PS5: Output pin (S5/P5) state settings

PS5	Output pin (S5/P5) state
0	Segment output port (S5)
1	General-purpose output port (P5)

PS6: Output pin (S6/P6) state settings

PS6	Output pin (S6/P6) state
0	Segment output port (S6)
1	General-purpose output port (P6)

PS7: Output pin (S7/P7) state settings

PS7	Output pin (S7/P7) state
0	Segment output port (S7)
1	General-purpose output port (P7)

PS8: Output pin (S8/P8) state settings

PS8	Output pin (S8/P8) state
0	Segment output port (S8)
1	General-purpose output port (P8)

For example, if PS10 and PS11 are set to 0 and 1 respectively, PS20 and PS21 to 0 and 1 respectively, PS30 and PS31 to 0 and 1 respectively, PS40 and PS41 to 1 and 0 respectively, PS5 to 1, PS6 to 1, PS7 to 0, and PS8 to 0, the output pins S1/P1 to S3/P3 are selected as PWM output ports, the output pins S4/P4 to S6/P6 as general-purpose output ports, and the output pins S7/P7 and S8/P8 as segment output ports.

(4) CT0 to CT2: Display contrast setting control data
This control data is used to set the display contrast.

CT0 to CT2: Display contrast settings (7 steps)

CT0	CT1	CT2	Level of LCD drive bias 3/3 voltage power supply $V_{LCD}0$
0	0	0	$1.00V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times0)$
1	0	0	$0.95V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times1)$
0	1	0	$0.90V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times2)$
1	1	0	$0.85V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times3)$
0	0	1	$0.80V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times4)$
1	0	1	$0.75V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times5)$
0	1	1	$0.70V_{LCD} = V_{LCD}$- $(0.05V_{LCD}\times6)$

Note that although the contrast of the display can be adjusted by running the internal display contrast adjustment circuit, it is also possible to adjust it by changing the voltage level on the LCD driver block power supply V_{LCD} pin. However, $V_{LCD}0$ must always be greater than or equal to 2.7V.

(5) DR: 1/2 bias drive or 1/3 bias drive switching control data
This control data bit selects either 1/2 bias drive or 1/3 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

(6) DT: 1/3 duty drive or 1/4 duty drive switching control data

This control data bit selects either 1/3 duty drive or 1/4 duty drive.

DT	Duty drive scheme	Output pin state (COM4/S129)
0	1/4 duty drive	COM4
1	1/3 duty drive	S129

Note: COM4: Common output
S129: Segment output

(7) OC: RC oscillator operating mode/external clock operating mode switching control data

This control data bit selects either RC oscillator operating mode or external clock operating mode.

OC	OSC pin function
0	RC oscillator operating mode
1	External clock operating mode

Note: When selecting the RC oscillator operating mode, be sure to connect an external resistor Rosc and an external capacitor Cosc to the OSC pin.

(8) FC0 to FC2: Common and segment output waveforms frame frequency setting control data

This control data bits set the frame frequency for the common and segment output waveforms.

Control data			Common/segment output waveform frame frequency fo [Hz]
FC0	FC1	FC2	
0	0	0	fosc/6144, f_{CK}/6144
1	0	0	fosc/4608, f_{CK}/4608
0	1	0	fosc/3072, f_{CK}/3072
1	1	0	fosc/2304, f_{CK}/2304
0	0	1	fosc/1536, f_{CK}/1536

(9) PF0 to PF2: PWM output waveforms frame frequency setting control data

This control data bits set the frame frequency for the PWM output waveforms.

Control data			PWM output waveform frame frequency fp [Hz]
PF0	PF1	PF2	
0	0	0	fosc/1536, f_{CK}/1536
1	0	0	fosc/1408, f_{CK}/1408
0	1	0	fosc/1280, f_{CK}/1280
1	1	0	fosc/1152, f_{CK}/1152
0	0	1	fosc/1024, f_{CK}/1024
1	0	1	fosc/896, f_{CK}/896
0	1	1	fosc/768, f_{CK}/768
1	1	1	fosc/640, f_{CK}/640

(10) SC: Segments on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that the segments are turned off by setting SC to 1, the segments are turned off by outputing segment off waveforms from the segment output pins.

(11) BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power save mode The LC75897PW stops the oscillation at the OSC pin if it is set up for the RC oscillator operating mode (OC = 0) and stops receiving the external clock if it is set up for the external clock operating mode (OC = 1). The IC also sets the common and segment output pins to the V_{SS} level. The output pins S1/P1 to S8/P8, however, remain available as general-purpose output ports as configured by control data bits PS10, PS11, PS20, PS21, PS30, PS31, PS40, PS41, and PS5 to PS8 (not available as PWM output or clock output ports).

Display Data to Segment Output Pin Correspondence

1. 1/3 duty

Segment Output pins	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5/P5	D13	D14	D15
S6/P6	D16	D17	D18
S7/P7	D19	D20	D21
S8/P8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129

Segment Output pins	COM1	COM2	COM3
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189
S64	D190	D191	D192
S65	D193	D194	D195
S66	D196	D197	D198
S67	D199	D200	D201
S68	D202	D203	D204
S69	D205	D206	D207
S70	D208	D209	D210
S71	D211	D212	D213
S72	D214	D215	D216
S73	D217	D218	D219
S74	D220	D221	D222
S75	D223	D224	D225
S76	D226	D227	D228
S77	D229	D230	D231
S78	D232	D233	D234
S79	D235	D236	D237
S80	D238	D239	D240
S81	D241	D242	D243
S82	D244	D245	D246
S83	D247	D248	D249
S84	D250	D251	D252
S85	D253	D254	D255
S86	D256	D257	D258

Segment Output pins	COM1	COM2	COM3
S87	D259	D260	D261
S88	D262	D263	D264
S89	D265	D266	D267
S90	D268	D269	D270
S91	D271	D272	D273
S92	D274	D275	D276
S93	D277	D278	D279
S94	D280	D281	D282
S95	D283	D284	D285
S96	D286	D287	D288
S97	D289	D290	D291
S98	D292	D293	D294
S99	D295	D296	D297
S100	D298	D299	D300
S101	D301	D302	D303
S102	D304	D305	D306
S103	D307	D308	D309
S104	D310	D311	D312
S105	D313	D314	D315
S106	D316	D317	D318
S107	D319	D320	D321
S108	D322	D323	D324
S109	D325	D326	D327
S110	D328	D329	D330
S111	D331	D332	D333
S112	D334	D335	D336
S113	D337	D338	D339
S114	D340	D341	D342
S115	D343	D344	D345
S116	D346	D347	D348
S117	D349	D350	D351
S118	D352	D353	D354
S119	D355	D356	D357
S120	D358	D359	D360
S121	D361	D362	D363
S122	D364	D365	D366
S123	D367	D368	D369
S124	D370	D371	D372
S125	D373	D374	D375
S126	D376	D377	D378
S127	D379	D380	D381
S128	D382	D383	D384
COM4/S129	D385	D386	D387

Note: This applies to the case where the S1/P1 to S8/P8, and COM4/S129 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data			Segment output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are off.
0	0	1	The LCD segment corresponding to COM3 is on.
0	1	0	The LCD segment corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM2 and COM3 are on.
1	0	0	The LCD segment corresponding to COM1 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1, COM2, and COM3 are on.

2. 1/4 duty

Segment Output pins	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5/P5	D17	D18	D19	D20
S6/P6	D21	D22	D23	D24
S7/P7	D25	D26	D27	D28
S8/P8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144

Segment Output pins	COM1	COM2	COM3	COM4
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	D267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276
S70	D277	D278	D279	D280
S71	D281	D282	D283	D284
S72	D285	D286	D287	D288

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Segment Output pins	COM1	COM2	COM3	COM4
S73	D289	D290	D291	D292
S74	D293	D294	D295	D296
S75	D297	D298	D299	D300
S76	D301	D302	D303	D304
S77	D305	D306	D307	D308
S78	D309	D310	D311	D312
S79	D313	D314	D315	D316
S80	D317	D318	D319	D320
S81	D321	D322	D323	D324
S82	D325	D326	D327	D328
S83	D329	D330	D331	D332
S84	D333	D334	D335	D336
S85	D337	D338	D339	D340
S86	D341	D342	D343	D344
S87	D345	D346	D347	D348
S88	D349	D350	D351	D352
S89	D353	D354	D355	D356
S90	D357	D358	D359	D360
S91	D361	D362	D363	D364
S92	D365	D366	D367	D368
S93	D369	D370	D371	D372
S94	D373	D374	D375	D376
S95	D377	D378	D379	D380
S96	D381	D382	D383	D384
S97	D385	D386	D387	D388
S98	D389	D390	D391	D392
S99	D393	D394	D395	D396
S100	D397	D398	D399	D400

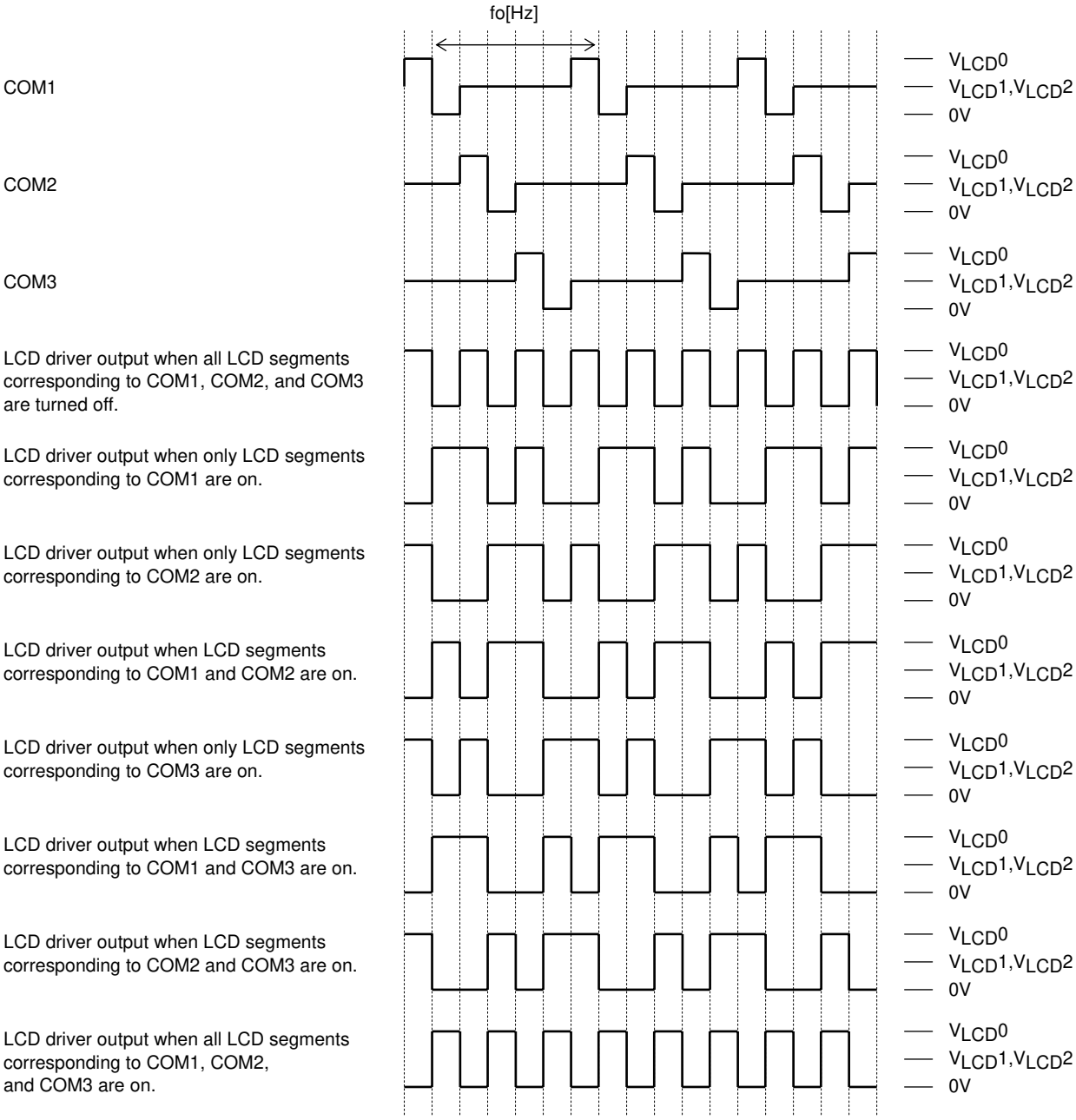
Segment Output pins	COM1	COM2	COM3	COM4
S101	D401	D402	D403	D404
S102	D405	D406	D407	D408
S103	D409	D410	D411	D412
S104	D413	D414	D415	D416
S105	D417	D418	D419	D420
S106	D421	D422	D423	D424
S107	D425	D426	D427	D428
S108	D429	D430	D431	D432
S109	D433	D434	D435	D436
S110	D437	D438	D439	D440
S111	D441	D442	D443	D444
S112	D445	D446	D447	D448
S113	D449	D450	D451	D452
S114	D453	D454	D455	D456
S115	D457	D458	D459	D460
S116	D461	D462	D463	D464
S117	D465	D466	D467	D468
S118	D469	D470	D471	D472
S119	D473	D474	D475	D476
S120	D477	D478	D479	D480
S121	D481	D482	D483	D484
S122	D485	D486	D487	D488
S123	D489	D490	D491	D492
S124	D493	D494	D495	D496
S125	D497	D498	D499	D500
S126	D501	D502	D503	D504
S127	D505	D506	D507	D508
S128	D509	D510	D511	D512

Note: This applies to the case where the S1/P1 to S8/P8 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

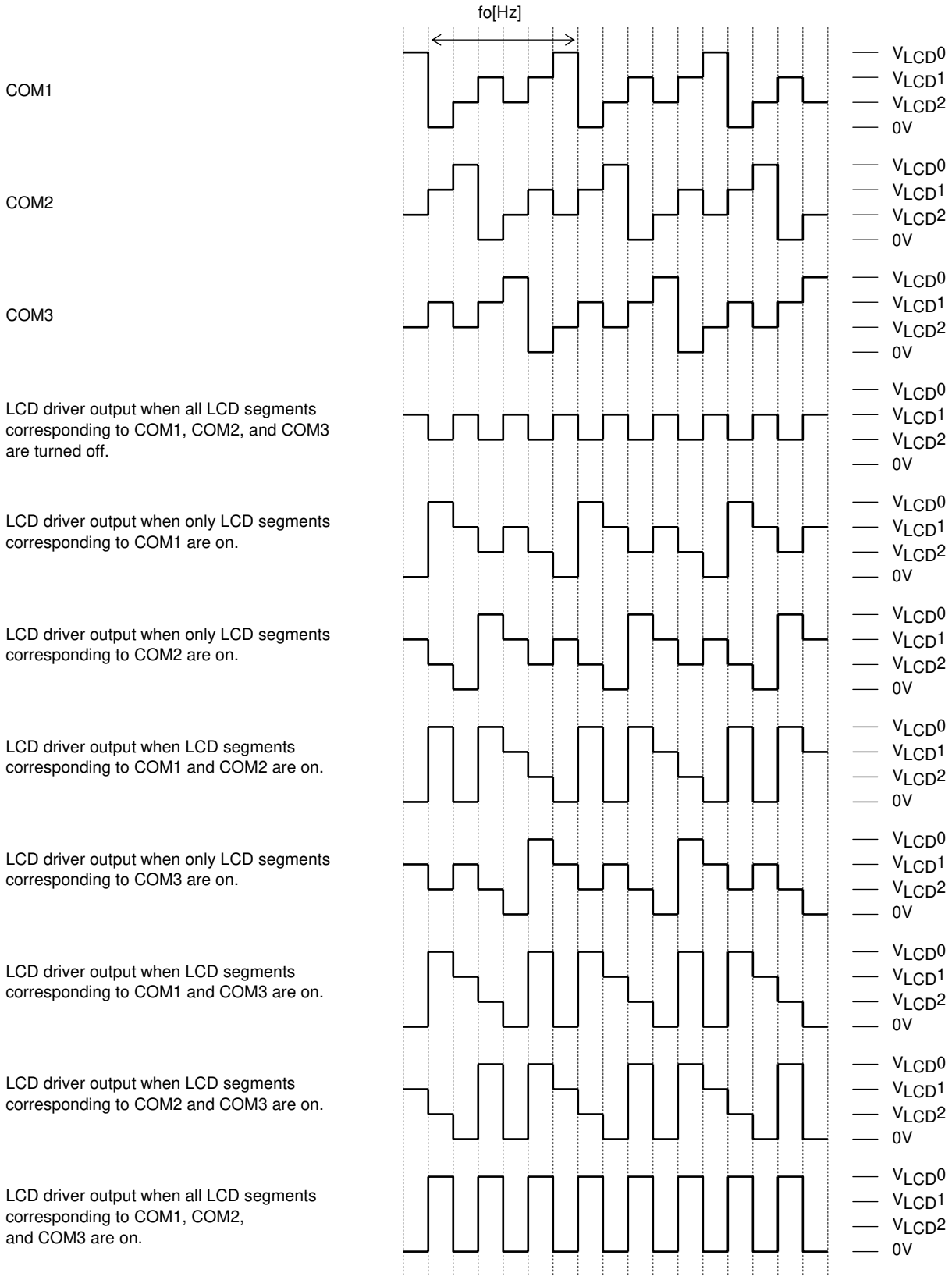
Display data				Segment output pin (S11) state
D41	D42	D43	D44	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Output Waveforms (1/3-Duty 1/2-Bias Drive Scheme)



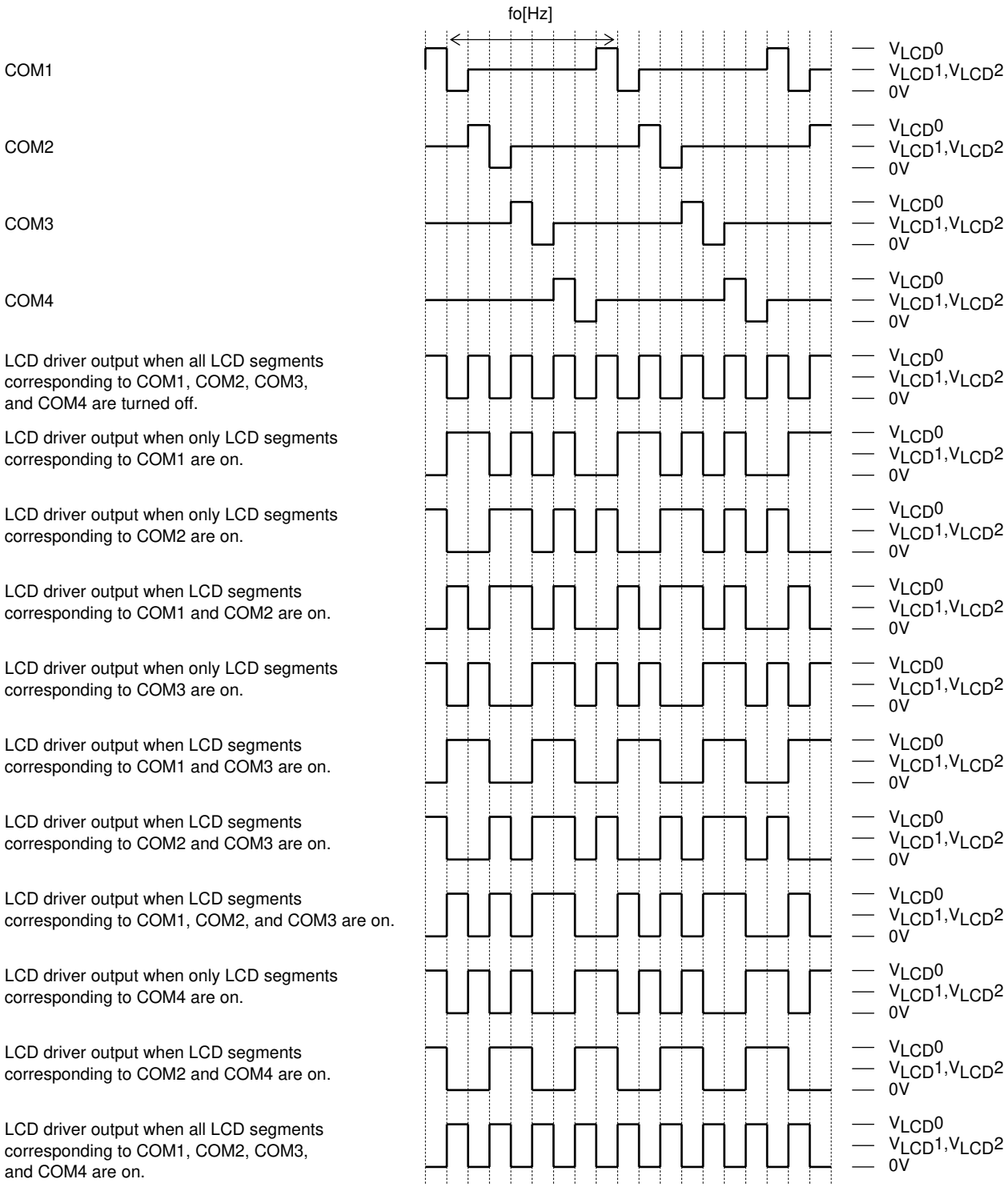
Control data			Common/segment output waveform frame frequency fo [Hz]
FC0	FC1	FC2	
0	0	0	fosc/6144, f_{CK}/6144
1	0	0	fosc/4608, f_{CK}/4608
0	1	0	fosc/3072, f_{CK}/3072
1	1	0	fosc/2304, f_{CK}/2304
0	0	1	fosc/1536, f_{CK}/1536

Output Waveforms (1/3-Duty 1/3-Bias Drive Scheme)



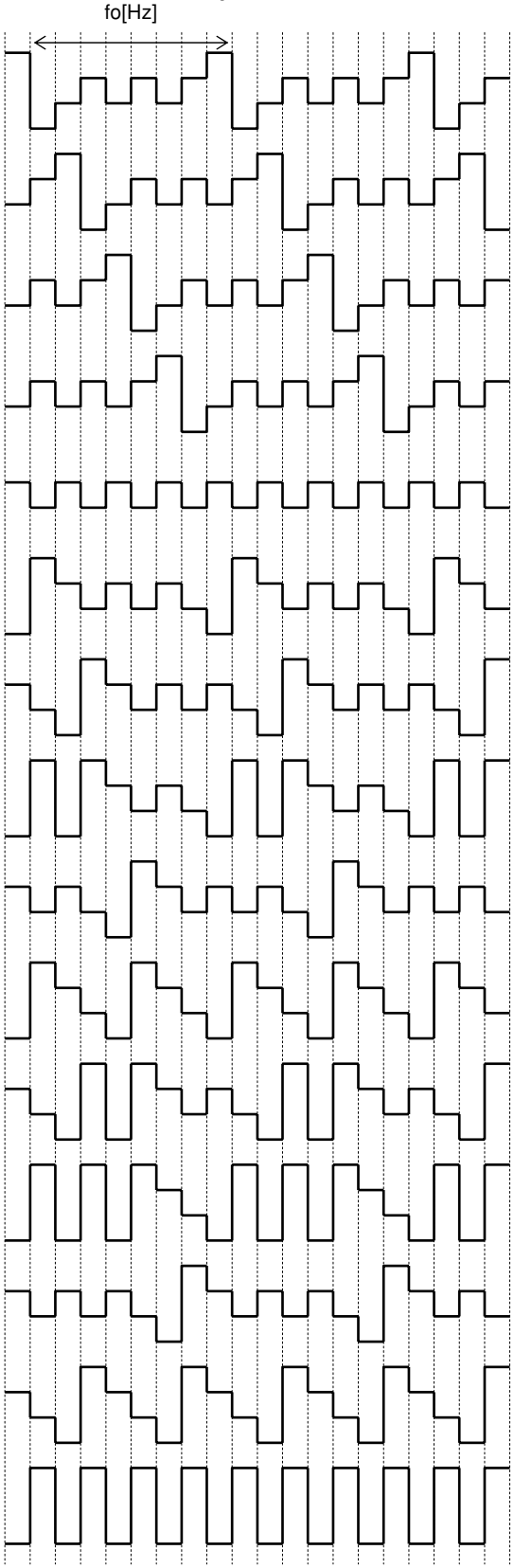
Control data			Common/segment output waveform frame frequency fo [Hz]
FC0	FC1	FC2	
0	0	0	fosc/6144, f_{CK}/6144
1	0	0	fosc/4608, f_{CK}/4608
0	1	0	fosc/3072, f_{CK}/3072
1	1	0	fosc/2304, f_{CK}/2304
0	0	1	fosc/1536, f_{CK}/1536

Output Waveforms (1/4-Duty 1/2-Bias Drive Scheme)



Control data			Common/segment output waveform frame frequency fo [Hz]
FC0	FC1	FC2	
0	0	0	fosc/6144, f_{CK}/6144
1	0	0	fosc/4608, f_{CK}/4608
0	1	0	fosc/3072, f_{CK}/3072
1	1	0	fosc/2304, f_{CK}/2304
0	0	1	fosc/1536, f_{CK}/1536

Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)



LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are turned off.

LCD driver output when only LCD segments corresponding to COM1 are on.

LCD driver output when only LCD segments corresponding to COM2 are on.

LCD driver output when LCD segments corresponding to COM1 and COM2 are on.

LCD driver output when only LCD segments corresponding to COM3 are on.

LCD driver output when LCD segments corresponding to COM1 and COM3 are on.

LCD driver output when LCD segments corresponding to COM2 and COM3 are on.

LCD driver output when LCD segments corresponding to COM1, COM2, and COM3 are on.

LCD driver output when only LCD segments corresponding to COM4 are on.

LCD driver output when LCD segments corresponding to COM2 and COM4 are on.

LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Control data			Common/segment output waveform frame frequency fo [Hz]
FC0	FC1	FC2	
0	0	0	fosc/6144, f_{CK}/6144
1	0	0	fosc/4608, f_{CK}/4608
0	1	0	fosc/3072, f_{CK}/3072
1	1	0	fosc/2304, f_{CK}/2304
0	0	1	fosc/1536, f_{CK}/1536