Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LC823450

Low Power & High-Resolution Audio Processing System LSI for Portable Sound Solution

LC823450 is audio processing system LSI for record and playback, and High-Resolution 32-bit & 192 kHz audio processing capable. It is possible to cover the most of functions necessary for a portable audio with only this LSI as follows.
It has Dual CPU and DSP with High processing capability, and internal 1656K-Byte SRAM, which make it possible to implement large scale program. And it has integrated analog functions so that PCB space and cost is reduced, and it has various interface to make extensibility high. Also it is provided with various function including SBC/AAC codec by DSP and UART and ASRC for Bluetooth® audio. It is very small chip size in spite of the multi-funciton as described above and it realizes the low power consumption. Therefore, it is applicable to porable audio markets such as Wireless headsets and will show high performance.
This document describes features, basic functions, electrical specifications, characteristics, application diagram and package dimension of this LSI.

Features

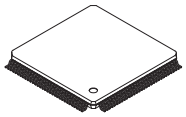
- Ultra low power consumption
- ARM® Cortex®-M3 Dual Core
- Proprietary 32-bit DSP Core (LPDSP32)
- Internal large scale size SRAM : 1656 KB (1.5 MB + 120 KB)
- High-Resolution 32-bit & 192 kHz audio processing capability
- Several DSP codes available for audio functions
- Hard wired audio functions built-in
  MP3 decoder, MP3 encoder
  6 band Equalizer
  Synchronous SRC, Asynchronous SRC, etc.
- Analog blocks built-in
  System PLL, Audio PLL
  16-bit DAC, Class-D amp, etc.
- USB2.0 device and USB2.0 host with a integrated PHY
  eMMC and SD card I/F
  Serial Flash I/F(Quad) with cache memory
  SPI, UART, I^2C, etc.

Typical Applications

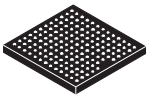
- Sound Recorders
- Wearable Audio Players
- Bluetooth Headsets
- Smart Phone Accessories

ON Semiconductor®

www.onsemi.com



TQFP128 14x14 / TQFP128L
[LC823450TA-2H]



WLCSP154, 5.52x5.33
[LC823450XATBG, LC823450XBTBG,
LC823450XCTBG, LC823450XDTBG]

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 55 of this data sheet.

ARM®

December 2015 - Rev. 3
Publication Order Number :
LC823450/D

1 Abstract

1-1 Features

- Cortex-M3 Dual Core, AMBA® (AHB/APB) system
  - Internal SRAM (1.5M-byte)
  - Internal ROM (256k-byte). Boot code, Standard Functions
  - SDRAM Controller (1 * CS)
    64M to 256Mbit SDRAM / Mobile SDRAM
  - External Memory Controller (2 * CS)
    NOR FLASH, SRAM, ROM supported, 8/16 bit I/F LCD controller supported
    Internal ROM boot and External memory device boot available
  - DMA Controller (8ch)
  - Interrupt Controller (External 90ch, Internal 82ch)
  - SPI (1ch)
  - Serial Flash I/F (1ch)
    Quad SPI, cache memory (16k-byte, 4way set associative, 128line) function available
    1.8V dedicated power supply
  - UART (3ch)
    UART1 : w/flow control (CTS, RTS)
    UART0, UART2 : w/o flow control
  - I2C (2ch) Single Master, Full/Standard
  - GPIO (90 ch)
  - Plain Timer w/ Watch Dog Timer (1ch×3)
  - Multiple Timer (2ch×4)
  - 10bit ADC (6ch)
  - SD Card I/F (3ch)
    eSD/eMMC, UHS-I, w/o CPRM
    ・SD0 : eSD/eMMC boot supported (Internal ROM Boot function)
      1.8V dedicated power supply
    ・SD1 : Multiplexed w/ Memory Stick I/F
      1.8V dedicated power supply
    ・SD2 :
      1.8V dedicated power supply
  - Memory Stick I/F (1ch)
    Multiplexed w/ SD1
  - USB2.0 Host (HS/FS/LS) Controller, Device (HS/FS) Controller. Integrated PHY
    Xtal (XT1) is required for USB function.
    48 MHz for Host, and 12,20,24,48 MHz for device
    w/o OTG function. Host and Device share an integrated PHY.
  - Real Time Clock
    2 modes below are available
    ・General RTC mode : RTC w/o key input
    ・KeyInt RTC mode : RTC w/ key input which enables power on function
  - SWD (Serial Wire Debug) is supported as the debug interface
    SWV (Serial Wire Viewer) is supported as the trace interface
    Only one of Cortex-M3 Dual Core can be traced.

1 Availability of features explained here depends on products.

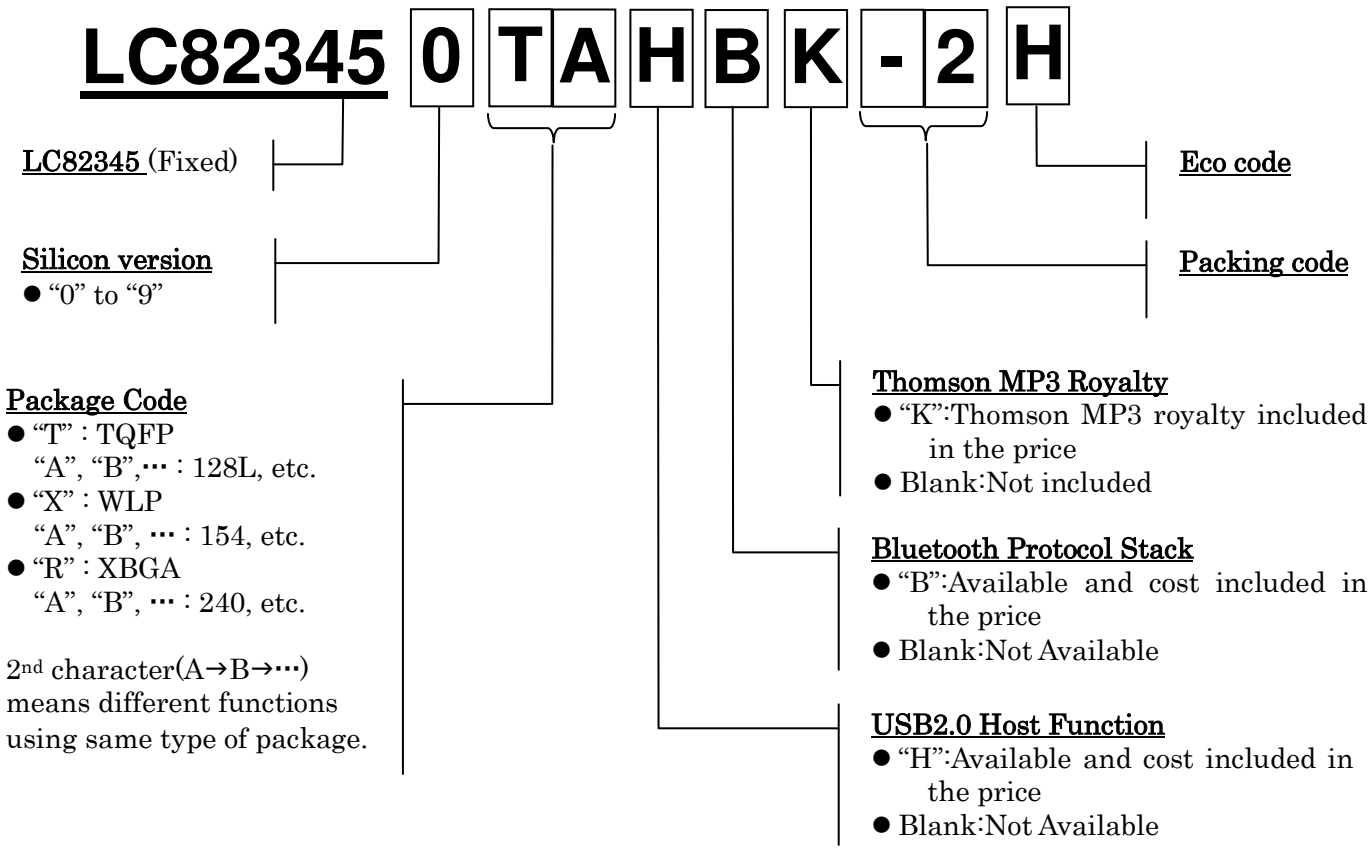
- MP3[1] hard wired encoder/decoder
  - MP3 MPEG1, MPEG2, MPEG2.5
    Sampling rate : 8kHz,11.025kHz,12kHz,16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
    Bit rate :8 Kbps to 320 Kbps (Decoder-VBR supported)
- LPDSP32 system
  - Internal SRAM (120kbyte)
  - Internal ROM (220kbyte)
  - WMA[2] (Microsoft WMA Decoder Profile Level3)
    Sampling rate : 8kHz,11.025kHz,16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz
    Bit rate :5 Kbps to 320 Kbps (VBR supported)
  - AAC (MPEG4 LC-AAC)
    Sampling rate : 8kHz,11.025kHz,12kHz,16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
    Bit rate : 8Kbps to 320Kbps (VBR supported)
  - Variable Speed Control playback (0.5 to 4.0 times speed)
    - While WMA and AAC playback, up to 2.0 time speed
    - While PCM playback, up to 4.0 times speed
    - While MP3 playback w/ hard wired decoder, up to 4.0 times speed
  - Noise Canceller, etc.
  - JTAG ICE
- Bluetooth Protocol Stack available[3]
- Other audio functions available
  - 6band Equalizer (EQ3)
  - Volume, Mute
  - Level Meter
  - Audio Timer w/ interrupt generation
  - 16/24/32bit 192 kHz PCM I/F (2ch×2). Master/slave, I2S
  - SSRC (Synchronous Sampling Rate Converter)
    0.25 to 64 conversion capable
  - ASRC (Asynchronous Sampling Rate Converter)
    jitter reducing function supporting USB audio class and Bluetooth streaming
  - Beep generator
  - Digital Microphone I/F (2ch×1)
  - 16bit Audio DAC (2ch)
    w/ Class-D Amplifier for Head Phone (2ch). Need external LC LPF
- Audio clock generation
  - Dedicated PLL for audio(PLL2:1V and PLL3:3V operation integrated)
  - Selectable PLL reference clock
    XT1 (1 to 50MHz Main xtal)
    XTRTC (32.768KHz RTC xtal)
    PCM I/F MCLK0 (/MCLK1), BCK0, BCK1
- Power supply
  - Typical voltage
    - LOGIC(Vdd1), XT1(VddXT1), PLL1(AVddPLL1), PLL2(AVddPLL2) = 1.0V
    - PLL3(AVddPLL3) = 3.3V
    - RTC(VddRTC) = 1.0V
    - I/O(Vdd2) = 1.8V or 3.3V
    - SD0(VddSD0) = 1.8V or 3.3V
    - SD1(VddSD1) = 1.8V or 3.3V
    - SD2(VddSD2) = 1.8V or 3.3V
    - S-Flash I/F(VddQSPI) = 1.8V or 3.3V
    - ADC(AVddADC) = 3.3V
    - USB PHY1(AVddUSBPHY1, DVddUSBPHY1) = 1.0V(w/o USB connection) or 1.2V(w/ USB connection)
    - USB PHY2(AVddUSBPHY2) = 2.8V(w/o USB connection) or 3.3V(w/ USB connection)
    - Class-D Amplifier(AVddDAMPL,AVddDAMPR) = 1.2V

1 MPEG Layer-3 audio coding technology licensed from Fraunhofer IIS and Thomson.
Supply of this product does not convey license nor imply any right to distribute content created with this product in revenue-generating broadcast systems (terrestrial, satellite, cable and/or other distribution channels), streaming applications (via Internet, intranets and/or networks), other content distribution systems (pay-audio or audio-on-demand applications and the like) or on physical media (compact discs, digital versatile discs, semiconductor chips, hard drives, memory cards and the like). For details, please visit http://mp3licensing.com/
Supply of this product does not convey license under the relevant intellectual property of Thomson and/or Fraunhofer Gesellschaft nor imply any right to use this product in any finished end user or ready-to-use final product. An independent license for such use is required. For details, please visit http://mp3licensing.com/.

2 This product contain technology of Microsoft company ownership, and you cannot distribute or use without getting license from Microsoft Licensing company.

3 The product name for which Bluetooth Protocol Stack is available is determined. Refer to Page 4. Please contact our representative for license fee for the Stack.

1-2 Device naming rule



1-3 Package Code and Functional Difference

The product of Package Code="RA" is under planning

Table of Functinal Difference				
Function	Package Code			
	TA	XA, XC	XB, XD	RA
Package	TQFP128L	WLP154		XBGA240
Cortex-M3 Dual Core	Single	Single	Dual	Dual
SDRAM Controller				Available
External Memory Controller		8bit I/F (LCD I/F, etc.)	8bit I/F (LCD I/F, etc.)	Available
SD2	Available		Available	Available
10bit ADC conversion speed	MAX 5MHz (*2)			MAX 20MHz (*4)
10bit ADC reference voltage	VRH=AVddADC VRL=AVssADC (*3)			VRH=AVddADC and lower VRL=AVssADC and higher
PCM1(PCM I/F ch1)	BCK1/LRCK1 share pins with other function	Available	Available	Available
MP3 hard wired encoder	Available		Available	Available
16bit Audio DAC, Class-D AMP	Available		Available	Available
PLL2(1V PLL) PLL3(3V PLL)	Only PLL2	Available	Available	Only PLL2
XTALINFO[1:0] input	"00" (24 MHz)	Available	Available	Available
RTCMODE input	"1" (General RTC mode)	Available	Available	Available
KEYINT[2:0] input		Available	Available	Available
External Interrupt	45 ch	61 ch	61 ch	90 ch
GPIO	45 ch	61 ch	61 ch	90 ch

[Note]

・Pin shared for multiple function. Refer to Terminal Functions for details.

・(*1) Intentionally not used

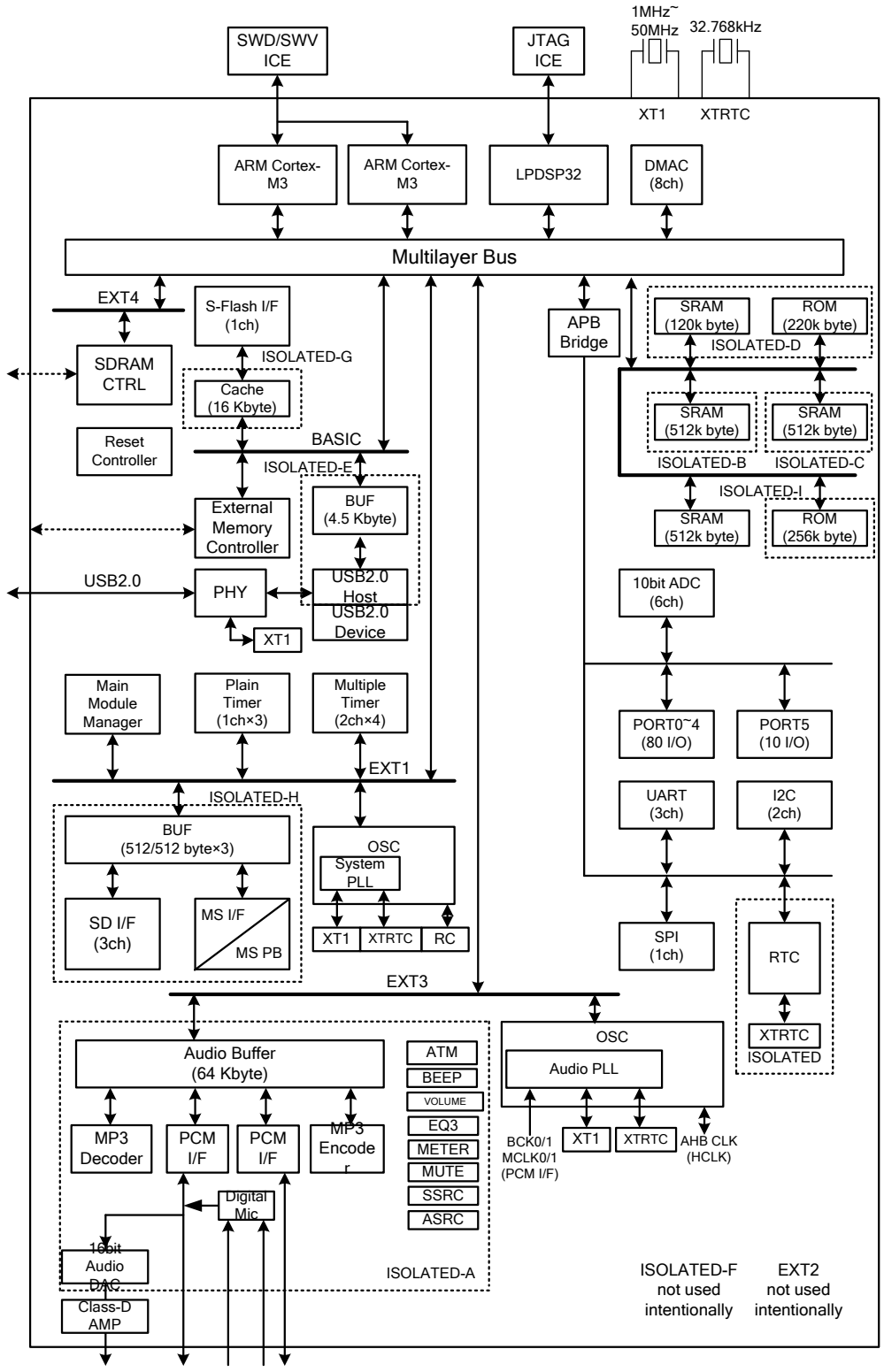
・(*2) VR is open inside

・(*3) VRH=AVddADC, VRL=AVssADC inside

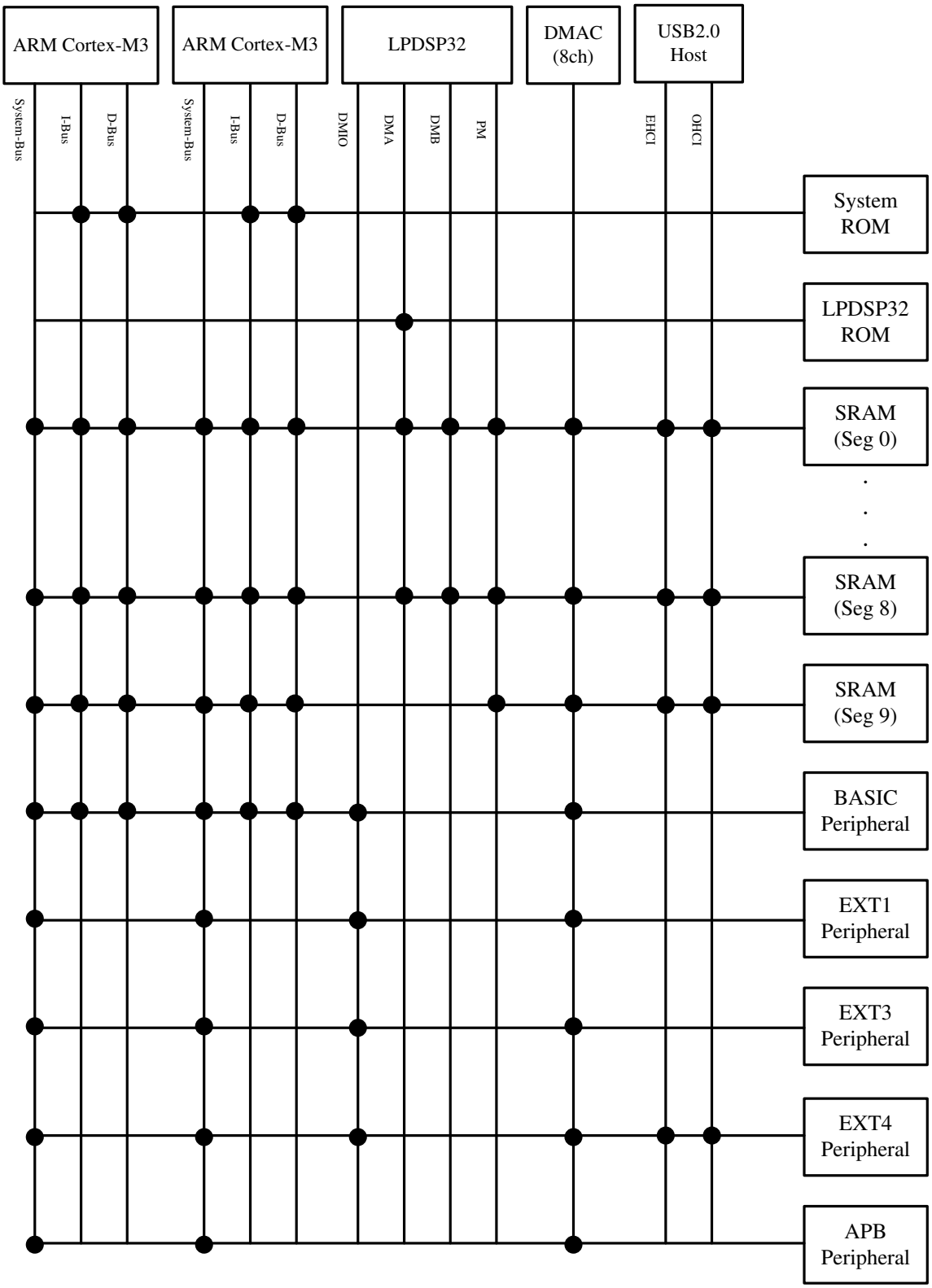
・(*4) Decoupling capacitor is required.
MAX 5MHz in case of open

1-4 Block Diagram

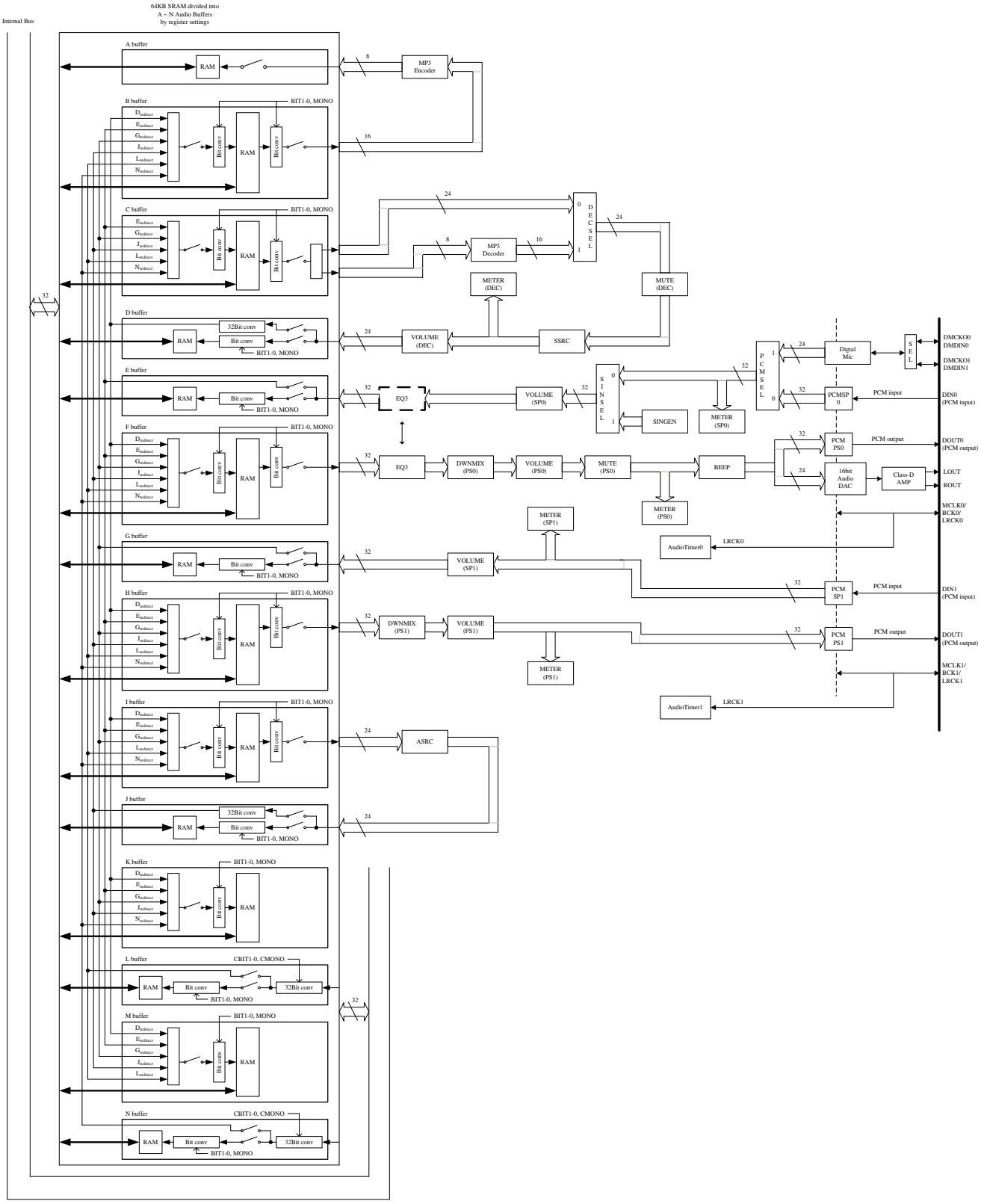
1-4-1 Top



1-4-2 Bus Matrix



1-4-3 Audio


Internal Bus
64KB SRAM divided into
A ~ N Audio Buffers
by register settings
A buffer
B buffer
C buffer
D buffer
E buffer
F buffer
G buffer
H buffer
I buffer
J buffer
K buffer
L buffer
M buffer
N buffer
RAM
Bit conv
32Bit conv
BIT1-0, MONO
CBIT1-0, CMONO
MP3 Encoder
MP3 Decoder
DESEL
METER (DEC)
MUTE (DEC)
VOLUME (DEC)
SSRC
EQ3
VOLUME (SP0)
SINSEL
SINGEN
METER (SP0)
PCMSEL
Digtal Mic
SEL
PCMSP 0
PCM input
DMCKO0
DMDIN0
DMCKO1
DMDIN1
DIN0 (PCM input)
PCM output
PCM PS0
DOUT0 (PCM output)
DWNMIX (PS0)
MUTE (PS0)
BEEP
16bit Audio DAC
Class-D AMP
LOUT
ROUT
METER (PS0)
MCLK0/ BCK0/ LRCK0
AudioTimer0
LRCK0
METER (SP1)
VOLUME (SP1)
PCM SP1
DIN1 (PCM input)
DWNMIX (PS1)
VOLUME (PS1)
PCM PS1
DOUT1 (PCM output)
METER (PS1)
MCLK1/ BCK1/ LRCK1
AudioTimer1
LRCK1
ASRC

2 Terminal Functions

TA : Package Code="TA"
XA : Package Code="XA"
XB : Package Code="XB"
XC : Package Code="XC"
XD : Package Code="XD"

(A) JTAG/SWD

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
TDO	–	O	JTAG test data output	VddSD1	○	○	○
SDWP1	Pos	I	SD I/F Ch1 write protect		○	○	○
INS	Neg	I	Memory Stick INS		○	○	○
GPIO21	–	B	GPIO		○	○	○
EXTINT21	–	I	External Interrupt 2-bit1		○	○	○
TDI	–	I	JTAG test data input	VddSD1	○	○	○
SDCD1	Neg	I	SD I/F Ch1 detect		○	○	○
SWO	–	O	serial wire view data		○	○	○
GPIO20	–	B	GPIO		○	○	○
EXTINT20	–	I	External Interrupt 2-bit0		○	○	○
TMS	–	I	JTAG test data select	VddSD2	○	○	○
SDWP2	Pos	I	SD I/F Ch2 write protect		○	(*)	○
GPIO28	–	B	GPIO		○	○	○
EXTINT28	–	I	External Interrupt 2-bit8		○	○	○
TCK	Pos	I	JTAG test clock	VddSD2	○	○	○
SDCD2	Neg	I	SD I/F Ch2 detect		○	(*)	○
GPIO29	–	B	GPIO		○	○	○
EXTINT29	–	I	External Interrupt 2-bit9		○	○	○
SWDCLK	Pos	I	Serial wire clock	Vdd2	○	○	○
DMCKO1	–	O	Digital MicCh1Clock Output		○	○	○
GPIO58	–	B	GPIO		○	○	○
EXTINT58	–	I	External Interrupt 5-bit8		○	○	○
SWDIO	–	B	Serial wire Data	Vdd2	○	○	○
DMDIN1	–	I	Digital MicCh1 Data Input		○	○	○
GPIO59	–	B	GPIO		○	○	○
EXTINT59	–	I	External Interrupt 5-bit9		○	○	○
Sum					6	6	6

(*) This function is not available

(B) RTC

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
XIN32K	Pos	I	32.768kHz XTAL Input (XTRTC)	VddRTC	○	○	○
XOUT32K	–	O	32.768kHz XTAL Output (XTRTC)	VddRTC	○	○	○
VDET	Neg	I	RTC power detect Input	VddRTC	○	○	○
RTCINT	Neg	O	RTC Interrupt Output (Normal:Hiz, Interrupt enabled:Low Output)	VddRTC	○	○	○
BACKUPB	Neg	I	RTC backup mode input	VddRTC	○	○	○
KEYINT[2:0]	–	I	RTC KEY input can be used when KeyInt RTC mode	VddRTC		○	○
RTCMODE	–	I	RTC mode input(*1) Set General RTC or KeyInt RTC mode RTCMODE = ・“0” : KeyInt RTC mode ・“1” : General RTC mode Bonding internally for “TA” product	VddRTC		○	○
VddRTC	–	P	RTC power supply	–	○	○	○
VssRTC	–	P	RTC ground	–	○	○	○
Sum					7	11	11

(*1) Set according to the General RTC mode or KeyInt RTC mode.
Bonding internally for “TA” product as described on Page 5

(C) External Interrupt/GPIO

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
SDRADDR12	–	O	SDRAM address	Vdd2			
GPIO2A	–	B	GPIO				
EXTINT2A	–	I	External Interrupt 2-bit10				
SCL1	–	O	I2C ch1 Clock (open drain output)	Vdd2	○	○	○
GPIO2B	–	B	GPIO		○	○	○
EXTINT2B	–	I	External Interrupt 2-bit11		○	○	○
SDA1	–	B	I2C ch1 Data (open drain output)	Vdd2	○	○	○
GPIO2C	–	B	GPIO		○	○	○
EXTINT2C	–	I	External Interrupt 2-bit12		○	○	○
SDRADDR11	–	O	SDRAM address	Vdd2			
DMCKO0	–	O	Digital Mic Clock Ch0 Output		○	○	○
GPIO2D	–	B	GPIO		○	○	○
EXTINT2D	–	I	External Interrupt 2-bit13		○	○	○
EXTINT2E	–	I	External Interrupt 2-bit14	Vdd2	○	○	○
GPIO2E	–	B	GPIO * While Internal ROM boot, this terminal is used as external power circuit enable signal.		○	○	○
EXTINT2F	–	I	External Interrupt 2-bit15	Vdd2	○	○	○
GPIO2F	–	B	GPIO * While Internal ROM boot, this terminal is used as boot monitor signal.		○	○	○
Sum					5	5	5

(D) SPI(Serial I/F Ch0)/S-Flash I/F(Serial I/F Ch1)

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
SCK0	Neg	B	Serial I/F Ch0 Clock	Vdd2	○	○	○
GPIO1D	–	B	GPIO		○	○	○
EXTINT1D	–	I	External Interrupt 1-bit13		○	○	○
SDI0	–	I	Serial I/F Ch0 Data Input	Vdd2	○	○	○
GPIO1E	–	B	GPIO		○	○	○
EXTINT1E	–	I	External Interrupt 1-bit14		○	○	○
SDO0	–	O	Serial I/F Ch0 Data Output	Vdd2	○	○	○
GPIO1F	–	B	GPIO		○	○	○
EXTINT1F	–	I	External Interrupt 1-bit15		○	○	○
SCK1	Neg	O	Serial I/F Ch1 Clock (QSPI Clock)	VddQSPI	○	○	○
GPIO0D	–	B	GPIO		○	○	○
EXTINT0D	–	I	External Interrupt 0-bit13		○	○	○
SDI1(QIO0)	–	O(B)	Serial I/F Ch1 Data Output (QSPI Data 0)	VddQSPI	○	○	○
GPIO0E	–	B	GPIO		○	○	○
EXTINT0E	–	I	External Interrupt 0-bit14		○	○	○
SDO1(QIO1)	–	I(B)	Serial I/F Ch1 Data Input (QSPI Data 1)	VddQSPI	○	○	○
GPIO0F	–	B	GPIO		○	○	○
EXTINT0F	–	I	External Interrupt 0-bit15		○	○	○
SWP1(QIO2)	Neg	O(B)	Serial I/F Ch1 write protect (QSPI Data 2)	VddQSPI	○	○	○
GPIO11	–	B	GPIO		○	○	○
EXTINT11	–	I	External Interrupt 1-bit1		○	○	○
SHOLD1(QIO3)	Neg	O(B)	Serial I/F Ch1 hold (QSPI Data 3)	VddQSPI	○	○	○
GPIO12	–	B	GPIO		○	○	○
EXTINT12	–	I	External Interrupt 1-bit2		○	○	○
Sum					8	8	8

(E) I2C

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
SCL0	–	O	I2C ch0 Clock (open drain output)	Vdd2	○	○	○
GPIO07	–	B	GPIO		○	○	○
EXTINT07	–	I	External Interrupt 0-bit7		○	○	○
SDA0	–	B	I2C ch0 Data (open drain output)	Vdd2	○	○	○
GPIO08	–	B	GPIO		○	○	○
EXTINT08	–	I	External Interrupt 0-bit8		○	○	○
Sum					2	2	2

(F) UART

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
TXD1	–	O	UART Ch1 transmit Data	VddSD2	○	○	○
SDAT20	–	B	SD I/F Ch2 Data 0		○	(*)	○
GPIO04	–	B	GPIO		○	○	○
EXTINT04	–	I	External Interrupt 0-bit4		○	○	○
RXD1	–	I	UART Ch1 receive Data	VddSD2	○	○	○
SDAT21	–	B	SD I/F Ch2 Data 1		○	(*)	○
GPIO05	–	B	GPIO		○	○	○
EXTINT05	–	I	External Interrupt 0-bit5		○	○	○
CTS1	Neg	I	UART Ch1 clear to send	VddSD2	○	○	○
SDAT22	–	B	SD I/F Ch2 Data 2		○	(*)	○
RXD0	–	I	UART Ch0 receive Data		○	○	○
GPIO56	–	B	GPIO		○	○	○
EXTINT56	–	I	External Interrupt 5-bit6		○	○	○
RTS1	Neg	O	UART Ch1 request to send	VddSD2	○	○	○
SDAT23	–	B	SD I/F Ch2 Data 3		○	(*)	○
TXD0	–	O	UART Ch0 transmit Data		○	○	○
GPIO57	–	B	GPIO		○	○	○
EXTINT57	–	I	External Interrupt 5-bit7		○	○	○
TXD2	–	O	UART Ch2 transmit Data	VddQSPI	○	○	○
TIOCA10	–	B	MTM1 Ch0A - target signal of pulse-length-reader function - output of sentinel-inform-function - output of PWM output		○	○	○
GPIO0B	–	B	GPIO		○	○	○
EXTINT0B	–	I	External Interrupt 0-bit11		○	○	○
RXD2	–	I	UART Ch2 receive Data	VddQSPI	○	○	○
TIOCA11	–	B	MTM1 Ch1A - target signal of pulse-length-reader function - output of sentinel-inform-function - output of PWM output		○	○	○
GPIO0C	–	B	GPIO		○	○	○
EXTINT0C	–	I	External Interrupt 0-bit12		○	○	○
Sum					6	6	6

(*)This function is not available

(G) Timer

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
TIOCA00	–	B	MTM0 Ch0A - target signal of pulse-length-reader function - output of sentinel-inform-function - output of PWM output	VddSD2	○	○	○
SDCLK2	–	O	SD I/F Ch2 Clock Output		○	(*)	○
PHI0	–	O	System Clock Output 0		○	○	○
GPIO09	–	B	GPIO		○	○	○
EXTINT09	–	I	External Interrupt 0-bit9		○	○	○
TIOCA01	–	B	MTM0 Ch1A - target signal of pulse-length-reader function - output of sentinel-inform-function - output of PWM output	VddSD2	○	○	○
SDCMD2	–	B	SD I/F Ch2 command line		○	(*)	○
PHI1	–	O	System Clock Output 1		○	○	○
GPIO0A	–	B	GPIO		○	○	○
EXTINT0A	–	I	External Interrupt 0-bit10		○	○	○
TIOCB00	–	B	MTM0 Ch0B - target signal of pulse-length-reader function - output of sentinel-inform-function	Vdd2	○	○	○
DIN1	–	I	PCM1 Data Input		○	○	○
DMDIN0	–	I	Digital Mic Data Ch0 Input		○	○	○
GPIO02	–	B	GPIO		○	○	○
EXTINT02	–	I	External Interrupt 0-bit2		○	○	○
TIOCB01	–	B	MTM0 Ch1B - target signal of pulse-length-reader function - output of sentinel-inform-function	VddQSPI	○	○	○
DMCKO0	–	O	Digital Mic Clock Ch0 Output		○	○	○
QSCS	Neg	O	Serial I/FCh1 QSPI chip select * While Serial Flash Boot, this is used as chip select of Serial Flash		○	○	○
GPIO03	–	B	GPIO		○	○	○
EXTINT03	–	I	External Interrupt 0-bit3		○	○	○
TCLKA0	–	I	MTM0 external Clock A	Vdd2	○	○	○
BCK1	–	B	PCM1 bit Clock		○	○	○
GPIO00	–	B	GPIO		○	○	○
EXTINT00	–	I	External Interrupt 0-bit0		○	○	○
TCLKB0	–	I	MTM0 external Clock B	Vdd2	○	○	○
LRCK1	–	B	PCM1 LR Clock		○	○	○
GPIO01	–	B	GPIO		○	○	○
EXTINT01	–	I	External Interrupt 0-bit1		○	○	○
Sum					6	6	6

(*)This function is not available

(H) PCM I/F

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
MCLK0	Pos	B	PCM0 maser Clock	Vdd2	○	○	○
MCLK1	Pos	B	PCM1 master Clock		○	○	○
GPIO18	–	B	GPIO		○	○	○
EXTINT18	–	I	External Interrupt 1-bit8		○	○	○
BCK0	–	B	PCM0 bit Clock	Vdd2	○	○	○
DMCKO1	–	O	Digital Mic Ch1 Clock Output		○	○	○
GPIO19	–	B	GPIO		○	○	○
EXTINT19	–	I	External Interrupt 1-bit9		○	○	○
LRCK0	–	B	PCM0 LR Clock	Vdd2	○	○	○
DMDIN1	–	I	Digital Mic Ch1 Data Input		○	○	○
GPIO1A	–	B	GPIO		○	○	○
EXTINT1A	–	I	External Interrupt 1-bit10		○	○	○
DIN0	–	I	PCM0 Data Input	Vdd2	○	○	○
DMDIN0	–	I	Digital Mic Ch0 Data Input		○	○	○
GPIO1B	–	B	GPIO		○	○	○
EXTINT1B	–	I	External Interrupt 1-bit11		○	○	○
DOUT0	–	O	PCM0 Data Output	Vdd2	○	○	○
DMCKO0	–	O	Digital Mic Ch0 Clock Output		○	○	○
GPIO1C	–	B	GPIO		○	○	○
EXTINT1C	–	I	External Interrupt 1-bit12		○	○	○
BCK1	–	B	PCM1 bit Clock	Vdd2		○	○
GPIO13	–	B	GPIO			○	○
EXTINT13	–	I	External Interrupt 1-bit3			○	○
LRCK1	–	B	PCM1 LR Clock	Vdd2		○	○
GPIO14	–	B	GPIO			○	○
EXTINT14	–	I	External Interrupt 1-bit4			○	○
DOUT1	–	O	PCM1 Data Output	Vdd2	○	○	○
GPIO15	–	B	GPIO		○	○	○
EXTINT15	–	I	External Interrupt 1-bit5		○	○	○
Sum					6	8	8

(I) SD IF/MS IF

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
SDCLK0	–	O	SD I/F Ch0 Clock Output	VddSD0	○	○	○
SDCMD0	–	B	SD I/F Ch0 command line	VddSD0	○	○	○
SDAT0[3:0]	–	B	SD I/F Ch0 Data	VddSD0	○	○	○
SDCLK1	–	O	SD I/F Ch1 Clock Output	VddSD1	○	○	○
SCLK	–	O	Memory Stick Clock Output		○	○	○
GPIO22	–	B	GPIO		○	○	○
EXTINT22	–	I	External Interrupt 2-bit2		○	○	○
SDCMD1	–	B	SD I/F Ch1 command line	VddSD1	○	○	○
BS	–	O	Memory Stick BS		○	○	○
GPIO23	–	B	GPIO		○	○	○
EXTINT23	–	I	External Interrupt 2-bit3		○	○	○
SDAT1[3:0]	–	B	SD I/F Ch1 Data	VddSD1	○	○	○
DATA[3:0]	–	B	Memory Stick Data		○	○	○
GPIO2[7:4]	–	B	GPIO		○	○	○
EXTINT2[7:4]	–	I	External Interrupt 2-bit7 to bit4		○	○	○
Sum					12	12	12

(*)This function is not available

(J) SDRAM I/F

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
SDRCLK	Neg	O	SDRAM Clock Output	Vdd2			
SDRCKE	Pos	O	SDRAM Clock enable Output	Vdd2			
SDRCS	Neg	O	SDRAM chip select Output	Vdd2			
SDRWE	Neg	O	SDRAM write enable Output	Vdd2			
SDRCAS	Neg	O	SDRAM CAS Output	Vdd2			
SDRRAS	Neg	O	SDRAM RAS Output	Vdd2			
SDRDQM[1:0]	Pos	O	SDRAM Data mask byte lane select	Vdd2			
SDRADDR[10:0]	–	O	SDRAM address(*)	Vdd2			
SDRBA[1:0]	–	O	SDRAM bank select	Vdd2			
SDRDATA[15:0]	–	B	SDRAM Data	Vdd2			
Sum					0	0	0

(*) SDRAM address bit is 13bit including SDRADDR [12:11].

(K) External Memory I/F

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
NCS0	Neg	O	chip select0	Vdd2		○	○
GPIO06	–	B	GPIO			○	○
EXTINT06	–	I	External Interrupt 0-bit6			○	○
NCS1	Neg	O	chip select1	Vdd2		○	○
RXD0	–	I	UART Ch0 receive Data			○	○
GPIO10	–	B	GPIO			○	○
EXTINT10	–	I	External Interrupt 1-bit0			○	○
NRD	Neg	O	read enable	Vdd2		○	○
GPIO17	–	B	GPIO			○	○
EXTINT17	–	I	External Interrupt 1-bit7			○	○
NWRENWRL	Neg	O	write enable, write enable low	Vdd2		○	○
GPIO30	–	B	GPIO			○	○
EXTINT30	–	I	External Interrupt 3-bit0			○	○
NHBNWRH	Neg	O	high byte select, write enable high	Vdd2		○	○
TXD0	–	O	UART Ch0 transmit Data			○	○
GPIO31	–	B	GPIO			○	○
EXTINT31	–	I	External Interrupt 3-bit1			○	○
NLBEXA0	–	O	low byte select, address0	Vdd2		○	○
GPIO16	–	B	GPIO			○	○
EXTINT16	–	I	External Interrupt 1-bit6			○	○
EXA[20:15]	–	O	address	Vdd2			
GPIO4[5:0]	–	B	GPIO				
EXTINT4[5:0]	–	I	External Interrupt 4-bit5 to bit0				
EXA[14:9]	–	O	address	Vdd2			
GPIO3[F:A]	–	B	GPIO				
EXTINT3[F:A]	–	I	External Interrupt 3-bit15 to bit10				
EXA[8:1]	–	O	address	Vdd2			
GPIO3[9:2]	–	B	GPIO				
EXTINT3[9:2]	–	I	External Interrupt 3-bit9 to bit2				
EXD[7:0]	–	B	Data	Vdd2		○	○
GPIO4[D:6]	–	B	GPIO			○	○
EXTINT4[D:6]	–	I	External Interrupt 4-bit13 to bit6			○	○
EXD[15:8]	–	B	Data	Vdd2			
GPIO5[5:0], GPIO4[F:E]	–	B	GPIO				
EXTINT5[5:0], EXTINT4[F:E]	–	I	External Interrupt 5-bit5 to bit0, External Interrupt 4-bit15 to bit14				
Sum					0	14	14

(L) Xtal, PLL

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
XIN1	–	I	XTAL input (XT1)	VddXT1	○	○	○
XOUT1	–	O	XTAL output (XT1)	VddXT1	○	○	○
VddXT1	–	P	XTAL power supply (XT1)	–	○	○	○
VssXT1	–	P	XTAL ground (XT1)	–	○	○	○
XTALINFO[1:0]	–	B	XTAL frequency input (*1) XTALINFO[1:0] = ・“00” : 24MHz ・“01” : 12MHz ・“10” : 20MHz ・“11” : 48MHz Used for determining clock frequency setting while internal ROM boot. Bonding internally for “TA” product	Vdd2		○	○
VCNT1	–	O	PLL1 VCO control	AVddPLL1	○	○	○
AVddPLL1	–	P	PLL1 analog power supply	–	○	○	○
AVssPLL1	–	P	PLL1 analog ground	–	○	○	○
VCNT2	–	O	PLL2 VCO control	AVddPLL2	○ (*2)	○	○
AVddPLL2	–	P	PLL2 analog power supply	–	○ (*2)	○	○
VCNT3	–	O	PLL3 VCO control	AVddPLL3	○ (*3)	○	○
AVddPLL3	–	P	PLL3 analog power supply	–	○ (*3)	○	○
AVssPLL2	–	P	PLL2/3 analog ground(*4)	–	○	○	○
Sum					10	14	14

(*1) Set according to the frequency of XT1(12/20/24/48MHz).
Bonding internally for “TA” product as described on Page 5.

(*2),(*3) Audio clock is generated by one of PLL2(1V) or PLL3(3V).
One of PLL2 or PLL3 is available for “TA” and “RA” product. Please refer to Page 5 for more information.
Both of PLL2 and PLL3 are available for “XA”, “XB”, “XC” and “XD” products.

(*4) Analog ground is shared by PLL2 and PLL3.

(M) USB-PHY

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
USBDP	–	B	USB D+	AVddUSBPHY2 or AVddUSBPHY1	○	○	○
USBDM	–	B	USB D–	AVddUSBPHY2 or AVddUSBPHY1	○	○	○
USBEXT12	–	O	USB-PHY reference resister	AVddUSBPHY2	○	○	○
AVddUSBPHY1	–	P	USB-PHY 1.0V analog power supply	–	○ 2	○ 2	○ 2
DVddUSBPHY1	–	P	USB-PHY 1.0V digital power supply. Connected to AVddUSBPHY1 internally in case of no DVddUSBPHY1 port available	–			
AVddUSBPHY2	–	P	USB-PHY 3.3V analog power supply	–	○ 2	○ 2	○ 2
AVssUSBPHY	–	P	USB-PHY analog ground	–	○ 4	○ 4	○ 4
Sum					11	11	11

(N) 10bit ADC

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
AN[5:0]	–	I	ADC Input	AVddADC	○	○	○
VRH	–	I	ADC High reference	AVddADC			
VRL	–	I	ADC Low reference	AVddADC			
VR	–	O	ADC reference voltage	AVddADC			
AVddADC	–	P	ADC analog power	–	○	○	○
AVssADC	–	P	ADC analog ground	–	○	○	○
Sum					8	8	8

(O) Class-D AMP

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
LOUT	–	O	Lch Class D AMP Output	AVddDAMPL	○		○
GPLOUT	–	O	General purpose Output (GPO)		○	○	○
ROUT	–	O	Rch Class D AMP Output	AVddDAMPR	○		○
GPROUT	–	O	General purpose Output (GPO)		○	○	○
AVddDAMPL	–	P	Lch Class D AMP analog power supply	–	○	○	○
AVddDAMPR	–	P	Rch Class D AMP analog power supply	–	○	○	○
AVssDAMPL	–	P	Lch Class D AMP analog ground	–	○	○	○
AVssDAMPR	–	P	Rch Class D AMP analog ground	–	○	○	○
Sum					6	6	6

(P) Other, Power

Terminal name / Multiplexed function	Polarity	Direction	Function	IO POWER	Available(○) TA	XA, XC	XB, XD
BMODE[1:0]	–	B	Boot mode select	Vdd2	○	○	○
TEST	Pos	I	test mode(normally connect to ground)	Vdd2	○	○	○
NRES	Neg	I	LSI reset Input	Vdd2	○	○	○
Vdd1	–	P	Digital core power	–	○ 7	○ 7	○ 7
Vdd2	–	P	Digital IO power	–	○ 8	○ 8	○ 8
VddSD0	–	P	Digital IO power(SDI/F Ch0)	–	○	○	○
VddSD1	–	P	Digital IO power (SD(MS)I/F Ch1)	–	○	○	○
VddSD2	–	P	Digital IO power (SDI/F Ch2)	–	○	○	○
VddQSPI	–	P	Digital IO power (QSPI)	–	○	○	○
Vss	–	P	Digital ground	–	○ 12	○ 14	○14
Sum					35	37	37

All sum	128	154	154

Note : Unused Input terminals and input state terminals of bidirectional should be set Pull-up/Down resister ON or connect to digital power supply or ground (don't left open).

2-1 Boot mode

Boot modes available depend on BMODE[1:0] port status

IPL mode	BMODE1	BMODE0	explanation
Physical Boot USB	PD 470kΩ	PD 470kΩ	Internal ROM boot(eMMC Physical Boot with USB download –SD card I/F Ch0 + USB Device + EXTINT2E + EXTINT2F)
			By using Boot operation mode of eMMC, load IPL2(program) from eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through USB.
Physical Boot SD	PD 470kΩ	PU 470kΩ	Internal ROM boot(eMMC Physical Boot with SD Ch1 download –SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2E + EXTINT2F)
			By using Boot operation mode of eMMC, load IPL2(program) from eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through SD1.
User Area Boot USB	PD 1kΩ	PU or PD 470kΩ	Internal ROM boot(User Area Boot with USB download –SD card I/F Ch0 + USB Device + EXTINT2E + EXTINT2F)
			Load IPL2(program) from user area of eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through USB.
User Area Boot SD	PU 470kΩ	PD 1kΩ	Internal ROM boot(User Area Boot with SD Ch1 download –SD card I/F Ch0 + SD card I/F Ch1 + EXTINT2E + EXTINT2F)
			Load IPL2(program) from user area of eMMC connected to SD0 to internal SRAM and jump to IPL2. IPL2 is written through SD1.
SPI Boot USB	PU 470kΩ	PU 470kΩ	Internal ROM boot(external Serial Flash SPI Boot with USB download –S-Flash I/F + USB Device + EXTINT2E + EXTINT2F + TIOCB01)
			Load IPL2(program) from Serial Flash connected to S-Flash I/F to internal SRAM and jump to IPL2. IPL2 is written through USB.
SPI Boot SD	PD 470kΩ	PU 1kΩ	Internal ROM boot(external Serial Flash SPI Boot with SD Ch1 download –S-Flash I/F + SD card I/F Ch1 + EXTINT2E + EXTINT2F + TIOCB01)
			Load IPL2(program) from Serial Flash connected to S-Flash I/F to internal SRAM and jump to IPL2. IPL2 is written through SD1.
QSPI Boot USB	PU 1kΩ	PU 470kΩ	Internal ROM boot(external Serial Flash QSPI Boot with USB download –S-Flash I/F(QSPI) + USB Device + EXTINT2E + EXTINT2F + TIOCB01)
			Fetch IPL2(program) from Serial Flash connected to S-Flash I/F. IPL2 is written by using DO command directly through USB.
QSPI Boot SD	PU 1kΩ	PD 470kΩ	Internal ROM boot(external Serial Flash QSPI Boot with SD Ch1 download –S-Flash I/F(QSPI) + SD card I/F Ch1 + EXTINT2E + EXTINT2F + TIOCB01)
			Fetch IPL2(program) from Serial Flash connected to S-Flash I/F. IPL2 is written through SD1.
User Area Delete	PD 1kΩ	PU 1kΩ	Internal ROM boot(User Area IPL2 delete –SD card I/F Ch0 + EXTINT2E + EXTINT2F)

			After deleting IPL2 by using this mode, IPL2 can be written again while User Area Boot mode.
Partition Delete	PD 470kΩ	PD 1kΩ	Internal ROM boot(Partition Area IPL2 delete –SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			After deleting IPL2 by using this mode, IPL2 can be written again while eMMC Physical Boot mode.
SPI All Erase	PU 470kΩ	PU 1kΩ	Internal ROM boot(external Serial Flash SPI all area delete –S-Flash I/F + EXTINT2E + EXTINT2F + TIOCB01)
			Delete all content of Serial Flash. This mode should be used in case of SPI mode operation of Serial Flash
SDCH0 All Erase	PD 1kΩ	PD 1kΩ	Internal ROM boot(all area delete –SD card I/F Ch0 + EXTINT2E + EXTINT2F)
			Delete all content of eMMC including Partition area. Take a lot of time to delete. Trim also processed in case of eMMC supporting Trim function.
QSPI All Erase	PU 1kΩ	PD 1kΩ	Internal ROM boot(external Serial Flash QSPI all area delete –S-Flash I/F(QSPI) + EXTINT2E + EXTINT2F + TIOCB01)
			Delete all content of Serial Flash. This mode should be used in case of QSPI fetch mode operation of Serial Flash
External ROM Boot	PU 470kΩ	PD 470kΩ	External memory boot(External-0)
			Fetch from external memory(External0) connected to XMC(external memory controller)
Hi-z	PU 1kΩ	PU 1kΩ	External I/F ports below forced to Hiz - EXA[20:1],EXD[15:0],NCS[1:0],NRD,NWRENWRL,NHBNWRH,NLBEXA0 - SDCLK0,SDCMD0,SDAT0[3:0] - CK1,SDI1(QIO0),SDO1(QIO1),SWP1(QIO2),SHOLD1(QIO3),TIOCB01

・In case of TQFP128L, WLP154, don't use external memory boot (External-0)

2-2 Boot port

Some ports are used in internal ROM code while booting as below.

・EXTINT2E(GPIO2E) : OUT for power supply control
・EXTINT2F(GPIO2F) : OUT for indicating status of boot, start of USB connection and USB disconnection, error status by Low/High of this port.
・Use SDCMD1, SDAT1[3:0], SDCLK1 as SD1. SDCD1 and SDWP1 are not used.
Port function switch is processed during write from SD1.
・SPI Boot/SPI All Erase is processed by using 4 ports SCK1, QSCS, SDO1,SDI1.
SHOLD1 and SWP1 are not used.
・QSPI Boot/QSPI All Erase is processed by using SCK1, QSCS, SDO1, SDI1, SHOLD1, SWP1.
・External ROM Boot is processed by using NCS0 and external memory controller ports.
GPIO2E is not used.
・In case of External I/F ports Hiz mode, external memory interface ports such as NCS0, NCS1 and external memory controller ports is used. GPIO2E is used as input port.

Ports used during IPL	
IPL mode	Ports used(*)
Physical Boot USB	P2E(power supply control), P2F(status monitoring)
Physical Boot SD	P2E(power supply control), P2F(status monitoring) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
User Area Boot USB	P2E(power supply control), P2F(status monitoring)
User Area Boot SD	P2E(power supply control), P2F(status monitoring) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
SPI Boot USB	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1)
SPI Boot SD	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
QSPI Boot USB	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P11(SWP1) P12(SHOLD1)
QSPI Boot SD	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P011(SWP1) P12(SHOLD1) P22(SDCLK1) P23(SDCMD1) P24(SDDATA10) P25(SDDATA11) P26(SDDATA12) P27(SDDATA13)
User Area Delete	P2E(power supply control), P2F(status monitoring)
Partition Delete	P2E(power supply control), P2F(status monitoring)
SPI Erase	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SPIOUT) P0E(SDI1)
SDCH0 All Erase	P2E(power supply control), P2F(status monitoring)
QSPI All Erase	P2E(power supply control), P2F(status monitoring) P0D(SCK1) P03(QSCS) P0F(SDO1) P0E(SDI1) P11(SWP1) P12(SHOLD1)
External ROM Boot	P06(NCS0) P17(NRD) P30(NWRENWRL) P31(NHBNWRH) P16(NLBEXA0) P32(EXA01) P33(EXA02) P34(EXA03) P35(EXA06) P36(EXA05) P37(EXA06) P38(EXA07) P39(EXA08) P3A(EXA09) P3B(EXA10) P3C(EXA11) P3D(EXA12) P3E(EXA13) P3F(EXA14) P40(EXA15) P41(EXA16) P42(EXA17) P43(EXA18) P44(EXA19) P45(EXA20) P46(EXD00) P47(EXD01) P48(EXD02) P49(EXD03) P4A(EXD04) P4B(EXD05) P4C(EXD06) P4D(EXD07) P4E(EXD08) P4F(EXD09) P50(EXD10) P51(EXD11) P52(EXD12) P53(EXD13) P54(EXD14) P55(EXD15)
HI-z	SDCLK0 Hi-z state

(*) In this table, ”Pxx” means ”GPIOxx”. For example ”P2E” means ”GPIO2E”.

2-3 SDIF PullUp

In case of boot mode using SDIF port, internal PullUp resistor is used (SDCMD0, SDAT0[3:0] / SDCMD1, SDAT1[3:0]). So, external PullUp resistor is not required on board.

2-4 QSCS PullUp

In case of boot mode using QSCS, PullUp of GPIO03(QSCS) is active by the hard reset. After GPIO2E is set to high, GPIO03 set to QSCS and PullUp set to inactive.
In case of Hi-z boot, PullUp is forced to inactive

2-5 GPIO2F

During boot, GPIO2F is used as GPIO and indicates boot status and error occurrence by output of Low/High.
When errors occur during boot sequences, for example writing of IPL2, GPIO2F reports the sort of error. GPIO0F can indicate the status of USB connection and the completion of USB file transfer. And Delete Mode, completion of Erase, and status of Erase can be reported by sequence of Low/High.

For more detail about the behavior of ports used during boot, refer to the document LC823450 Series IPL specification.

3 Pin Assignment
3-1 Pin Assignment

I/O		Input Type		Output Type	
I	Input	CMOS	CMOS Input	3-State	Tristate Output
O	Output	schmitt	schmitt Input	OD	open drain Output
B	Bidirectional	X	Xtal	X	Xtal
P	power	3A	3.3V analog	3A	3.3V analog
NC	Non Connect	1A	1.0Vanalog	1A	1.0/1.2Vanalog

Drive (example)		PU/PD		IO Circuit Type	
4mA	3.3V 4mA Output	PU	pull-up resister	Refer to Page 34 for circuit diagram	
4/8mA	3.3V with 4mA, 8mA output drivability switch	PD	pull-down resister		
0.3mA-OD	1.0V 0.3mA open drain Output	PU/PD	pull-up, pull-down resister		

XBGA240		TQFP128L	WLP154		PIN NAME	I/O	Input Type	Output Type	Drive	PU/PD	IO Pwr Grp	IO Circuit Type
No.	Ball	No.	No	Ball								
1	R16	-	-		SDRDATA2	B	CMOS	3-State	2/4/8mA	PD	Vdd2	3ICD/3T2(4)(8)
2	N14	1	1	M11	Vss	G						
3	P15	2	2	N12	Vdd2	P						
4	P16	3	3	H8	TCLKA0/ BCK1/ GPIO00/ EXTINT00	I/ B/ B/ I	schmitt	3-State	1/2/4mA	PU/PD	Vdd2	3ISUD/3T1(2)(4)
5	N15	-	-		SDRDATA3	B	CMOS	3-State	2/4/8mA	PD	Vdd2	3ICD/3T2(4)(8)
6	N16	4	4	L10	TCLKB0/ LRCK1/ GPIO01/ EXTINT01	I/ B/ B/ I	schmitt	3-State	1/2/4mA	PU/PD	Vdd2	3ISUD/3T1(2)(4)
7	M16	-	5	K9	NHBNWRH/ TXD0/ GPIO31/ EXTINT31	O/ O/ B/ I	schmitt	3-State	2/4/8mA	PD	Vdd2	3ISD/3T2(4)(8)
8	M15	-	6	N11	NCS1/ RXD0/ GPIO10/ EXTINT10	O/ I/ B/ I	schmitt	3-State	2/4/8mA	PU	Vdd2	3ISU/3T2(4)(8)
9	M14	-	-		SDRDATA4	B	CMOS	3-State	2/4/8mA	PD	Vdd2	3ICD/3T2(4)(8)
10	M13	-	7	M10	NCS0/ GPIO06/ EXTINT06	O/ B/ I	schmitt	3-State	2/4/8mA	PU	Vdd2	3ISU/3T2(4)(8)
11	L16	-	-		GPIO2A/ EXTINT2A/ SDRADDR12	B/ I/ O	schmitt	3-State	2/4/8mA	PU/PD	Vdd2	3ISUD/3T2(4)(8)
12	L15	-	-		Vdd2	P						
13	L14	-	-		Vss	G						
14	L13	5	8	L9	Vdd1	P						
15	L12	-	9	N10	NRD/ GPIO17/ EXTINT17	O/ B/ I	schmitt	3-State	2/4/8mA	PD	Vdd2	3ISD/3T2(4)(8)
16	K16	-	-		SDRADDR5	O	-	3-State	2/4/8mA		Vdd2	3T2(4)(8)
17	K15	-	-		SDRADDR6	O	-	3-State	2/4/8mA		Vdd2	3T2(4)(8)
18	K14	-	10	M9	NWRENWRL/ GPIO30/ EXTINT30	O/ B/ I	schmitt	3-State	2/4/8mA	PD	Vdd2	3ISD/3T2(4)(8)