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# LC87F5N62B

**CMOS IC**
**FROM 66K byte, RAM 2048 byte on-chip**
# 8-bit 1-chip Microcontroller

ON Semiconductor®
http://onsemi.com

## Overview

The LC87F5N62B is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrate on a single chip a number of hardware features such as 66K-byte flash ROM (onboard rewritable), 2048byte RAM, Onchip debugging function, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, two synchronous SIO ports (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), four 12-bit PWM channels, an 8-bit 15-channel AD converter, a system clock frequency divider, and a 29-source 10-vector interrupt feature.

## Features

■Flash ROM
- Capable of on-board-programing with wide range, 2.7 to 5.5V, of voltage source
- Block-erase in 128-byte units
- 67584 × 8 bits ( Address: 00000H to 0FFFFH, 1F800H to 1FFFFH)

■RAM
- 2048 × 9 bits

■Minimum Bus Cycle Time
- 83.3ns (12MHz) $V_{DD}$=2.8 to 5.5V
- 125ns (8MHz) $V_{DD}$=2.5 to 5.5V
- 500ns (2MHz) $V_{DD}$=2.2 to 5.5V

Note: Bus cycle time indicates the speed to read ROM.

* This product is licensed from Silicon Storage Technology, Inc. (USA).

■Minimum Instruction Cycle Time (tCYC)

- 250ns (12MHz) $V_{DD}$=2.8 to 5.5V
- 375ns (8MHz) $V_{DD}$=2.5 to 5.5V
- 1.5μs (2MHz) $V_{DD}$=2.2 to 5.5V

■Ports

- Normal withstand voltage I/O ports
  - Ports whose I/O direction can be designated in 1-bit units: 64 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn, S2Pn, PWM0, PWM1, XT2)
  - Ports whose I/O direction can be designated in 2-bit units: 16 (PEn, PFn)
  - Ports whose I/O direction can be designated in 4-bit units: 8 (P0n)
- Normal withstand voltage input port: 1 (XT1)
- Dedicated oscillator ports: 2 (CF1, CF2)
- Reset pins: 1 ($\overline{RES}$)
- Power pins: 8 ($V_{SS}1$ to $V_{SS}4$, $V_{DD}1$ to $V_{DD}4$)

■Timers

- Timer 0: 16-bit timer/counter with a capture register
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture registers) ×2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture registers) + 8-bit counter (with an 8-bit capture registers)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with 16-bit capture registers)
  - Mode 3: 16-bit counter (with 16-bit capture registers)
- Timer 1: 16-bit timer/counter that support PWM/toggle output
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter(with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also from the lower-order 8-bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes.

■High-speed Clock Counter

1) Can count clocks with a maximum clock rate of 24MHz (at a main clock of 12MHz).
2) Can generate output real-time.

■SIO

- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO2: 8 bit synchronous serial interface
  1) LSB first mode
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 32 bytes)

■UART: 2 channels
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bit in continuous transmission mode)
- Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

■AD Converter: 8 bits × 15 channels

■PWM: Multifrequency 12-bit PWM × 4 channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
2) Able to output oscillation clock of sub clock.

■Interrupts
- 29 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|---|---|---|---|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4 |
| 4 | 0001BH | H or L | INT3/INT5/base timer0/base timer1 |
| 5 | 00023H | H or L | T0H/INT6 |
| 6 | 0002BH | H or L | T1L/T1H/INT7 |
| 7 | 00033H | H or L | SIO0/UART1 receive/UART2 receive |
| 8 | 0003BH | H or L | SIO/SIO2/UART1 transmit/UART2 transmit |
| 9 | 00043H | H or L | ADC/T6/T7/PWM4, PWM5 |
| 10 | 0004BH | H or L | Port 0/T4/T5/PWM0, PWM1 |

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 1024 levels maximum (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions
- 16-bits × 8-bits (5 tCYC execution time)
- 24-bits × 16-bits (12 tCYC execution time)
- 16-bits ÷ 8-bits (8 tCYC execution time)
- 24-bits ÷ 16-bits (12 tCYC execution time)

■Oscillation Circuits
- RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf
- Crystal oscillation circuit : For low-speed system clock
- Multifrequency RC oscillation circuit (internal) : For system clock

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0µs, 2.0µs, 4.0µs, 8.0µs, 16.0µs, 32.0µs, and 64.0µs (at a main clock rate of 12MHz).

■Standby Function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the HOLD mode is entered is retained.
  3) There are four ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit

■On-chip Debugger Function
- Permits software debugging with the test device installed on the target board.

■Package Form
- QIP100E (14 × 20) : “Lead-free type”

■Development Tools
- Evaluation (EVA) chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875C00 + POD100QFP
  ICE-B877300 + SUB875C00 + POD100QFP
- On-chip-debugger : TCB87-TypeB + LC87F5NC8A or LC87F5N62B

■Programming Boards

| Package | Programming boards |
|---|---|
| QIP100E (14 × 20) | W87F52256Q |

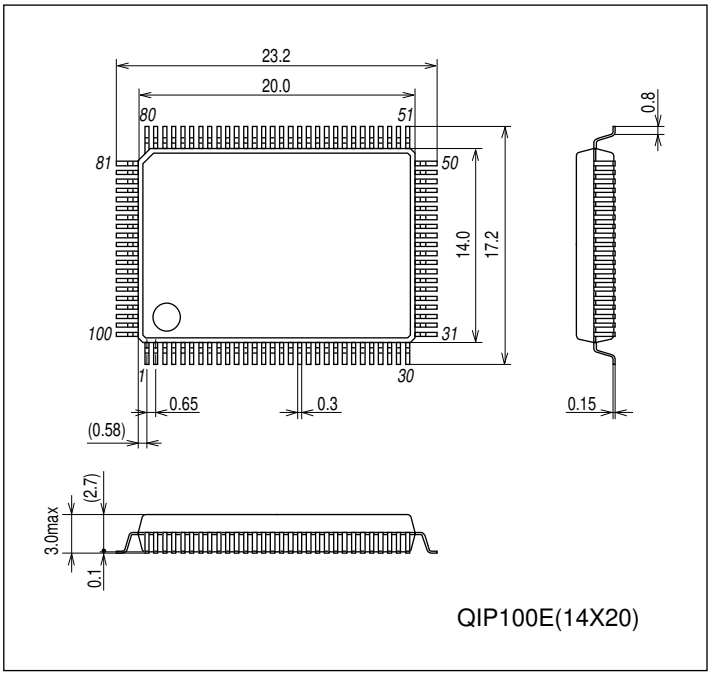
■Flash ROM Programmer

| Maker | Model | Support version(Note) | Device |
|---|---|---|---|
| Flash Support Group, Inc. (Single) | AF9708/09/09B (including product of Ando Electric Co.,Ltd) | Revision : After Rev.02.73 | LC87F76C8A |
| Flash Support Group, Inc.(Gang) | AF9723(Main body) (including product of Ando Electric Co.,Ltd) | Revision : After Rev.02.29 | LC87F5NC8A |
| | AF9833(Unit) (including product of Ando Electric Co.,Ltd) | Revision : After Rev.01.88 | |
| Our company | SKK/SKK Type-B/SKK DBG Type-B (SANYO FWS) | Application Version: After 1.04 Chip Data Version: After2.14 | LC87F5NC8A |

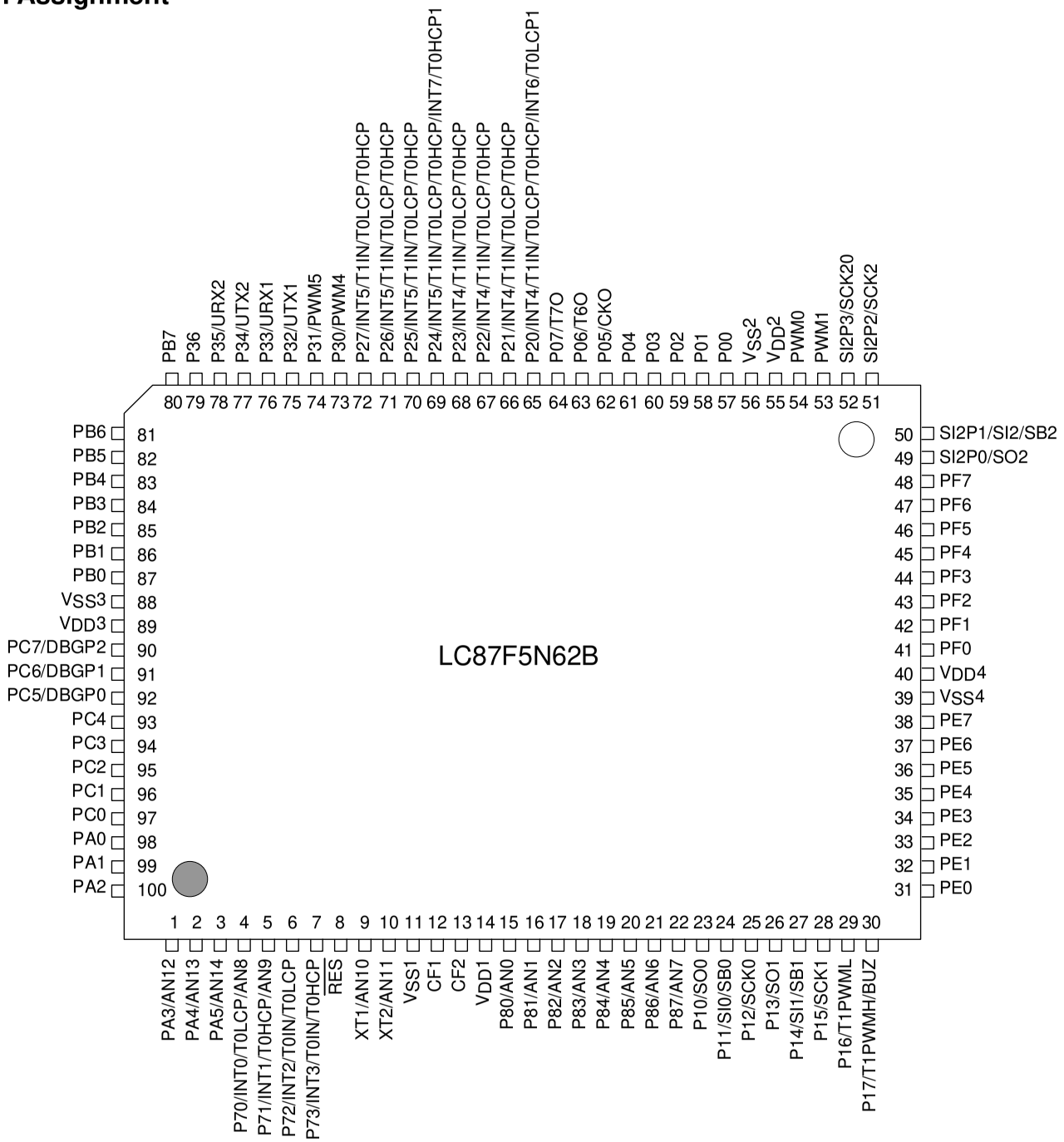
## Package Dimensions

unit : mm (typ)

3151A



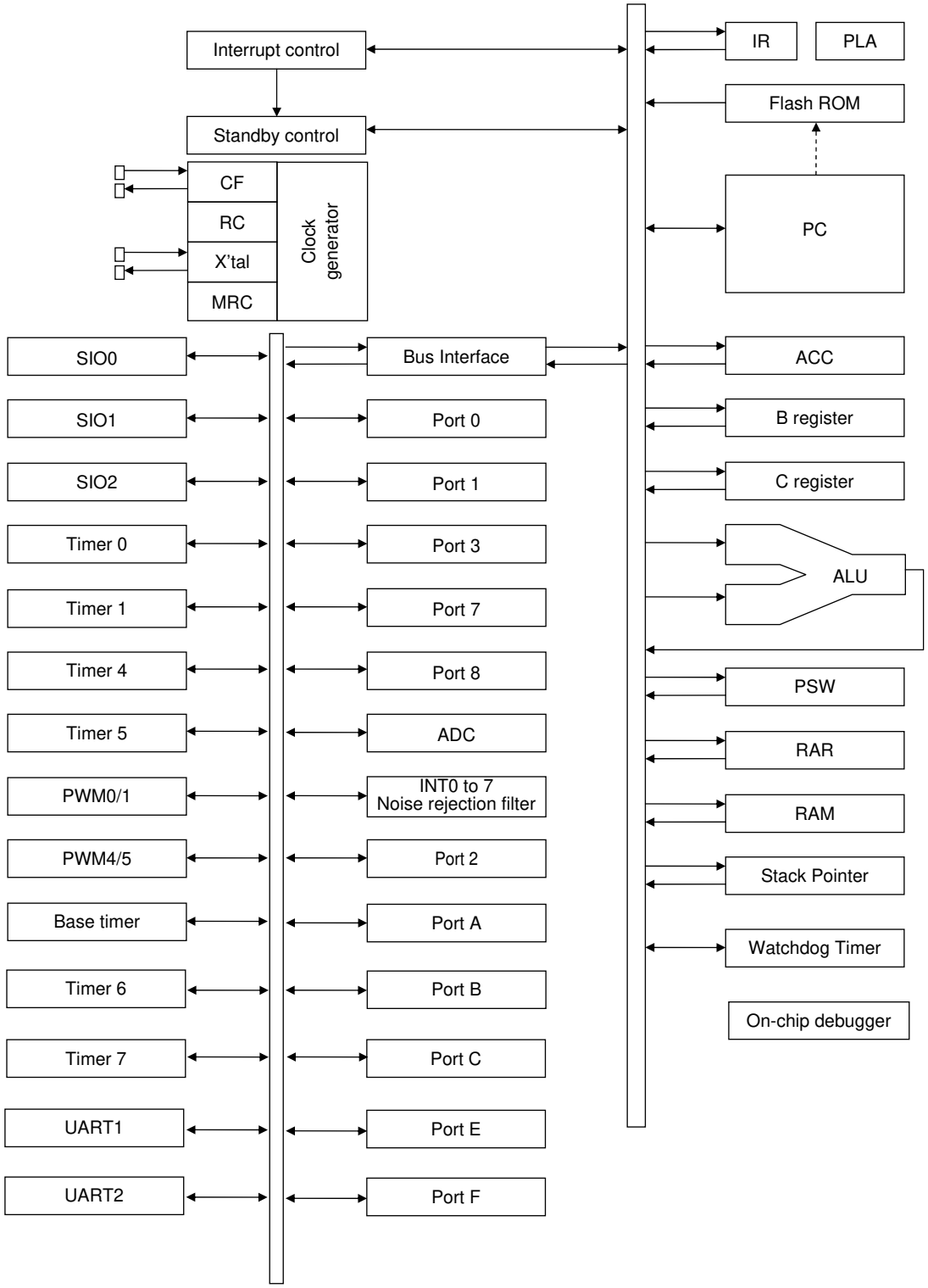
## Pin Assignment




Top view

QIP100E(14×20) “Lead-free Type”

## System Block Diagram



## Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$<br>$V_{SS}3$, $V_{SS}4$</td><td>-</td><td>- Power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$<br>$V_{DD}3$, $V_{DD}4$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>Port 0<br>P00 to P07</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 4-bit units<br>• Pull-up resistor can be turned on and off in 4-bit units<br>• HOLD release input<br>• Port 0 interrupt input<br>• Pin functions<br>P05: System clock output<br>P06: Timer 6 toggle output<br>P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1<br>P10 to P17</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units<br>• Pin functions<br>P10: SIO0 data output<br>P11: SIO0 data input, bus I/O<br>P12: SIO0 clock I/O<br>P13: SIO1 data output<br>P14: SIO1 data input, bus I/O<br>P15: SIO1 clock I/O<br>P16: Timer 1 PWML output<br>P17: Timer 1 PWMH output, Beeper output</td><td>Yes</td></tr>
<tr><td>Port 2<br>P20 to P27</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units<br>• Other functions<br>P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input/INT6 input/timer 0L capture 1 input<br>P21 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input<br>P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input/INT7 input/timer 0H capture 1 input<br>P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input<br>• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/<br>Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3<br>P30 to P36</td><td>I/O</td><td>• 7-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units<br>• Pin functions<br>P30: PWM4 output<br>P31: PWM5 output<br>P32: UART1 transmit<br>P33: UART1 receive<br>P34: UART2 transmit<br>P35: UART2 receive</td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7<br>P70 to P73</td><td>I/O</td><td>• 4-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units<br>• Other functions<br>P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer<br>P71: INT1 input/HOLD release input/Timer 0H capture input<br>P72: INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input<br>P73: INT3 input with noise filter/Timer 0 event input/Timer 0H capture input<br>• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/<br>Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
• AD converter input port: AN8 (P70), AN9 (P71)</td><td>No</td></tr>
<tr><td>Port 8<br>P80 to P87</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Other functions<br>P80 to P87: AD converter input port</td><td>No</td></tr>
<tr><td>Port A<br>PA0 to PA5</td><td>I/O</td><td>• 6-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port B<br>PB0 to PB7</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units</td><td>Yes</td></tr>
<tr><td>Port C<br>PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units<br>• Pin functions<br>DBGP0 to DBGP2 (PC5 to PC7): On-chip Debugger</td><td>Yes</td></tr>
<tr><td>Port E<br>PE0 to PE7</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 2-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units</td><td>No</td></tr>
<tr><td>Port F<br>PF0 to PF7</td><td>I/O</td><td>• 8-bit I/O port<br>• I/O specifiable in 2-bit units<br>• Pull-up resistor can be turned on and off in 1-bit units</td><td>No</td></tr>
<tr><td>SIO2 Port<br>SI2P0 to SI2P3</td><td>I/O</td><td>• 4-bit I/O port<br>• I/O specifiable in 1-bit units<br>• Shared functions:<br>SI2P0: SIO2 data output<br>SI2P1: SIO2 data input, bus input/output<br>SI2P2: SIO2 clock input/output<br>SI2P3: SIO2 clock output</td><td>No</td></tr>
<tr><td>PWM0, PWM1</td><td>O</td><td>• PWM0, PWM1 output port<br>• General-purpose I/O available</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>• Input terminal for 32.768kHz X'tal oscillation<br>• Shared functions:<br>AN10: AD converter input port<br>General-purpose input port<br>Must be connected to $V_{DD}1$ if not to be used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• Output terminal for 32.768kHz X'tal oscillation<br>• Shared functions:<br>AN11: AD converter input port<br>General-purpose I/O port<br>Must be set for oscillation and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>I</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>O</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

## Port Output Types

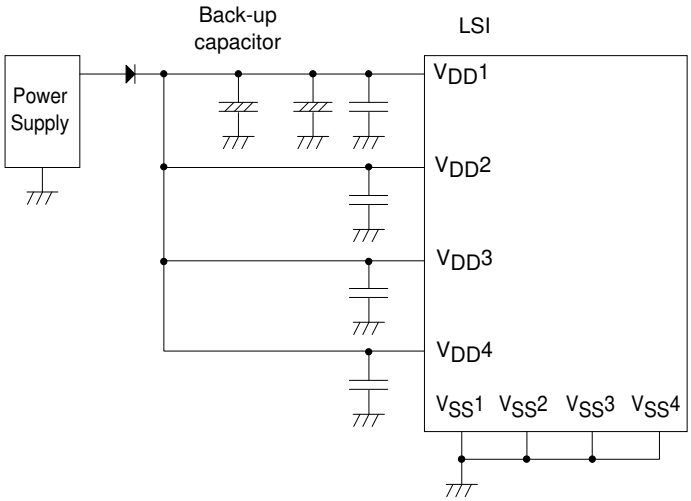
The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

| Port | Options Selected in Units of | Option Type | Output Type | Pull-up Resistor |
|---|---|---|---|---|
| P00 to P07 | 1 bit | 1 | CMOS | Programmable (Note 1) |
| | | 2 | N-channel open drain | No |
| P10 to P17 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| P20 to P27 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| P30 to P36 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| P70 | - | No | N-channel open drain | Programmable |
| P71 to P73 | - | No | CMOS | Programmable |
| P80 to P87 | - | No | N-channel open drain | No |
| PA0 to PA5 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| PB0 to PB7 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| PC0 to PC7 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| PE0 to PE7 | - | No | CMOS | Programmable |
| PF0 to PF7 | - | No | CMOS | Programmable |
| SI2P0, SI2P2 SI2P3 | - | No | CMOS | No |
| SI2P1 | - | No | CMOS (when selected as ordinary port)<br>N-channel open drain (When SIO2 data is selected) | No |
| PWM0, PWM1 | - | No | CMOS | No |
| XT1 | - | No | Input only | No |
| XT2 | - | No | Output for 32.768kHz quartz oscillator<br>N-channel open drain (when in general-purpose No output mode) | No |

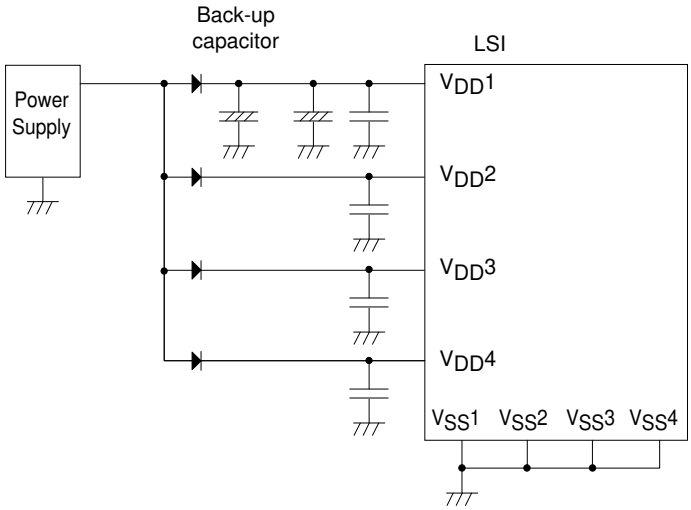
Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

*1: Make the following connection to minimize the noise input to the $V_{DD}1$ pin and prolong the backup time.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, $V_{SS}3$ and $V_{SS}4$ pins.

(Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.




## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

| Parameter | | Symbol | Pins/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Maximum Supply voltage | | $V_{DD}$ max | $V_{DD}1$, $V_{DD}2$, $V_{DD}3$, $V_{DD}4$ | $V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$ | | -0.3 | | +6.5 | V |
| Input voltage | | $V_I$(1) | XT1, CF1 | | | -0.3 | | $V_{DD}$+0.3 | |
| Input/Output Voltage | | $V_{IO}$(1) | Ports 0, 1, 2<br>Ports 3, 7, 8<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3<br>PWM0, PWM1, XT2 | | | -0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1, 2, 3<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3 | CMOS output select per 1 application pin | | -10 | | | mA |
| | | IOPH(2) | PWM0, PWM1 | Per 1 application pin. | | -20 | | | |
| | | IOPH(3) | P71 to P73 | Per 1 application pin. | | -5 | | | |
| | Average output current (Note1-1) | IOMH(1) | Ports 0, 1, 2, 3<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3 | CMOS output select per 1 application pin | | -7.5 | | | |
| | | IOMH(2) | PWM0, PWM1 | Per 1 application pin. | | -10 | | | |
| | | IOMH(3) | P71 to P73 | Per 1 application pin. | | -3 | | | |
| | Total output current | ΣIOAH(1) | P71 to P73 | Total of all applicable pins | | -10 | | | |
| | | ΣIOAH(2) | PWM0, PWM1<br>SI2P0 to SI2P3 | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(3) | Port 0 | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(4) | Port 0<br>PWM0, PWM1<br>SI2P0 to SI2P3 | Total of all applicable pins | | -45 | | | |
| | | ΣIOAH(5) | Ports 2, 3, B | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(6) | Ports A, C | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(7) | Ports 2, 3, A, B, C | Total of all applicable pins | | -45 | | | |
| | | ΣIOAH(8) | Port F | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(9) | Ports 1, E | Total of all applicable pins | | -25 | | | |
| | | ΣIOAH(10) | Ports 1, E, F | Total of all applicable pins | | -45 | | | |

Note 1-1: Average output current is average of current in 100ms interval.

Continued on next page.

Continued from preceding page.

| Parameter | | Symbol | Pins/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$[V] | min | typ | max | unit |
| Low level output current | Peak output current | IOPL(1) | P02 to P07<br>Ports 1, 2, 3<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3<br>PWM0, PWM1 | Per 1 application pin. | | | | 20 | mA |
| | | IOPL(2) | P00, P01 | Per 1 application pin. | | | | 30 | |
| | | IOPL(3) | Ports 7, 8, XT2 | Per 1 application pin. | | | | 10 | |
| | Average output current (Note1-1) | IOML(1) | P02 to P07<br>Ports 1, 2, 3<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3<br>PWM0, PWM1 | Per 1 application pin. | | | | 15 | |
| | | IOML(2) | P00, P01 | Per 1 application pin. | | | | 20 | |
| | | IOML(3) | Ports 7, 8, XT2 | Per 1 application pin. | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | Port 7, XT2 | Total of all applicable pins | | | | 15 | |
| | | ΣIOAL(2) | Port 8 | Total of all applicable pins | | | | 15 | |
| | | ΣIOAL(3) | Ports 7, 8, XT2 | Total of all applicable pins | | | | 20 | |
| | | ΣIOAL(4) | PWM0, PWM1<br>SI2P0 to SI2P3 | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(5) | Port 0 | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(6) | Port 0<br>PWM0, PWM1<br>SI2P0 to SI2P3 | Total of all applicable pins | | | | 80 | |
| | | ΣIOAL(7) | Ports 2, 3, B | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(8) | Ports A, C | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(9) | Ports 2, 3, A, B, C | Total of all applicable pins | | | | 80 | |
| | | ΣIOAL(10) | Port F | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(11) | Ports 1, E | Total of all applicable pins | | | | 45 | |
| | | ΣIOAL(12) | Ports 1, E, F | Total of all applicable pins | | | | 80 | |
| Maximum power dissipation | | Pd max | QIP100E(14×20) | Ta=-40 to +85°C | | | | 320 | mW |
| Operating ambient temperature | | Topr | | | | -40 | | +85 | °C |
| Storage ambient temperature | | Tstg | | | | -55 | | +125 | |

Note 1-1: Average output current is average of current in 100ms interval.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Recommended Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

| Parameter | Symbol | Pins/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Operating supply voltage (Note2-1) | $V_{DD}(1)$ | $V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$ | 0.245µs≤ tCYC≤200µs | | 2.8 | | 5.5 | V |
| | | | 0.367µs≤ tCYC≤200µs | | 2.5 | | 5.5 | |
| | | | 1.470µs≤ tCYC≤200µs | | 2.2 | | 5.5 | |
| Memory sustaining supply voltage | VHD | $V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$ | RAM and register contents in HOLD mode. | | 2.0 | | 5.5 | |
| High level input voltage | $V_{IH}(1)$ | Ports 1, 2, 3<br>SI2P0 to SI2P3<br>P71 to P73<br>P70 port input/ interrupt side | | 2.2 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(2)$ | Ports 0, 8<br>Ports A, B, C, E, F<br>PWM0, PWM1 | | 2.2 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(3)$ | P70 Watchdog timer side | | 2.2 to 5.5 | $0.9V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}(4)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.2 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | Ports 1, 2, 3<br>SI2P0 to SI2P3<br>P71 to P73<br>P70 port input/ interrupt | | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}$ +0.4 | |
| | | | | 2.2 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(2)$ | Ports 0, 8<br>Ports A, B, C, E, F<br>PWM0, PWM1 | | 2.5 to 5.5 | $V_{SS}$ | | $0.15V_{DD}$ +0.4 | |
| | | | | 2.2 to 5.5 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(5)$ | Port 70 Watchdog Timer | | 2.5 to 5.5 | $V_{SS}$ | | $0.8V_{DD}$ -1.0 | |
| | $V_{IL}(6)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.5 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time | tCYC (Note2-2) | | | 2.8 to 5.5 | 0.245 | | 200 | µs |
| | | | | 2.5 to 5.5 | 0.367 | | 200 | |
| | | | | 2.2 to 5.5 | 1.470 | | 200 | |
| External system clock frequency | FEXCF(1) | CF1 | • CF2 pin open<br>• System clock frequency division rate=1/1<br>• External system clock duty=50±5% | 2.8 to 5.5 | 0.1 | | 12 | MHz |
| | | | | 2.5 to 5.5 | 0.1 | | 8 | |
| | | | | 2.2 to 5.5 | 0.1 | | 2 | |
| | | | • CF2 pin open<br>• System clock frequency division rate=1/2 | 2.8 to 5.5 | 0.2 | | 24.4 | |
| | | | | 2.5 to 5.5 | 0.2 | | 16 | |
| | | | | 2.2 to 5.5 | 0.2 | | 4 | |
| Oscillation frequency Range (Note2-3) | FmCF(1) | CF1, CF2 | 12MHz ceramic oscillation See Fig. 1. | 2.8 to 5.5 | | 12 | | MHz |
| | FmCF(2) | CF1, CF2 | 8MHz ceramic oscillation See Fig. 1. | 2.5 to 5.5 | | 8 | | |
| | FmCF(3) | CF1, CF2 | 4MHz ceramic oscillation See Fig. 1. | 2.2 to 5.5 | | 4 | | |
| | FmRC | | Internal RC oscillation | 2.2 to 5.5 | 0.3 | 1.0 | 2.0 | |
| | FmMRC | | Frequency variable RC oscillation source oscillation | 2.2 to 5.5 | | 16 | | |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal oscillation. See Fig. 2. | 2.2 to 5.5 | | 32.768 | | kHz |

Note 2-1: $V_{DD}$ must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

## Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| High level input current | $I_{IH}(1)$ | Ports 0, 1, 2<br>Ports 3, 7, 8<br>Ports A, B, C<br>SI2P0 to SI2P3<br>$\overline{RES}$<br>PWM0, PWM1 | Output disable<br>Pull-up resistor OFF<br>$V_{IN}=V_{DD}$<br>(including the off-leak current of the output Tr.) | 2.2 to 5.5 | | | 1 | μA |
| | $I_{IH}(2)$ | XT1, XT2 | Using as an input port<br>$V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 1 | |
| | $I_{IH}(3)$ | CF1 | $V_{IN}=V_{DD}$ | 2.2 to 5.5 | | | 15 | |
| Low level input current | $I_{IL}(1)$ | Ports 0, 1, 2<br>Ports 3, 7, 8<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3<br>$\overline{RES}$<br>PWM0, PWM1 | Output disable<br>Pull-up resistor OFF<br>$V_{IN}=V_{SS}$<br>(including the off-leak current of the output Tr.) | 2.2 to 5.5 | -1 | | | |
| | $I_{IL}(2)$ | XT1, XT2 | Using as an input port<br>$V_{IN}=V_{SS}$ | 2.2 to 5.5 | -1 | | | |
| | $I_{IL}(3)$ | CF1 | $V_{IN}=V_{SS}$ | 2.2 to 5.5 | -15 | | | |
| High level output voltage | $V_{OH}(1)$ | Ports 0, 1, 2, 3<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3 | $I_{OH}$=-1.0mA | 4.5 to 5.5 | $V_{DD}$-1 | | | V |
| | $V_{OH}(2)$ | | $I_{OH}$=-0.4mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(3)$ | | $I_{OH}$=-0.2mA | 2.2 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(4)$ | Ports 71, 72, 73 | $I_{OH}$=-0.4mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(5)$ | | $I_{OH}$=-0.2mA | 2.2 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(6)$ | PWM0, PWM1<br>P30, P31(PWM4, 5 output mode) | $I_{OH}$=-10mA | 4.5 to 5.5 | $V_{DD}$-1.5 | | | |
| | $V_{OH}(7)$ | | $I_{OH}$=-1.6mA | 3.0 to 5.5 | $V_{DD}$-0.4 | | | |
| | $V_{OH}(8)$ | | $I_{OH}$=-1.0mA | 2.2 to 5.5 | $V_{DD}$-0.4 | | | |
| Low level output voltage | $V_{OL}(1)$ | Ports 0, 1, 2, 3<br>Ports A, B, C, E, F<br>SI2P0 to SI2P3<br>PWM0, PWM1, | $I_{OL}$=10mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(2)$ | | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(3)$ | | $I_{OL}$=1.0mA | 2.2 to 5.5 | | | 0.4 | |
| | $V_{OL}(4)$ | P00, P01 | $I_{OL}$=30mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(5)$ | | $I_{OL}$=5.0mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(6)$ | | $I_{OL}$=2.5mA | 2.2 to 5.5 | | | 0.4 | |
| | $V_{OL}(7)$ | Ports 7, 8, XT2 | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(8)$ | | $I_{OL}$=1.0mA | 2.2 to 5.5 | | | 0.4 | |
| Pull-up resistation | Rpu(1) | Ports 0, 1, 2, 3<br>Port 7<br>Ports A, B, C, E, F | $V_{OH}=0.9V_{DD}$ | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | Rpu(2) | | | 2.2 to 5.5 | 15 | 35 | 120 | |
| Hysteresis voltage | VHYS | $\overline{RES}$<br>Ports 1, 2, 7<br>SI2P0 to SI2P3 | | 2.2to 5.5 | | $0.1V_{DD}$ | | V |
| Pin capacitance | CP | All pins | • For pins other than that under test: $V_{IN}=V_{SS}$<br>• f=1MHz<br>• Ta=25°C | 2.2 to 5.5 | | 10 | | pF |

## Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | | Symbol | Pins /Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | • See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | | | tSCKHA(1a) | | • Continuous data transmission/reception mode<br>• SIO2 is not in use simultaneous.<br>• See Fig. 6.<br>• (Note 4-1-2) | | 4 | | | |
| | | | tSCKHA(1b) | | • Continuous data transmission/reception mode<br>• SIO2 is in use simultaneous.<br>• See Fig. 6.<br>• (Note 4-1-2) | | 6 | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • CMOS output selected.<br>• See Fig. 6. | 2.2 to 5.5 | 4/3 | | | tCYC |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(2) | | | | 1/2 | | | |
| | | | tSCKHA(2a) | | • Continuous data transmission/reception mode<br>• SIO2 is not in use simultaneous.<br>• CMOS output selected.<br>• See Fig. 6. | | tSCKH(2) +2tCYC | | tSCKH(2) +(10/3) tCYC | tCYC |
| | | | tSCKHA(2b) | | • Continuous data transmission/reception mode<br>• SIO2 is in use simultaneous.<br>• CMOS output selected.<br>• See Fig. 6. | | tSCKH(2) +2tCYC | | tSCKH(2) +(16/3) tCYC | |
| Serial input | Data setup time | | tsDI(1) | SI0(P11), SB0(P11) | • Must be specified with respect to rising edge of SIOCLK<br>• See fig. 6. | 2.2 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(1) | | | | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdD0(1) | SO0(P10), SB0(P11), | • Continuous data transmission/reception mode<br>• (Note 4-1-3) | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | |
| | | | tdD0(2) | | • Synchronous 8-bit mode.<br>• (Note 4-1-3) | | | | 1tCYC +0.05 | |
| | Output clock | | tdD0(3) | | • (Note 4-1-3) | | | | (1/3)tCYC +0.05 | |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | | Symbol | Pins/ Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | • See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • CMOS output selected.<br>• See Fig. 6. | 2.2 to 5.5 | 2 | | | |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(2) | SI1(P14), SB1(P14) | • Must be specified with respect to rising edge of SIOCLK<br>• See fig. 6. | 2.2 to 5.5 | 0.03 | | | µs |
| | Data hold time | | thDI(2) | | | | 0.03 | | | |
| Serial output | Output delay time | | tdD0(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 6. | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

### 3. SIO2 Serial I/O Characteristics (Note 4-3-1)

| Parameter | | | Symbol | Pins/ Remarks | Conditions | $V_{DD}$[V] | Specification min. | typ | max. | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(5) | SCK2 (SI2P2) | • See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(5) | | | | 1 | | | |
| | | High level pulse width | tSCKH(5) | | | | 1 | | | |
| | | | tSCKHA(5a) | | • Continuous data transmission/ reception mode of SIO0 is not in use simultaneous.<br>• See Fig. 6.<br>• (Note 4-3-2) | | 4 | | | |
| | | | tSCKHA(5b) | | • Continuous data transmission/ reception mode of SIO0 is in use simultaneous.<br>• See Fig. 6.<br>• (Note 4-3-2) | | 7 | | | |
| | Output clock | Frequency | tSCK(6) | SCK2 (SI2P2), SCK2O (SI2P3) | • CMOS output selected.<br>• See Fig. 6. | 2.2 to 5.5 | 4/3 | | | tSCK |
| | | Low level pulse width | tSCKL(6) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(6) | | | | 1/2 | | | |
| | | | tSCKHA(6a) | | • Continuous data transmission/ reception mode of SIO0 is not in use simultaneous.<br>• CMOS output selected.<br>• See Fig. 6. | | tSCKH(6) +(5/3)tCYC | | tSCKH(6) +(10/3)tCYC | tCYC |
| | | | tSCKHA(6b) | | • Continuous data transmission/ reception mode of SIO0 is in use simultaneous.<br>• CMOS output selected.<br>• See Fig. 6. | | tSCKH(6) +(5/3)tCYC | | tSCKH(6) +(19/3)tCYC | |
| Serial input | Data setup time | | tsDI(3) | SI2(SI2P1), SB2(SI2P1) | • Must be specified with respect to rising edge of SIOCLK<br>• See fig. 6. | 2.2 to 5.5 | 0.03 | | | µs |
| | Data hold Time | | thDI(3) | | | | 0.03 | | | |
| Serial output | Output delay time | | tdD0(5) | SO2 (SI2P0), SB2(SI2P1) | • Must be specified with respect to falling edge of SIOCLK<br>• Must be specified as the time to the beginning of output state change in open drain output mode.<br>• See Fig. 6. | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | |

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input , a time from SI2RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

## Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70),<br>INT1(P71),<br>INT2(P72)<br>INT4(P20 to P23),<br>INT5(P24 to P27),<br>INT6(P20)<br>INT7(P24) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 or 1 are enabled. | 2.2 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3(P73) when noise filter time constant is 1/1. | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3(P73)(The noise rejection clock is selected to 1/32.) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 64 | | | |
| | tPIH(4)<br>tPIL(4) | INT3(P73)(The noise rejection clock is selected to 1/128.) | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{RES}$ | Reset acceptable. | 2.2 to 5.5 | 200 | | | µs |

## AD Converter Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Resolution | N | AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2), AN12(PA3), AN13(PA4), AN14(PA5) | | 3.0 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2) | 4.5 to 5.5 | 11.74 (tCYC= 0.367µs) | | 97.92 (tCYC= 3.06µs) | µs |
| | | | | 3.0 to 5.5 | 23.53 (tCYC= 0.735µs) | | 97.92 (tCYC= 3.06µs) | |
| | | | AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2) | 4.5 to 5.5 | 15.68 (tCYC= 0.245µs) | | 97.92 (tCYC= 1.53µs) | |
| | | | | 3.0 to 5.5 | 23.49 (tCYC= 0.367µs) | | 97.92 (tCYC= 1.53µs) | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | µA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | -1 | | | |

Note 6-1: The quantization error (±1/2 LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

## Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

| Parameter | Symbol | Pins/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Normal mode consumption current (Note 7-1) | IDDOP(1) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$ | • FmCF=12MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio. | 4.5 to 5.5 | | 9.3 | 20.5 | mA |
| | | | | 2.8 to 4.5 | | 5.4 | 14.8 | |
| | IDDOP(2) | | • FmCF=8MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to 8MHz side<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio. | 4.5 to 5.5 | | 6.9 | 15.5 | |
| | IDDOP(3) | | | 2.5 to 4.5 | | 3.9 | 11 | |
| | IDDOP(4) | | • FmCF=4MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to 4MHz side<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio. | 4.5 to 5.5 | | 2.75 | 6.6 | |
| | IDDOP(5) | | | 2.2 to 4.5 | | 1.45 | 4.2 | |
| | IDDOP(6) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to internal RC oscillation<br>• frequency variable RC oscillation stopped<br>•1/2 frequency division ratio. | 4.5 to 5.5 | | 1 | 4.8 | |
| | IDDOP(7) | | | 2.2 to 4.5 | | 0.55 | 3.3 | |
| | IDDOP(8) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz by crystal oscillation mode.<br>• System clock set to 1MHz with frequency variable RC oscillation<br>• Internal RC oscillation stopped<br>• 1/2 frequency division ratio. | 4.5 to 5.5 | | 1.3 | 5.7 | |
| | IDDOP(9) | | | 2.2 to 4.5 | | 0.7 | 4.6 | |
| | IDDOP(10) | | • FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz by crystal oscillation mode.<br>• System clock set to 32.768kHz side.<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/2 frequency division ratio. | 4.5 to 5.5 | | 40 | 120 | µA |
| | IDDOP(11) | | | 2.2 to 4.5 | | 20 | 77 | |
| HALT mode consumption current (Note 7-1) | IDDHALT(1) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$ | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio. | 4.5 to 5.5 | | 3.6 | 8.3 | mA |
| | | | | 2.8 to 5.5 | | 2.1 | 4.4 | |
| | IDDHALT(2) | | • HALT mode<br>• FmCF=8MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to 8MHz side<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio. | 4.5 to 5.5 | | 2.7 | 5.8 | |
| | IDDHALT(3) | | | 2.5 to 4.5 | | 1.4 | 3.1 | |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| HALT mode consumption current (Note 7-1) | IDDHALT(4) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$ | • HALT mode<br>• FmCF=4MHz ceramic oscillation mode<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to 4MHz side<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/1 frequency division ratio. | 4.5 to 5.5 | | 1.1 | 2.6 | mA |
| | IDDHALT(5) | | | 2.2 to 4.5 | | 0.57 | 1.5 | |
| | IDDHALT(6) | | • HALT mode<br>• FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz by crystal oscillation mode<br>• System clock set to internal RC oscillation<br>• frequency variable RC oscillation stopped<br>•1/2 frequency division ratio. | 4.5 to 5.5 | | 0.38 | 1.0 | |
| | IDDHALT(7) | | | 2.2 to 4.5 | | 0.19 | 0.8 | |
| | IDDHALT(8) | | • HALT mode<br>• FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz by crystal oscillation mode.<br>• System clock set to 1MHz with frequency variable RC oscillation<br>• Internal RC oscillation stopped<br>• 1/2 frequency division ratio. | 4.5 to 5.5 | | 1.15 | 4.2 | |
| | IDDHALT(9) | | | 2.2 to 4.5 | | 0.57 | 3.0 | |
| | IDDHALT(10) | | • HALT mode<br>• FmCF=0Hz (oscillation stopped)<br>• FmX'tal=32.768kHz by crystal oscillation mode.<br>• System clock set to 32.768kHz side.<br>• Internal RC oscillation stopped<br>• frequency variable RC oscillation stopped<br>• 1/2 frequency division ratio. | 4.5 to 5.5 | | 20 | 77 | µA |
| | IDDHALT(11) | | | 2.2 to 4.5 | | 6 | 70 | |
| HOLD mode consumption current | IDDHOLD(1) | $V_{DD}1$ | • HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 0.04 | 19 | |
| | IDDHOLD(2) | | | 2.2 to 4.5 | | 0.02 | 14 | |
| Timer HOLD mode consumption current | IDDHOLD(3) | | • Timer HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• FmX'tal=32.768kHz by crystal oscillation mode | 4.5 to 5.5 | | 17 | 70 | |
| | IDDHOLD(4) | | | 2.2 to 4.5 | | 4 | 55 | |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

## F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

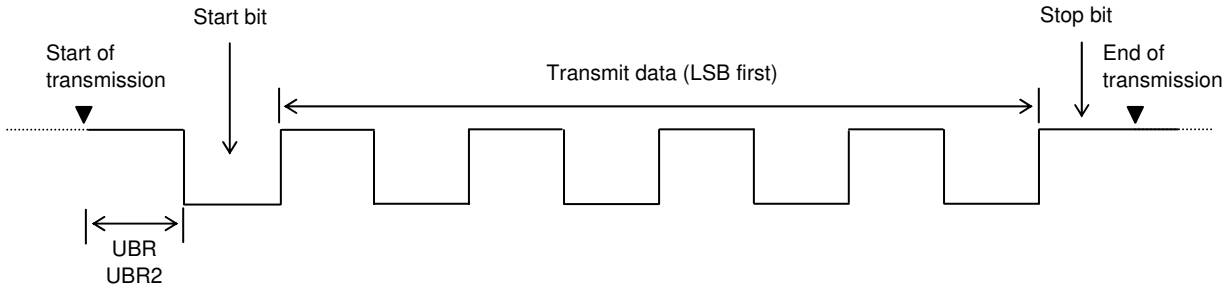
| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | $V_{DD}1$ | • Without CPU current | 2.7 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | • Erasing | 2.7 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | • programming | 2.7 to 5.5 | | 40 | 60 | µs |

## UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

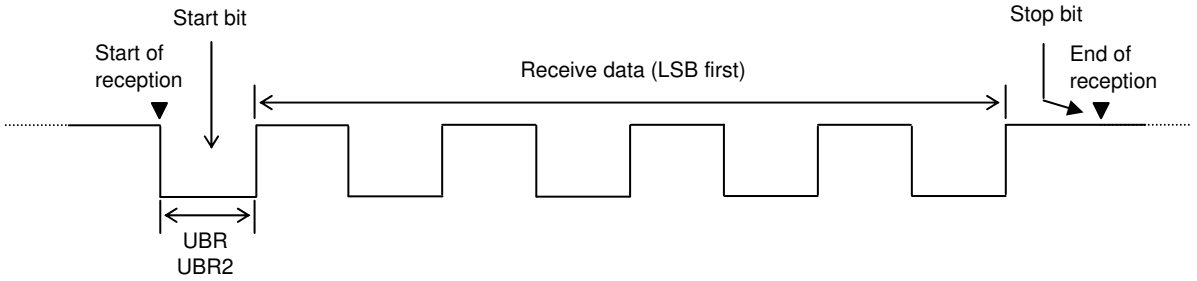
| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Transfer rate | UBR, UBR2 | UTX1(P32), RTX1(P33), UTX2(P33), RTX2(P34) | | 2.5 to 5.5 | 16/3 | | 8192/3 | tCYC |

Data length : 7/8/9 bits (LSB first)
Stop bits : 1-bit (2-bit in continuous data transmission)
Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



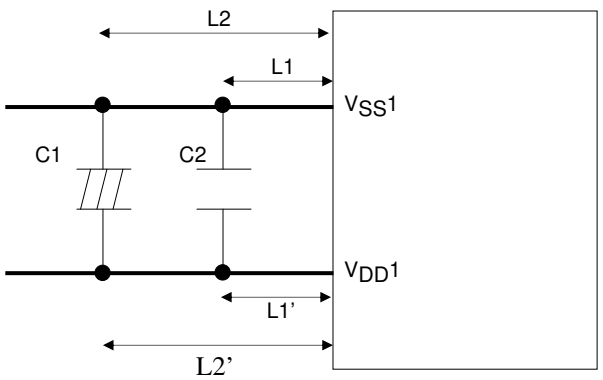

Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)




## $V_{DD}1$, $V_{SS}1$ Terminal Condition

It is necessary to place capacitors between $V_{DD}1$ and $V_{SS}1$ as describe below.

- Place capacitors as close to $V_{DD}1$ and $V_{SS}1$ as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- Capacitance of C2 must be more than 0.1µF.
- Use thicker pattern for $V_{DD}1$ and $V_{SS}1$.



## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rf1 [Ω] | Rd1 [Ω] | | typ [ms] | max [ms] | |
| 12MHz | MURATA | CSTCE12M0G52-R0 | (10) | (10) | Open | 470 | 2.5 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| 10MHz | | CSTCE10M0G52-R0 | (10) | (10) | Open | 680 | 2.4 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| | | CSTLS10M0G53-B0 | (15) | (15) | Open | 680 | 2.5 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| 8MHz | | CSTCE8M00G52-R0 | (10) | (10) | Open | 1k | 2.3 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| | | CSTLS8M00G53-B0 | (15) | (15) | Open | 1k | 2.5 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| 4MHz | | CSTCR4M00G53-R0 | (15) | (15) | Open | 1.5k | 2.2 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| | | CSTLS4M00G53-B0 | (15) | (15) | Open | 1.5k | 2.2 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after $V_{DD}$ goes above the operating voltage lower limit (see Fig. 4).

## Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C3 [pF] | C4 [pF] | Rf2 [Ω] | Rd2 [Ω] | | typ [s] | max [s] | |
| 32.768kHz | EPSON TOYOCOM | MC-306 | 18 | 18 | Open | 560k | 2.2 to 5.5 | 1.5 | 3.0 | Applicable CL value=12.5pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure. 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

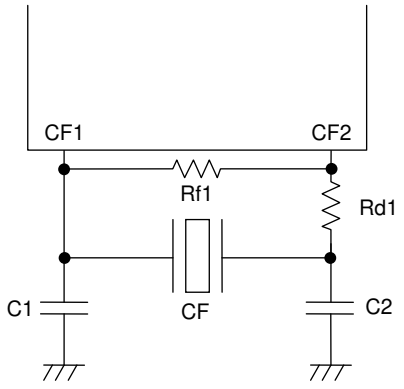



Figure 1 Ceramic Oscillator Circuit

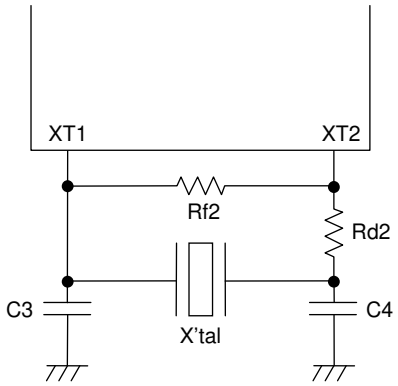



Figure 2 Crystal Oscillator Circuit

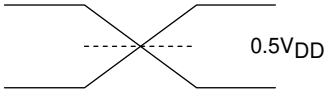
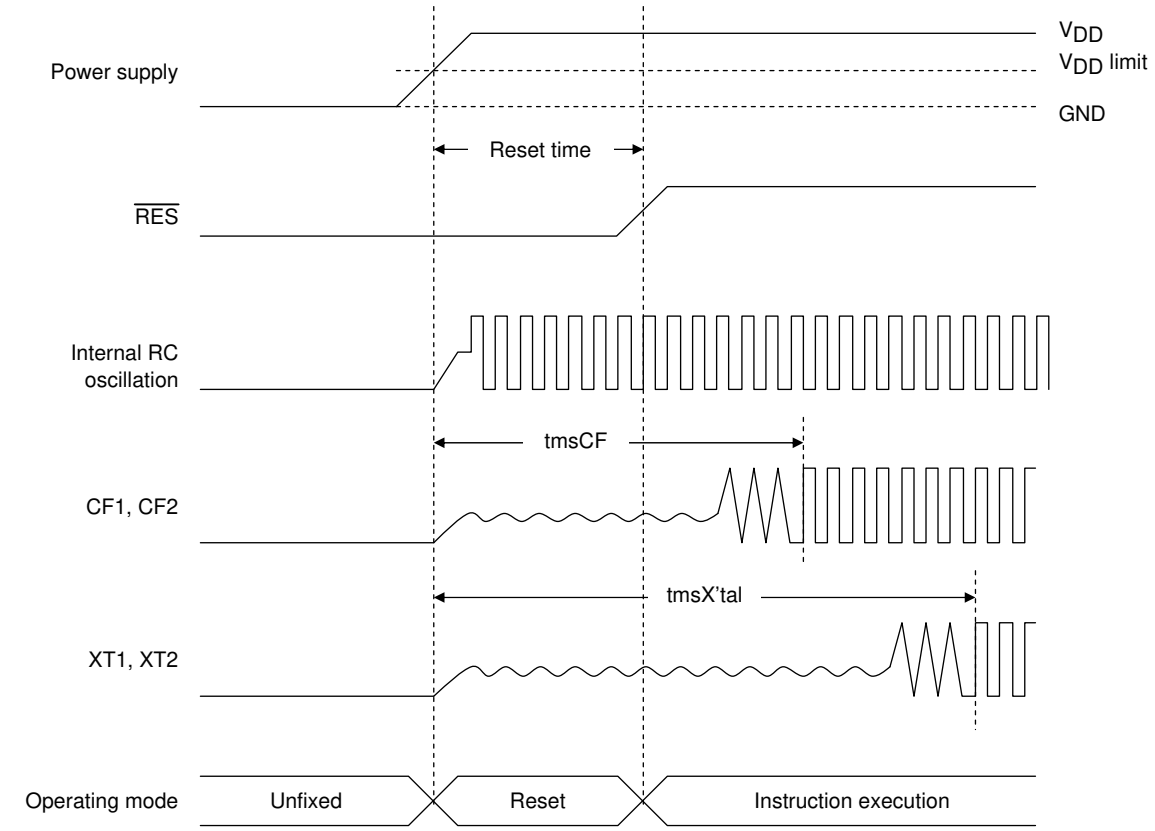
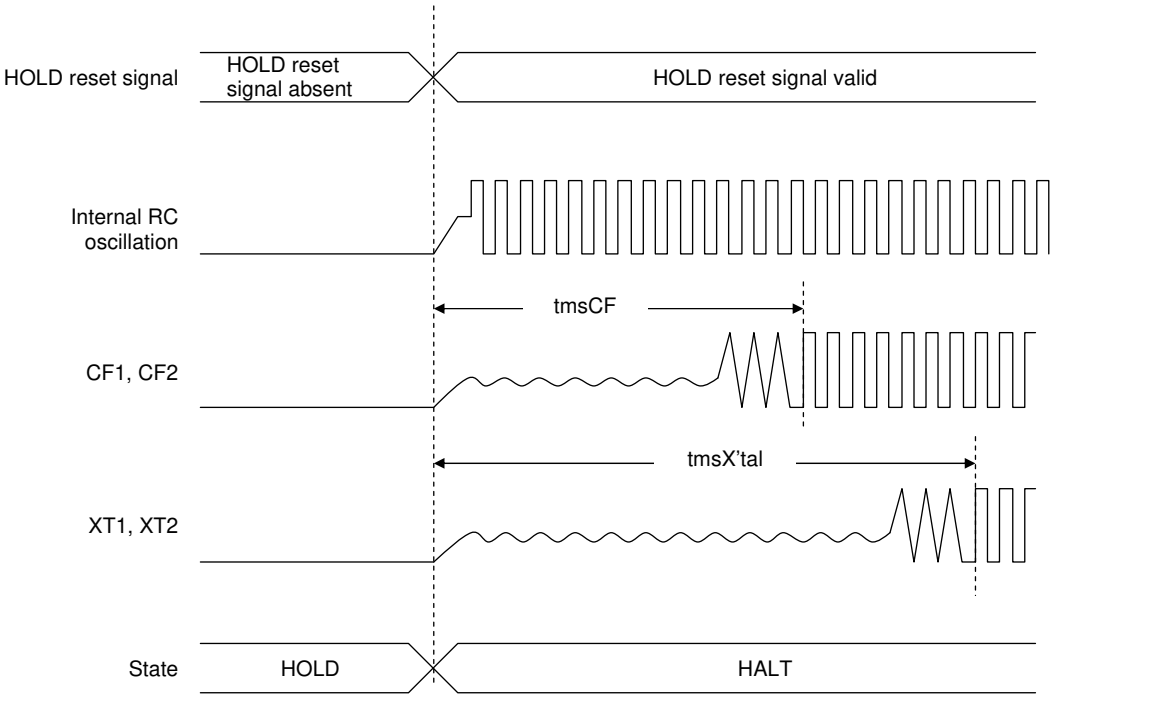



Figure 3 AC Timing Measurement Point

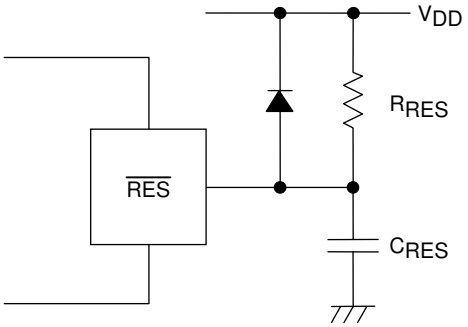



Reset Time and Oscillation Stabilization Time




HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times




Note:
Select $C_{RES}$ and $R_{RES}$ value to assure that at least 200µs reset time is generated after the $V_{DD}$ becomes higher than the minimum operating voltage.

Figure 5 Reset Circuit

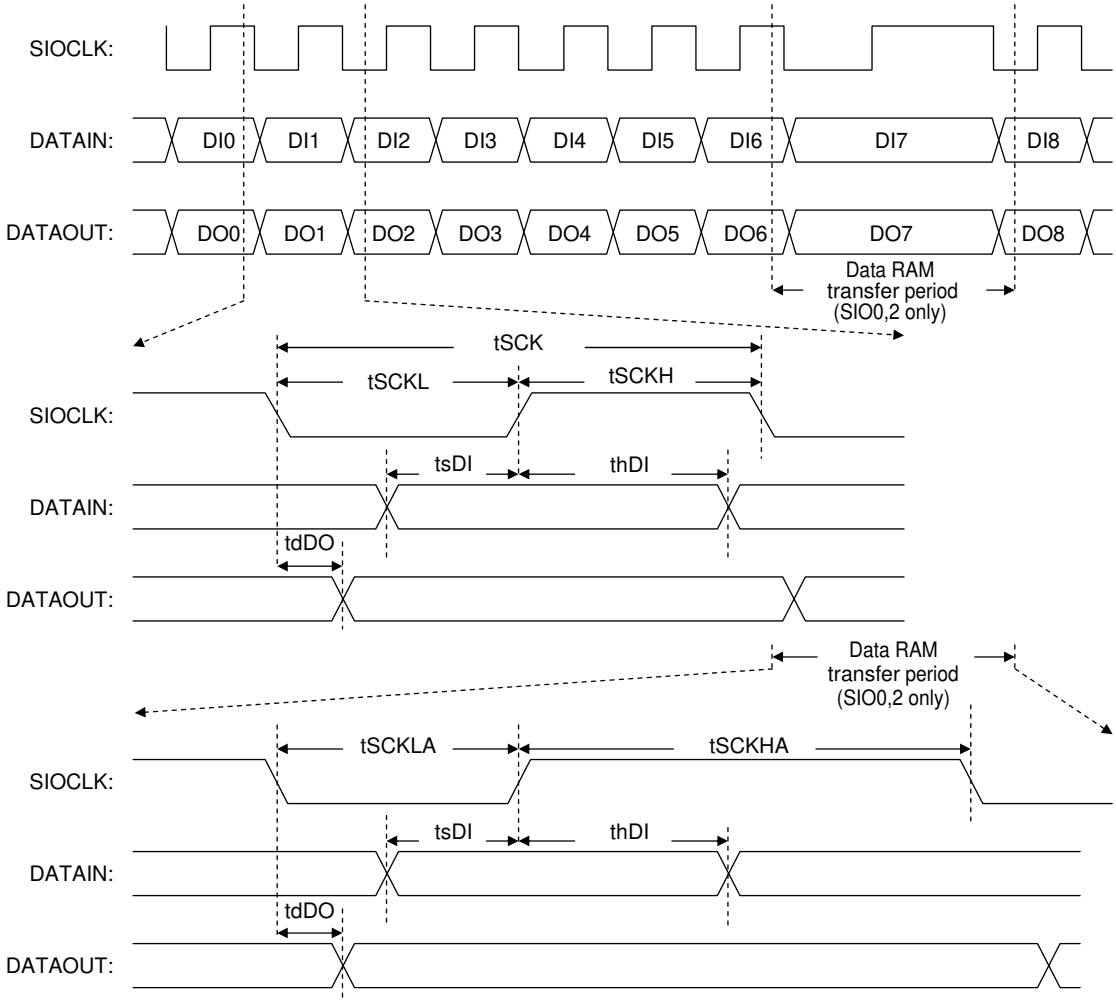



Figure 6 Serial I/O Waveforms

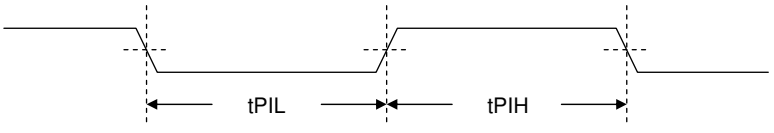



Figure 7 Pulse Input Timing Signal Waveform