Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ordering number : EN7202A

LC89057W-VF4A-E

CMOS IC

Digital Audio Interface Transceiver

ON Semiconductor®

http://onsemi.com

1. Overview

The LC89057W-VF4A-E is an audio IC that demodulates and modulates signals according to data transfer format between digital audio devices via the IEC60958/61937 and EIAJ CP-1201 and supports up to 192kHz of sampling frequency. It features a built-in VCO and oscillation amplifier, two bit clock circuits that are capable of setting independently the frequency-dividing ratios that can also be used for the DSP data input/output clocks, and LR clock output pins. A multi-channel PCM interface using multiple LC89057W-VF4A-E ICs is also available through a master/slave function.

This IC is optimal for use in high performance AV amplifiers and a multi-channel PCM interface for DVD audio equipment.

2. Features

2.1 Realizes full demodulation for high performance AV equipment

- Possible to receive the sampling frequency of 32kHz to 192kHz and 24 bits data at a maximum.
- Supports I^2S data output that facilitates interfacing with DSP.
- Output clock: 512fs, 256fs, 128fs, 64fs, 32fs, 2fs, fs, and fs/2
- Possible to output oscillation amplifier and external input clocks regardless of the PLL status.
- Maintains output clock continuity during clock switching.
- Supports Multi-channel transfer and reception, using master/slave function.
- Possible to process demodulation functions using common low-jitter clock without using PLL (external clock synchronization function)
- Built-in PLL error lock prevention circuit to provide accurate lock

2.2 Outputs various information to make system configuration easy

- Outputs DTS-CD/LD detection flag by DTS sync signal detection.
- Outputs burst preamble Pc from microcontroller interface.
- Calculates sampling frequency of input signal and outputs it from microcontroller interface.
- Outputs interrupt signal for microcontroller (interrupt source can be selected).
- Outputs signal of transitional period switching between VCO clock and oscillation amplifier clock.
- Outputs bit 1 of channel status (non-PCM data detection bit).
- Outputs emphasis information of channel status.
- Outputs renewed flag of the first 48 bits channel status.
- Channel status bit, validity flag and user data output are selectable.
- Outputs modulation/demodulation preamble B information.
- Possible to carry out and output various settings through microcontroller interface.

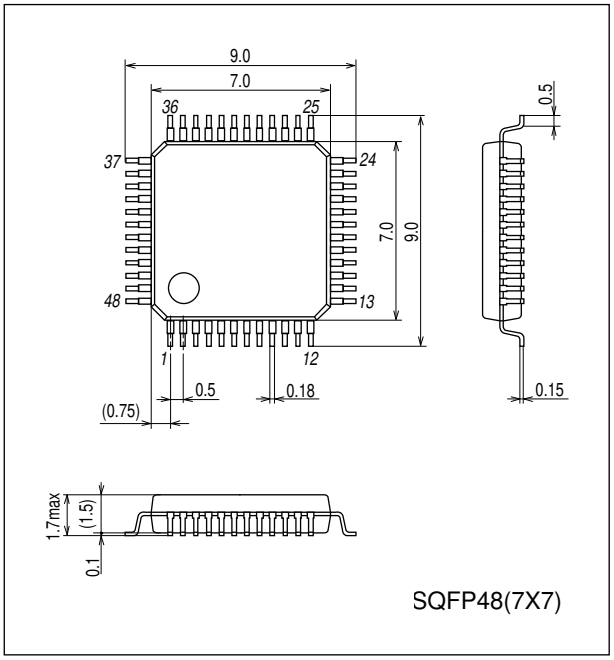
2.3 Plenty of built-in functions to reduce peripheral circuits

- Includes modulation function that can attach channel status, validity flag, and user data.
- Equipped with a total of 7 digital data input pins: 1 input pin with an amplifier and 6 input pins with 5V tolerable TTL level signal.
- Possible to monitor input pin status with microcontroller by mounting a bi-phase input data detection function.
- Possible to select input data among 8 system input data including modulation function output.
- Possible to select output of input-data through among 8 system input data aside from selecting demodulation data.
- Includes 2 system bit clock and LR clock outputs. Various frequency-dividing ratios can be set to one of these two systems.
- Equipped with a serial digital audio data input pin. Possible to switch with demodulation output.
- Possible to modulate the data that is input to the serial digital audio data input pin.
- Includes built-in oscillation amplifier and frequency divider for quartz resonator and also possible to use them as clock generator.
- Includes 4 bits general-purpose parallel I/O port. It can be used for interface with peripheral ICs.
- All the channel status can be decoded through peripheral circuit using preamble B information.
- A continuous switching operation between external clock synchronous mode and PLL clock synchronous mode is possible.
- Single 3.3V-power supply operation. TTL input port supports 5V interface.
- Adopts small SQFP48 package for efficient use of substrate mounting area.

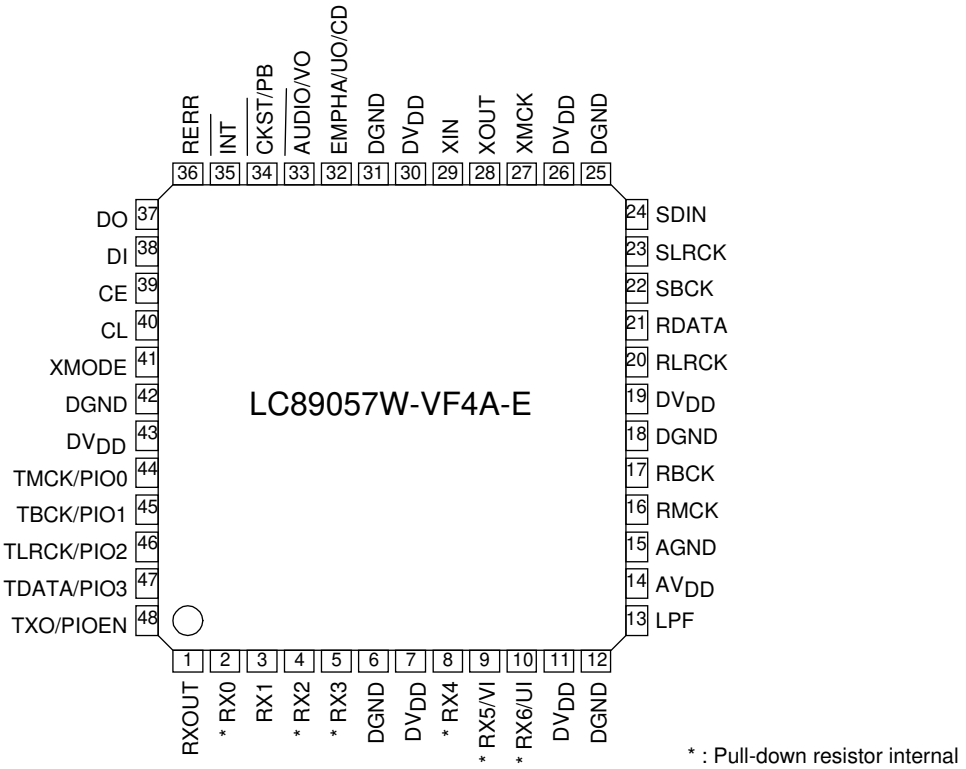
Package Dimensions

unit : mm (typ)

3163B



4. Pin Assignment



Top view

5. Pin Functions

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	RXOUT	O	Output pin of Input bi-phase selection data
2	RX0	I_5	Input pin of TTL-compatible digital data
3	RX1	I	Digital data input pin with built-in amplifier that supports coaxial
4	RX2	I_5	Input pin of TTL-compatible digital data
5	RX3	I_5	Input pin of TTL-compatible digital data
6	DGND		Digital GND
7	DV_{DD}		Digital power supply
8	RX4	I_5	Input pin of TTL-compatible digital data
9	RX5/VI	I_5	TTL-compatible digital data || Validity flag input pin for modulation
10	RX6/UI	I_5	TTL-compatible digital data || User data input pin for modulation
11	DV_{DD}		Digital power supply for PLL
12	DGND		Digital GND for PLL
13	LPF	O	PLL loop filter connection pin
14	AV_{DD}		Analog power supply for PLL
15	AGND		Analog GND for PLL
16	RMCK	O	R system clock output pin (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	R system bit clock input/output pin (64fs)
18	DGND		Digital GND
19	DV_{DD}		Digital power supply
20	RLRCK	O/I	R system LR clock input/output pin (fs)
21	RDATA	O	Output pin of serial audio data
22	SBCK	O	S system bit clock output pin (32fs, 64fs, 128fs)
23	SLRCK	O	S system LR clock output pin (fs/2, fs, 2fs)
24	SDIN	I_5	Input pin of serial audio data

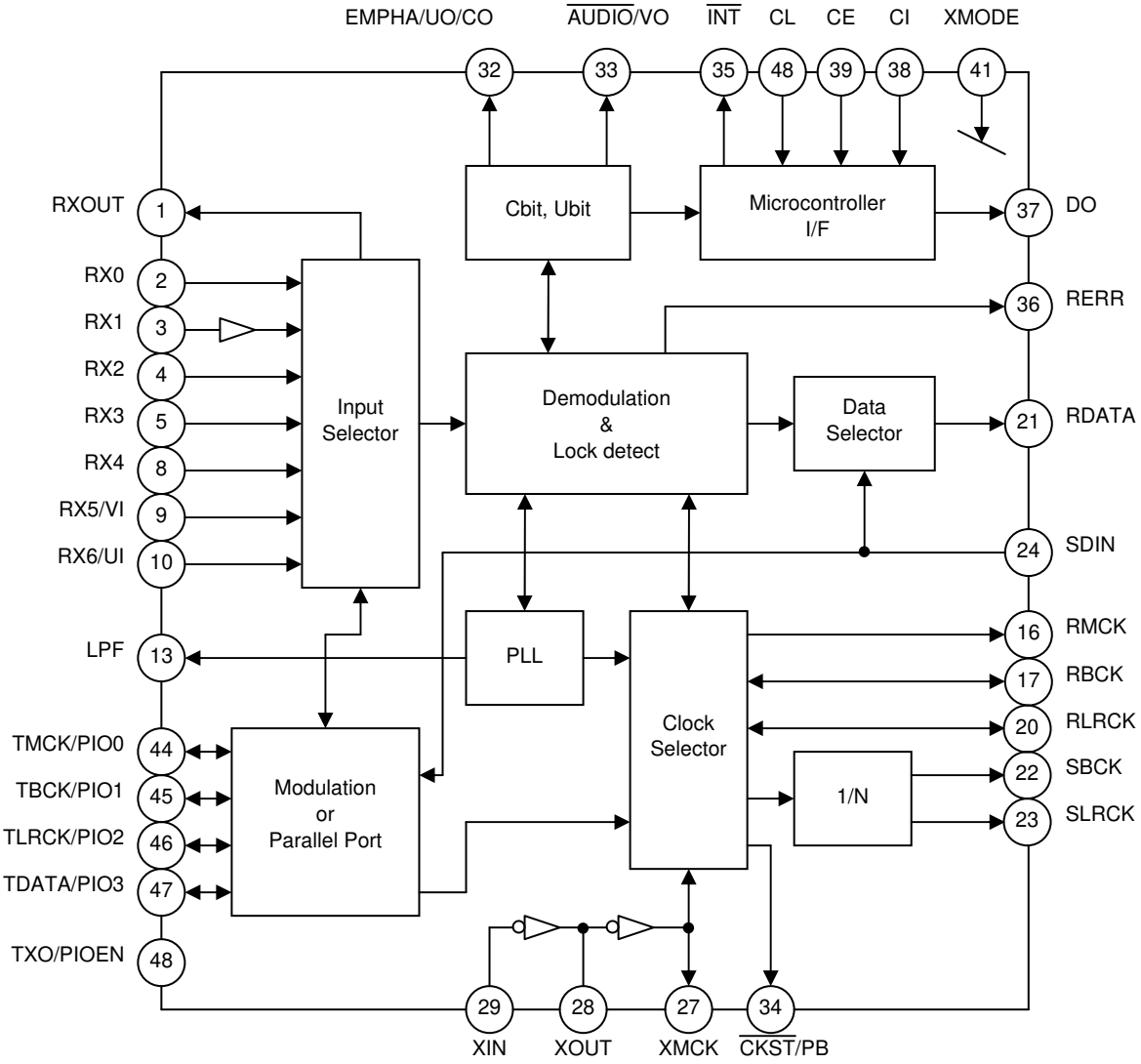
Continued on next page.

Continued from preceding page.

Pin No.	Name	I/O	Function
25	DGND		Digital GND
26	DV_{DD}		Digital power supply
27	XMCK	O	Oscillation amplifier output pin
28	XOUT	O	Quartz resonator connection output pin
29	XIN	I	Quartz resonator connection, input pin of external supply clock (24.576MHz or 12.288MHz)
30	DV_{DD}		Digital power supply
31	DGND		Digital GND
32	EMPHA/UO/CO	I/O	Emphasis information || U data output || C data output || Chip address setting pin
33	$\overline{\text{AUDIO}}$/VO	I/O	Non-PCM detection || V flag output || Chip address setting pin
34	$\overline{\text{CKST}}$/PB	I/O	Output of clock switch transitional period signal || Preamble B output || Demodulation master or slave function switch pin
35	$\overline{\text{INT}}$	I/O	Interrupt output for Microcontroller (Possible to select an interrupt factor.) || Modulation or general-purpose I/O switch pin
36	RERR	O	PLL clock error, data error flag output
37	DO	O	Microcontroller I/F, read data output pin (3-state)
38	DI	I_5	Microcontroller I/F, write data input pin
39	CE	I_5	Microcontroller I/F, chip enable input pin
40	CL	I_5	Microcontroller I/F, clock input pin
41	XMODE	I_5	System reset input pin
42	DGND		Digital GND
43	DV_{DD}		Digital power supply
44	TMCK/PIO0	I/O	256fs or 128fs system clock input for modulation || 256fs or 512fs system clock input for external clock sync function || General-purpose I/O pin
45	TBCK/PIO1	I/O	64fs bit clock input for modulation || General-purpose I/O pin
46	TLRCK/PIO2	I/O	fs clock input for modulation || General-purpose I/O pin
47	TDATA/PIO3	I/O	serial audio data input for modulation || General-purpose I/O pin
48	TXO/PIOEN	O/I	Modulation data output || General-purpose I/O enable input pin

1) Withstand voltage input/output: I or O = -0.3 to 3.6V, I_5 = -0.3 to 5.5V
2) Pins 32 and 33 are input pins for chip address setting, when pin 41 = "L".
3) Pin 34 is a demodulation function master or an input pin for slave setting, when pin 41 = "L".
4) Pin 35 is a modulation function or an input pin for general-purpose I/O function switch setting, when pin 41 = "L".
5) ON/OFF for all power supplies must be done at the same timing as a latch-up countermeasure.

6. Block Diagram



7. Comparison between LC89057W-VF4 and LC89057W-VF4A

Table 7.1 Difference between LC89057W-VF4 and LC89057W-VF4A

Item	LC89057W-VF4	LC89057W-VF4A
DIR function: External synchronization mode	256fs clock input	256fs or 512fs clock input
DIR function: Setting of RERR wait time after PLL is locked	After preamble B is counted 6. After preamble B is counted 12. After preamble B is counted 24. After preamble B is counted 48.	After preamble B is counted 3. After preamble B is counted 6. After preamble B is counted 12. After preamble B is counted 24.
DIR function: Setting of clock wait time after PLL is unlocked	50µs from when oscillation amplifier starts 100µs from when oscillation amplifier starts 200µs from when oscillation amplifier starts 400µs from when oscillation amplifier starts	0µs from when oscillation amplifier starts 50µs from when oscillation amplifier starts 100µs from when oscillation amplifier starts 200µs from when oscillation amplifier starts
DIR function: Channel status bit output	Microcontroller read out	Microcontroller read out or terminal output (full decode processing possible)
DIR function: Preamble B info output	×	○
DIT function: System clock	256fs clock input	256fs or 128fs clock input
DIT function: Preamble B info output	×	○

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 8.1: Absolute Maximum Ratings at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	AV_{DD} max	8-1-1	-0.3 to +4.6	V
Maximum supply voltage	DV_{DD} max	8-1-2	-0.3 to +4.6	V
Input voltage 1	$V_{IN}1$	8-1-3	-0.3 to +3.9	V
Input voltage 2	$V_{IN}2$	8-1-4	-0.3 to +5.8	V
Output voltage	V_{OUT}	8-1-5	-0.3 to +3.9	V
Storage ambient temperature	Tstg		-55 to +125	°C
Operating ambient temperature	Topr		-30 to +70	°C
Maximum input/output current	I_{IN}, I_{OUT}	8-1-6	±20	mA

8-1-1: AV_{DD} pin
8-1-2: DV_{DD} pin
8-1-3: RX1, RBCK, RLRCK, XIN, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2, TDATA/PIO3, TXO/PIOEN pins
8-1-4: RX0, RX2, RX3, RX4, RX5/VI, RX6/UI, SDIN, DI, CE, CL, XMODE pins
8-1-5: $\overline{\text{RXOUT}}$, RMCK, $\overline{\text{RBCK}}$, RL$\overline{\text{RCK}}$, SBCK, SLRCK, RDATA, XMCK, XOUT, EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO pins, $\overline{\text{CKST}}$/PB, $\overline{\text{INT}}$, RERR, DO, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2, TDATA/PIO3, TXO/PIOEN pins
8-1-6: Per input/output pin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

8.2 Allowable Operating Ranges

Table 8.2: Allowable Operating Ranges at Ta = -30 to 70°C, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	AV_{DD}, DV_{DD}		3.0	3.3	3.6	V
Input voltage range 1	$V_{IN}1$	8-2-1	0	3.3	3.6	V
Input voltage range 2	$V_{IN}2$	8-2-2	0	3.3	5.5	V
Operating temperature	Topr		-30		70	°C

8-2-1: RX1, RBCK, RLRCK, XIN, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2, TDATA/PIO3, TXO/PIOEN pins
8-2-2: RX0, RX2, RX3, RX4, RX5/VI, RX6/UI, SDIN, DI, CE, CL, XMODE pins

8.3 DC Characteristics

Table 8.3: DC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input, High	V_{IH}	8-3-1	$0.7V_{DD}$			V
Input, Low	V_{IL}				$0.2V_{DD}$	V
Input, High	V_{IH}	8-3-2	2.0		5.8	V
Input, Low	V_{IL}		-0.3		0.8	V
Output, High	V_{OH}	8-3-3	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-4	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-5	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-6	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Input amplitude	V_{PP}	8-3-7	200			mV
Consumption current	$I_{DD}1$	8-3-8		1.7	3.4	mA
Consumption current	$I_{DD}2$	8-3-9		17	34	mA
Consumption current	$I_{DD}3$	8-3-10		19	38	mA

8-3-1: CMOS compatible: RBCK, RLRCK, XIN input pins
8-3-2: TTL compatible: Input pins other than those listed above
8-3-3: I_{OH} = −12mA, I_{OL} = 8mA: RMCK output pin
8-3-4: I_{OH} = −8mA, I_{OL} = 8mA: XMCK, XOUT output pins
8-3-5: I_{OH} = −4mA, I_{OL} = 4mA: RXOUT, RBCK, RLRCK, RDATA, SBCK, SLRCK, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2 output pins, TDATA/PIO3, TXO/PIOEN output pins
8-3-6: I_{OH} = −2mA, I_{OL} = 2mA: Output pins other than those listed above
8-3-7: Before capacitance of RX1 input pin
8-3-8: Demodulation function and oscillation amplifier stopped, modulation only, output sampling frequency = 96kHz
8-3-9: XIN input continuous 24.576MHz oscillation, demodulation only, input sampling frequency = 96kHz
8-3-10: XIN input continuous 24.576MHz oscillation, modulation, input/output sampling frequency = 96kHz

8.4 AC Characteristics

Table 8.4: AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RX0 to RX6 sampling frequency	f_{RFS}		28		195	kHz
XIN clock frequency	$f_{XF}1$	8-4-1	8	12.288	19	MHz
XIN clock frequency	$f_{XF}2$	8-4-2	20	24.576	30	MHz
RMCK clock frequency	f_{RCK}		4		100	MHz
RMCK clock jitter	tj			200		ps
RMCK, RBCK delay	t_{MBO}				10	ns
RBCK, RDATA delay	t_{BDO}				10	ns
RMCK, SBCK delay	t_{MBO}	8-4-3			10	ns
SBCK, RDATA delay	t_{BDO}	8-4-4			10	ns
TMCK input pulse width	t_{WMI}		10			ns
RX*, TMCK delay	t_{RDI}				1/4TMCK	ns
TBCK input pulse width	t_{WBI}		40			ns
TLRCK sampling frequency	t_{TFS}		28		195	kHz
TBCK, TDATA setup	t_{DSI}			20		ns
TBCK, TDATA hold	t_{DHI}			20		ns
TMCK, TBCK delay	t_{MBI}	8-4-5			10	ns
TBCK, TDATA delay	t_{BDI}				10	ns

8-4-1: XINSEL = 0 setting, 12.288MHz must be set when calculating input sampling frequency
8-4-2: XINSEL =1 setting, 24.576MHz must be set when calculating input sampling frequency
8-4-3: When RMCK and SBCK source clocks are identical
8-4-4: When SBCK is the PLL source clock
8-4-5: TCKSEL = 0 setting (256fs), the falling edge of TBCK is in synchronization with the rising edge of TMCK.
TCKSEL = 1 setting (128fs), the falling edge of TBCK is in synchronization with the falling edge of TMCK.

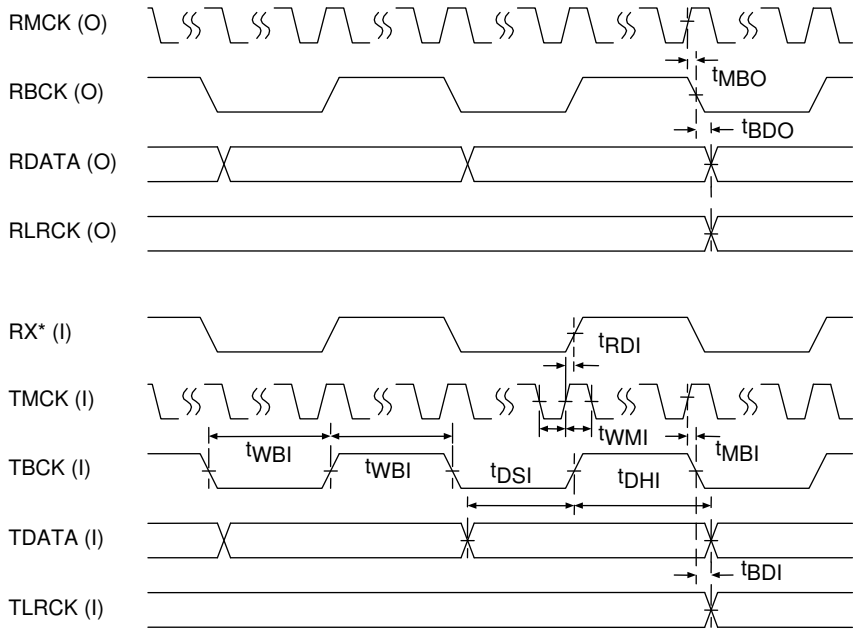


Figure 8.1 AC Characteristics

8.5 Microcontroller Interface AC Characteristics

Table 8.5: I/F AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XMODE pulse width, Low	$t_{RST\ dw}$		200			µs
$\overline{INT}$ pulse width, Low	$t_{INT\ wd}$	8-5-1	5	1/fs	36	µs
CL pulse width, Low	$t_{CL\ dw}$		100			ns
CL pulse width, High	$t_{CL\ uw}$		100			ns
CL, CE setup time	$t_{CE\ setup}$		50			ns
CL, CE hold time	$t_{CE\ hold}$		50			ns
CL, DI setup time	$t_{DI\ setup}$		50			ns
CL, DI hold time	$t_{DI\ hold}$		50			ns
CL, CE hold time	$t_{CL\ hold}$		50			ns
CL, DO delay time	$t_{CL\ to\ DO}$				20	ns
CE, DO delay time	$t_{CE\ to\ DO}$				20	ns

8-5-1: When INTOPF is set to "1", fs = input sampling frequency

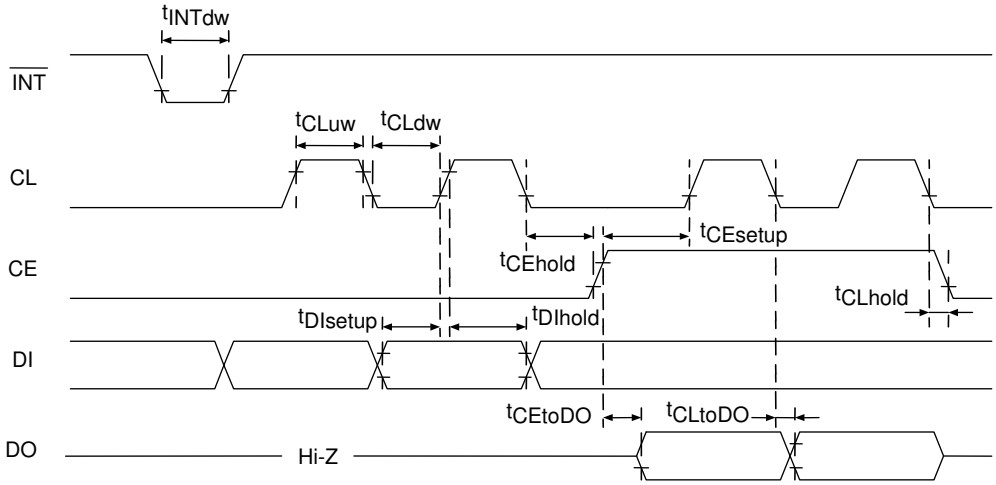


Figure 8.2 Microcontroller Interface AC Characteristics

9. Initial System Settings

9.1 System Reset (XMODE)

- The system operates correctly when XMODE is set to "H" after 3.0V or higher supply voltage is applied. When XMODE is set to "L" after power is turned on, the system is reset.
- When setting chip address, demodulation function master or slave, and modulation function or general-purpose I/O function, connect a 10kΩ pull-down or pull-up resistor to EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO, $\overline{\text{CKST}}$/PB, and $\overline{\text{INT}}$ pins.
- If EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO, $\overline{\text{CKST}}$/PB, and $\overline{\text{INT}}$ are not pulled up or down, their pin state is unstable at the time of input. Consequently proper setting cannot be realized. For these pins, pull-up or pull-down resistor must be connected.

Table 9.1: Pin Names and Settings

Setting	Pins
Chip address	EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO
Demodulation function master or slave	$\overline{\text{CKST}}$/PB
Modulation function or general-purpose I/O function	$\overline{\text{INT}}$

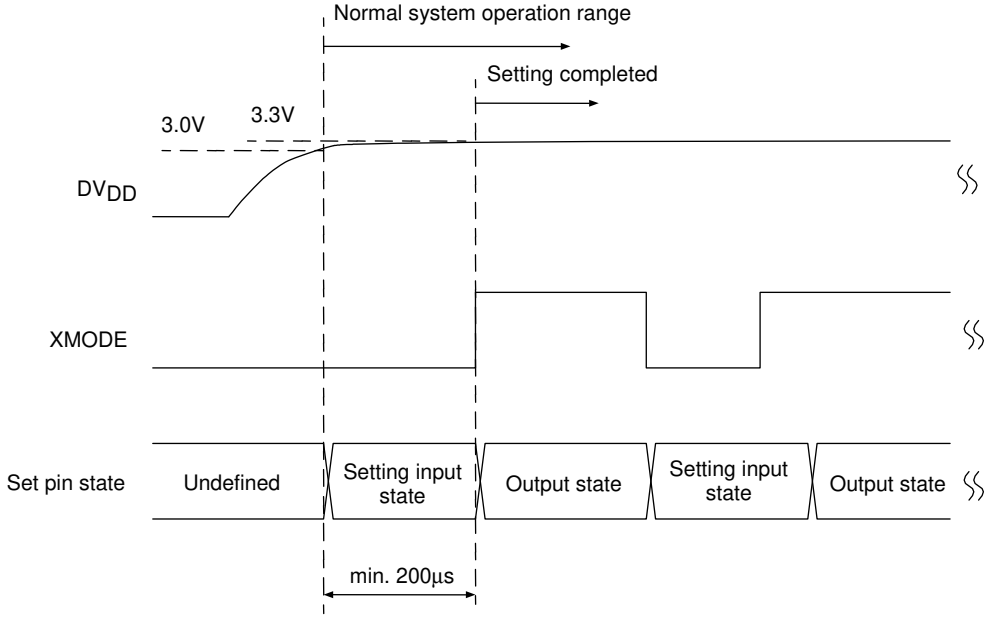


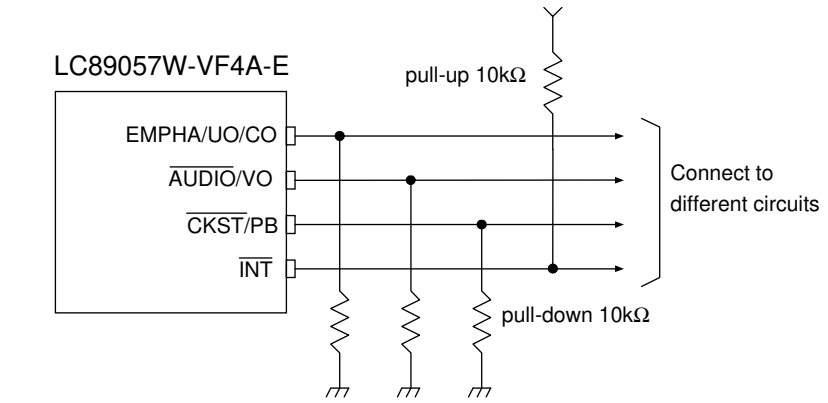
Figure 9.1 Setting Timing Chart of Function Setting Input Pins

9.2 Chip Address Settings (EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO)

- The LC89057W-VF4A-E comes with a function to set a unique chip address to allow the use of several LC89057W-VF4A-E on the same microcontroller interface bus.
- In chip address setting, connect a 10kΩ pull-down or pull-up resistor to EMPHA/UO/CO and $\overline{\text{AUDIO}}$/VO. By this setting, 4 kinds of chip addresses can be set at a maximum.
- Chip addresses in the microcontroller interface are set with CAL and CAU provided as the first two bits on the LSB side. CAL corresponds to the lower chip address and CAU to the higher chip address.
- Command writing is enabled by making the chip address settings with EMPHA/UO/CO and $\overline{\text{AUDIO}}$/VO identical to the chip addresses sent from the microcontroller.
- The chip address setting is required even when only one LC89057W-VF4A-E is used in the system. If the chip address is not set, the chip address is undefined and the microcontroller cannot control the system. When the microcontroller is not used, a chip address-setting pin is input open while XMODE is "L". Be sure to connect either a pull-down resistor or a pull-up resistor to EMPHA/UO/CO and $\overline{\text{AUDIO}}$/VO.

Table 9.2 Chip Address Settings (Register Connection)

$\overline{\text{AUDIO}}$/VO	EMPHA/UO/CO	CAU	CAL
Pull-down	Pull-down	0	0
Pull-down	Pull-up	0	1
Pull-up	Pull-down	1	0
Pull-up	Pull-up	1	1



Setting Contents of Above Figure

Chip address setting	→ CAIL=CAU=0
Demodulation function master or slave setting	→ Master
Modulation function or General-purpose I/O port switch	→ General-purpose I/O function

Figure 9.2 Setting Example of Function Setting Input Pin

9.3 Demodulation Function Master/Slave Settings ($\overline{\text{CKST}}$/PB)

- A master/slave function that allows multi-channel synchronized transfer using multiple LC89057W-VF4A-E ICs is included. For this setting, connects either a 10kΩ pull-down or a pull-up resistor to $\overline{\text{CKST}}$/PB.
- Set to the master mode normally, when single LC89057W-VF4A-E IC is used. When multiple LC89057W-VF4A-E ICs are used, set one of them to the master mode and the others to the slave mode.
- In the multi-channel synchronous transfer mode using multiple LC89057W-VF4A-E ICs, connect RBCK and RLRCK (output) on the master side to RBCK and RLRCK (input) on the slave side. Also connect XMCK on the master side to XIN on the slave side. At this time, the polarity of RBCK and RLRCK, and the frequency of XIN and XMCK must be identical.
- If the input data sampling frequency or the phase are different between the master mode and slave mode or if the clock sources differ while the sampling frequencies are not different, some of the output data may get dropped or read twice on the slave side. You can see if these are happening by $\overline{\text{INT}}$ and the microcontroller interface.

Table 9.3 Master/Slave Switching (Register Connection)

$\overline{\text{CKST}}$/PB	Mode
Pull-down	Master
Pull-up	Slave

Table 9.4 Clock Pin State

Pin	Master mode	Slave mode
RMCK	Output	Output
RBCK	Output	Input
RLRCK	Output	Input

9.4 Switching between Modulation Function and General-Purpose I/O Port ($\overline{\text{INT}}$)

- The modulation function and the general-purpose I/O function share same pins. Therefore, these two functions cannot be used simultaneously.
- To switch functions, connect either a 10kΩ pull-down or pull-up resistor to $\overline{\text{INT}}$ pin.

Table 9.5 Switching between Modulation Function and General-Purpose I/O Port (Register Connection)

$\overline{\text{INT}}$ State	Function
Pull-down	Modulation function
Pull-up	General-purpose I/O

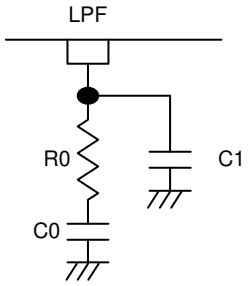
10 Description of Demodulation Function

• The demodulation function is set with RXOPR. An initial value is set to an operating status.

10.1 Clocks

10.1.1 PLL (LPF)

• The LC89057W-VF4A-E incorporates a VCO (Voltage Controlled Oscillator) that can be stopped with PLLOPR and it synchronizes with sampling frequencies from 32kHz to 192kHz and with the data with transfer rate from 4MHz to 25MHz.
• The PLL lock frequency is selected with PLLSEL. For systems whose input data sampling frequency is 105kHz or lower, the initial setting of 512fs is recommended. Since the initial output value of the system clock RMCK is set to 1/2 of PLLSEL, the RMCK output is 256fs when a PLL clock frequency is 512fs.
• For reception systems whose sampling frequency is higher than 105kHz, switch the PLL clock frequency to 256fs. If the same initial output setting is applied, RMCK is 128fs. Then set with PRSEL[1:0] when necessary.
• When the PLL lock frequency is selected with PLLSEL after PLL is locked, unlock is generated. Accordingly, PLLSEL must be set prior to bi-phase data input.
• LPF is a pin for PLL loop filter. Connect the following resistance and capacitances regardless of PLLSEL settings.



Clock	R0	C0	C1
512fs	220Ω	0.1μF	0.022μF
256fs			

Figure 10.1 Loop Filter Configuration

10.1.2 Demodulation function without using PLL (TMCK)

• The LC89057W-VF4A-E has a function that processes input bi-phase data using an external clock (external clock synchronization function). In normal demodulation processing, the built-in PLL generates a clock that is synchronized with data and carries out data processing with the clock. In the LC89057W-VF4A-E, data processing can be also done by providing a clock synchronized with data instead of the PLL-generated clock via an independent transmission path.
• To use the external clock synchronization function, set the PLL unused demodulation function with EXSYNC, set the 256fs or 512fs clock with PLLSEL, and set 1/1 of PLLSEL set frequency with PRSEL[1:0]. After that input the clock synchronized with input data to TMCK. By this settings, the same operation as PLL demodulation processing is performed. For example, 512fs clock should be supplied with TMCK because the setting of PLLSEL is at 512fs in case EXSYNC is set on initial condition. In the event of switching the setting of TMCK clock frequency to 256fs, the setting of PLLSEL should be at 256fs.
• Jitter of input data and clock should be as small as possible. Excessive jitter might invite errors in operation of PLL. Pay attention to the noise of clock transmission path.
• In the external synchronization mode, supply clock with TMCK all the time. Without input of clock, system will shut down and be in malfunction.
• In case of using external clock synchronization mode only, it is not necessary to connect anything to LPF pin. However, configuring PLL loop filter enables to use both PLL clock synchronization mode and external clock synchronization mode by switching EXSYNC.
• Applying the external clock synchronization function can also configure a high-precision clock system using an external PLL.

10.1.3 Oscillation amplifiers (XIN, XOUT, XMCK)

- The LC89057W-VF4A-E features a built-in oscillation amplifier. Connecting a quartz resonator, feedback resistor, and load capacitance to XIN and XOUT can configure an oscillation circuit. When connecting a quartz resonator, use one with a fundamental wave. Be aware that the load capacitance depends on the quartz resonator characteristics.
- If the built-in oscillation amplifier is not used and oscillation module is used as the clock source instead, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Supply XIN with the 12.288MHz or 24.576MHz-clock set with XINSEL. If inputting other frequencies to XIN, it is necessary to set that the result of change in sampling frequency fs of input data is not reflected to an error flag. By this setting, the operation functions properly. However, since time definition gap occurs in relation to the operation with recommended frequency, the encoding result cannot be used for input fs calculations. In this case, the input fs can be calculated by dividing decimally the calculation count value with 1/2000th of the XIN input frequency. For details, see Chapter 12. Microcontroller Interface.
- Since the XIN clock serves as the reference for internal processing, complete the XINSEL setting prior to bi-phase data input.
- Supply XIN with clocks all the time to be used in the following applications.
    (1) Detection whether or not bi-phase data is input
    (2) Clock source while PLL is unlocked
    (3) Calculation of input data sampling frequency
    (4) Time definition when switching input data
    (5) External source of supply clock (clock for an AD converter, etc.) in XIN source mode.

- The oscillation amplifier automatically stops while PLL is locked. However, it can be also set for continuous operation with AMPOPR[1:0]. In the continuous operation mode, data detection and calculation of input sampling frequency become possible while the PLL is locked. In that case, both the oscillator amplifier clock and the PLL clock signals coexist, and then users must pay attention and make sure sound quality is not adversely affected.
- If the oscillation amplifier is set to continuous operation with AMPOPR[1:0] while PLL is locked, RERR temporarily outputs an error ("H"). When oscillation amplifier is switched to an operation state, fs calculation value maintained during a stop state is reset at the same time. This process is regarded as an error, since fs seems to change. This error has no influence on clock output, but RDATA is muted during this error period. Therefore, setting of the AMPOPR[1:0] must be completed either prior to bi-phase data input or while PLL is unlocked.
- The oscillation amplifier can be stopped if it is unnecessary. However, when the normal operation is resumed, it must wait for 10ms or longer until the resonator oscillation gets stable.
- XMCK outputs the XIN clock. The XMCK output is set with XMSEL[1:0]. The XIN clock can be set to 1/1, 1/2, or muted output.
- When only the modulation function is used, no clock needs to be supplied to XIN. In this case, the built-in oscillation amplifier and frequency divider can be also used for MCK, BCK, and LRCK clock generation. If you use only the oscillation amplifier, input the quartz resonator to XIN and XOUT or an external clock to XIN, and fix the electric potential of digital data input pins of RX0 to RX6. At this time, do not set to stop the DIR function with RXOPR and PLLOPR. The output clock may be muted.

10.1.4 Switching between Master clock and clock source

- The RMCK, RBCK, and RLRCK (hereunder, R system), and the SBCK and SLRCK (hereunder, S system) clock sources can be selected among the following three master clocks.
  (1) PLL source (256fs or 512fs)
  (2) XIN source (12.288MHz or 24.576MHz)
  (3) TMCK source (256fs or 512fs)

- There are two ways available for clock source switching; one is to set with the R system and the S system interlocked, and the other is to set only the R system while XIN source is fixed in the S system. This setting is carried out with SELMTD, OCKSEL, and RCKSEL.
- The clock source is automatically switched between PLL clock and XIN clock by locking/unlocking the PLL. During this period, continuity of the clock is maintained. However, if the clock source is switched with SELMTD, continuity of the S system is not maintained.
- The clock source can be switched to XIN with OCKSEL and RCKSEL, regardless of the PLL status. The clock source switch command and each clock output of the R and S systems are shown below.

Table 10.1 Correspondence between Clock Source Switch Commands and Clock Output Pins

SELMTD	R System Output Clock	S System Output Clock
0	According to OCKSEL	According to OCKSEL
1	According to RCKSEL	Fixed to XIN source

Table 10.2 Relationship between Clock Source Switch Commands and Clock Sources when PLL Locked/Unlocked

SELMTD	OCKSEL	RCKSEL	R System Clock Source		S System Clock Source	
			Locked	Unlocked	Locked	Unlocked
0	0	X	PLL	XIN	PLL	XIN
	1	X	XIN	XIN	XIN	XIN
1	X	0	PLL	XIN	XIN	XIN
	X	1	XIN	XIN	XIN	XIN

- TMCK source should be selected with EXYSNC and the input clock frequency (256fs or 512fs) should be set with PLLSEL. The same action as the one of PLL source should be taken except inputting clock from TMCK on this setting.
- When data synchronized with the TMCK source is input, various clocks are output with the TMCK source as the master clock, in a manner similar to the PLL clock status. In this case as well, the source is switched to XIN with OCKSEL and RCKSEL. When the TMCK source is not supplied or the input data is not synchronized, the source is switched to the XIN source, in a manner similar to the PLL source unlocked status.
- The PLL status can be always monitored with RERR even after switching to the XIN source. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.
- When the PLL changes from the locked status to the unlocked, the timing for switching the clock from the PLL source to the XIN source can be changed with XTWT [1:0]. Use these commands if noise occurs during clock switching.

10.1.5 Points to notice about switching clock source while PLL is locked

- In the state where the PLL is locked, if the clock is switched to XIN source with SELMTD, OCKSEL, and RCKSEL while the oscillator amplifier is stopped (initial setting), clock continuity is maintained but RERR temporarily outputs an error (high level) indication. When switched to XIN source, the oscillator amplifier is switched to the operating state at the same time. Consequently the input fs calculation restarts. At this time, the previous fs calculation value is reset and compared with the newly calculated fs value. Then those two values are found not identical, that's why the error is temporarily issued.
- The following settings are required to switch the clock source with SELMTD, OCKSEL, and RCKSEL without changing the RERR status while PLL is locked.
  (1) Set the oscillation amplifier to the continuous operation mode with AMPOPR[1:0].
  (2) Set with FSERR to the mode where fs change is not reflected to the error flag.

- By one of the above settings, changing of the RERR status can be constrained when the clock source is switched with SELMTD, OCKSEL, and RCKSEL.
- When switching the clock source to XIN from the state where the oscillation amplifier is stopped while the PLL is locked, the output clock using XIN as the source starts being output after the oscillation amplifier starts operating. When the PLL is locked, switching of the clock source from XIN to PLL is performed instantaneously. In either case, clock continuity is maintained.

10.1.6 Master clock block diagram (TMCK, XIN, XOUT, RMCK, XMCK)

- The relationships between the three master clocks, switching, and the frequency division function, are described below.
- The contents in the square brackets [***] by the switch and function blocks correspond to the write command names.
- Lock/Unlock is automatically switched by PLL locking/unlocking.

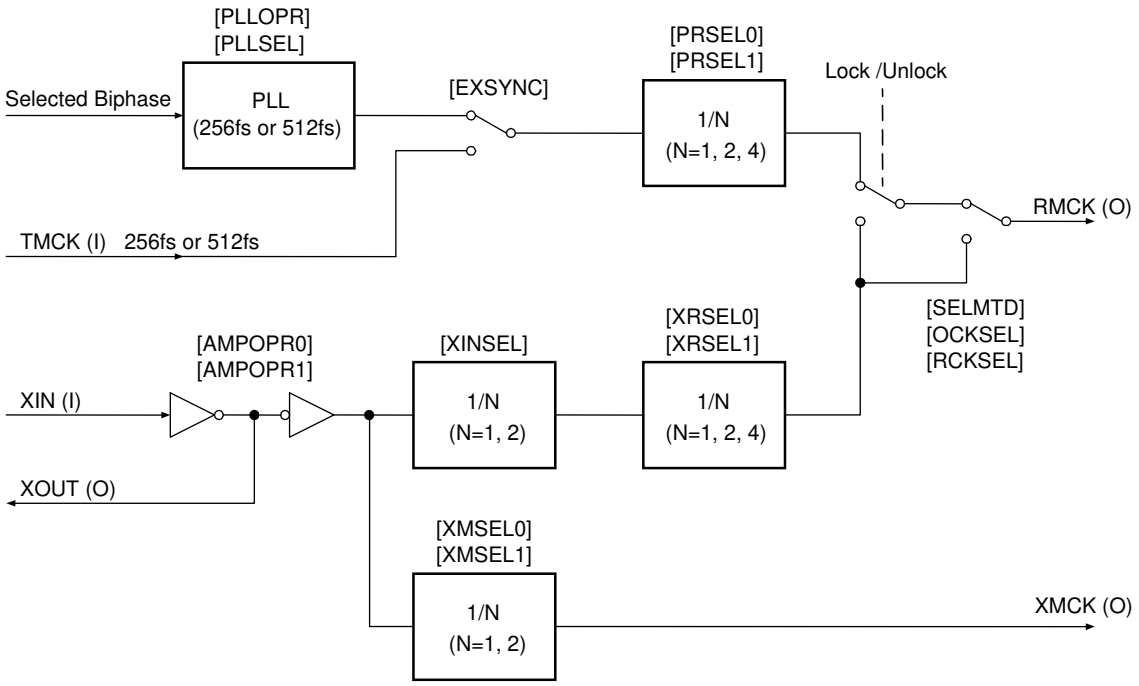


Figure 10.2 Master Clock Block Diagram

10.1.7 Output clocks (RMCK, RBCK, RLRCK, SBCK, SLRCK)

- The LC89057W-VF4A-E features two clock systems (R and S systems) in order to supply the various needed clocks to peripheral devices such as A/D converter and DSP.
- The clock output settings for the R and S systems are done with PRSEL[1:0], XRSEL[1:0], XRBCK[1:0], XRLRCK[1:0], PSBCK[1:0], PSLRCK[1:0], XSBCK[1:0], and XSLRCK[1:0].
- Setting range for each clock output pin when the PLL is used as source
  - (1) RMCK: Selection from 1/1, 1/2, and 1/4 of 512fs or 256fs
  - (2) RBCK: 64fs output
  - (3) RLRCK: fs output
  - (4) SBCK: Selection from 128fs, 64fs, and 32fs
  - (5)SLRCK: Selection from 2fs, fs, and fs/2
- Setting range for each clock output pins when the XIN is used as source
  - (1) RMCK: Selection from 1/1, 1/2, and 1/4 of 12.288MHz or 24.576MHz
  - (2) RBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  - (3) SBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  - (4) RLRCK: Selection from 192kHz, 96kHz, and 48kHz
  - (5) SLRCK: Selection from 192kHz, 96kHz, and 48kHz
- Setting range for each clock output pins when the TMCK is used as source
  - (1) RMCK: selection from 1/1, 1/2,1/4 of 512fs or 256fs.
  - (2) RBCK: 64fs output
  - (3) RLRCK: fs output
  - (4) SBCK: selection from 128fs, 64fs, 32fs
  - (5) SLRCK: selection from 2fs, fs, fs/2
- The polarity of RBCK, RLRCK, SBCK, and SLRCK can be reversed with RBCKP, RLRCKP, SBCKP, and SLRCKP.
- Clock switching is processed from the rising edge of RLRCK output after the falling edge of microcontroller interface CE.

Table 10.3 List of Output Clock Frequencies (Bold Items = Initial Settings)

Output Pin Name	PLL Source (Internal VCO CK)		TMCK Source (TMCK input CK)		XIN Source (XIN input CK)	
	512fs	256fs	512fs	256fs	12.288MHz	24.576MHz
RMCK	512fs **256fs** 128fs	256fs **128fs** 64fs	512fs **256fs** 128fs	256fs **128fs** 64fs	**12.288MHz** 6.144MHz 3.072MHz	**24.576MHz** 12.288MHz 6.144MHz
RBCK	**64fs**				12.288MHz 6.144MHz **3.072MHz**	
RLRCK	**fs**				192kHz 96kHz **48kHz**	
SBCK	128fs **64fs** 32fs				12.288MHz 6.144MHz **3.072MHz**	
SLRCK	2fs **fs** fs/2				192kHz 96kHz **48kHz**	

10.1.8 Output clocks block diagram (RMCK, RBCK, RLRCK, SBCK, SLRCK, XMCK)

- The relationships between the output clock and switch function are shown below.
- PLL in the figure indicates the PLL source (or TMCK source), and XIN the XIN source.
- The contents in the square brackets [***] by the switch function blocks correspond to the write command names.
- The broken lines connecting the switches indicate coordinated switching.
- Lock/Unlock is switched automatically by PLL locking/unlocking.
- Master/Slave is switched by master/slave function switching of demodulation function.

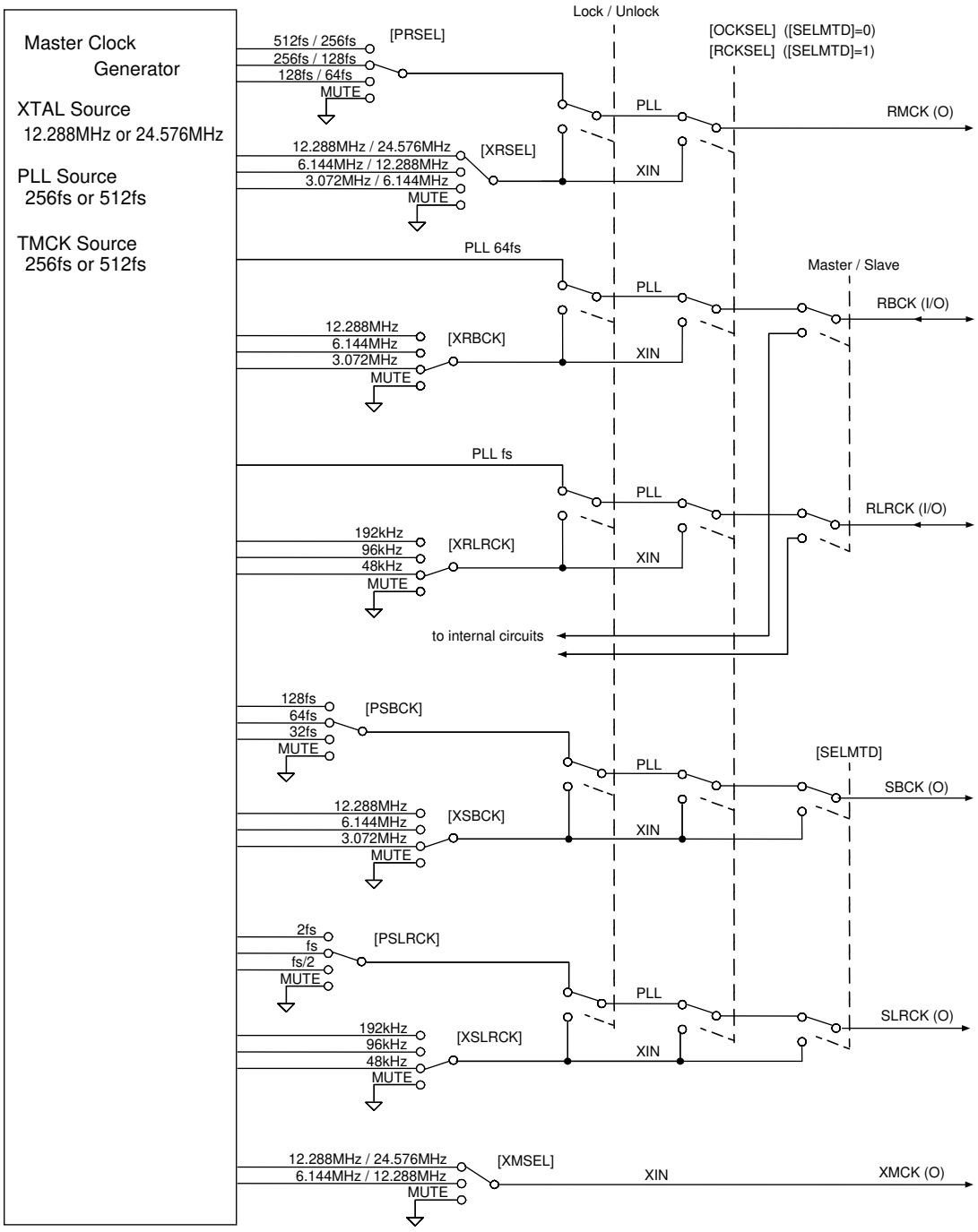
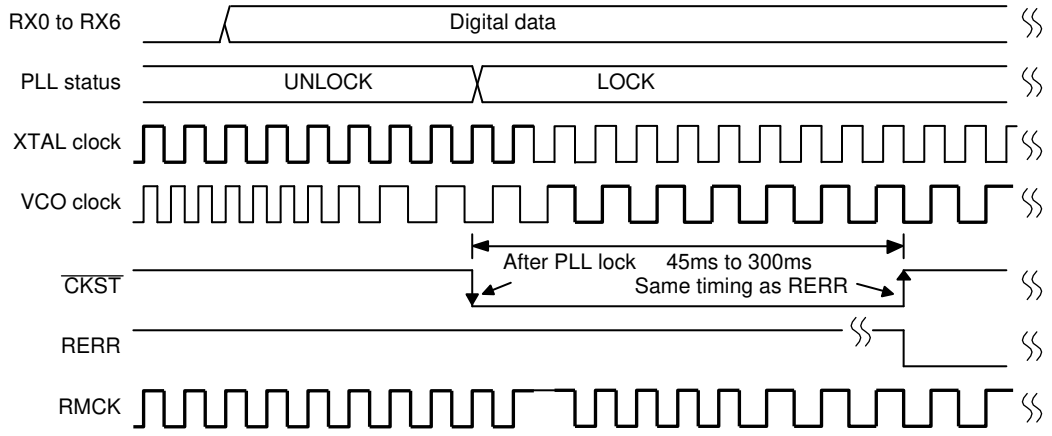


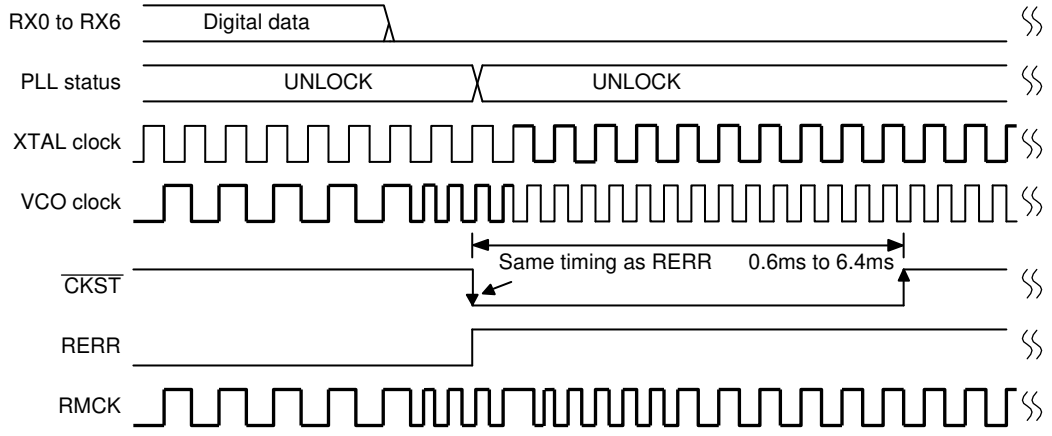
Figure 10.3 Clock Output Block Diagram

10.1.9 Output of Clock switch transition signal ($\overline{\text{CKST}}$)

- $\overline{\text{CKST}}$ outputs "L" pulse when the output clock changes by PLL lock/unlock.
- In the lock-in stage, the $\overline{\text{CKST}}$ "L" pulse falls at the word clock generated from the XIN clock after PLL is locked following detection of input data, and rises at the same timing as RERR after a designated period.
- In the unlock stage, the $\overline{\text{CKST}}$ "L" pulse falls at the same timing as RERR, PLL lock detection signal, and rises after word clocks generated from the XIN clock are counted for a designated period.
- Change of the PLL lock status and timing of the clock change can be seen by detecting the rising and falling edges of the $\overline{\text{CKST}}$ "L" pulse.



(a): Lock-in stage



(b): Unlock stage

Figure 10.4 Clock Switch Timing

10.2 Bi-phase Signal I/O

10.2.1 Reception range of bi-phase signal input

• Reception range of the input data depends on the PLL lock frequency setting done with PLLSEL. The relationship between this setting and the guaranteed reception range is shown below.

Table 10.4 Relationship between PLL Output Clock Setting and Reception Range (FSLIM [1:0] = 00)

PLL Output Clock Setting	Input Data Reception Range
512fs (PLLSEL = 0)	28kHz to 105kHz
256fs (PLLSEL = 1)	28kHz to 195kHz

• The fs reception range for input data can be limited within the set range of PLL output clocks stated above. This setting is carried out with FSLIM [1:0]. When this function is adopted, input data exceeding the set range is considered as an error, the clock source is automatically switched to the XIN source, and RDATA output data is subject to the RDTSEL setting.

10.2.2 Bi-phase signal I/O pins (RX0 to RX6, RXOUT)

• There are 7 kinds of digital data input pins. Moreover, data modulated with the modulation function is also available and thus there are 8 options in total. However, the pins to be selected are restricted, depending on the setting conditions.
  (1) The six pins of RX0 and RX2 to RX6 are TTL level input pins with 5V-tolerance voltage.
  (2) RX1 is an input pin with built-in amplifier, which is coaxial-compatible and it, can receive up to min, 200mVp-p data.
• The demodulation input and RXOUT output signals could each be selected independently.
  (1) The demodulation data is selected with RISEL [2:0].
  (2) The RXOUT output data is selected with ROSEL [2:0].
• RXOUT can be muted with RXOFF. Muting is recommended to reduce clock jitter when RXOUT is not used.
• The data input status can be monitored with the RXMON setting. The status of each data input pin is stored in CCB address 0xEA and output registers DO0 to DO7. Since this function uses the XIN clock, the oscillation amplifier must be set to the continuous operation mode when RXMON is set.
• Demodulation input pin can be switched via PLL unlock with the ULSEL setting. Thus data switching can be accurately conveyed to peripheral devices.
  The interval from pin switching through RISEL [2:0] until the data is received is about 250µs to 350µs. In this function, the oscillation amplifier also needs to be set to the continuous operation mode.

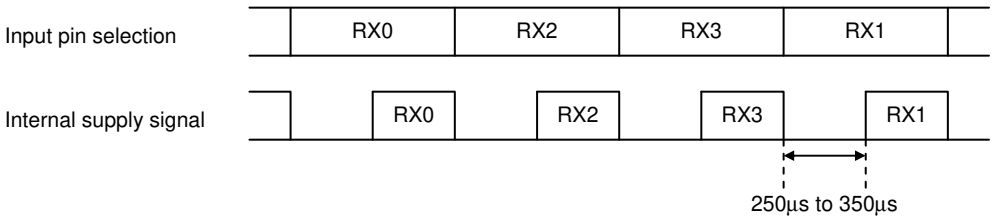


Figure 10.5 Input Pin Selecting Process via PLL Unlock

10.2.3 Bi-phase signal input circuits (RX0, RX1, RX2)

- If RX1 with a built-in amplifier is used as a coaxial input pin, malfunction may occur due to the influence from the adjacent RX0 and RX2 input pins. To avoid the influences from those pins, fix RX0 and RX2 to "L".
- When RX1 is selected and the input signal to RX1 is temporarily open because of AC coupling, the RX0 and RX2 potential must be fixed. In this case, there are 5 bi-phase signal input pins available, which are RX1 and RX3 to RX 6.
- When RX1 is selected and the input signal to RX1 is always fixed to either "H" or "L", RX0 and RX2 processes are not required. In this case, all 7 input pins can be used validly.

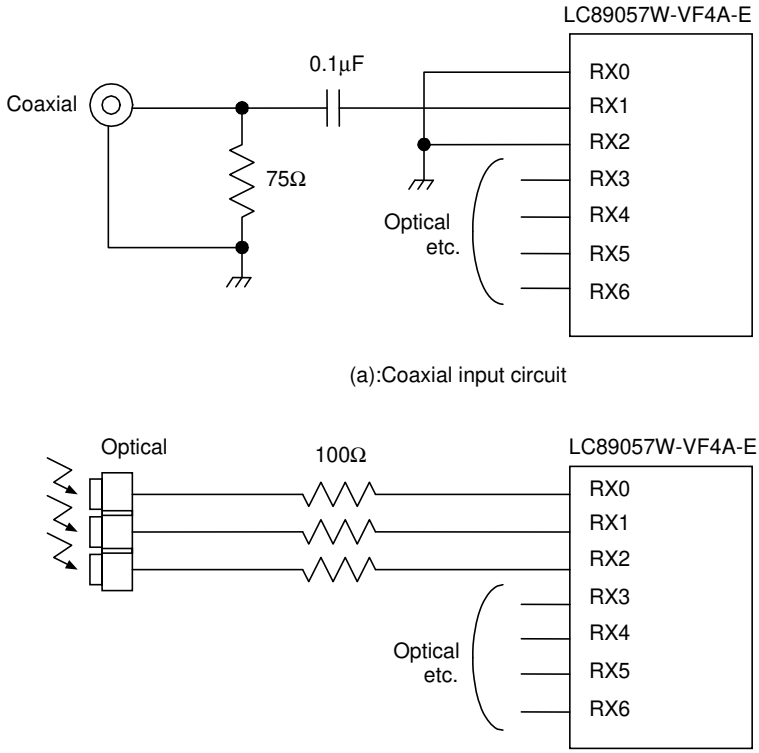
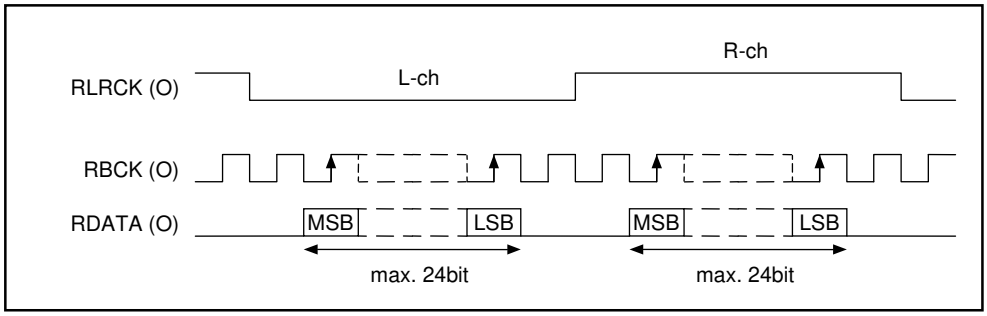


Figure 10.6 Bi-Phase Signal Input Circuits

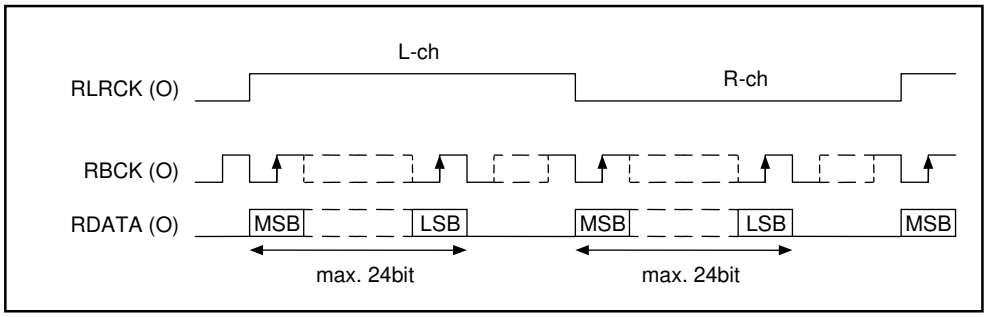
10.3 Serial Audio Data I/O

10.3.1 Output data format (RDATA)

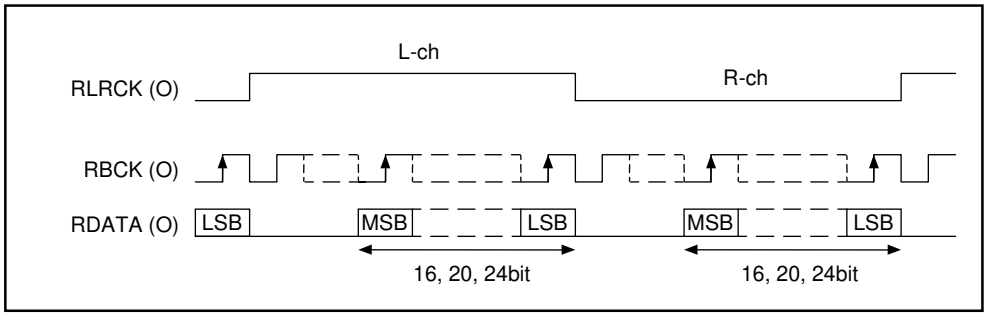
- The output format is set with OFSEL [2:0].
- The initial value of output format is I^2S.
- Right-adjusted output is valid only in the master mode. In the slave mode, data is not output correctly.
- Output data is output synchronized with the RLRCK edge immediately after the RERR output becomes "L".



(0): I^2S data output



(1): MSB-first front-loading data output

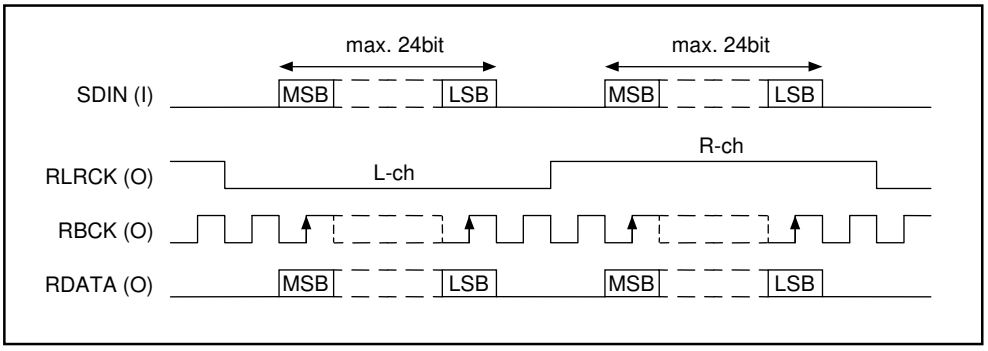


(2): MSB-first back-loading data output

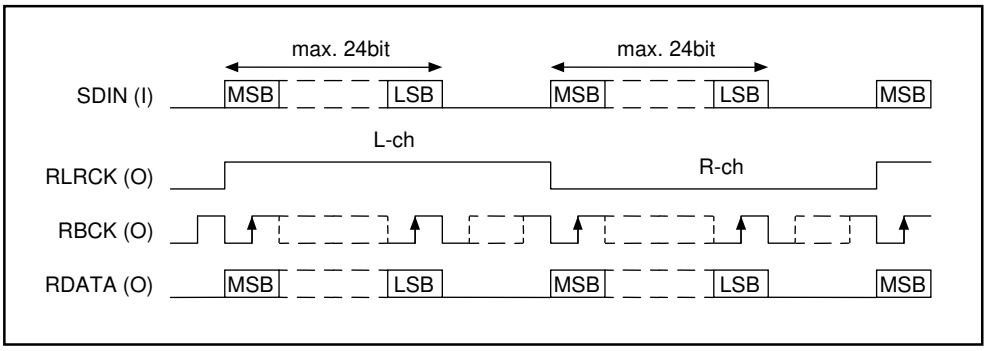
Figure 10.7 Data Output Timing

10.3.2 Serial audio data input format (SDIN)

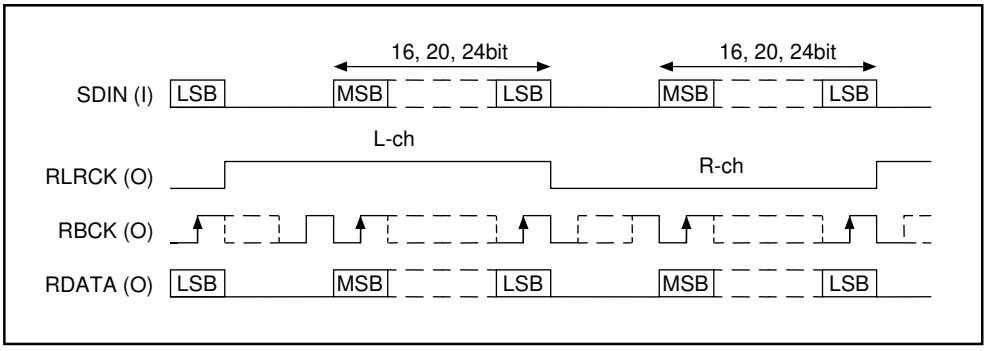
- Serial digital audio data input pin of SDIN capable of 24 bits input is provided.
- The format of the serial audio data input to SDIN and the demodulation data output format must be identical. The initial value of modulation data output is I^2S.



(0): I^2S data input



(1): MSB-first front-loading data input



(2): MSB-first back-loading data input

Figure 10.8 Serial Audio Data Input Timing

10.3.3 Output data switching (SDIN, RDATA)

- RDATA outputs demodulation data when the PLL is locked, and outputs SDIN input data when the PLL is unlocked. This output is automatically switched according to the PLL locked/unlocked status. For details, see the timing charts below.
- When SDIN input data is selected, switch to a clock source synchronized to the SDIN data.
- With the RDTSTA setting, the SDIN input data is output to RDATA regardless of the locked/unlocked status of the PLL.
- With the RDTMUT setting, the RDATA output data can be also muted forcibly.
- Even when the clock source is set to XIN with OCKSEL and RCKSEL, the PLL continues operating as long as the PLL is not stopped with PLLOPR. At this time, the PLL status is continuously output from RERR unless error output is forcibly set with RESTA. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.

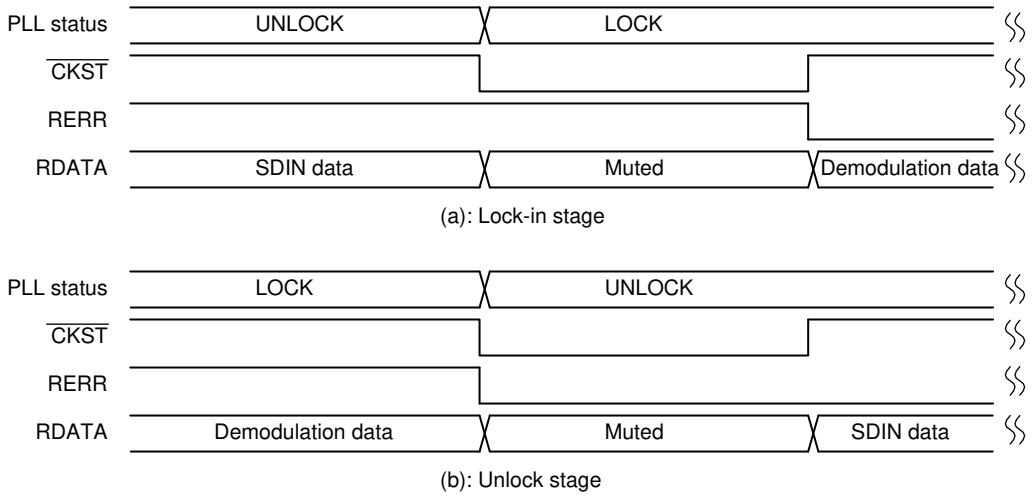


Figure 10.9 Timing Chart of RDATA Output Data Switching

10.3.4 Data block diagram (RX0 to RX6, TX0, RXOUT, TDATA, RDATA, SDIN)

- The RDATA output data can be switched to SDIN input data with RDTSEL.
- The SDIN input data can be input to the modulation function with TDTSEL.
- Since the modulation output is input to the input switch multiplexer, it can be fetched from RXOUT. Using this function, it is possible to use a signal digitized with the A/D converter for digital recording output, etc.

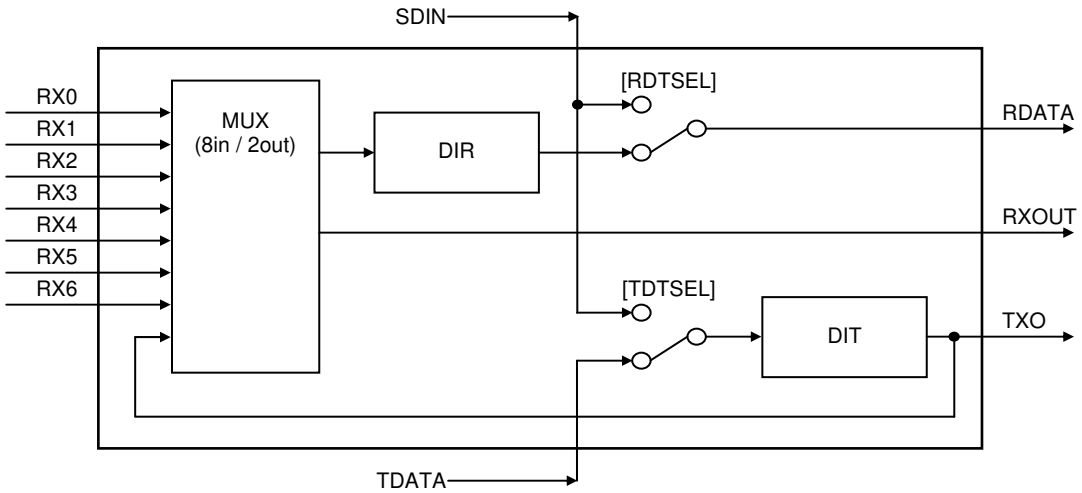


Figure 10.10 Data System Diagram

10.3.5 Calculation of input data sampling frequency

- The input data sampling frequency is calculated using the XIN clock.
- In the mode where the oscillation amplifier automatically stops according to the lock status of the PLL, the input data sampling frequency is calculated during the RERR error period and completed when the oscillation amplifier stops with holding the value. Therefore, the value remains unchanged until the PLL becomes unlocked.
- If the oscillation amplifier is in a continuous operation mode, calculation is repeated constantly. Even if sampling changes within the PLL capture range for input data whose channel status sampling information does not change, the calculation results that follow the input data can be read.
- The calculation result can be read from CCB address 0xEB and output registers DO4 to DO7 and DO8 to DO15. Registers DO4 through DO7 hold the encoded result, while DO8 through DO15 hold the calculated counter value. However, as the calculation count value is output in 8 bit units, fs capable of being calculated are greater than 24kHz. For details, see Chapter 12. Microcontroller Interface.