Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Ordering number : ENA1056A

LC89058W-E

CMOS IC

Digital Audio Interface Receiver

ON Semiconductor®
http://onsemi.com

1. Overview

The LC89058W-E is a digital audio interface receiver IC that demodulates signals according to a data transfer format between digital audio devices via the IEC60958/61937 and JEITA CPR-1205. It supports demodulation sampling frequencies of up to 192kHz. The LC89058W-E can easily replace the existing LC89057W-VF4A-E.
The LC89058W-E incorporates a number of features for its low cost and is optimal for receiving digital data for AV amplifiers and receivers.

2. Features

2.1 Clock

- Built-in PLL false lock prevention circuit to provide accurate lock.
- Includes built-in oscillation amplifier and frequency divider for quartz resonator.
- Output clock: 512fs, 256fs, 128fs, 64fs, 32fs, 16fs, 2fs, fs, 1/2fs, and 1/4fs.
- Possible to set the oscillation amplifier (external input) clock output regardless of the PLL status.
- Generates transition period signal for switching between the PLL clock and oscillation amplifier (external input) clock.
- Allows the user to set the PLL clock output frequency for each sampling frequency band of input data.

2.2 Data

- Can receive S/PDIF and serial data at sampling frequencies of 32kHz to 192kHz.
- Equipped with a total of 7 digital data input pins: 1 input pin with an amplifier and 6 input pins with 5V tolerable TTL level signal.
- Can generate data to be demodulated and through output data separately from a maximum of 7 kinds of S/PDIFs.
- Equipped an S/PDIF input data detection function. Possible to monitor the data input status of 32kHz to 192kHz with microcontroller.

Continued on next page.

Continued from preceding page.

- Equipped with a serial data input pin. Possible to switch with demodulation output automatically according to the state of the PLL circuit.
- The fs reception range of S/PDIF interface can be limited. LC89058W-E can be set to a no-signal input state if the reception range is exceeded.
- Supports I^2S data output that facilitates interfacing with DSP.

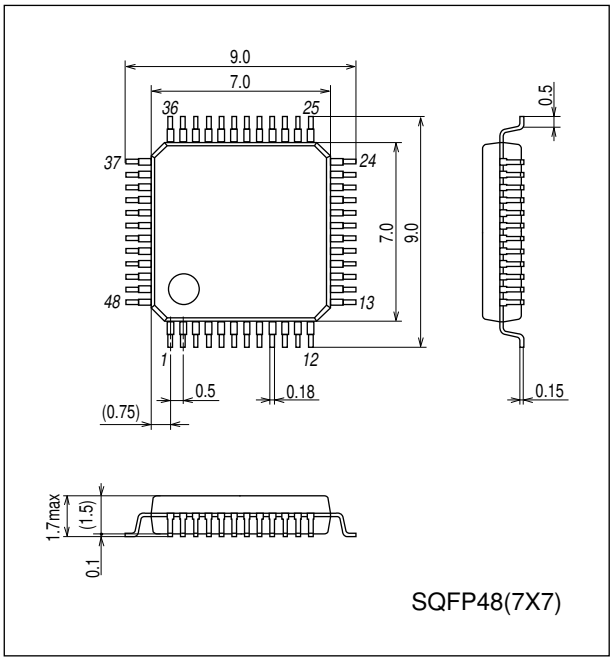
2.3 Other

- Supports Multi-channel transfer and reception, using master/slave function.
- Equipped with a 4bits general-purpose I/O pins. They can be used for interface with peripheral ICs.
- The general-purpose I/O pins can also serve as selector inputs. Possible to switch with HDMI and XM-radio signals.
- Generates a DTS-CD/LD detection flag on detection of a DTS synchronization signal.
- Outputs interrupt signal for microcontroller (interrupt source can be selected).
- Calculates sampling frequency of input signal and outputs it from the terminal or microcontroller interface.
- Outputs IEC61937 burst preamble Pc from microcontroller interface.
- Outputs IEC60958 bit 1 of channel status (non-PCM data delimiter bit).
- Outputs emphasis information of channel status.
- Can use up to four LC89058W-Es at the same time by setting the 2-bit chip address.
- Runs on a single 3.3V power supply (S/PDIF input and microcontroller interface support 5V TTL interface.)
- SQFP48 package

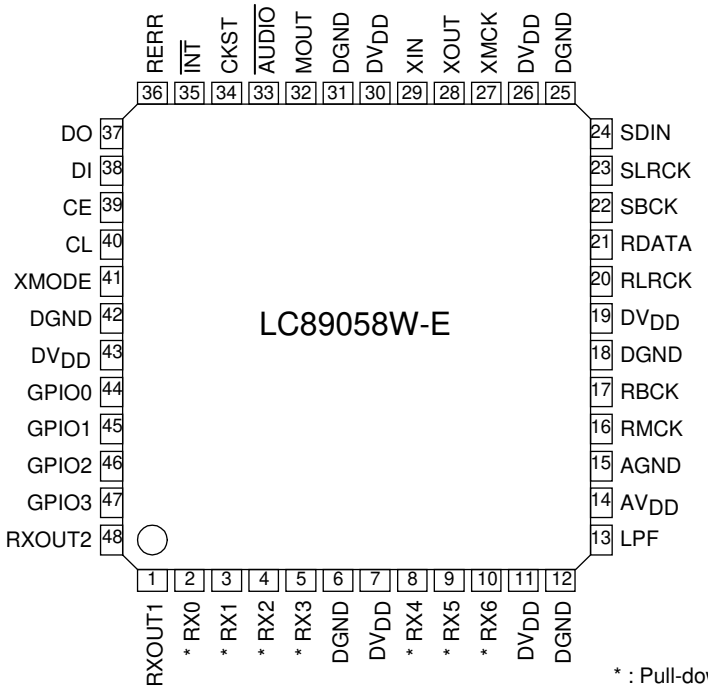
Package Dimensions

unit : mm (typ)

3163B



4. Pin Assignment



* : Pull-down resistor internal at no selection

Top view

5. Pin Functions

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	RXOUT1	O	RX0-6 input S/PDIF through output pin 1
2	RX0	I_5(pd)	5V withstand voltage TTL input level compatible S/PDIF input pin (connected to GND when RX1 is set)
3	RX1	I(pd)	Co-axial compatible S/PDIF input pin (supported demodulation sampling frequency of up to 96kHz)
4	RX2	I_5(pd)	5V withstand voltage TTL input level compatible S/PDIF input pin (connected to GND when RX1 is set)
5	RX3	I_5(pd)	5V withstand voltage TTL input level compatible S/PDIF input pin
6	DGND		Digital GND
7	DV_{DD}		Digital power supply (3.3V)
8	RX4	I_5(pd)	5V tolerable TTL input level compatible S/PDIF input pin
9	RX5	I_5(pd)	5V tolerable TTL input level compatible S/PDIF input pin
10	RX6	I_5(pd)	5V tolerable TTL input level compatible S/PDIF input pin
11	DV_{DD}		Digital power supply (3.3V)
12	DGND		Digital GND
13	LPF	O	PLL loop filter connection pin
14	AV_{DD}		Analog power supply (3.3V)
15	AGND		Analog GND
16	RMCK	O	R system clock output pin (VCO, 512fs, XIN)
17	RBCK	O/I	R system bit clock I/O pin (64fs)
18	DGND		Digital GND
19	DV_{DD}		Digital power supply (3.3V)
20	RLRCK	O/I	R system LR clock I/O pin (fs)
21	RDATA	O	Serial audio data output pin
22	SBCK	O	S system bit clock output pin (16fs, 32fs, 64fs, 128fs)
23	SLRCK	O	S system LR clock output pin (fs/4, fs/2, fs, 2fs)
24	SDIN	I_5	External serial audio data input pin

Continued on next page.

Continued from preceding page.

Pin No.	Name	I/O	Function
25	DGND		Digital GND
26	DV_{DD}		Digital power supply (3.3V)
27	XMCK	O	Oscillation amplifier clock output pin
28	XOUT	O	Output pin connected to the resonator
29	XIN	I	External clock input pin, connected to the resonator (12.288MHz/24.576MHz)
30	DV_{DD}		Digital power supply
31	DGND		Digital GND
32	MOUT	I/O	Emphasis information || Input fs monitor output || Chip address setting input pin
33	$\overline{\text{AUDIO}}$	I/O	Channel status bit 1 output || Chip address setting input pin
34	CKST	I/O	Clock switching transition period signal output || Master/slave setting input pin
35	$\overline{\text{INT}}$	I/O	Microcontroller interrupt signal output || Pins44-48 I/O setting input pin
36	RERR	O	PLL lock error, data error flag output pin
37	DO	O	CCB microcontroller I/F, read data output pin (3-state)
38	DI	I_5	CCB microcontroller I/F, write data input pin
39	CE	I_5	CCB microcontroller I/F, chip enable input pin
40	CL	I_5	CCB microcontroller I/F, clock input pin
41	XMODE	I_5	System reset input pin
42	DGND		Digital GND
43	DV_{DD}		Digital power supply (3.3V)
44	GPIO0	O/I	General-purpose I/O pin || Selector input pin (output referred to RDATA pin)
45	GPIO1	O/I	General-purpose I/O pin || Selector input pin (output referred to RLRCK pin)
46	GPIO2	O/I	General-purpose I/O pin || Selector input pin (output referred to RBCK pin)
47	GPIO3	O/I	General-purpose I/O pin || Selector input pin (output referred to RMCK pin)
48	RXOUT2	O	RX0-6 input S/PDIF through output pin 2

* Input voltage: I= -0.3 to 3.6V, I_5 = -0.3 to 5.5V
* Output voltage: O= -0.3 to 3.6V
* Pins 2, 4, 5, 8, 9, 10, 24, 38, 39, 40, and 41 have an internal pull-down resistor (pd).
  Their level is fixed when they are unselected.
* Pins 32 and 33 are input pins for chip address setting when pin 41 is held at the low level.
* Pin 34 serves as the input pin for designating as the master or slave when pin 41 is held at the low level.
* Pin 35 serves as the input pin for configuring the I/O of pins 44 to 47 when pin 41 is held at the low level.
* The DV_{DD} and AV_{DD} pins must be held at the same level and turned on and off at the same timing to preclude Latch-up conditions.

6. Block Diagram

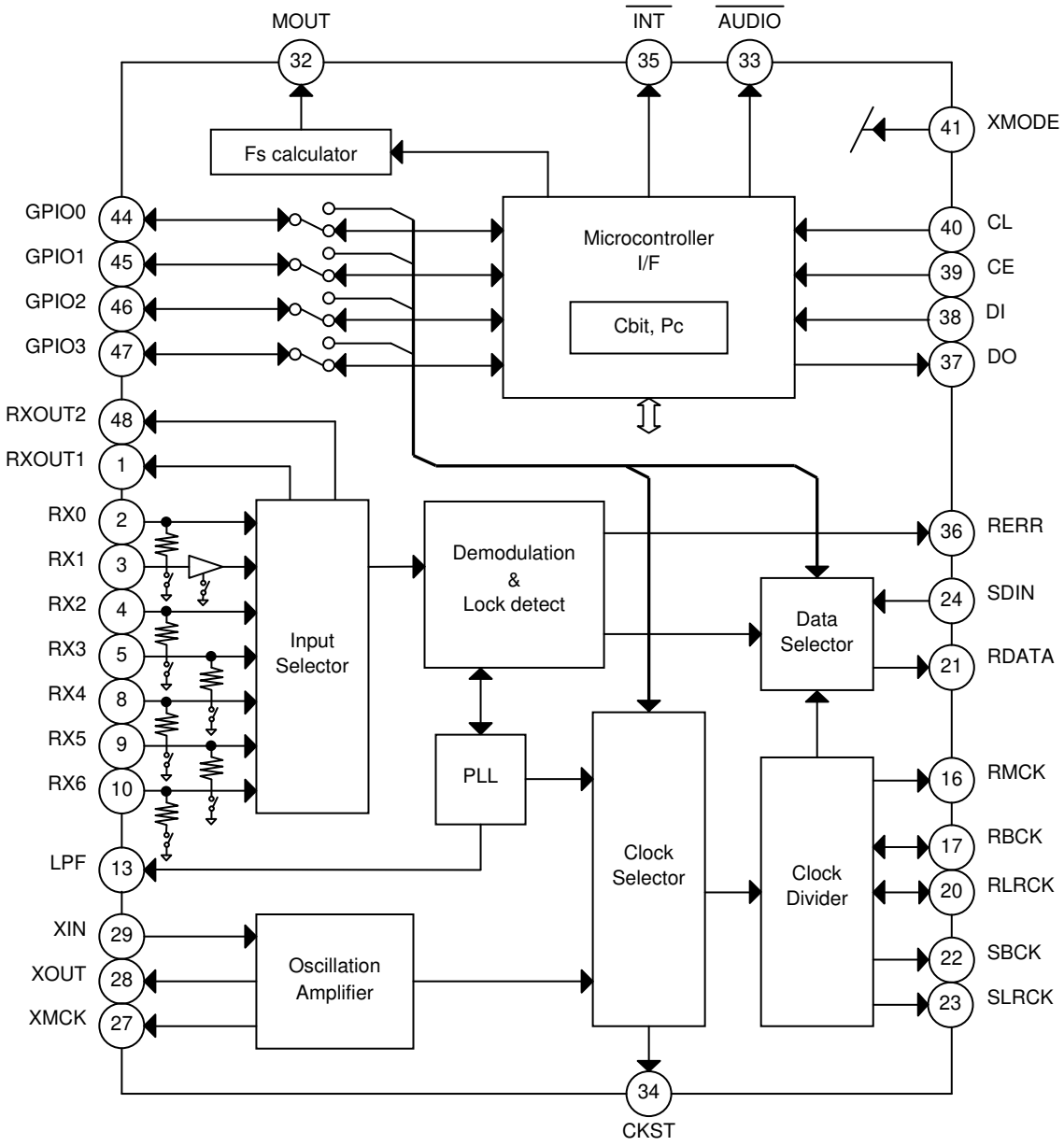


Figure 6.1 LC89058W-E Block Diagram

7 Common and Different Points between LC89057W-VF4A-E and LC89058W-E

7.1 Common Features

Table 7.1: Common of LC89057W-VF4A-E and LC89058W-E functions (Hardware/Software Compatibility)

Item	LC89057W-VF4A-E	LC89058W-E
Package	SQFP48(9x9)	←
Supply voltage	3.3V single source	←
DIR reception range	32kHz to 192kHz	←
Oscillation amplifier input frequency	12.288MHz/24.576MHz	←
2-system-clock pin output	RMCK, RBCK, RLRCK, SBCK, SLRCK	← SBCK: 16fs, SLRCK: 1/4 output added
S/PDIF inputs	7 maximum (1 coaxial, 6 optical)	←
Serial data input	SDIN	←
Non-PCM flag output	$\overline{\text{AUDIO}}$	←
Emphasis information output	EMPHA (consumer and professional)	← MOUT (consumer only)
DTS-CD/LD detection function	14-bit format detection supported	←
General-purpose I/O	4 bits	←
Chip address setting	4 addresses maximum (master/salve supported)	←
Mode setting external resistor	4 resistors used	←
Microcontroller interface	CCB (Our company proprietary IF)	← DI input regulations has.
Register configuration	4 command address bits, 8 data bits	←

7.2 Removed Functions

Table 7.2: Differences between LC89057W-VF4A-E and LC89058W-E (Removed Functions)

Item	LC89057W-VF4A-E	LC89058W-E
Function	Modulation and demodulation	Modulation removed (demodulation only)
S/PDIF unlock path switching	Yes	Removed
External clock synchronization mode	Yes	Removed
R and S system clock synchronization	Asynchronous system	Synchronization clock (SELMTD, RCKSEL removed)
Data output format	16, 20, 24 bits/left-justified/right-justified MSB, I^2S	Right-justified removed (left-justified MSB, I^2S only)
C, V, U pin output	Yes	Removed
Input fs computed output	16kHz to 192kHz	32kHz to 192kHz (fs < 32kHz, removed)
Microcontroller interrupt signal	Yes (Low pulse, Low level output)	Pulse output mode removed (level output only)

7.3 Added or Modified Functions

Table 7.3: Differences between LC89057W-VF4A-E and LC89058W-E (Added or Modified Functions)

Item	LC89057W-VF4A-E	LC89058W-E	Page
Oscillation amplifier initial setting	Suspended while PLL is locked	Permanent operation	19
PLL clock output	256fs or 512fs	512fs	20-26
Master clock output	Multiple of input fs is output	Multiple of input fs on each band is output	22
Clock output when XIN source	No limitation	RBCK and SBCK must 1/2 or less of RMCK	23
Clock switching	Clock count is preserved (to maintain continuity)	Switched during the CKST pulse output	25
RMCK and CKST polarity	Polarity cannot be switched	Polarity can be switched	23, 25
S/PDIF reception limitation	Reflected only to error flag.	Reflected to both error flag and clock output	26
S/PDIF input detection range	32kHz to 96kHz (XIN=24.57M/12.28MHz)	32kHz to 192kHz (XIN=24.576MHz only)	27
Input fs value monitor output	Microcontroller interface output only	Microcontroller interface and pin outputs	32
General-purpose I/O input pin	No timing control	Polling supported (with interrupt)	36
General-purpose I/O input/output pin	Parallel I/O function only	Internal selector input also supported.	37

7.4 Differences in Microcontroller Registers

7.4.1 Differences in write commands

Table 7.4: LC89057W-VF4A-E Write Register Map

Addr	Setting Item	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	All system	TESTM	0	TXOPR	RXOPR	INTOPF	0	DOEN	SYSRST
1	Demodulator system	PBSEL1	PBSEL0	FSLIM1	FSLIM0	RXMON	AOSEL	VOSEL	UOSEL
2	Master clock	AMPOPR1	AMPOPR0	EXSYNC	PLLOPR	XMSEL1	XMSEL0	XINSEL	PLLSEL
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switching	0	RDTMUT	RDTSTA	RDTSEL	0	RCKSEL	OCKSEL	SELMTD
6	Data input/output	RXOFF	ROSEL2	ROSEL1	ROSEL0	ULSEL	RISEL2	RISEL1	RISEL0
7	Output format	SLRCKP	SBCKP	RLRCKP	RBCKP	0	OFSEL2	OFSEL1	OFSEL0
8	$\overline{\text{INT}}$ source selection	EMPF	SLIPO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR conditions	ERWT1	ERWT0	FSERR	RESTA	XTWT1	XTWT0	REDER	RESEL
10	Modulation system	PI3	PI2	PI1	PI0	0	VMODE	VISEL	UISEL
11	Modulation data	TCKSEL	0	TXMOD1	TXMOD0	TXMUT	TDTSEL	TXLRP	TXDFS
12	Test	0	0	0	0	0	0	0	0
13	Test	0	0	0	0	0	0	0	0
14	Test	0	0	0	0	0	0	0	0
15	Test	0	0	0	0	0	0	0	0

Table 7.5: LC89058W-E Write Register Map

Addr	Setting Item	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	System setting 1	TESTM	0	“0”	“0”	“0”	0	DOEN	SYSRST
1	System setting 2	“0”	“0”	FSLIM1	FSLIM0	RXMON	AOSEL	“0”	MOSEL
2	Master clock	AMPOPR1	AMPOPR0	“0”	PLLOPR	XMSEL1	XMSEL0	XINSEL	“0”
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switching	0	RDTMUT	RDTSTA	RDTSEL	0	0	OCKSEL	0
6	Data input/output 1	“0”	ROSEL2	ROSEL1	ROSEL0	“0”	RISEL2	RISEL1	RISEL0
7	Output format	SLRCKP	SBCKP	RLRCKP	RBCKP	0	“0”	“0”	OFDSEL
8	$\overline{\text{INT}}$ source selection	EMPF	GPIO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR condition setting	ERWT1	ERWT0	FSERR	RESTA	“0”	“0”	REDER	RESEL
10	General-purpose I/O	PI3	PI2	PI1	PI0	0	“0”	“0”	“0”
11	Test	“0”	0	“0”	“0”	“0”	“0”	“0”	“0”
12	System setting 3	0	0	CKSTP	RMCKP	0	PLLDV1	PLLDV0	PLLACC
13	Data input/output 2	0	RXSEL2	RXSEL1	RXSEL0	EDTMUT	EMCKP	EXTSEL	GPIOS
14	Other output settings	FSSEL1	FSSEL0	0	0	PTOXW1	PTOXW0	0	0
15	Test	0	0	0	0	0	0	0	0

- Except MOSEL, PRSEL [1:0], OFDSEL, GPIO, SELMTD and RCKSEL, the command address of any inadvertently specified commands that are removed from the LC89057W-VF4A-E is assumed to be “0” and ignored.
  The new commands added to the LC89058W-E are allocated to command addresses 12, 13, and 14.

7.4.2 Differences in read commands

Table 7.6: Changes in the Register Function between LC89057W-VF4A-E and LC89058W-E

CCB Address	LC89057W-VF4A-E	LC89058W-E
0xE9	DIT channel status write register	Removed

Table 7.7: Differences in Read Registers between the LC89057W-VF4A-E and LC89058W-E

Register	LC89057W-VF4A-E		LC89058W-E	
	0xEA	0xEB	0xEA	0xEB
DO0	RXDET0	PO0	RXDET0	PO0
DO1	RXDET1	PO1	RXDET1	PO1
DO2	RXDET2	PO2	RXDET2	PO2
DO3	RXDET3	PO3	RXDET3	PO3
DO4	RXDET4	FSC0	RXDET4	FSC0
DO5	RXDET5	FSC1	RXDET5	FSC1
DO6	RXDET6	FSC2	RXDET6	FSC2
DO7	RXDET7	FSC3	0	FSC3
DO8	OERROR	FSDAT0	OERROR	-
DO9	OINDET	FSDAT1	OINDET	-
DO10	OFSCHG	FSDAT2	OFSCHG	-
DO11	OCSRNW	FSDAT3	OCSRNW	-
DO12	OUNPCM	FSDAT4	OUNPCM	-
DO13	OPCRNW	FSDAT5	OPCRNW	-
DO14	OSLIPO	FSDAT6	OGPIO	-
DO15	OEMPF	FSDAT7	OEMPF	-
DO16	CSBIT1	-	CSBIT1	-
DO17	IEC1937	-	IEC1937	-
DO18	DTS51	-	DTS51	-
DO19	DTSES	-	DTSES	-
DO20	F0512	-	0	-
DO21	F1024	-	0	-
DO22	F2048	-	0	-
DO23	F4096	-	0	-

• The CCB addresses 0xEC and 0xED remain the same for both the LC89057W-VF4A-E and LC89058W-E.

7.5 Points to Notice about Replacing

- When replacing the LC89057W-VF4A-E with the LC89058W-E, it may be necessary to review the circuit pattern design of the printed circuit board in advance depending how the device is used. Particular attention should be directed to pins 44 to 48 whose I/O functionality can be set according to the $\overline{\text{INT}}$ pin setting. This section contains the notes and cautions to be observed when replacing the LC89057W-VF4A-E with the LC89058W-E. For details of the $\overline{\text{INT}}$ pin, see Chapter 9, Initial System Settings and Chapter 10, Description of Demodulation Function.
- Refer to the specifications of LC89057W-VF4A-E when replacing LC89058W-E with LC89057W-VF4A-E.

Table 7.8: Differences between LC89057W-VF4A-E and LC89058W-E (Pins 44 to 48)

$\overline{\text{INT}}$ Pin	LC89057W-VF4A-E					LC89058W-E				
Pull-down	Modulation function					General-purpose I/O function				S/PDIF
	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48
	TMCK	TBCK	TLRCK	TDATA	TXO	GPIO0	GPIO1	GPIO2	GPIO3	RXOUT2
	Input	Input	Input	Input	Output	Input	Input	Input	Input	Output
Pull-up	General-purpose I/O function					General-purpose I/O function				S/PDIF
	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48
	PIO0	PIO1	PIO2	PIO3	PIOEN	GPIO0	GPIO1	GPIO2	GPIO3	RXOUT2
	In/Output	In/Output	In/Output	In/Output	Input	Output	Output	Output	Output	Output

7.5.1 Change from LC89057W-VF4A-E to LC89058W

7.5.1 When the $\overline{\text{INT}}$ pin is set to pull-down

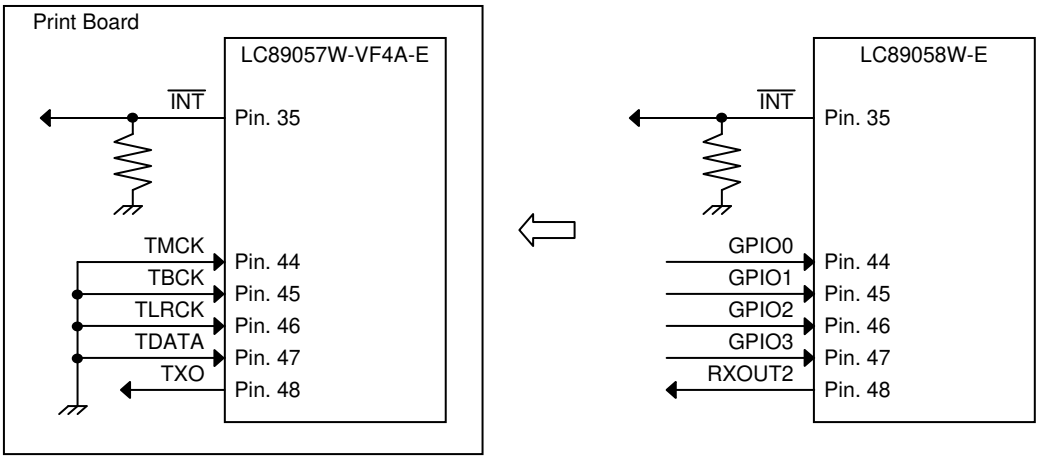


Figure 7.1 Change from LC89057W-VF4A-E to LC89058W-E (when the $\overline{\text{INT}}$ pin is set to pull-down)

- In this case, the system that doesn't use a modulation function or a general-purpose I/O function can be replaced with LC89058W-E.
- After the replacement, LC89058W-E is used on condition that it pins 44 to 47 connect with GND and pin 48 open.

7.5.1.2 When the $\overline{INT}$ pin is set to pull-up

7.5.1.2.1 In case of "Pin 48 = GND"

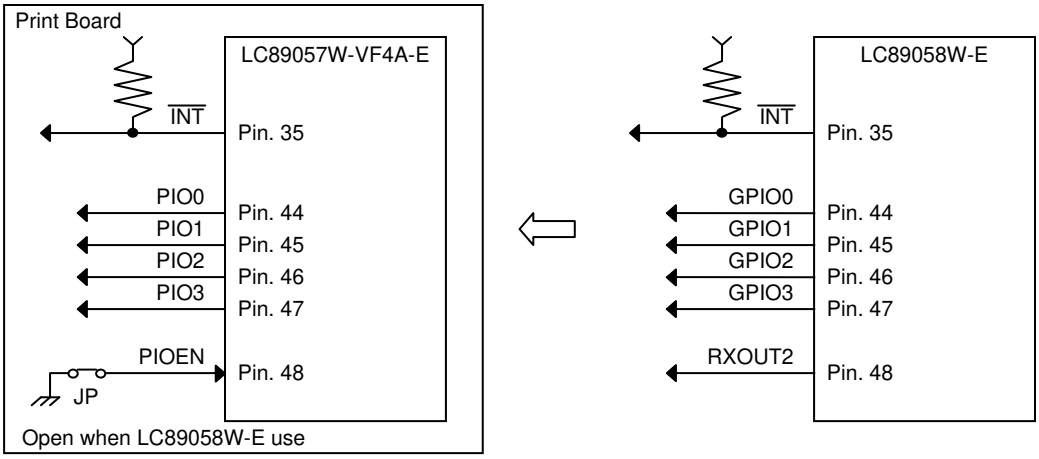


Figure 7.2 Change from LC89057W-VF4A-E to LC89058W-E (when the $\overline{INT}$ pin is set to pull-up) 1

- After the replacement, pins 44 to 47 can be used as general purpose I/O output function. (pin 48 open)
- It is necessary to review the circuit pattern of the printed circuit board because the I/O setting of pin 48 differs from each other.

7.5.1.2.2 In case of "Pin 48 = V_{DD}"

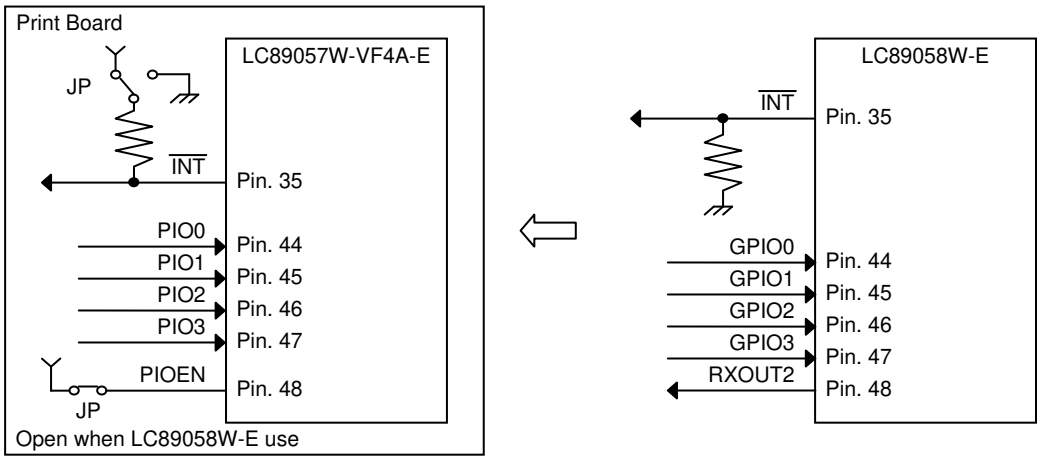


Figure 7.3 Change from LC89057W-VF4A-E to LC89058W-E (when the $\overline{INT}$ pin is set to pull-up) 2

- It is necessary to review the circuit pattern of the printed circuit board to change the pull-up resistor of pin 35 to the pull-down resistor because pins 44 to 47 is used as general purpose I/O input function.
- It is necessary to review the circuit pattern of the printed circuit board because the I/O setting of pin 48 differs from each other.

7.5.2 Change from LC89058W-E to LC89057W-VF4A-E

7.5.2.1 When the $\overline{\text{INT}}$ pin is set to pull-down

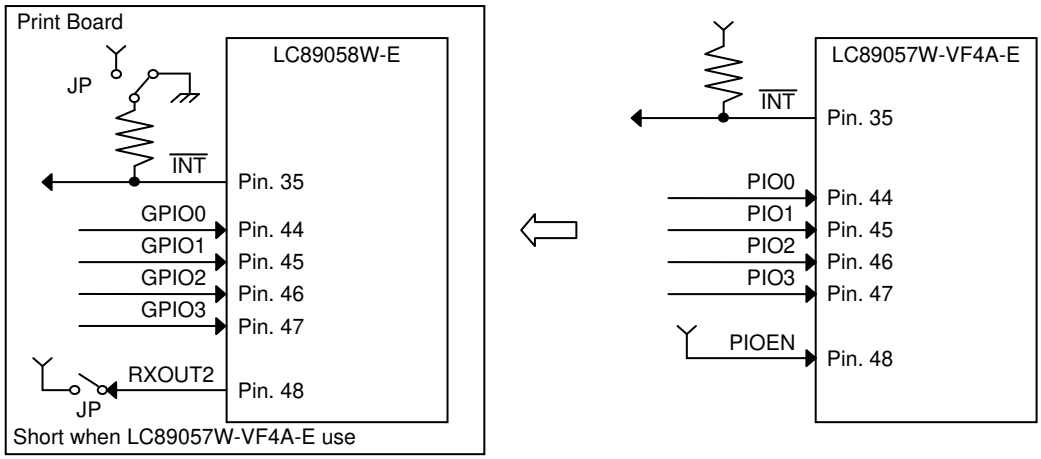


Figure 7.4 Change from LC89058W-E to LC89057W-VF4A-E (when the $\overline{\text{INT}}$ pin is set to pull-down)

- It is necessary to review the circuit pattern of the printed circuit board to change the pull-up resistor of pin 35 to the pull-down resistor because pins 44 to 47 is used as general purpose I/O input function.
- It is necessary to review the circuit pattern of the printed circuit board because the I/O setting of pin 48 differs from each other.
- After the replacement, the RXOUT2 output of LC89057W-VF4A-E cannot be used.

7.5.2.2 When the $\overline{\text{INT}}$ pin is set to pull-up

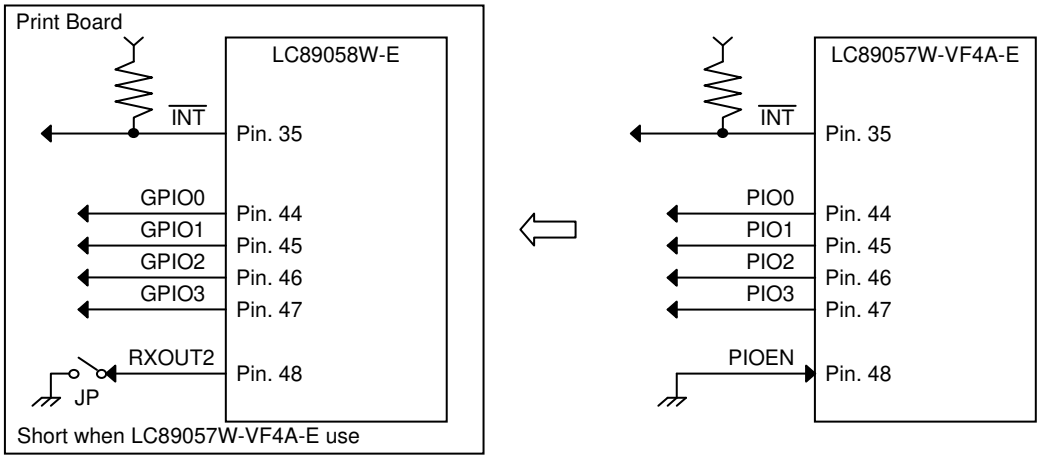


Figure 7.5 Change from LC89058W-E to LC89057W-VF4A-E (when the $\overline{\text{INT}}$ pin is set to pull-up)

- After the replacement, pins 44 to 47 can be used as general purpose I/O output function. However, it is necessary to review the circuit pattern of printed circuit board because pin 48 has to GND.
- After the replacement, the RXOUT2 output of LC89057W-VF4A-E cannot be used.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 8.1: Absolute Maximum Ratings at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	AV_{DD} max	8-1-1	-0.3 to +4.6	V
Maximum supply voltage	DV_{DD} max	8-1-2	-0.3 to +4.6	V
Input voltage 1	$V_{IN}1$	8-1-3	-0.3 to V_{DD}+0.3 (max.3.9V)	V
Input voltage 2	$V_{IN}2$	8-1-4	-0.3 to +5.8	V
Output voltage	V_{OUT}	8-1-5	-0.3 to V_{DD}+0.3 (max.3.9V)	V
Storage ambient temperature	Tstg		-55 to +125	°C
Operating ambient temperature	Topr		-30 to +70	°C
Maximum input/output current	I_{IN}, I_{OUT}	8-1-6	±20	mA

8-1-1: AV_{DD} pin
8-1-2: DV_{DD} pin
8-1-3: RX1, RBCK, RLRCK, XIN, GPIO0, GPIO1, GPIO2, GPIO3 pins
8-1-4: RX0, RX2, RX3, RX4, RX5, RX6, SDIN, DI, CE, CL, XMODE pins
8-1-5: RXOUT1, RMCK, RBCK, RLRCK, RDATA, SBCK, SLRCK, XMCK, XOUT, MOUT, $\overline{\text{AUDIO}}$ pins, CKST, $\overline{\text{INT}}$, RERR, DO, GPIO0, GPIO1, GPIO2, GPIO3, RXOUT2 pins
8-1-6: Per input/output pin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

8.2 Allowable Operating Ranges

Table 8.2: Recommended Operating Conditions at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	AV_{DD}, DV_{DD}		3.0	3.3	3.6	V
Input voltage range 1	$V_{IN}1$	8-2-1	0	3.3	AV_{DD}, DV_{DD}	V
Input voltage range 2	$V_{IN}2$	8-2-2	0	3.3	5.5	V
Operating temperature	Topr		-30		70	°C

8-2-1: RX1, RBCK, RLRCK, XIN, GPIO0, GPIO1, GPIO2, GPIO3 pins
8-2-2: RX0, RX2, RX3, RX4, RX5, RX6, SDIN, DI, CE, CL, XMODE pins

8.3 DC Characteristics

Table 8.3: DC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input, High	V_{IH}	8-3-1	$0.7V_{DD}$			V
Input, Low	V_{IL}				$0.2V_{DD}$	V
Input, High	V_{IH}	8-3-2	2.0		5.8	V
Input, Low	V_{IL}		-0.3		0.8	V
Output, High	V_{OH}	8-3-3	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-4	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-5	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-6	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Input amplitude	V_{PP}	8-3-7	200			mV
Consumption current	I_{DD}	8-3-8			40	mA
Pull-down resistance	R_{DN}	8-3-9	25	50	100	kΩ

8-3-1: CMOS compatible: RBCK, RLRCK input pins during XIN and slave settings
8-3-2: TTL compatible: Input pins other than those listed above
8-3-3: I_{OH} = −12mA, I_{OL} = 8mA: RMCK output pin
8-3-4: I_{OH} = −8mA, I_{OL} = 8mA: XOUT, XMCK output pins
8-3-5: I_{OH} = −4mA, I_{OL} = 4mA: RXOUT1, RBCK, RLRCK, RDATA, SBCK, SLRCK, RERR, MOUT, GPIO0, GPIO1, GPIO2, GPIO3, RXOUT2 output pins
8-3-6: I_{OH} = −2mA, I_{OL} = 2mA: Output pins other than those listed above
8-3-7: Before capacitance of RX1 input pin, and reception frequency is possible up to 96kHz.
8-3-8: Ta=25°C, fs=96kHz
8-3-9: RX0, RX2, RX3, RX4, RX5, RX6 input pins

8.4 AC Characteristics

Table 8.4: AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RX0, RX2 to RX6 fs frequency	f_{RFS1}		28		195	kHz
RX1 fs frequency	f_{RFS2}		28		108	kHz
RX0, RX2 to RX6 pulse width	t_{WDI1}		20			ns
RX1 pulse width	t_{WDI2}		40			ns
RX0 to RX6 duty factor	t_{DUY}		40		60	%
XIN clock frequency	f_{XF}	8-4-1	12		25	MHz
RMCK clock frequency	f_{MCK}		4		50	MHz
RMCK clock jitter	tj			200		ps
RMCK, RBCK delay	t_{MBO}				10	ns
RBCK, RDATA delay	t_{BDO}				10	ns
RMCK, SBCK delay	t_{MBO}	8-4-2			10	ns
SBCK, RDATA delay	t_{BDO}	8-4-3			10	ns

8-4-1 A frequency compatible with the XINSEL setting must be applied to XIN.
8-4-2: When RMCK and SBCK source clocks are identical
8-4-3: When SBCK is the PLL source clock

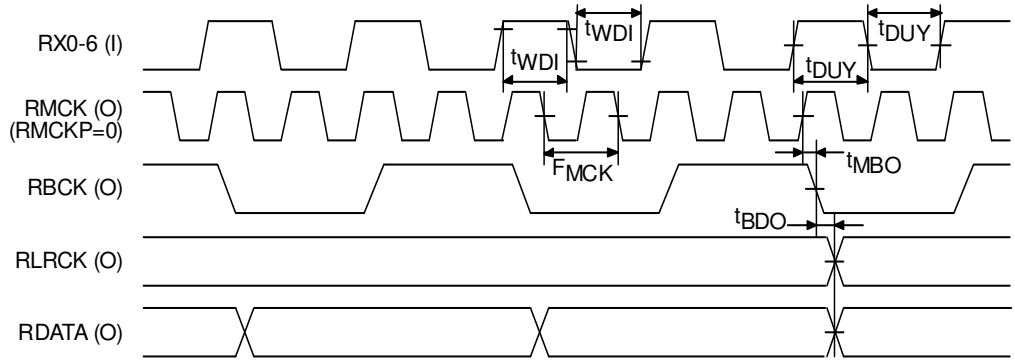


Figure 8.1 AC Characteristics of Demodulation function

8.5 CCB Microcontroller Interface AC Characteristics

Table 8.5: CCB Microcontroller Interface AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XMODE pulse width, Low	$t_{RST\ dw}$		200			µs
CL pulse width, Low	$t_{CL\ dw}$		100			ns
CL pulse width, High	$t_{CL\ uw}$		100			ns
CL to CE setup time	$t_{CE\ setup}$		50			ns
CL to CE hold time	$t_{CE\ hold}$	8-5-1	50			ns
CL to CE hold time	$t_{CE\ hold}$	8-5-2	0			ns
CL to DI setup time	$t_{DI\ setup}$		50			ns
CL to DI hold time	$t_{DI\ hold}$		50			ns
CL to CE hold time	$t_{CL\ hold}$		50			ns
CL to DO delay time	$t_{CL\ to\ DO}$				20	ns
CE to DO delay time	$t_{CE\ to\ DO}$				20	ns
DI pulse width	$t_{DI\ dw}$	8-5-3	200			ns

8-5-1: CL has to lower before CE is H when CL is normal H clock.
8-5-2: Only when data write with CL of normal H clock.
8-5-3: DI has to L period when DI is normal H.

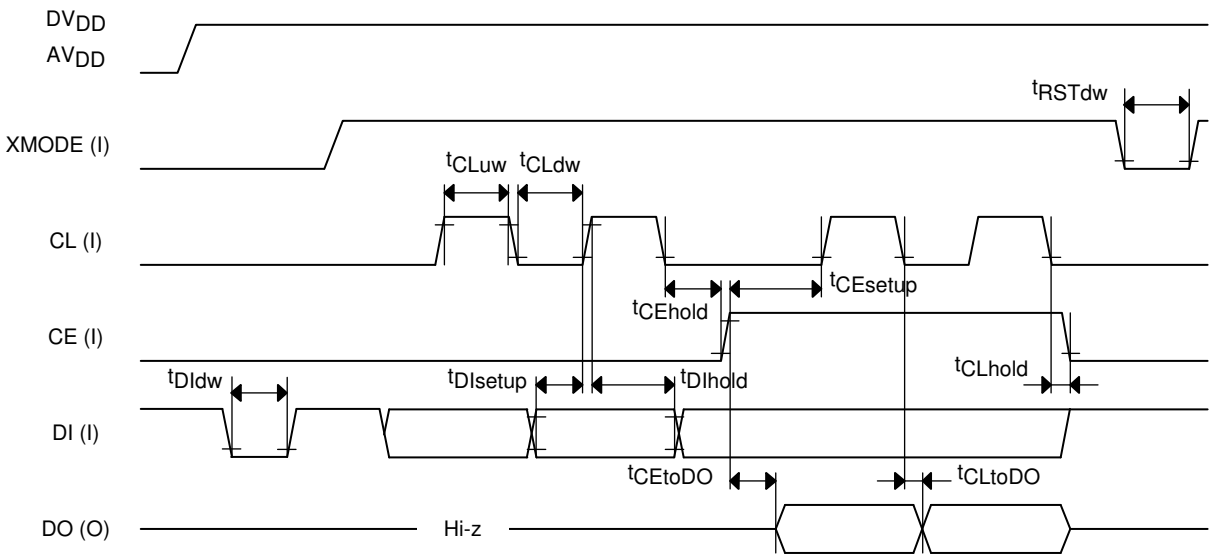


Figure 8.2 CCB Microcontroller Interface AC Characteristics

9. Initial System Settings

9.1 System Reset (XMODE)

- The system operates correctly when XMODE is set to "H" after 3.0V or higher supply voltage is applied. When XMODE is set to "L" after power is turned on, the system is reset.
- To set chip address, master/slave, or pins 44 to 47 I/O, 10kΩ pull-down or pull-up resistors must be connected to MOUT, $\overline{\text{AUDIO}}$, CKST, and $\overline{\text{INT}}$.
- If none of MOUT, $\overline{\text{AUDIO}}$, CKST, and $\overline{\text{INT}}$ are pulled down or pulled up, their pin state will get unstable when the settings are entered, resulting in wrong setting. Pull-up or pull-down resistors must be connected to these pins without fail.

Table 9.1: Pin Names and Settings

Setting	Pins
Chip address	MOUT
	$\overline{\text{AUDIO}}$
Master/slave setting	CKST
Pins 44 to 47 I/O setting	$\overline{\text{INT}}$

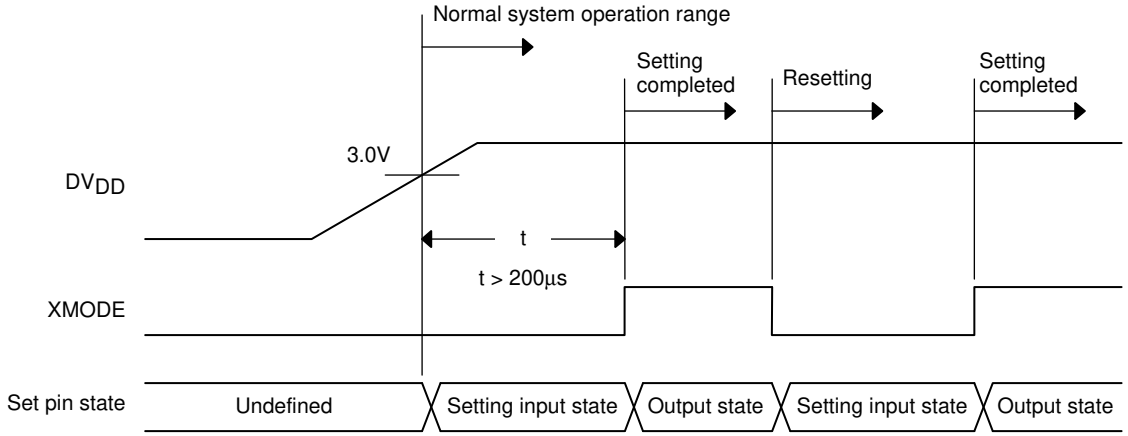


Figure 9.1 Setting Timing Chart of Function Setting Input Pins

Table 9.2: Output Pin State When XMODE is Reset (XMODE=L)

No.	Pin name	Pin State	No.	Pin name	Pin State
1	RXOUT1	RXO output	32	MOUT	Input state
16	RMCK	XIN output	33	$\overline{\text{AUDIO}}$	Input state
17	RBCK	Low output	34	CKST	Input state
20	RLRCK	High output	35	$\overline{\text{INT}}$	Input state
21	RDATA	Low output	36	RERR	High output
22	SBCK	Low output	37	DO	Hi-z output
23	SLRCK	High output	48	RXOUT2	Low output
27	XMCK	XIN output			

9.2 Chip Address Settings (MOUT, $\overline{\text{AUDIO}}$)

- The LC89058W-E comes with a function to set a unique chip address to allow the use of several LC89058W-E on the same microcontroller interface bus.
- In chip address setting, connect a 10kΩ pull-down or pull-up resistor to MOUT and $\overline{\text{AUDIO}}$. By this setting, 4 kinds of chip addresses can be set at a maximum.
- Chip addresses in the microcontroller interface are set with CAL and CAU provided as the first two bits on the LSB side. CAL corresponds to the lower chip address and CAU to the higher chip address.
- Command writing is enabled by making the chip address settings with MOUT and $\overline{\text{AUDIO}}$ identical to the chip addresses sent from the microcontroller.
- The chip address setting is required even when only one LC89058W-E is used in the system. If the chip address is not set, the chip address is undefined and the microcontroller cannot control the system. When the microcontroller is not used, a chip address-setting pin is input open while XMODE is "L". Be sure to connect either a pull-down resistor or a pull-up resistor to MOUT and $\overline{\text{AUDIO}}$.

Table 9.3: Chip Address Settings (Resistor Connection)

$\overline{\text{AUDIO}}$	MOUT	CAU	CAL
Pull-down	Pull-down	0	0
Pull-down	Pull-up	0	1
Pull-up	Pull-down	1	0
Pull-up	Pull-up	1	1

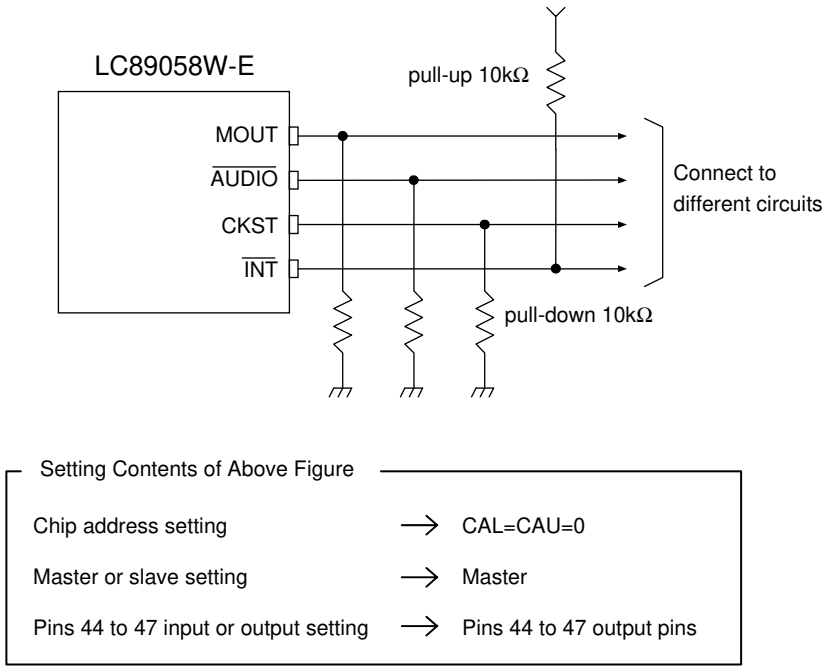


Figure 9.2 Setting Example of Function Setting Input Pin

9.3 Master/Slave Settings (CKST)

- A master/slave function that allows multi-channel synchronized transfer using multiple LC89058W-Es is included. For this setting, connects either a 10kΩ pull-down or a pull-up resistor to CKST.
- Set to the master mode normally, when single LC89058W-E IC is used. When multiple LC89058W-Es are used, set one of them to the master mode and the others to the slave mode.
- In the multi-channel synchronous transfer mode using multiple LC89058W-Es, connect RBCK and RLRCK (output) on the master side to RBCK and RLRCK (input) on the slave side. Also connect XMCK on the master side to XIN on the slave side. At this time, the polarity of RBCK and RLRCK, and the frequency of XIN and XMCK must be identical.
- The master/slave function runs correctly with the multiple LC89058W-Es connected.
- Be sure to connect either a pull-down resistor or a pull-up resistor to CKST.
- Always supply the clock to RBCK and RLRCK when the slave function is set.

Table 9.4: Master/Slave Switching (Register Connection)

CKST	Mode
Pull-down	Master
Pull-up	Slave

Table 9.5: Clock Pin State

Pin	Master mode	Slave mode
RMCK	Output	Output
RBCK	Output	Input
RLRCK	Output	Input

9.4 Pins 44 to 47 I/O settings ($\overline{\text{INT}}$)

- Pins 44 to 47 are provided with a bidirectional buffer.
- When setting I/O function of pins 44 to 47, connect a 10kΩ pull-down or pull-up resistor to $\overline{\text{INT}}$.
- Be sure to connect either a pull-down resistor or a pull-up resistor to $\overline{\text{INT}}$.

Table 9.6: Pins 44 to 47 I/O Settings (Resistor Connection)

$\overline{\text{INT}}$	Mode
Pull-down	Input.
Pull-up	Output.

10 Description of Demodulation Function

10.1 Clocks

10.1.1 PLL (LPF)

- The LC89058W-E incorporates a VCO (Voltage Controlled Oscillator) that can be stopped with PLLOPR and it synchronizes with sampling frequencies (fs) from 32kHz to 192kHz and with the data with transfer rate from 4MHz to 25MHz. PLL is locked at 512fs.
- LPF is a pin for PLL loop filter. Connect the following resistance and capacitance shown in the figure.

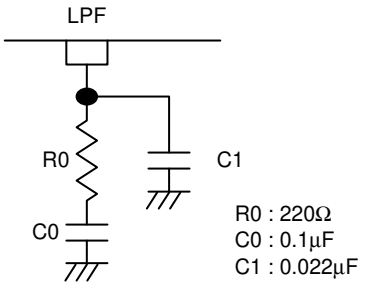


Figure 10.1 Loop Filter Configuration

10.1.2 Oscillation amplifiers (XIN, XOUT, XMCK)

- The LC89058W-E features a built-in oscillation amplifier. Connecting a quartz resonator, feedback resistor, and load capacitance to XIN and XOUT can configure an oscillation circuit. When connecting a quartz resonator, use one with a fundamental wave. Be aware that the load capacitance depends on the quartz resonator characteristics.
- If the built-in oscillation amplifier is not used and oscillation module is used as the clock source instead, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Always supply XIN with the 12.288MHz or 24.576MHz clock set with XINSEL. If supplying other frequencies to XIN, it is necessary to set that the result of change in sampling frequency fs of input data with FSERR is not reflected to an error flag. By this setting, the operation functions properly. Since it is not a recommended frequency, it cannot be used for input fs calculations.
- The setting of XINSEL must be completed prior to S/PDIF input.
- Supply XIN with clocks all the time to be used in the following applications.

  (1) Detection of presence or absence of S/PDIF input
  (2) Clock source while PLL is unlocked
  (3) Calculation of input data sampling frequency
  (4) Time definition when switching input data
  (5) External source of supply clock (clock for an AD converter, etc.) in XIN source mode.
  (6) Polling processing performed when setting the general-purpose I/O input function

- The oscillation amplifier runs even when the PLL is locked. Therefore, data detection and calculation of input sampling frequency become possible while the PLL is locked. In that case, both the oscillation amplifier clock and the PLL clock signals coexist, and then user must pay attention and make sure sound quality is not adversely affected.
- If adverse effects on the sound quality are recognized, it is possible to set with the AMPOPR [1:0] that the oscillation amplifier automatically stop operation while the PLL is locked. Therefore, setting of the AMPOPR [1:0] must be completed either prior to S/PDIF input or while PLL is unlocked.
- The oscillation amplifier can be stopped if it is unnecessary. However, when the normal operation is resumed, it must wait for 10ms or longer until the resonator oscillation gets stable.
- XMCK outputs the XIN clock. The XMCK output is set with XMSEL [1:0]. The XIN clock can be set to 1/1, 1/2, 1/4, or muted output.
- If you use only the oscillation amplifier, input the quartz resonator to XIN and XOUT or an external clock to XIN, and fix the electric potential of digital data input pins of RX0 to RX6, or set with RISEL [2:0] that all the inputs are deselected.

10.1.3 Switching between master clock and clock source

- The RMCK, RBCK, and RLRCK (hereunder, R system), and the SBCK and SLRCK (hereunder, S system) clock sources can be selected between the following two master clocks.
  (1) PLL source (512fs)
  (2) XIN source (12.288MHz or 24.576MHz)

- Clock source switching is to set with the R and S systems interlocked. This setting is carried out with OCKSEL.
- The clock source is automatically switched to the PLL or XIN clock by locking/unlocking the PLL. The clock source can be switched to XIN with OCKSEL, regardless of the PLL status.

Table 10.1: Relationship between Clock Source Switch Commands and Clock Sources when PLL Locked/Unlocked

OCKSEL	R System Clock Source		S System Clock Source	
	Locked	Unlocked	Locked	Unlocked
0	PLL	XIN	PLL	XIN
1	XIN	XIN	XIN	XIN

- The PLL status can be always monitored with RERR even after switching to the XIN source. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.

10.1.4 Points to notice about switching clock source while PLL is locked

- It is necessary to set the oscillation amplifier to the continuous operation mode at the same time with AMPOPR [1:0] to do the clock switch to the XIN source with OCKSEL when the oscillation amplifier has stopped in the state where the PLL is locked. The clock is not output when switching to the XIN clock source without executing this setting.
- In the state where the PLL is locked, if the clock is switched to XIN source with OCKSEL while the oscillator amplifier is stopped, RERR is temporarily outputs an error (high level) indication. When switched to XIN source, the oscillator amplifier is switched to the operating state at the same time.
  RERR is temporality outputs an error (H level) indication when the oscillation amplifier switches from the stop condition to the continuous mode. Consequently the input fs calculation restarts. At this time, the previous fs calculation value is reset and compared with the newly calculated fs value. Then those two values are found not identical, that’s why the error is temporarily issued.

10.1.5 Master clock block diagram (XIN, XOUT, RMCK, XMCK)

- The relationships between the two types of PLL and XIN source master clocks, switching, and the frequency division function are described below.
- The contents in the quotation marks "*** " by the switch and function blocks correspond to the write command names.
- Lock/Unlock is automatically switched by PLL locking/unlocking.

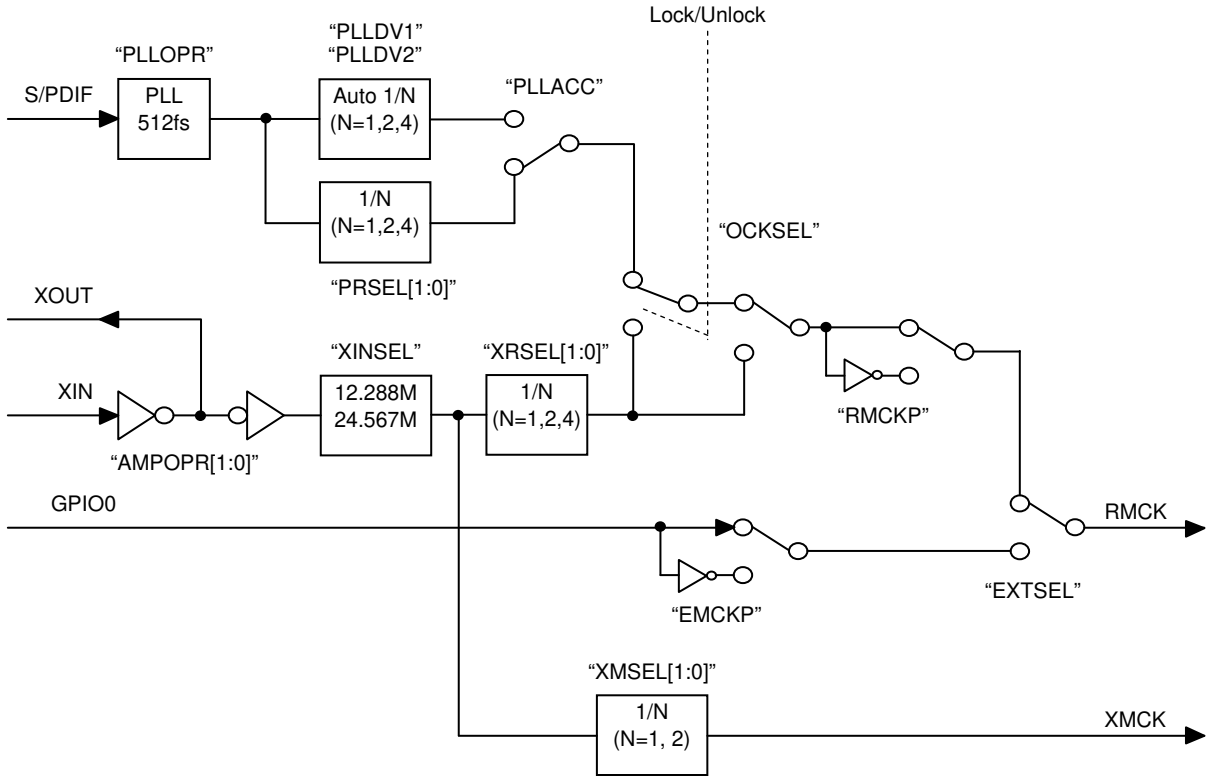


Figure 10.2 Master Clock Block Diagram

10.1.6 PLL clock output

- The PLL clock output is controlled by the PLLACC, PLLDV1, PLLDV2, or PRSEL[1:0].
- PLLACC can be used to generate a PLL lock frequency for each S/PDIF input sampling frequency band.

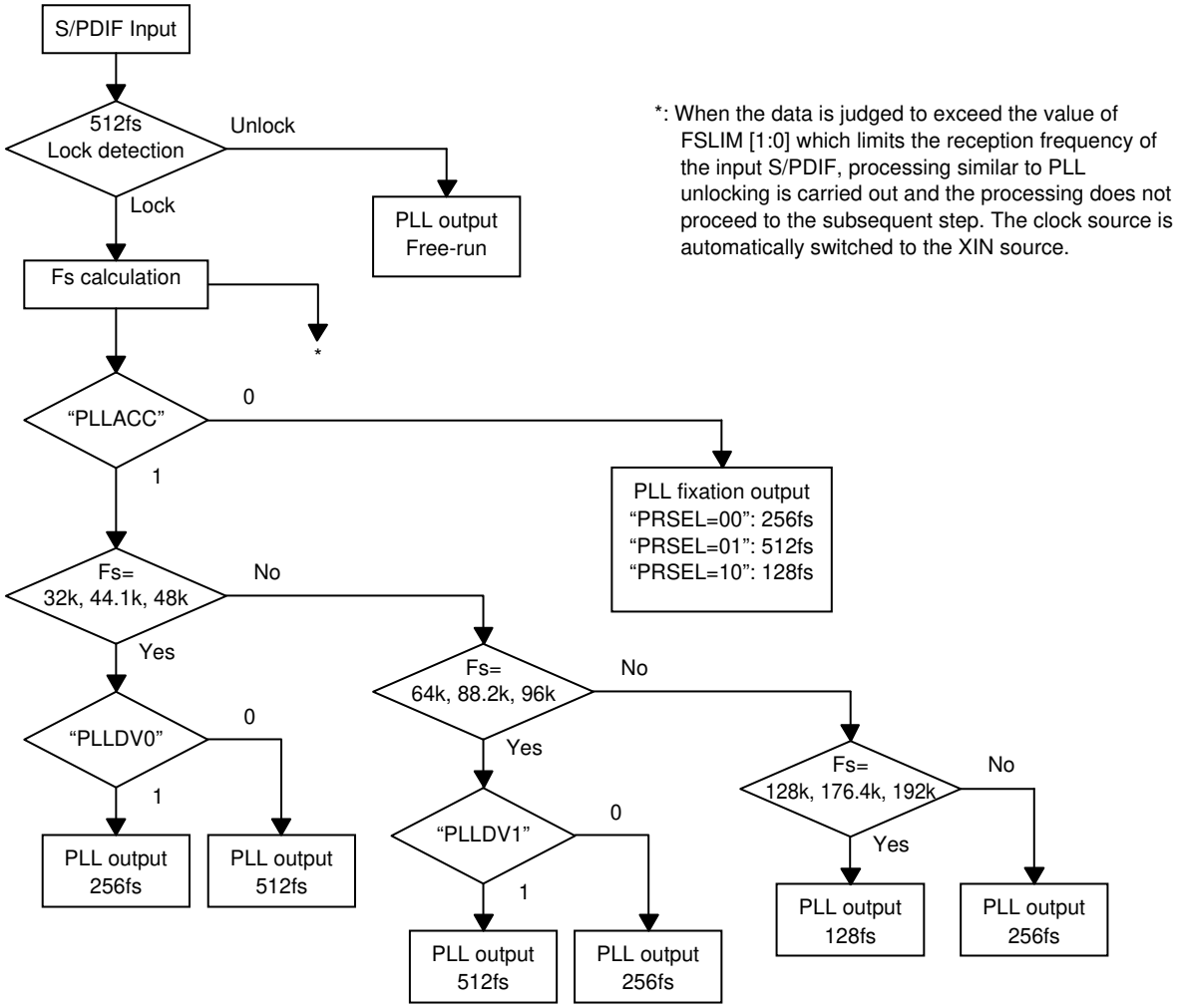


Figure 10.3 PLL Clock Output Control

Table 10.2: PLL Clock Output Frequencies (Bold settings are recommended values.)

S/PDIF fs	PLL Output						
	PLLACC=0 (Fixed multiple outputs of input fs)			PLLACC=1 (Fixed multiple outputs for each input fs band)			
	PRSEL=00 (256fs)	PRSEL=01 (512fs)	PRSEL=10 (128fs)	**PLLDV0=0 PLLDV1=0**	PLLDV0=1 PLLDV1=0	PLLDV0=0 PLLDV1=1	PLLDV0=1 PLLDV1=1
32kHz	8.19MHz	16.38MHz	4.09MHz	**16.38MHz**	8.19MHz	16.38MHz	8.19MHz
44.1kHz	11.28MHz	22.57MHz	5.64MHz	**22.57MHz**	11.28MHz	22.57MHz	11.28MHz
48kHz	12.28MHz	24.57MHz	6.14MHz	**24.57MHz**	12.28MHz	24.57MHz	12.28MHz
64kHz	16.38MHz	32.76MHz	8.19MHz	**16.38MHz**	16.38MHz	32.76MHz	32.76MHz
88.2kHz	22.57MHz	45.15MHz	11.28MHz	**22.57MHz**	22.57MHz	45.15MHz	45.15MHz
96kHz	24.57MHz	49.15MHz	12.28MHz	**24.57MHz**	24.57MHz	49.15MHz	49.15MHz
128kHz	32.76MHz	65.53MHz	16.38MHz	**16.38MHz**	16.38MHz	16.38MHz	16.38MHz
176.4kHz	45.15MHz	90.31MHz	22.57MHz	**22.57MHz**	22.57MHz	22.57MHz	22.57MHz
192kHz	49.15MHz	98.30MHz	24.57MHz	**24.57MHz**	24.57MHz	24.57MHz	24.57MHz

- If 128kHz, 176.4kHz or 192kHz input is received when the PLLACC is set to 0 and the PRSEL [1:0] to 01, the DC characteristics of output directly sent to the RMCK pin cannot be guaranteed. In such a case, set the frequency to one half or quarter of the PLL clock frequency (PRSEL [1:0]=00 or 10).

10.1.7 Output clocks (RMCK, RBCK, RLRCK, SBCK, SLRCK)

- The LC89058W-E features two clock systems (R and S systems) in order to supply the various needed clocks to peripheral devices such as A/D converter and DSP.
- The clock output settings for the R and S systems are done with PLLACC, PLLDV1, PLLVD2, PRSEL[1:0], XRSEL[1:0], XRBCK[1:0], XRLRCK[1:0], PSBCK[1:0], PSLRCK[1:0], XSBCK[1:0], and XSLRCK[1:0].
- Setting range for each clock output pin when the PLL is used as source
  (1) RMCK: Selection from 1/1, 1/2, and 1/4 of PLLACC, PLLDV0, PLLDV1, or 512fs
  (2) RBCK: 64fs output
  (3) RLRCK: fs output
  (4) SBCK: Selection from 128fs, 64fs, 32fs, and 16fs
  (5)SLRCK: Selection from 2fs, fs, 1/2fs, and 1/4fs
- Setting range for each clock output pins when the XIN is used as source
  (1) RMCK: Selection from 1/1, 1/2, and 1/4 of 12.288MHz or 24.576MHz
  (2) RBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  (3) SBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  (4) RLRCK: Selection from 192kHz, 96kHz, and 48kHz
  (5) SLRCK: Selection from 192kHz, 96kHz, and 48kHz
- The polarity of RMCK can be reversed with RMCKP.
- The polarity of RBCK, RLRCK, SBCK, and SLRCK can be reversed with RBCKP, RLRCKP, SBCKP, and SLRCKP.

Table 10.3 List of Output Clock Frequencies (Bold Items = Initial Settings)

Output Pin Name	PLL Source (Internal VCO CK)	XIN Source (XIN input CK)	
	512fs	12.288MHz	24.576MHz
RMCK	512fs **256fs** 128fs	**12.288MHz** 6.144MHz	24.576MHz 12.288MHz 6.144MHz
RBCK	**64fs**	12.288MHz (RMCK=24.576MHz) 6.144MHz (RMCK≥12.288MHz) **3.072MHz** (RMCK≥6.144MHz)	
RLRCK	**fs**	192kHz 96kHz **48kHz**	
SBCK	128fs **64fs** 32fs 16fs	12.288MHz (RMCK=24.576MHz) 6.144MHz (RMCK≥12.288MHz) **3.072MHz** (RMCK≥6.144MHz)	
SLRCK	2fs **fs** fs/2 fs/4	192kHz 96kHz **48kHz**	

Notes:

- RBCK and SBCK output clock must not quicken more than RMCK output clock frequency. Also, RBCK and SBCK output clock are set to become 1/2 or less of RMCK output clock at XIN source. If it doesn't follow these conditions, RBCK and SBCK clocks are not output.

10.1.8 Output clocks block diagram (RMCK, RBCK, RLRCK, SBCK, SLRCK, XMCK)

- The relationships between the output clock and switch function are shown below.
- PLL in the figure indicates the PLL source and XIN the XIN source.
- The contents in the quotation marks "***" by the switch function blocks correspond to the write command names.
- The broken lines connecting the switches indicate coordinated switching.
- Lock/Unlock is switched automatically by PLL locking/unlocking.

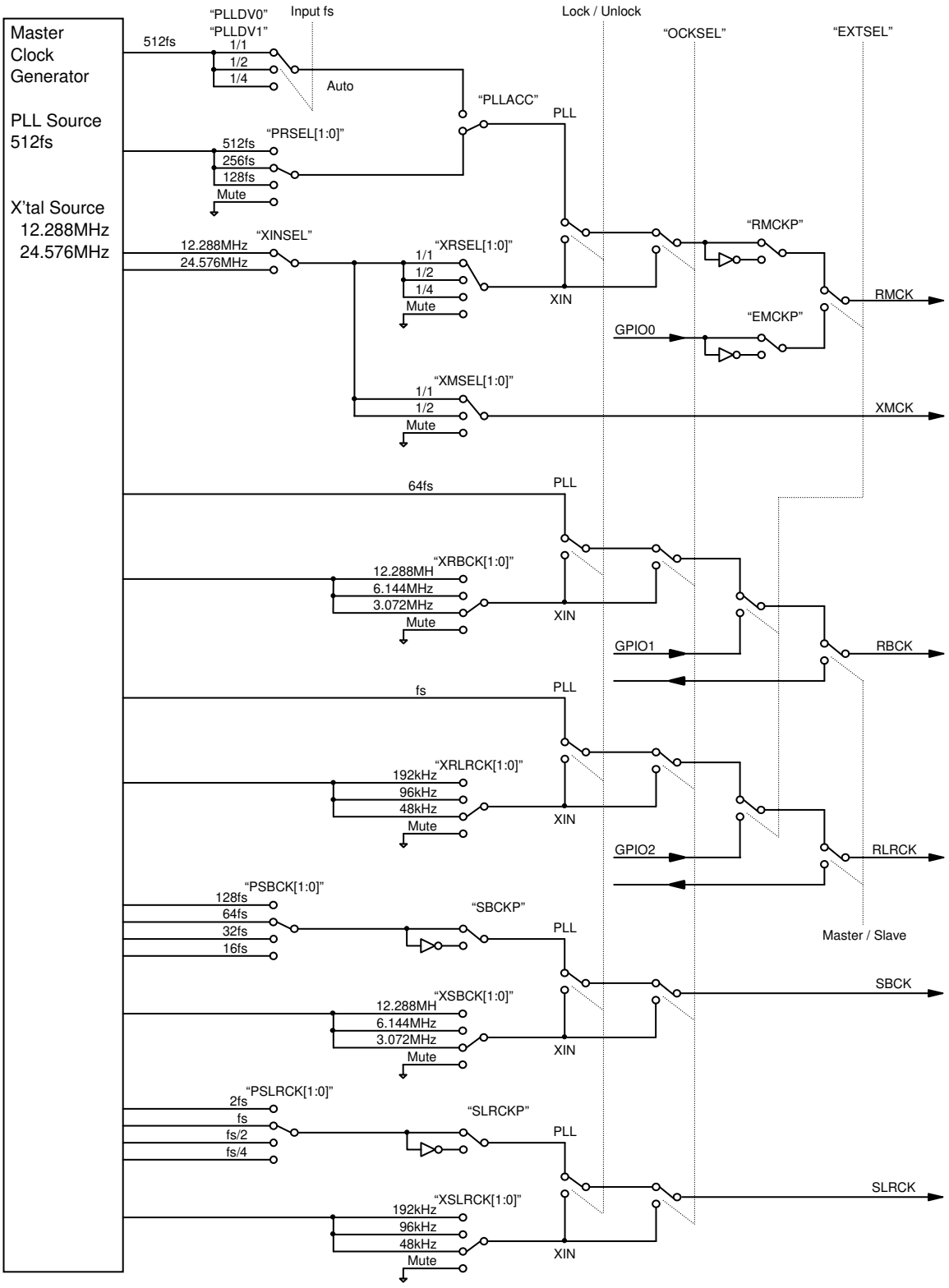
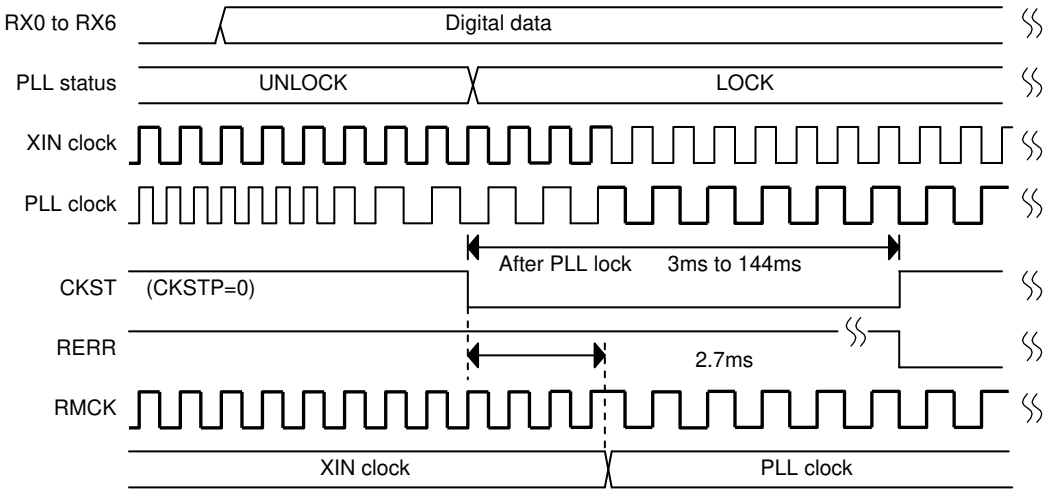


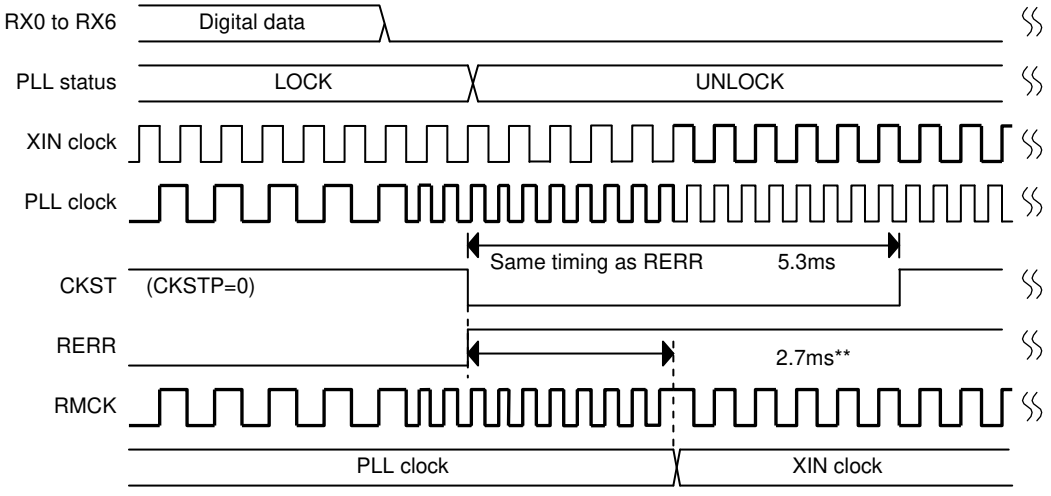
Figure 10.4 Clock Output Block Diagram

10.1.9 Output of clock switch transition signal (CKST)

- CKST outputs pulse when the output clock changes by PLL lock/unlock.
- The polarity of the CKST pulse output can be reversed with CKSTP. Subsequently, CKSTP is assumed to be 0.
- In the lock-in stage, the CKST falls at the word clock generated from the XIN clock after PLL is locked following detection of input data, and rises at the same timing as RERR after a designated period.
- In the unlock stage, the CKST falls at the same timing as RERR, PLL lock detection signal, and rises after word clocks generated from the XIN clock are counted for a designated period.
- Change of the PLL lock status and timing of the clock change can be seen by detecting the rising and falling edges and pulses of CKST.
- The clock is switched after the PLL lock condition is tested and identified. The timing of this clock switching is determined by setting the PTOXW [1:0]. The initial value is such that the clock is switched in 2.7ms after the falling edge of CKST. The value, however, assumes that the oscillation amplifier is set to permanent operation mode. If the oscillation amplifier is set to be stopped after PLL locking, the startup time before the oscillation amplifier stabilizes after PLL unlocking, is added.
- A free-running clock is output from the clock output pin immediately after PLL unlocking.



(a): Lock-in stage



**: When set to PTOXW[1:0]=00 (max.)

(b): Unlock stage

Figure 10.5 Clock Switch Timing