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LC89075WA

ON Semiconductor®

http://onsemi.com

CMOS LSI
Digital Audio Interface Receiver
with Stereo ADC and Audio Selector

1. Overview

The LC89075WA is a digital audio interface receiver that demodulates signals according to the data transfer format between digital audio devices via IEC60958/61937 and JEITA CPR-1205 and supports demodulation sampling frequencies of up to 192kHz.

The LC89075WA also incorporates a high performance 24-bit single-end input ΔΣ stereo analog to digital converter that supports sampling frequencies of up to 96kHz, and an audio selector that can support 8-channel data.

The LC89075WA is a complete analog and digital front-end for use in various systems including AV receivers, digital TVs, and DVD recorders.

2. Features

2.1 ADC

SQFP64(10X10)

- ΔΣ stereo ADC
- Built-in anti-aliasing digital filter
- Single-end input (3Vp-p)
- Built-in digital HPF for canceling DC offset
- Built-in PGA (-4.5dB to 6dB/1.5dB step)
- Built-in soft mute and attenuator (0dB to -63.5dB/0.25dB step, -∞)
- Sampling frequency: 8kHz to 96kHz
- Master clock: 512fs, 256fs (master/slave)
- Audio data output interface: 24-bit I^{2}S/left justified
- Analog audio data detection (threshold level: -30dB to -60dB/adjustable in 2dB steps)
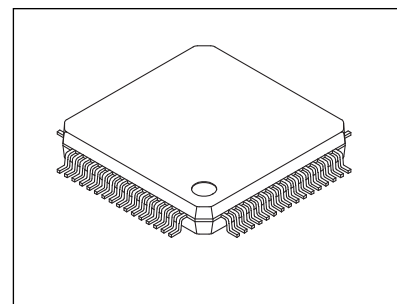
2.2 DIR

- S/PDIF demodulation process according to IEC60958/61937 and JEITA CPR-1205
- Reception frequency: 32kHz to 192kHz (PLL lock range)
- Built-in 15:3 digital data selector enables separate selection of data to be demodulated and data output to pins.
    - S/PDIF input: Up to 15 systems that support TTL (3 systems can support coaxial)
    - S/PDIF output: Possible to select two systems of pin outputs, and one system of demodulation data
- Possible to limit the acceptable sampling frequency and set the no-signal input status when the reception range is exceeded.
- Built-in a PLL low clock jitter and an oscillation amplifier.
- Outputs the monitor signal that is switched between PLL and crystal.
- Outputs master clock: 512fs, 256fs and 128fs (with automatic adjustment function)
- Audio data output interface: 24-bit I^{2}S/left justified
- Outputs DTS-CD detection flag.
- Outputs interrupt signal for microcontroller.
- Calculates input sampling frequency.
- Reads IEC61937 burst preamble PC data from microcontroller.
- Reads first 40 bits of channel status from microcontroller.
- Outputs bit 1 (non-PCM data delimiter bit) and main bits of channel status to the pin.

ORDERING INFORMATION
See detailed ordering and shipping information on page 70 of this data sheet.

2.3 Other

- Built-in audio selector supports up to 8-channel data.
  Selector configuration to support 2-ch data: 4-line input ×6 and 4-line output ×2
  Selector configuration to support 6-ch and 2-ch data: 6-line input ×1, 4-line input ×5 and 6-line output ×1
  Selector configuration to support 8-ch and 2-ch data: 7-line input ×1, 4-line input ×4 and 7-line output ×1
- Possible to take in external error flag, non-PCM flag, and mute flag
- PCM digital audio data detection (threshold level: -30dB to -60dB/adjustable in 2dB steps)
- SPI microcontroller interface (with automatic increment function)
- Built-in power-on reset circuit
- Input pin reverse bias control during power-off
- Supply voltages:
  ADC analog: 4.5 to 5.5V (3.0 to 3.6V possible when not using the ADC)
  PLL analog: 3.0 to 3.6V
  Digital: 3.0 to 3.6V
- Operation guarantee temperature: -30 to 85°C
- Package: SQFP64 (lead-free and halogen-free)

Package Dimensions
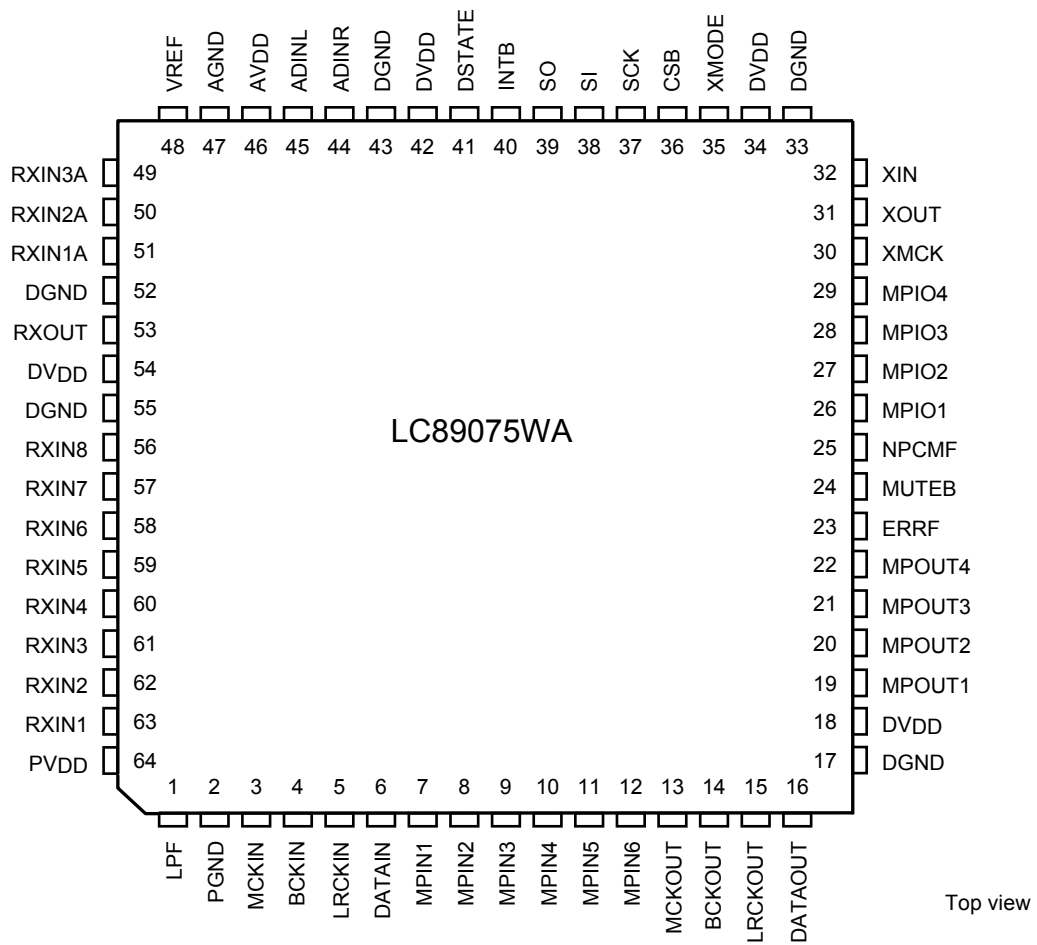
unit : mm (typ)

SQFP64(10X10)
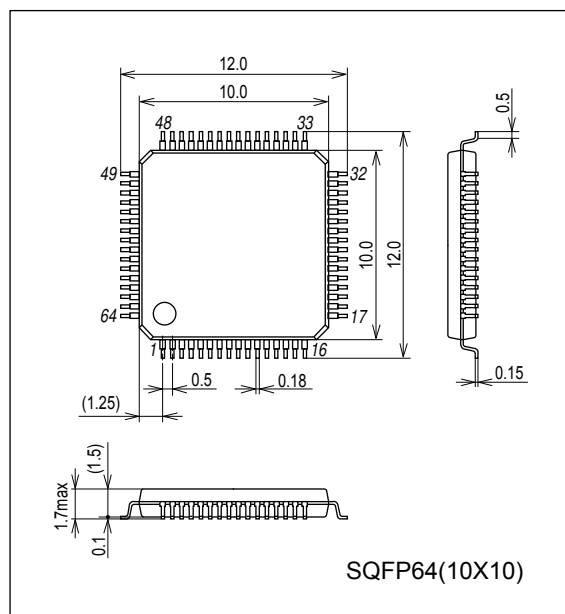
4. Pin Assignment

Figure 4.1 LC89075WA Pin Assignment

5. Pin Functions

Table 5.1 Pin Functions

No	Name	I/O	Function	
1	LPF	O	PLL: Loop filter connection pin	
2	PGND		PLL: Analog GND	
3	MCKIN	I	Group A : Master clock input pin	to [MCKOUT], [MPOUT1]
			Group A+B : Master clock input pin	to [MCKOUT]
4	BCKIN	I	Group A : Bit clock input pin	to [BCKOUT], [MPOUT2]
			Group A+B : Bit clock input pin	to [BCKOUT]
5	LRCKIN	I	Group A : LR clock input pin	to [LRCKOUT], [MPOUT3]
			Group A : DSD data input pin	to [LRCKOUT], [MPOUT3]
			Group A+B : LR clock input pin	to [LRCKOUT]
6	DATAIN	I	Group A : 2ch audio data input pin	to [DATAOUT], [MPOUT4]
			Group A : DSD data input pin	to [DATAOUT], [MPOUT4]
			Group A+B : 1, 2ch/8ch audio data input pin	to [DATAOUT]
7	MPIN1	I	Group B : Master clock input pin	to [MCKOUT], [MPOUT1]
			Group A+B : 3, 4ch/8ch audio data input pin	to [MPOUT1]
8	MPIN2	I	Group B : Bit clock input pin	to [BCKOUT], [MPOUT2]
			Group A+B : 5, 6ch/8ch audio data input pin	to [MPOUT2]
9	MPIN3	I	Group B : LR clock input pin	to [LRCKOUT], [MPOUT3]
			Group B : DSD data input pin	to [LRCKOUT], [MPOUT3]
			Group A+B : 7, 8ch/8ch audio data input pin	to [MPOUT3]
10	MPIN4	I	Group B : 2ch audio data input pin	to [DATAOUT], [MPOUT4]
			Group B : DSD data input pin	to [DATAOUT], [MPOUT4]
			Group B : 1, 2ch/6ch audio data input pin	to [DATAOUT]
			Group A+B : External error signal input pin	to [ERRF]
11	MPIN5	I	Group B : 3, 4ch/6ch audio data input pin	to [MPOUT1]
			Group A+B : External data mute signal input pin	to [MUTEB]
12	MPIN6	I	Group B : 5, 6ch/6ch audio data input pin	to [MPOUT2]
			Group A+B : External non-PCM signal input pin	to [NPCMF]
13	MCKOUT	O	Master clock output pin	from ADC, DIR, [MCKIN], [MPIN1], [MPIO1], [RXIN8]
14	BCKOUT	O	Bit clock output pin	from ADC, DIR, [BCKIN], [MPIN2], [MPIO2], [RXIN7]
15	LRCKOUT	O	LR clock output pin	from ADC, DIR, [LRCKIN], [MPIN3], [MPIO3], [RXIN6]
			DSD data output pin	from [LRCKIN], [MPIN3], [MPIO3], [RXIN6]
16	DATAOUT	O	2ch audio data output pin	from ADC, DIR, [DATAIN], [MPIN4], [MPIO4], [RXIN5]
			DSD data output pin	from [DATAIN], [MPIN4], [MPIO4], [RXIN5]
			1, 2ch/6ch audio data output pin	from [MPIN4]
			1, 2ch/8ch audio data output pin	from [DATAIN]
17	DGND		Digital GND	
18	DVDD		Digital power supply (3.3V)	
19	MPOUT1	O	Master clock output pin	from ADC, [MCKIN], [MPIN1], [MPIO1], [RXIN8]
			3, 4ch/6ch audio data output pin	from [MPIN5]
			3, 4ch/8ch audio data output pin	from [MPIN1]
20	MPOUT2	O	Bit clock output pin	from ADC, [BCKIN], [MPIN2], [MPIO2], [RXIN7]
			5, 6ch/6ch audio data output pin	from [MPIN6]
			5, 6ch/8ch audio data output pin	from [MPIN2]
21	MPOUT3	O	LR clock output pin	from ADC, [LRCKIN], [MPIN3], [MPIO3], [RXIN6]
			DSD data output pin	from [LRCKIN], [MPIN3], [MPIO3], [RXIN6]
			7, 8ch/8ch audio data output pin	from [MPIN3]

Continued from preceding page.

No	Name	I/O	Function	
22	MPOUT4	O	2ch audio data output pin	from ADC, [DATAIN], [MPIN4], [MPIO4], [RXIN5]
			DSD data output pin	from [DATAIN], [MPIN4], [MPIO4], [RXIN5]
			Input S/PDIF through output pin	
23	ERRF	O	PLL lock error, data error flag output pin	
			External error signal output pin	from [MPIN4]
24	MUTEB	O	Clock switching period data mute signal output pin	
			External data mute signal output pin	from [MPIN5]
25	NPCMF	O	Channel status data delimiter bit (bit 1) output pin	
			External non-PCM signal output pin	from [MPIN6]
26	MPIO1	O	Channel status data delimiter bit (bit 1) output pin	
			Microcontroller extended register output pin	
		I	Master clock input pin (ADC slave operation)	to ADC, [MPOUT1]
			Group C : Master clock input pin	to [MCKOUT], [MPOUT1]
			3.3V tolerance TTL-compatible S/PDIF input pin	
27	MPIO2	O	Channel status copy bit output pin	
			Microcontroller extended register output pin	
		I	Bit clock input pin (ADC slave operation)	to ADC, [MPOUT2]
			Group C : Bit clock input pin	to [BCKOUT], [MPOUT2]
			3.3V tolerance TTL-compatible S/PDIF input pin	
28	MPIO3	O	Channel status emphasis information output pin	
			Microcontroller extended register output pin	
		I	LR clock input pin (ADC slave operation)	to ADC
			Group C : LR clock input pin	to [LRCKOUT], [MPOUT3]
			Group C : DSD data input pin	to [LRCKOUT], [MPOUT3]
			3.3V tolerance TTL-compatible S/PDIF input pin	
29	MPIO4	O	Channel status age bit output pin	
			Microcontroller extended register output pin	
			2ch audio data output pin (ADC slave operation)	from ADC
		I	Group C : 2ch audio data input pin	to [DATAOUT], [MPOUT4]
			Group C : DSD data input pin	to [DATAOUT], [MPOUT4]
			3.3V tolerance TTL-compatible S/PDIF input pin	
30	XMCK	O	Oscillation amplifier clock output pin	
31	XOUT	O	Crystal resonator connection output pin	
32	XIN	I	Crystal resonator connection or external clock input pin	
			(12.288MHz or 24.576MHz)	
33	DGND		Digital GND	
34	DV_{DD}		Digital power supply (3.3V)	
35	XMODE	I	System reset input pin	
			(when power-on reset is used: fixed at "H")	
36	CSB	I	SPI microcontroller I/F, chip enable input pin	
37	SCK	I	SPI microcontroller I/F, shift clock input pin	
38	SI	I	SPI microcontroller I/F, write data input pin	
39	SO	O	SPI microcontroller I/F, read data output pin	
40	INTB	O	SPI microcontroller I/F, interrupt signal output pin	
41	DSTATE	O	Analog or digital data detection flag output pin	
42	DV_{DD}		Digital power supply (3.3V)	
43	DGND		Digital GND	

Continued from preceding page.

No	Name	I/O	Function	
44	ADINR	I_5	ADC: Analog Rch data input pin	
45	ADINL	I_5	ADC: Analog Lch data input pin	
46	AV_{DD}		ADC: Analog power supply (5V)	
47	AGND		ADC: Analog GND	
48	VREF	O	ADC: Common voltage output pin	
49	RXIN3A	I	3.3V tolerance TTL-compatible S/PDIF input pin	
			Coaxial-compatible S/PDIF input pin	
50	RXIN2A	I	3.3V tolerance TTL-compatible S/PDIF input pin	
			Coaxial-compatible S/PDIF input pin	
51	RXIN1A	I	3.3V tolerance TTL-compatible S/PDIF input pin	
			Coaxial-compatible S/PDIF input pin	
52	DGND		Digital GND	
53	RXOUT	O	Input S/PDIF through output pin	
54	DV_{DD}		Digital power supply (3.3V)	
55	DGND		Digital GND	
56	RXIN8	I_5	5V tolerance TTL-compatible S/PDIF input pin	
			Group D : Master clock input pin	to [MCKOUT], [MPOUT1]
57	RXIN7	I_5	5V tolerance TTL-compatible S/PDIF input pin	
			Group D : Bit clock input pin	to [BCKOUT], [MPOUT2]
58	RXIN6	I_5	5V tolerance TTL input level S/PDIF input pin	
			Group D : LR clock input pin	to [LRCKOUT], [MPOUT3]
			Group D : DSD data input pin	to [LRCKOUT], [MPOUT3]
59	RXIN5	I_5	5V tolerance TTL-compatible S/PDIF input pin	
			Group D : 2ch audio data input pin	to [DATAOUT], [MPOUT4]
			Group D : DSD data input pin	to [DATAOUT], [MPOUT4]
60	RXIN4	I_5	5V tolerance TTL-compatible S/PDIF input pin	
61	RXIN3	I_5	5V tolerance TTL-compatible S/PDIF input pin	
62	RXIN2	I_5	5V tolerance TTL-compatible S/PDIF input pin	
63	RXIN1	I_5	5V tolerance TTL-compatible S/PDIF input pin	
64	PV_{DD}		PLL: Analog power supply (3.3V)	

* Input tolerance: I = -0.3 to 3.6V, I_5 = -0.3 to 5.5V, Output tolerance: O = -0.3 to 3.6V

* Pin 35: it has a built-in power-on reset circuit.

* Pin 32: power-off reverse bias control is supported only when a resonator is connected.

* Pins 26, 27, 28 and 29: power-off reverse bias control are supported only when "L" level input during power-off.

* Pin 46: 3.3V can be supplied when not using the ADC. In this case, making the power-down setting is recommended.

* Each AV_{DD}, PV_{DD} and DV_{DD} power supply must be turned on and off at the same timing to prevent latch-up.
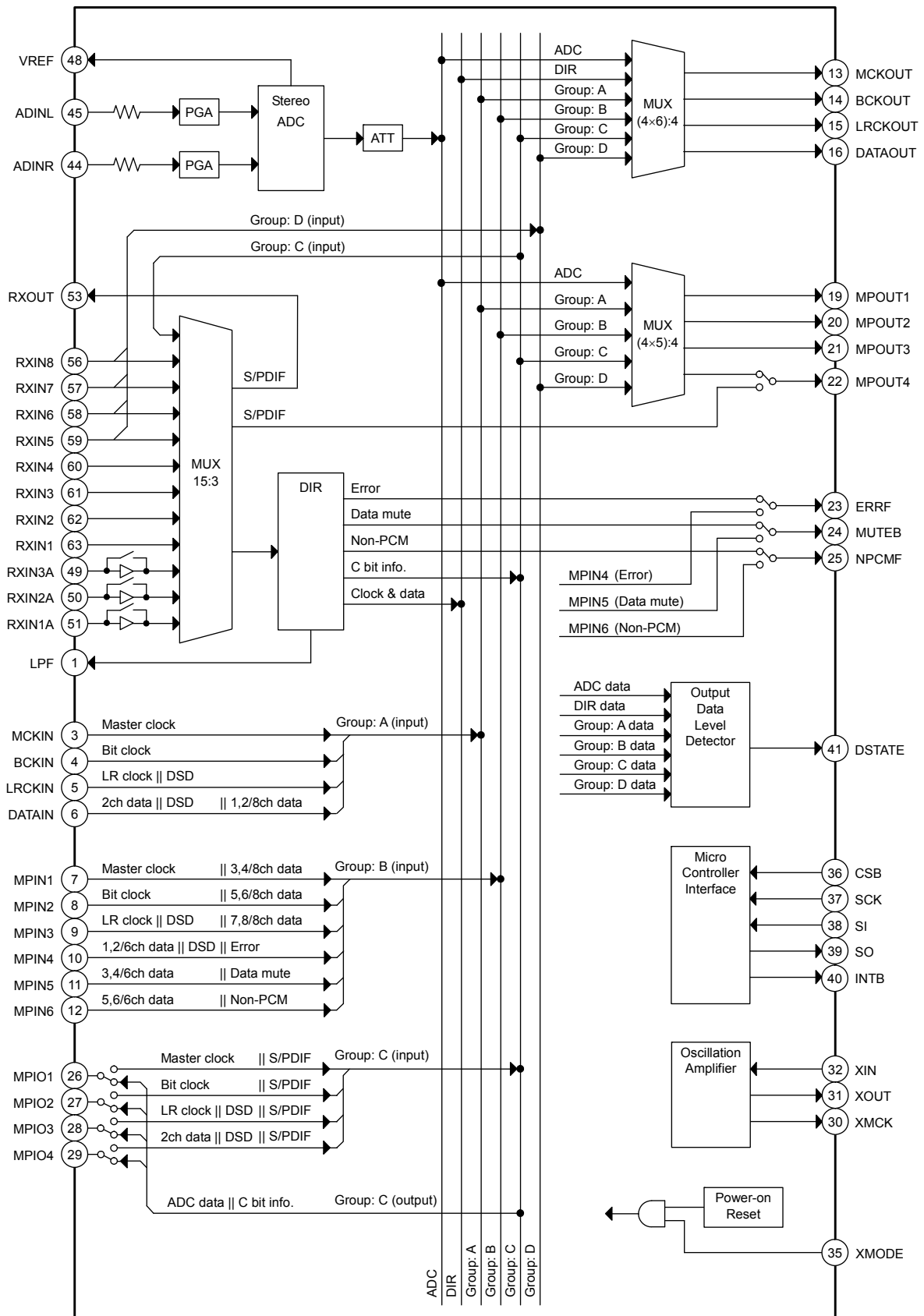
6. Block Diagram

Figure 6.1 LC89075WA Block Diagram

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings at AGND=PGND=DGND=0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	AV_{DD} max	7.1.1	-0.3 to 6.0	V
Maximum supply voltage	DV_{DD} max	7.1.2	-0.3 to 4.6	V
Input voltage 1	$V_{IN}1$	7.1.3	-0.3 to AV_{DD} max+0.3 (max.6.0Vp-p)	V
Input voltage 2	$V_{IN}2$	7.1.4	-0.3 to DV_{DD} max+0.3 (max.4.6Vp-p)	V
Output voltage	V_{OUT}	7.1.5	-0.3 to DV_{DD} max+0.3 (max.4.6Vp-p)	V
Storage ambient temperature	Tstg		-55 to 125	°C
Operating ambient temperature	Topr		-30 to 85	°C
Allowable power dissipation	Pd max	7.1.6	559	mW
Maximum input/output current	I_{IN}, I_{OUT}	7.1.7	±20	mA

7.1.1: AV_{DD} pin

7.1.2: PV_{DD} and DV_{DD} pins

7.1.3: ADINL, ADINR, RXIN1, RXIN2, RXIN3, RXIN4, RXIN5, RXIN6, RXIN7, and RXIN8 pins

7.1.4: MCKIN, BCKIN, LRCKIN, DATAIN, MPIN1, MPIN2, MPIN3, MPIN4, MPIN5, and MPIN6 pins
XIN, MPIO1, MPIO2, MPIO3, MPIO4, XMODE, CSB, SCK, SI, RXIN1A, RXIN2A, and RXIN3A pins

7.1.5: MCKOUT, BCKOUT, LRCKOUT, DATAOUT, MPOUT1, MPOUT2, MPOUT3, MPOUT4, and ERRF pins
MUTEB, NPCMF, XMCK, XOUT, MPIO1, MPIO2, MPIO3, MPIO4, SO, INTB, DSTATE, and RXOUT pins

7.1.6: Ta ≤ 85°C

7.1.7: Per input/output pin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

7.2 Allowable Operating Range

Table 7.2 Recommended Operating Conditions at AGND=PGND=DGND=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage 1	$AV_{DD}1$	7.2.1	4.5	5.0	5.5	V
Supply voltage 2	$AV_{DD}2$	7.2.2	3.0	3.3	3.6	V
Supply voltage 3	DV_{DD}	7.2.3	3.0	3.3	3.6	V
Input voltage range 1	$V_{IN}1$	7.2.4	0		5.5	V
Input voltage range 2	$V_{IN}2$	7.2.5	0		3.6	V
Output load capacitance 1	C_L1	7.2.6			20	pF
Output load capacitance 2	C_L2	7.2.7			30	pF
Operating temperature	Vopr		-30	25	85	°C

7.2.1: AV_{DD} pin (when ADC is used)

7.2.2: AV_{DD} pin (ADC must be set to power-down mode at all times. "ADCOPR[1:0]=11")

7.2.3: PV_{DD} and DV_{DD} pins
On/off of AV_{DD}, PV_{DD}, and DV_{DD} should desirably be done at the same timing. If that is not possible, PV_{DD} and DV_{DD} must be turned on earlier than AV_{DD}. AV_{DD} must also be turned off after PV_{DD} and DV_{DD}.

7.2.4: ADINL, ADINR, RXIN1, RXIN2, RXIN3, RXIN4, RXIN5, RXIN6, RXIN7, and RXIN8 pins

7.2.5: MCKIN, BCKIN, LRCKIN, DATAIN, MPIN1, MPIN2, MPIN3, MPIN4, MPIN5, and MPIN6 pins
XIN, MPIO1, MPIO2, MPIO3, MPIO4, XMODE, CSB, SCK, SI, RXIN1A, RXIN2A, and RXIN3A pins

7.2.6: MCKOUT pin

7.2.7: Output pins other than MCKOUT

7.3 Analog to Digital Converter Characteristics

Table 7.3 ADC Characteristics at Ta=25°C, AV$_{DD}$=5.0V, PV$_{DD}$=DV$_{DD}$=3.3V, AGND=PGND=DGND=0V
fs=48k: 96kHz, input=1kHz: 24-bit data, measurement=20Hz to 20kHz

Parameter	Conditions	min	typ	max	Unit
Resolution				24	bits
Sampling frequency	7.3.1	8	48	96	kHz
System clock frequency		2.048	12.288	24.576	MHz
Input voltage	7.3.2		3.0		Vp-p
PGA range	7.3.3	-4.5	0	6	dB
PGA step	7.3.3		1.5		dB
THD+N	7.3.4 (48kHz)		-92	-80	dB
	7.3.5 (96kHz)		-88		dB
S/N	7.3.6 (48kHz)	94	101		dB
	7.3.7 (96kHz)		103		dB
Dynamic range	7.3.8 (48kHz)	94	101		dB
	7.3.9 (96kHz)		103		dB
Input impedance			27		kΩ
Channel-to-channel crosstalk		90	100		dB
Channel gain error			0.2	0.5	dB
Pass band				0.45fs	Hz
Stop band		0.545fs			Hz
Pass band ripple				±0.041	dB
Stop band attenuation		-58.5			dB
Group delay	7.3.10		24.5		1/fs
HPF frequency response	7.3.11		0.0385fs/1000		

7.3.1: Sampling frequency is 6kHz when "ADCOPR[1:0]=10" and "SDMODE=1".

7.3.2: Proportional to AV$_{DD}$ voltage with a full scale value (0dB) of analog input voltage (V$_{IN}$=0.6×AV$_{DD}$)

7.3.3: -4.5dB to 6dB/1.5dB steps

7.3.4: fs=48kHz, -1dBFS, except when "ADCOPR[1:0]=10"

7.3.5: fs=96kHz, -1dBFS, except when "ADCOPR[1:0]=10"

7.3.6: fs=48kHz, A-weighted, except when "ADCOPR[1:0]=10"

7.3.7: fs=96kHz, A-weighted, except when "ADCOPR[1:0]=10"

7.3.8: fs=48kHz, -60dBFS, A-weighted

7.3.9: fs=96kHz, -60dBFS, A-weighted

7.3.10: Delay calculation for the digital filter

7.3.11: -3dB

LC89075WA

7.4 DC Characteristics

Table 7.4 DC Characteristics at Ta=-30 to 85°C,
AV_{DD}=4.5 to 5.5V, PV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=PGND=DGND=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input, High	V_{IH}	7.4.1	0.7 DV_{DD}			V
Input, Low	V_{IL}				0.2 DV_{DD}	V
Input, High	V_{IH}	7.4.2	2.0			V
Input, Low	V_{IL}				0.8	V
Output, High	V_{OH}	7.4.3	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Input amplitude	V_{P-P}	7.4.4	200			mV
Input impedance	Z_{in}	7.4.4	40		65	kΩ

7.4.1: CMOS-compatible: XIN input pin

7.4.2: TTL-compatible: Input pins other than XIN, ADINL, and ADINR pins

7.4.3: I_{OH}=-6mA, I_{OL}=6mA: MCKOUT, and MPOUT1 output pins
   I_{OH}=-4mA, I_{OL}=4mA: BCKOUT, LRCKOUT, DATAOUT, MPOUT[4:2], XMCK, and RXOUT output pins
   I_{OH}=-2mA, I_{OL}=2mA: ERRF, MUTEB, NPCMF, MPIO[4:1], SO, INTB, and DSTATE output pins

7.4.4: Before capacitance of RXIN1A, RXIN2A, and RXIN3A pins (when coaxial input is set to RXIN1A, RXIN2A, and RXIN3A)

7.5 Supply Current Characteristics

Table 7.5 DC Characteristics at Ta=25°C,
AV_{DD}=5V, PV_{DD}=DV_{DD}=3.3V, AGND=PGND=DGND=0V, Minimum load on output pins

Parameter	Symbol	Conditions	min	typ	max	Unit
AV_{DD} Supply Current	I_{ADD}	7.5.1		0.1	4	μA
PV_{DD}, DV_{DD} Supply Current	I_{DDD}			7	10	mA
AV_{DD} Supply Current	I_{ADD}	7.5.2		28	36	mA
PV_{DD}, DV_{DD} Supply Current	I_{DDD}			15	20	mA
AV_{DD} Supply Current	I_{ADD}	7.5.3		28	36	mA
PV_{DD}, DV_{DD} Supply Current	I_{DDD}			22	29	mA
AV_{DD} Supply Current	I_{ADD}	7.5.4		28	36	mA
PV_{DD}, DV_{DD} Supply Current	I_{DDD}			31	40	mA
AV_{DD} Supply Current	I_{ADD}	7.5.5		3	4	mA
PV_{DD}, DV_{DD} Supply Current	I_{DDD}			6	8	mA
AV_{DD} Supply Current	I_{ADD}	7.5.6		3	4	mA
PV_{DD}, DV_{DD} Supply Current	I_{DDD}			7	9	mA

7.5.1: XMODE=L, XIN=12.288MHz

7.5.2: XIN=24.576MHz, MCKOUT=512fs, fs=44.1kHz/DIR, ADC=Reset status

7.5.3: XIN=24.576MHz, MCKOUT=256fs, fs=96kHz/DIR, fs=48kHz/ADC, ADINL=ADINR=1kHz/Sine,
   "SW2SEL[2:0]=001", "SW1SEL[2:0]=000", "RXDSEL[3:0]=0000"

7.5.4: XIN=24.576MHz, MCKOUT=128fs, fs=192kHz/DIR, fs=96kHz/ADC, ADINL=ADINR=1kHz/Sine,
   "SW2SEL[2:0]=001", "SW1SEL[2:0]=000", "RXDSEL[3:0]=0000"

7.5.5: Analog audio data detection setting standby current,
   "ADCOPR[1:0]=10", "SDMODE=1", XIN=24.576MHz, fs=6kHz/ADC, when Figure 9.6 setting
   ADINL=ADINR=No signal

7.5.6: Analog and digital audio data detection setting standby current,
   "ADCOPR[1:0]=10", "SDMODE=1", "DSTASEL=1", XIN=24.576MHz, fs=6kHz/ADC,
   when Figure 9.6 setting, however "DIROPR=0", "RXDSEL[3:0]=0000"
   ADINL=ADINR=No signal, S/PDIF dose not input

7.6 AC Characteristics 1

Table 7.6 AC Characteristics at Ta=-30 to 85°C,
AV$_{DD}$=4.5 to 5.5V, PV$_{DD}$=DV$_{DD}$=3.0 to 3.6V, AGND=PGND=DGND=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
RXIN1 to 8, RXIN1A to 3A MPIO[4:1] input receive frequency	f$_{RFS}$		28		195	kHz
RXIN1 to 8, RXIN1A to 3A MPIO[4:1] input duty factor	t$_{RXDUY}$		40	50	60	%
XIN clock input frequency	f$_{XF}$	7.6.1		12.288		MHz
		7.6.2		24.576		MHz
XIN clock input duty factor	f$_{XDUY}$		40	50	60	%
MCKOUT clock output frequency	f$_{MCK1}$		4		50	MHz
MCKOUT clock output duty factor	f$_{MCKDUY}$		40	50	60	%
MCKOUT clock jitter	T$_j$	7.6.3		50		ps RMS
MPOUT1 clock output frequency	f$_{MCK2}$		2		25	MHz
BCKOUT, MPOUT2 clock output frequency	f$_{BCK4}$		0.5		12.5	MHz
LRCKOUT, MPOUT3 clock output frequency	f$_{LRCK4}$		8		192	kHz
MCKOUT-BCKOUT output delay	t$_{MBO}$		-10		10	ns
BCKOUT-LRCKOUT output delay	t$_{BLO}$	7.6.4	-10		10	ns
BCKOUT-DATAOUT output delay	t$_{BDO}$	7.6.4	-10		10	ns
BCKOUT-MPOUT[3:1](6ch, 8ch) output delay		7.6.5	-10		10	ns
LRCKOUT-DATAOUT output delay	t$_{LDO}$		-10		10	ns
LRCKOUT-MPOUT[3:1](6ch, 8ch) output delay		7.6.5	-10		10	ns

7.6.1: "XINSEL[1:0]=00"

7.6.2: Other than "XINSEL[1:0]=00"

7.6.3: Period jitter value

7.6.4: This also applies to the output when DSD data is input.

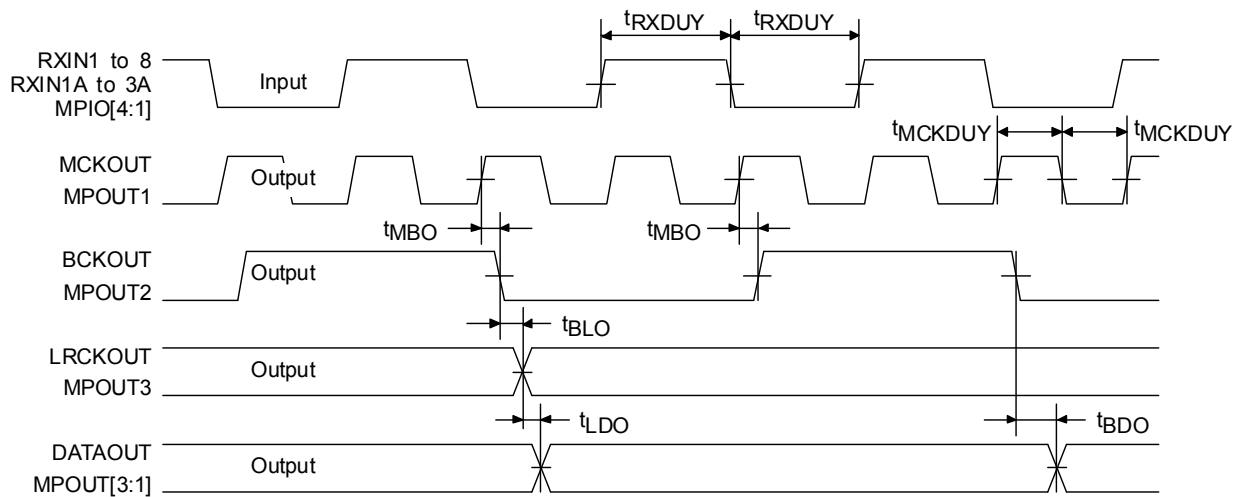7.6.5: "SW1SEL[1:0]=010 or 011", "SW2SEL[1:0]=110 or 111"

Figure 7.1 AC Characteristics 1

7.7 AC Characteristics 2

Table 7.7 AC Characteristics at Ta=-30 to 85°C,
AV_{DD}=4.5 to 5.5V, PV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=PGND=DGND=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Master clock input/output frequency	f_{MCKIN1}	7.7.1	2		25	MHz
Bit clock input/output frequency	f_{BCKIN}	7.7.2	0.5		12.5	MHz
LR clock input/output frequency	f_{LRCKIN}	7.7.3	8		195	kHz
Input delay	t_{IDLY}	7.7.4	0		40	ns
Setup/hold	t_{BDSH}	7.7.5	25			ns
Master clock input/output delay	t_{MMO}	7.7.6			25	ns
Bit clock input/output delay	t_{BBO}	7.7.7			25	ns
LR clock input/output delay	t_{LLO}	7.7.8			25	ns
Data input/output delay	t_{DDO}	7.7.9			25	ns

7.7.1: MCKIN, MPIN1, MPIO1, and RXIN8 input pins, MCKOUT and MPOUT1 output pins

7.7.2: BCKIN, MPIN2, MPIO2, and RXIN7 input pins, BCKOUT and MPOUT2 output pins

7.7.3: LRCKIN, MPIN3, MPIO3, and RXIN6 input pins, LRCKOUT and MPOUT3 output pins

7.7.4: MPIO2 to MPIO3 input pin-to-pin delay when in ADC slave operation

7.7.5: DATAIN, MPIN1, MPIN2, MPIN3, MPIN4, MPIN5, MPIN6, MPIO4, and RXIN5 input pins

7.7.6: MCKIN-MCKOUT, MPIN1-MCKOUT, MPIO1-MCKOUT, and RXIN8-MCKOUT I/O pin-to-pin delay
 MCKIN-MPOUT1, MPIN1-MPOUT1, MPIO1-MPOUT1, and RXIN8-MPOUT1 I/O pin-to-pin delay

7.7.7: BCKIN-BCKOUT, MPIN2-BCKOUT, MPIO2-BCKOUT, and RXIN7-BCKOUT I/O pin-to-pin delay
 BCKIN-MPOUT2, MPIN2-MPOUT2, MPIO2-MPOUT2, and RXIN7-MPOUT2 I/O pin-to-pin delay

7.7.8: LRCKIN-LRCKOUT, MPIN3-LRCKOUT, MPIO3-LRCKOUT, and RXIN6-LRCKOUT I/O pin-to-pin delay
 LRCKIN-MPOUT3, MPIN3-MPOUT3, MPIO3-MPOUT3, and RXIN6-MPOUT3 I/O pin-to-pin delay

7.7.9: DATAIN-DATAOUT, MPIN4-DATAOUT, MPIO4-DATAOUT, and RXIN5-DATAOUT I/O pin-to-pin delay
 DATAIN-MPOUT4, MPIN4-MPOUT4, MPIO4-MPOUT4, and RXIN5-MPOUT4 I/O pin-to-pin delay
 MPIN1-MPOUT1, MPIN2-MPOUT2, and MPIN3-MPOUT3 I/O pin-to-pin delay
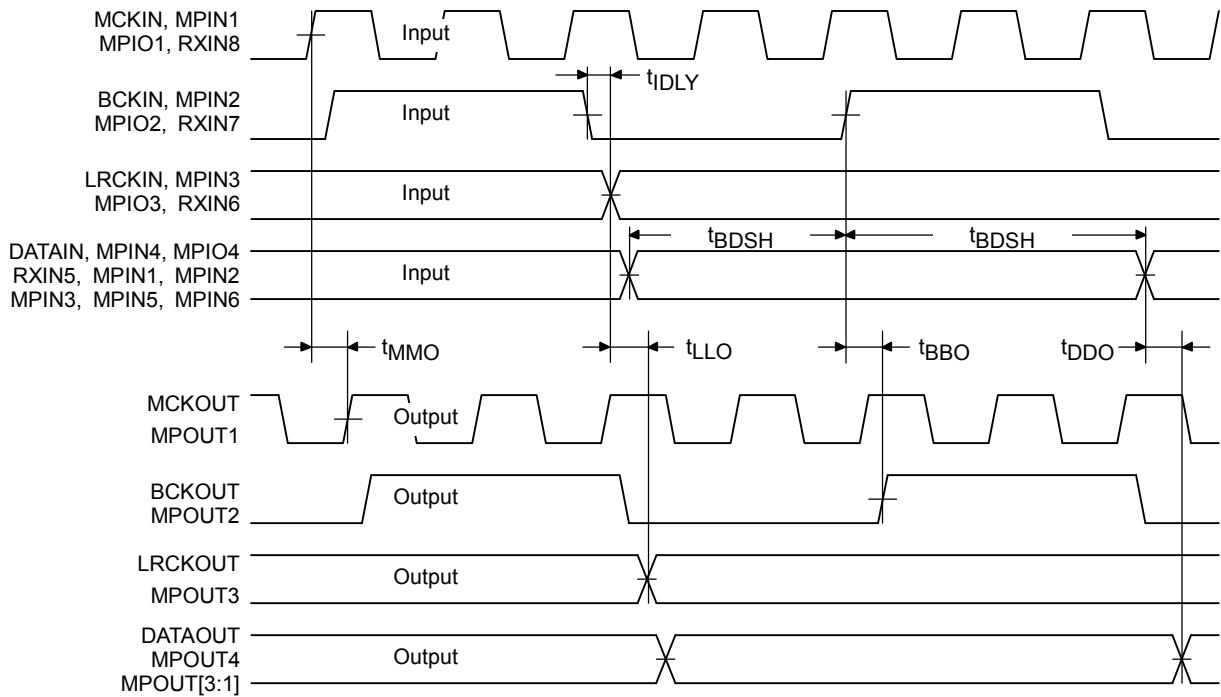 MPIN5-MPOUT1 and MPIN6-MPOUT2 I/O pin-to-pin delay

Figure 7.2 AC Characteristics 2

LC89075WA

7.8 SPI Microcontroller Interface AC Characteristics

Table 7.8 AC Characteristics at Ta=-30 to 85°C,
AV$_{DD}$=4.5 to 5.5V, PV$_{DD}$=DV$_{DD}$=3.0 to 3.6V, AGND=PGND=DGND=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Power-on reset DV$_{DD}$ slope	t$_{PORSL}$	7.8.1			100	ms
XMODE input pulse width (L)	t$_{RSTdw}$	7.8.2	200			μs
SCK input frequency	f$_{SCK}$				10	MHz
SCK input pulse width (L)	t$_{SCKdw}$		40			ns
SCK input pulse width (H)	t$_{SCKuw}$		40			ns
CSB input pulse width (H)	t$_{CSBuw}$		80			ns
CSB-SCK input delay	t$_{CSBtoSCK}$		20			ns
CSB-SCK hold	t$_{CSBhold}$		20			ns
SCK-SI setup	t$_{SIsetup}$		15			ns
SCK-SI hold	t$_{SIhold}$		15			ns
SCK-SO output delay	t$_{SCKtoSO}$				25	ns
CSB-SO output delay	t$_{CSBtoSO}$				20	ns

7.8.1: Each AV$_{DD}$, PV$_{DD}$ and DV$_{DD}$ power supply must be turned on and off at the same timing.

7.8.2: XMODE must be fixed to "H" before power is turned on in order to use the power-on reset function.
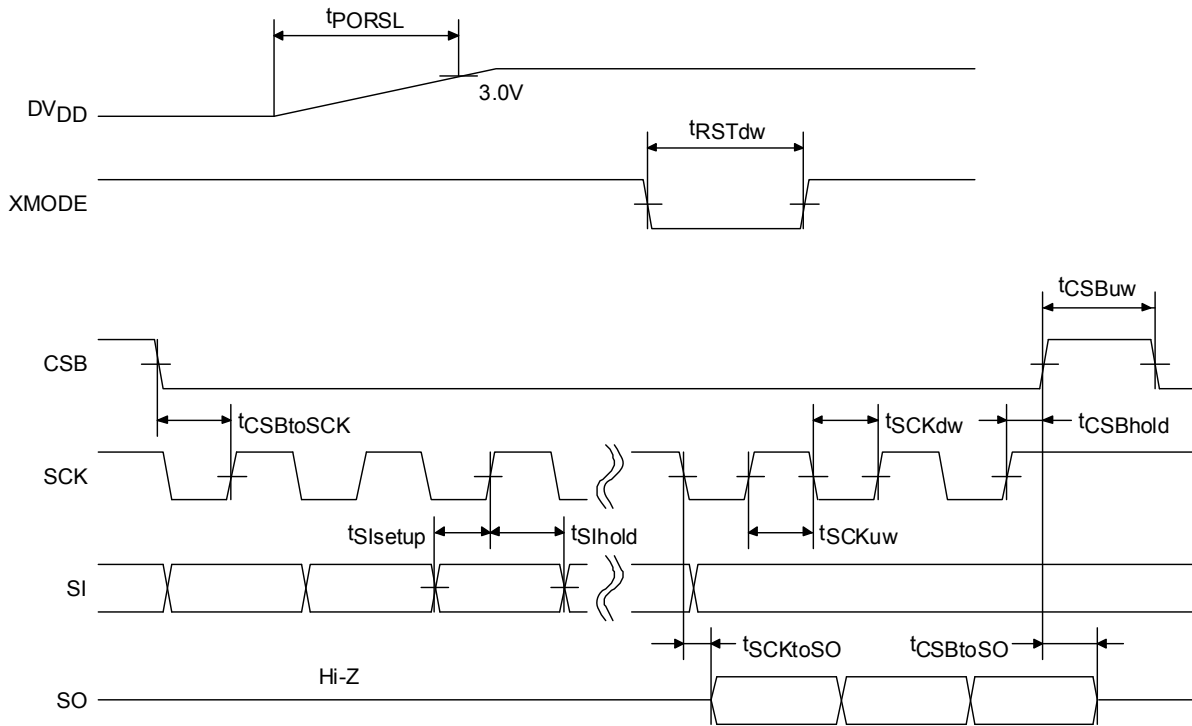
Figure 7.3 SPI Microcontroller Interface AC Characteristics

8. System Settings (Common to ADC, DIR, and Audio selector)

8.1 Oscillation Amplifier Pin Settings (XIN, XOUT, XMCK)

- The LC89075WA features a built-in oscillation amplifier. Connect a quartz resonator, feedback resistor, and load capacitance to XIN and XOUT to configure an oscillation circuit. The figure below shows the connection diagram. When connecting a quartz resonator, use one with a fundamental wave, and be aware that the load capacitance depends on the quartz resonator characteristics, so thorough investigation should be made.
- If the built-in oscillation amplifier is not used and an oscillation module is used as the clock source instead, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Always supply a 12.288MHz or 24.576MHz clock to XIN.
- The clock frequency is set with the XINSEL[1:0] register. The clock frequency set with the XINSEL[1:0] register and the clock frequency input to XIN must match.
- The clock set with the XINSEL[1:0] register is defined as the ADC operation clock and the MCKOUT, BCKOUT, and LRCKOUT output clocks when ADC data output is selected. Complete the XINSEL[1:0] register setting prior to bi-phase data input.
- XMCK outputs the XIN clock. The XMCK output is set with the XMSEL[1:0] register. 1/1, 1/2 or 1/4 of the XIN clock, or "L" output can be set.
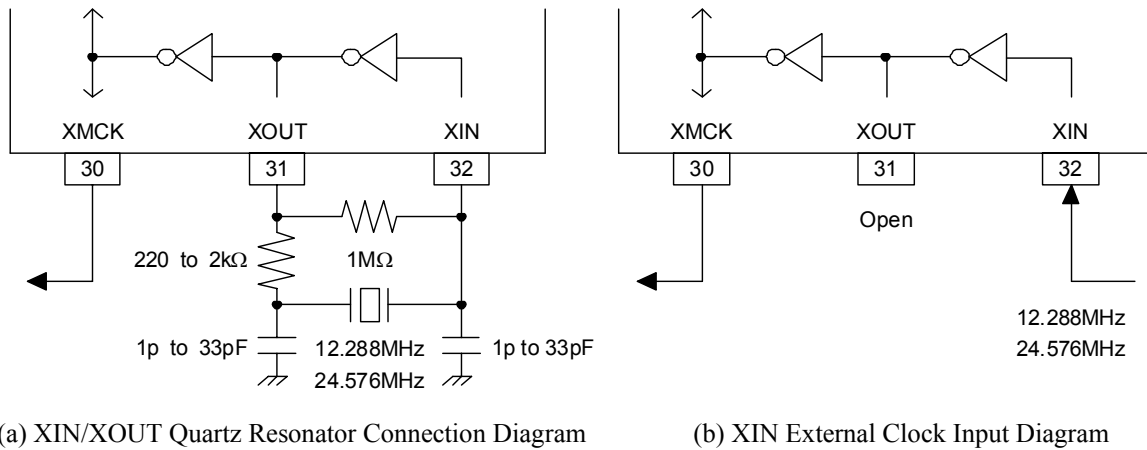
(a) XIN/XOUT Quartz Resonator Connection Diagram

(b) XIN External Clock Input Diagram

Figure 8.1 XIN/XOUT External Circuit Connection Diagram

8.2 ADC Common Voltage Output Pin Setting (VREF)

- VREF is used as the ADC analog signal common voltage and outputs the $1/2AV_{DD}$ voltage.
- Connect 10μF and 0.1μF capacitors between VREF and AGND, as close to the pins as possible. In addition, do not position clock or digital signal wiring close to these capacitors to avoid coupling to the converter.
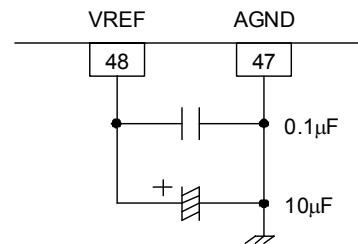
Figure 8.2 VREF External Circuit Connection Diagram

8.3 DIR Loop Filter Pin Setting (LPF)

- The DIR incorporates a VCO (Voltage Controlled Oscillator) that synchronizes with sampling frequencies from 32kHz to 192kHz and with the data with a transfer rate from 4MHz to 25MHz.
- The PLL is locked at 512fs.
- LPF is a pin for the PLL loop filter. Connect the resistor and capacitors shown in the right figure, as close to the pin as possible.
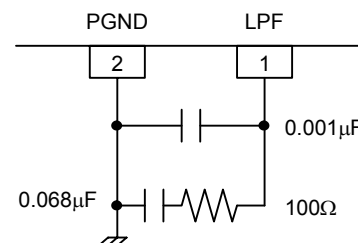
Figure 8.3 LPF External Circuit Connection Diagram

8.4 System Reset (XMODE)

- The LC89075WA features a built-in power-on reset circuit, and constantly monitors the power supply status.
- When XMODE is set to "H" and the power is turned on, the system is reset by this power-on reset circuit.
- When not using the power-on reset circuit, always set XMODE to "L" to reset the system during power-on. The system operates correctly when XMODE is set to "H" after the reset sequence. When XMODE is set to "L" again thereafter, the system is reset.
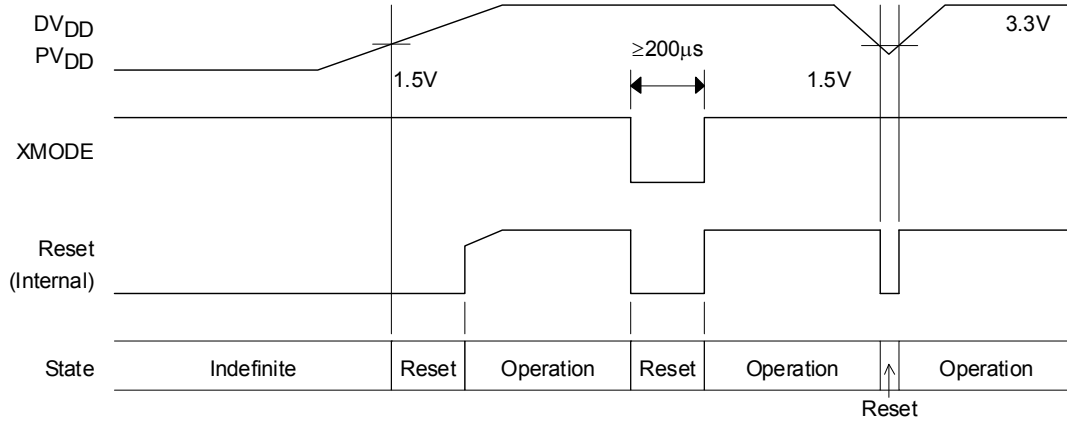
Figure 8.4 Power-on Reset and XMODE Reset Timing Chart

Table 8.1 Functional Block States When XMODE Is Reset (XMODE="L")

Functional Block	State
ADC	Stopped, power-down mode
DIR	Stopped, power-down mode (PLL stopped)
Oscillation amplifier	Running
Microcontroller registers	Initial Value

Table 8.2 Output Pin States When XMODE Is Reset (XMODE="L")

| Pin No.	Pin Name	Output State	Pin No.	Pin Name	Output State
13	MCKOUT	Output (XIN)	26	MPIO1	Hi-Z
14	BCKOUT	L	27	MPIO2	Hi-Z
15	LRCKOUT	L	28	MPIO3	Hi-Z
16	DATAOUT	L	29	MPIO4	Hi-Z
19	MPOUT1	L	30	XMCK	Output
20	MPOUT2	L	31	XOUT	Output
21	MPOUT3	L	39	SO	Hi-Z
22	MPOUT4	L	40	INTB	H
23	ERRF	H	41	DSTATE	L
24	MUTEB	L	53	RXOUT	L
25	NPCMF	L			

8.5 Output Data Format (Common to the ADC and DIR Blocks)

- The DATAOUT and MPOUT[4:1] output data format is set with the DAFORM register.
- The initial value of the output format is I^{2}S. Data is output synchronized with the BCKOUT falling edge.
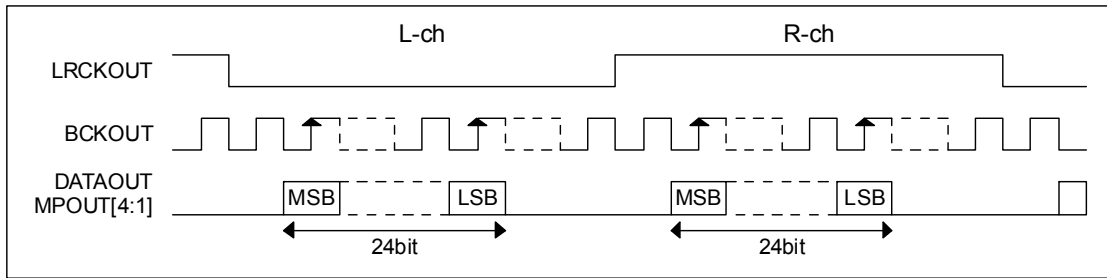
"DAFORM=0": I^{2}S Data Output

MPOUT[4:1]: Excluded when the clock output function is used
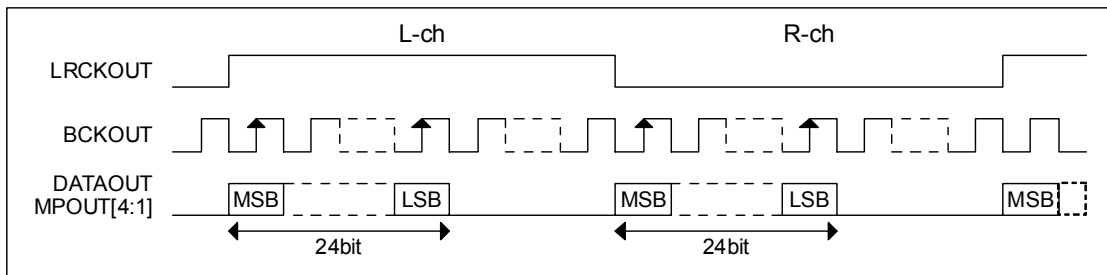
"DFORM=1": MSB First Left-Justified Output

Figure 8.5 ADC and DIR Data Output Timing Chart

8.6 Handling of Unused Pins

- Leave unused output pins open, and set unused input pins as shown in the table below.
- Always set input pins not noted in the table below as described in these specifications.

Table 8.3 Settings of Unused Input Pins

Pin No.	Pin Name	Input Setting	Pin No.	Pin Name	Input Setting
3	MCKIN	Connect to DGND (Pin No. 14)	44	ADINR	Open
4	BCKIN	Connect to DGND (Pin No. 14)	45	ADINL	Open
5	LRCKIN	Connect to DGND (Pin No. 14)	49	RXIN3A	Connect to DGND (Pin No. 52)
6	DATAIN	Connect to DGND (Pin No. 14)	50	RXIN2A	Connect to DGND (Pin No. 52)
7	MPIN1	Connect to DGND (Pin No. 14)	51	RXIN1A	Connect to DGND (Pin No. 52)
8	MPIN2	Connect to DGND (Pin No. 14)	56	RXIN8	Connect to DGND (Pin No. 55)
9	MPIN3	Connect to DGND (Pin No. 14)	57	RXIN7	Connect to DGND (Pin No. 55)
10	MPIN4	Connect to DGND (Pin No. 14)	58	RXIN6	Connect to DGND (Pin No. 55)
11	MPIN5	Connect to DGND (Pin No. 14)	59	RXIN5	Connect to DGND (Pin No. 55)
12	MPIN6	Connect to DGND (Pin No. 14)	60	RXIN4	Connect to DGND (Pin No. 55)
37	CSB	Connect to DGND (Pin No. 43)	61	RXIN3	Connect to DGND (Pin No. 55)
38	SCK	Connect to DGND (Pin No. 43)	62	RXIN2	Connect to DGND (Pin No. 55)
39	SI	Connect to DGND (Pin No. 43)	63	RXIN1	Connect to DGND (Pin No. 55)

- The MPIO[4:1] pins can be set to input or output. In the initial status, these pins are set to output of Hi-Z.
  When not using these pins, use the initial setting and leave the pins open.

9. Description of Analog to Digital Converter (ADC)

9.1 Operation Settings

- ADC operation can be selected from the automatic stop mode that follows DIR operation, continuous operation mode, low sampling rate operation mode, and power-down mode. The initial value is set to the automatic stop mode that follows DIR operation.

Table 9.1 ADC Operation Mode Comparison

Mode Setting	ADC State
Automatic stop mode (initial value)	When PLL is unlocked: Operating
	When PLL is locked: Reset (ADC also resets when ERRF is "H" and PLL is locked)
Continuous operation mode	Always operating
Low sampling rate operation mode	Operating (ADC's rate fixed at 6kHz)
Power-down mode	Complete stop

9.1.1 Automatic Stop Mode

- The automatic stop mode function sets ADC operation with priority on the DIR status, and controls ADC operation according to the PLL locked status and ERRF output status. ("ADCOPR[1:0]=00")
- The ADC is automatically set to the reset status in the PLL locked status. When the PLL changes to the unlocked status, the reset is canceled and the ADC restarts analog to digital conversion. However, ADC is set to the reset status when ERRF is "H" and PLL is locked. (when "RXRESEL=1" or "RXRESTA=1")
- When setting the ADC to automatic stop mode, it is recommended to simultaneously make the oscillation amplifier stop setting. The oscillation amplifier can be automatically stopped while the PLL is locked, by "AMPOPR[1:0]=01". This eliminates the possibility of coexistence of the XIN clock and PLL clock, enabling reduction of interference between the clocks. However, this excludes cases when the XIN clock cannot be stopped, such as when the oscillation amplifier clock output XMCK is constantly supplied to the DSP, etc.

9.1.2 Continuous Operation Mode

- The ADC can be set to the continuous operation mode that constantly continues analog to digital conversion operation regardless of the DIR status.
- Continuous operation mode can be set in the following states. This setting has priority over automatic stop mode.
    - When the ADC clock and data are set to constant output: "SW1SEL[2:0]=001" or "SW2SEL[2:0]=001"
    - When ADC slave operation is set: "MPSEL[1:0]=10 or 11"

9.1.3 Low Sampling Rate Operation Mode
   ### (Analog Audio Data Detection in Power Save Operation Mode)

- The low sampling rate operation mode performs analog audio data detection with low power consumption.
- To set this mode, both "ADCOPR[1:0]=10" and "SDMODE=1" must be set. These registers need to detect the existence of analog audio data in power save operation. When only the ADCOPR[1:0] register or the SDMODE register is set, this function does not operate.
- Low sampling rate operation mode operates only when set to master mode. When the ADC is operated in slave mode, low sampling rate operation cannot be set.
- After this mode is set, the ADC performs analog to digital conversion at a sampling rate of 6kHz.
- Current consumption can be further reduced by simultaneously setting to stop the DIR function and fix the output clock pin outputs to suppress current consumption other than the ADC. See below for further details, "9.6 Analog Audio Data Detection".

9.1.4 Power-down Mode

- The ADC is set to power-down mode by "ADCOPR[1:0]=11". In power-down mode, VREF is set to the AGND voltage.
- Power-on reset when turning the power on and system start-up from power-down mode are both executed via the ADC initialization cycle. Reset by power-on-reset or ADC initialization after power-down mode is canceled require a period of 85ms.
- The ADC advances the reset cancel when initialization is complete. Normally, 16384/fs period needs for the reset cancel. The offset generated in initial data of ADC is removed for this period. When the reset cancel period dose not need, it sets by the ADBMOD register. ("ADBMOD=1")
- DATAOUT outputs data "0" during power-down mode and reset cancel period.
- The ADC starts analog to digital conversion after reset is canceled. The digital data is output after fade-in processing by the digital volume. In addition, switching from normal operation to power-down mode is executed after fade-out processing.
- In cases such as when slave mode or an oscillation module is not used and an external clock is supplied instead, the clock may be disrupted when switching to power-down mode, and noise may be generated. In these cases, set power-down mode after performing soft mute processing. See below for further details, "9.5 Soft Mute/Attenuator".
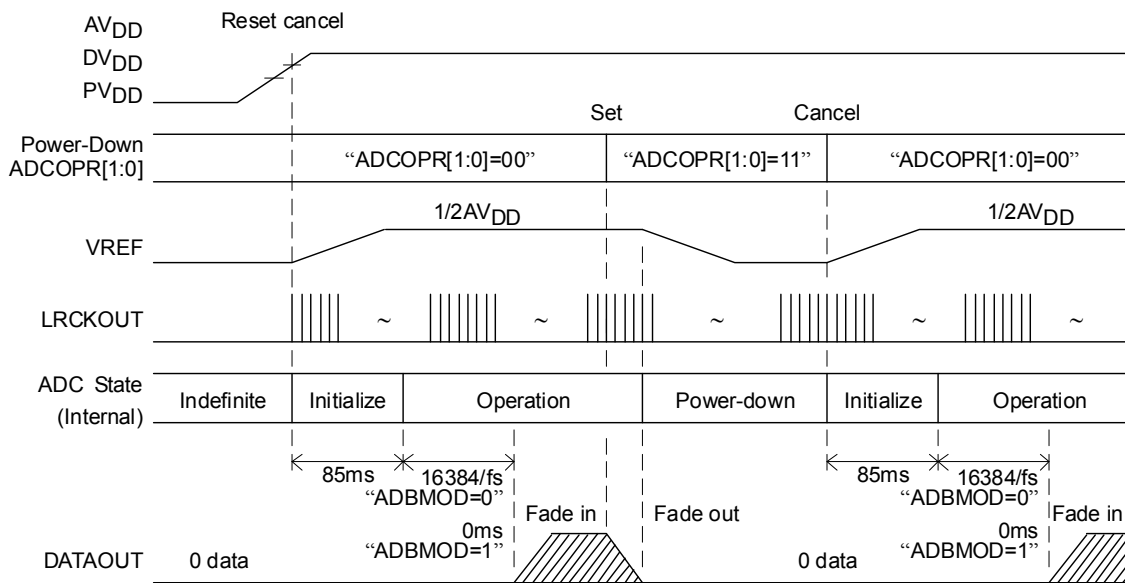
Figure 9.1 Timing Chart for Power-down Mode and When the Mode is Canceled

9.1.5 When Not Using the ADC

- When not using the built-in ADC, 3.3V can be supplied to the AV_{DD} pin that normally requires a 5V supply.
- The ADC can operate even when 3.3V is supplied, but the characteristics are not guaranteed. Therefore, it is recommended to set the power-down mode when not using the ADC.

9.2 Clock Input Settings (XIN, XOUT, XMCK)

• The ADC normally operates in master mode, and can be switched to slave mode by the register setting.

9.2.1 Master Mode 1 (Continuous Operation Mode and Automatic Stop Mode)

• In master mode, the sampling frequency operates at 48kHz or 96kHz.
• Master mode operates using the 12.288MHz or 24.576MHz clock input to the XIN pin.
• The clock set with the XINSEL[1:0] register is supplied to the ADC.
• The clock supplied to the ADC is output from MCKOUT, BCKOUT, LRCKOUT and MPOUT[3:1] when ADC data output is selected.

Table 9.2: ADC Supplied Clock and Output Clocks in Master Mode (Initial Value: "XINSEL[1:0]=00")

XINSEL[1:0]		XIN Pin Input Clock Frequency (Hz)	ADC Sampling Frequency (Hz)	Output Pin Clock Frequency (Hz)		
				MCKOUT MPOUT1	BCKOUT MPOUT2	LRCKOUT MPOUT3
0	0	12.288M	48k	12.288M	3.072M	48k
0	1	24.576M	48k	12.288M	3.072M	48k
1	0	24.576M	48k	24.576M	3.072M	48k
1	1	24.576M	96k	24.576M	6.144M	96k

9.2.2 Master Mode 2 (Low Sampling Rate Operation Mode)

• Operation is performed at the 12.288MHz or 24.576MHz clock input to the XIN pin, but analog to digital conversion is performed at a sampling frequency of 6kHz. See below for further details, "9.6 Analog Audio Data Detection".

9.2.3 Slave Mode

• Slave mode sets clock input and data output pins exclusively for the ADC, and performs analog to digital conversion unaffected by other functions. However, the clock (resonator or external input) must be supplied to XIN even when slave mode is set.
• In slave mode, the sampling frequency operates at 8kHz to 96kHz.
• The master clock operates at 512fs or 256fs.
• Slave mode and the master clock are set with the MPSEL[1:0] register.
• In slave mode, the following functions are assigned to MPIO[4:1].
    MPIO1: ADC master clock (512fs or 256fs) input pin
    MPIO2: ADC bit clock (64fs) input pin
    MPIO3: ADC channel clock (fs) input pin
    MPIO4: ADC audio data output pin

Table 9.3 Clocks That Can Be Input to MPIO[3:1] in Slave Mode

| Pin Name	MPIO1	MPIO2	MPIO3
Usage	Master clock	Bit clock	LR clock
Input clock	512fs or 256fs	64fs	fs
Input clock range	2.048MHz to 24.576MHz	512kHz to 6.144MHz	8kHz to 96kHz

• In slave mode, the ADC clocks output from MCKOUT, BCKOUT, LRCKOUT and MPOUT[3:1] are the signals input to MPIO[3:1]. The system doesn't operate normally when there is no clock input to MPIO[3:1]. Therefore, must be supply the clock to MPIO[3:1] in slave mode.
• The data that has been analog to digital converted according to the DAFORM register setting is output from MPIO4 and MPOUT4. These output data are not affected by MUTEB.

9.3 Digital HPF

- The ADC incorporates a digital HPF to cancel the DC offset.
- The HPF cutoff frequency is 1.85Hz when fs=48kHz. The frequency response is proportional to fs.

9.4 PGA

- The LC89075WA incorporates an analog PGA (Programmable Gain Amplifier).
- The PGA can be set to -4.5dB to +6dB in 1.5dB steps with the ADPGA[2:0] register.
- The input impedance is 27kΩ, and the ADC full-scale input is proportional to the AV_{DD} voltage. $V_{IN}=0.6\times AV_{DD}$

$Rin = 27k\Omega$
$R1 = 27k\Omega$
$C1 = 1\mu F$
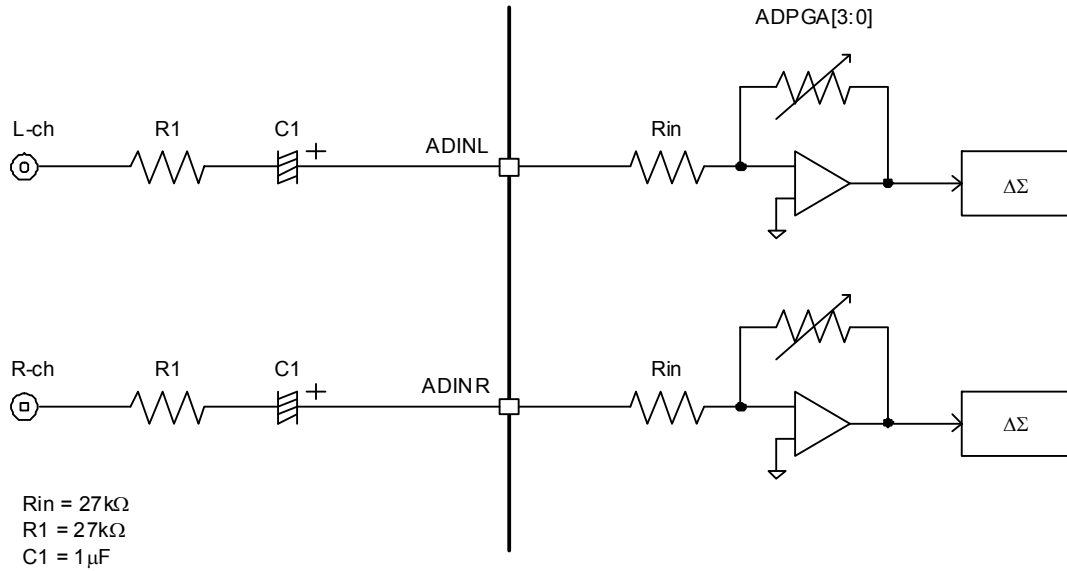
$fc = 1/(2\pi(Rin+R1)C1) = 1/(2\pi\times(27k+27k)\times1\mu) = 2.947\,Hz$
$Zi = Rin+R1 = 27k+27k = 54k\Omega$

Figure 9.2 Internal PGA Analog Input Configuration Diagram

9.5 Soft Mute/Attenuator

- The LC89075WA incorporates a digital volume that can adjust from 0dB to -63.5dB and -∞dB.
- The digital volume is set with the ADVOL[7:0] register. When the ADVOL[7:0] register setting is changed, the volume changes according to the ADFDSP[2:0] register setting. The volume changes the gain in 0.25dB steps.
- When "ADSMUTE=1", soft mute operation is performed to attenuate the volume from the ADVOL[7:0] register setting value to -63.5dB according to the ADFDSP[2:0] register setting, and then to -∞dB (0 data). The gain changes in 0.25dB steps during soft mute operation.
- When mute is canceled during mute execution, the process is stopped and the gain returns to 0dB in 0.25dB steps.
- When mute is set again during mute canceled, the cancel process is stopped and the mute process is performed to -∞dB.
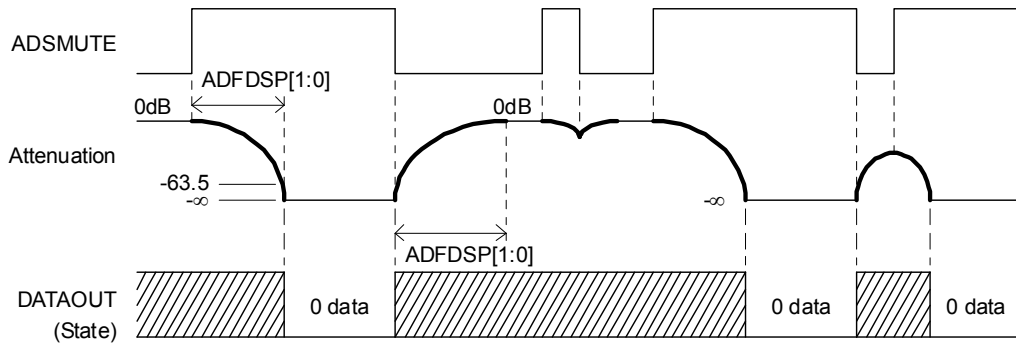

Figure 9.3 Soft Mute Timing Chart

Table 9.4 ADC Output Volume Gain Settings

ADVOL [7:0]	Gain [dB]
00h	0 (initial value)
01h	-0.25
02h	-0.50
03h-FDh	• • •
FEh	-63.5
FFh	-∞

Table 9.5 ADC Output Volume Fade Slope Settings

ADFDSP[2:0]	Fade Slope	0dB to -∞dB Transition Time (Reference)*1
000	1/fs (initial value)	256/fs
001	2/fs	512/fs
010	4/fs	1024/fs
011	8/fs	2048/fs
100	16/fs	4096/fs
101	Reserved	-
110	Reserved	-
111	Direct	1/fs

*1: The time required to attenuate from 0dB to -∞dB when "ADVOL[7:0]=00h".

9.6 Analog Audio Data Detection (DSTATE)

- The LC89075WA can detect the existence ('Sound' or 'Silence') of analog audio data. 'Sound' has the audio data above threshold level. 'Silence' has the audio data below threshold level.
- The 'Sound' detection can be performed in normal operation mode or low sampling rate operation mode.
- The 'Silence' detection can be performed in normal operation mode.
- These detections can be performed on the analog data while the ADC is operating. They cannot be performed while the ADC is in the reset or the power-down status.
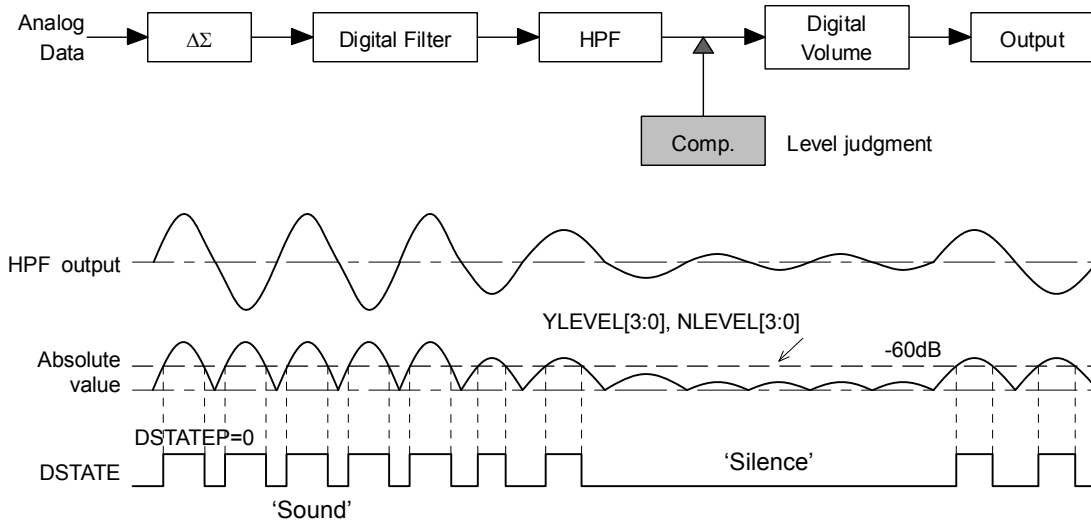
Figure 9.4 Analog Audio Data Detection Timing

9.6.1 'Sound' Detection

9.6.1.1 Detection in Normal Operation Mode

- To perform detection in normal operation mode, "SDMODE=1" is set.
- Analog to digital conversion is performed at a sampling frequency of 48kHz or 96kHz in master mode, or at the clock frequency input to MPIO[3:1] in slave mode.

9.6.1.2 Detection in Low Sampling Rate Operation Mode

- Low sampling rate operation mode can be used only when set to master mode. (See section 9.1.3)
- To perform detection in low sampling rate operation mode, "SDMODE=1" and "ADCOPR[1:0]=10" must be set.
- In this mode, analog to digital conversion is performed at a sampling frequency of 6kHz.
- In this operation mode, the following register settings are recommended to reduce current consumption other than by the ADC.

Table 9.6 Recommended Register Settings for the ADC Power Save Mode Operation

Adr	Register Name	Register Description	Recommended Value	Remarks
00h	ADCOPR[1:0]	ADC operation setting	10	Power save mode operation
00h	DIROPR	DIR operation setting	1	Stop
01h	SDMODE	Analog or digital audio data detection setting	1	'Sound' detection
02h	XMSEL[1:0]	XMCK pin output setting	11	"L" output
05h	OUTMUT	Clock and data output setting	1	"L" output
06h	SW2SEL[2:0]	MPOUT[4:1] pin output setting	000	"L" output
0Bh	RXTHR1[3:0]	RXOUT output data setting	1111	"L" output
0Bh	RXDSEL[3:0]	DIR data demodulation input setting	1111	Connected to GND
0Ch	RXTHR2[3:0]	MPOUT4 output data setting	1111	"L" output

9.6.1.3 Threshold and Output

- The 'Sound' threshold level is set with YLEVEL[3:0] register.
- The YLEVEL[3:0] register can adjust the level from -60dBFS to -30dBFS in 2dBFS steps.
- At YLEVEL[3:0] register initial value, 'Sound' is judged when the signal is larger than -60dBFS.
- The results of judging the data after passing through the HPF are output from DSTATE pin and ODATAM register.
- When a signal that is larger than the threshold level set by YLEVEL[3:0] register is detected, DSTATE outputs "H."

9.6.2 'Silence' Detection

- The 'Silence' detection operates in normal operation mode, and "SDMODE=0" is set.
- The 'Silence' threshold level is set with NLEVEL[3:0] register.
- The NLEVEL[3:0] register can adjust the level from -60dBFS to -30dBFS in 2dBFS steps.
- At NLEVEL[3:0] register initial value, 'Silence' is judged when the signal is smaller than -60dBFS.
- The results of judging the data after passing through the HPF are output from DSTATE pin and ODATAM register.
- When a signal that is smaller than the threshold level set by NLEVEL[3:0] register is detected, DSTATE outputs "L."

9.6.3 DSTATE Output

- The DSTATE output polarity can be changed with DSTATEP.
- The DSTATE pin status can also be read from ODATAM register.
- When ADC operation is stopped, DSTATE outputs "L."

Table 9.7 Analog Data and DSTATE Pin Output Status (When "DSTATEP=0")

DSTATE Output	SDMODE=0 ('Silence' detection)	SDMODE=1 ('Sound' detection)
L	Smaller than the value set by the NLEVEL register or the ADC is reset	Smaller than the value set by the YLEVEL register or the ADC is reset
H	Larger than the value set by the NLEVEL register	Larger than the value set by the YLEVEL register

- 'Sound' or 'Silence' detection can be performed for digital audio data in addition to analog audio data. See below for further details, "12. Digital Audio Data Detection".

9.7 Reset Process

- When the PLL is locked by setting "SYSRST=1" or "ADCOPR[1:0]=00", the ADC is in the reset status. When "ADBMOD=0" is set, 16384/fs period is normally necessary for the reset cancel. If "ADBMOD=1" is set, it has not wait time. The digital data is output after fade-in processing after reset cancel.
- 'Sound' or 'Silence' detection flag DSTATE after reset cancel is output after progress 32768/fs.
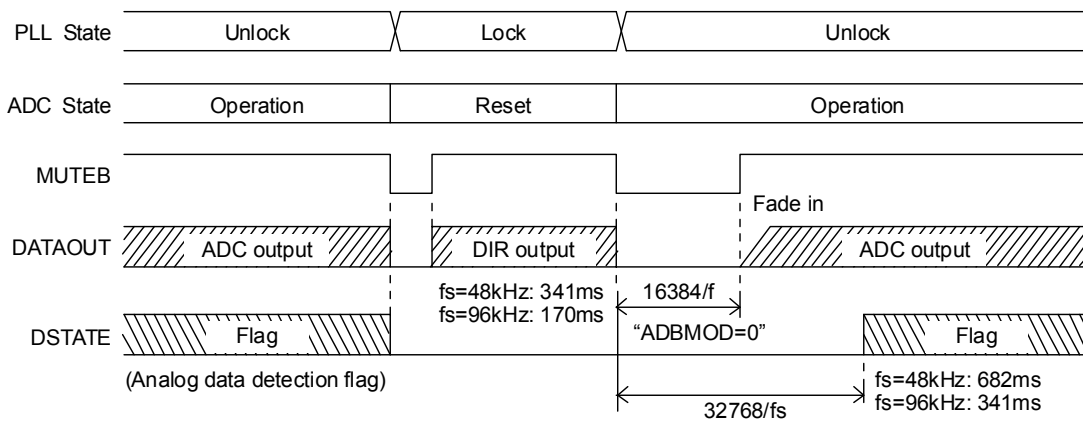

Figure 9.5 ADC Reset Processing Timing (When "ADBMOD=0")

10. Description of Digital Audio Interface Receiver (DIR)

10.1 Clocks

- When the PLL is unlocked, the DIR operates at the clock input to XIN. When the PLL is locked, the DIR operates at the internal VCO (PLL) clock.

10.1.1 PLL Source Master Clock

- The PLL synchronizes with the input S/PDIF and outputs a 512fs clock.
- The PLL clock is controlled by the RXCKAT, RXCKDV[1:0] and RXMCK[1:0] register settings.
- Normally, "RXCKAT=0" is set and a PLL clock is output for each input sampling frequency band. At this setting, output clock frequency fluctuation by varying the sampling frequency is kept to a narrow band, such as 512fs output when fs=32kHz to 48kHz, 256fs output when fs=64kHz to 96kHz, and 128fs output when fs=128kHz to 192kHz.
- When "RXCKAT=0" is set, the PLL clock is set by the RXCKDV[1:0] register
- To set an output clock that does not depend on the S/PDIF input sampling frequency, "RXCKAT=1" is set. At this setting, the clock frequency is always multiplied by a constant and output, such as output at 256fs for all sampling frequencies from 32kHz to 192kHz.
- When "RXCKAT=1" is set, the PLL clock is set by the RXMCK[1:0] register.
- When the PLL is locked, switching is not performed even when the RXCKAT, RXCKDV[1:0] and RXMCK[1:0] registers setting are changed. These registers switching are executed when the PLL is in unlocked status. This setting becomes valid after the PLL is locked again. And, only when "RXCKAT=1" is set, RXMCK[1:0] register can be changed by setting "RXCKMU=1" even PLL lock state. However, the change is not reflected in MUTEB.
- The PLL output clock setting flow is shown below. Note that the PLL can be stopped with the DIROPR register.
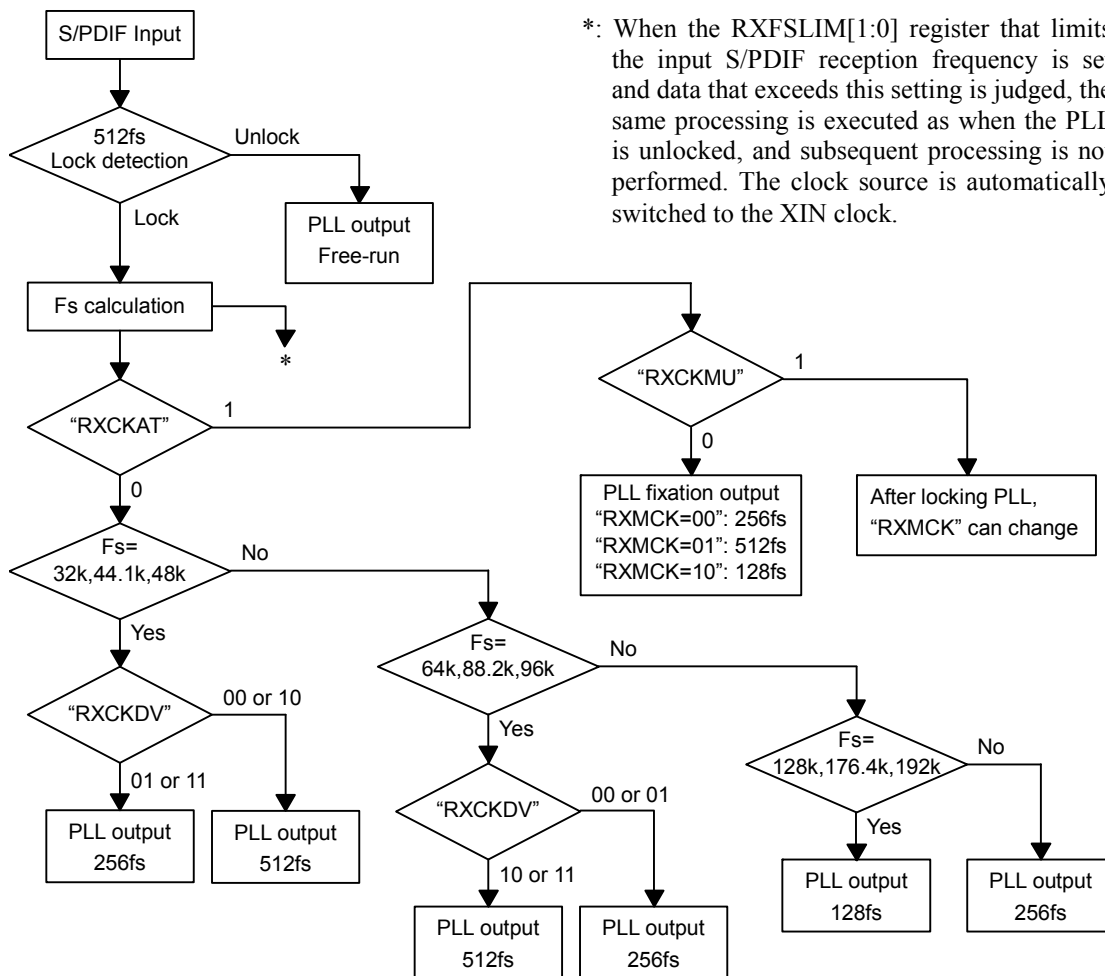
*: When the RXFSLIM[1:0] register that limits the input S/PDIF reception frequency is set and data that exceeds this setting is judged, the same processing is executed as when the PLL is unlocked, and subsequent processing is not performed. The clock source is automatically switched to the XIN clock.

Figure 10.1 PLL Output Clock Flow Diagram

- The PLL clock output frequencies are shown below.
- When "RXCKAT=1" and "RXMCK[1:0]=01" are set (512fs), 128kHz, 176.4kHz and 192kHz S/PDIF reception results in a PLL output frequency that exceeds 50MHz, so direct output to MCKOUT is not guaranteed.

Table 10.2 PLL Clock Output Frequencies (Bold settings are initial values.)

S/PDIF fs (kHz)	PLL Output (MHz)						
	"RXCKAT=0" (Fixed multiple outputs for each input fs band)				"RXCKAT=1" (Fixed multiple outputs of input fs)		
	"RXCKDV=00"	"RXCKDV=01"	"RXCKDV=10"	"RXCKDV=11"	"RXMCK=00" (256fs)	"RXMCK=01" (512fs)	"RXMCK=10" (128fs)
32	**16.38**	8.19	16.38	8.19	8.19	16.38	4.09
44.1	**22.57**	11.28	22.57	11.28	11.28	22.57	5.64
48	**24.57**	12.28	24.57	12.28	12.28	24.57	6.14
64	**16.38**	16.38	32.76	32.76	16.38	32.76	8.19
88.2	**22.57**	22.57	45.15	45.15	22.57	45.15	11.28
96	**24.57**	24.57	49.15	49.15	24.57	49.15	12.28
128	**16.38**	16.38	16.38	16.38	32.76	65.54 *	16.38
176.4	**22.57**	22.57	22.57	22.57	45.15	90.32 *	22.57
192	**24.57**	24.57	24.57	24.57	49.15	98.30 *	24.57

*: Direct output to the MCKOUT pin is not guaranteed.

10.1.2 XIN Source Master Clock (XIN, XOUT, XMCK)

- The DIR uses clock supply to XIN for the following applications.
   1) Clock source when the PLL is unlocked
   2) PLL lock-in support
   3) Calculation of the input data sampling frequency

- A clock must always be supplied to XIN.
- Normally, the oscillation amplifier always operates regardless of the PLL status, but operation that automatically stops the oscillation amplifier while the PLL is locked can also be set. This is set by the AMPOPR[1:0] register.
  The AMPOPR[1:0] register must be set before S/PDIF input, or the setting must be completed while the PLL is unlocked. In addition, when the oscillation amplifier is automatically stopped, the XMCK clock is not output.
- When "SW1SEL[2:0]=001", "SW2SEL[2:0]=001" or slave mode "MPSEL[1:0] =10 or 11", the oscillation amplifier is set to continuous operation mode. This has higher priority than the AMPOPR[1:0] register setting.