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# MachXO3-9400 Development Board

# Evaluation Board User Guide

FPGA-EB-02004 Version 1.0

May 2017

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| ASC | Analog Sense and Control |
| CMOS | Complementary Metal-Oxide Semiconductor |
| GDDR | Graphics Double Data Rate |
| FTDI | Future Technology Devices International |
| GPIO | General Purpose Input/Output |
| $I^2C$ | Inter-Integrated Circuit |
| LVDS | Low-Voltage Differential Signaling |
| SPI | Serial Peripheral Interface |

# 1. Introduction

The Lattice Semiconductor MachXO3-9400™ Development Board allows designers to investigate and experiment with the features of the MachXO3 complex programmable logic device (CPLD) and the L-ASC10 (L-Analog Sense and Control 10 rails) hardware management expander. The features of the MachXO3-9400 Development Board can assist engineers with the rapid prototyping and testing of their specific designs.

The MachXO3-9400 Development Board is part of the MachXO3-9400 Development Kit, which includes the following:

- MachXO3-9400 Development Board pre-loaded with the demo design
- Mini USB cable
- QuickStart Guide

This document is intended to be referenced in conjunction with demo user guides for MachXO3-9400. See the References

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the on-board headers, diodes and switches and a complete set of schematics.

## 1.1. MachXO3-9400 Development Board

Along with the MachXO3LF-9400 CPLD, the MachXO3-9400 Development Board also features an L-ASC10 device to enable designers to easily evaluate hardware management design and expand the usability of the MachXO3LF-9400 with Arduino, Raspberry, FX12, Versa and Aardvark headers.

Figure 1.1 shows the top view of the MachXO3-9400 Development Board. Figure 1.2 shows the bottom view of the board.

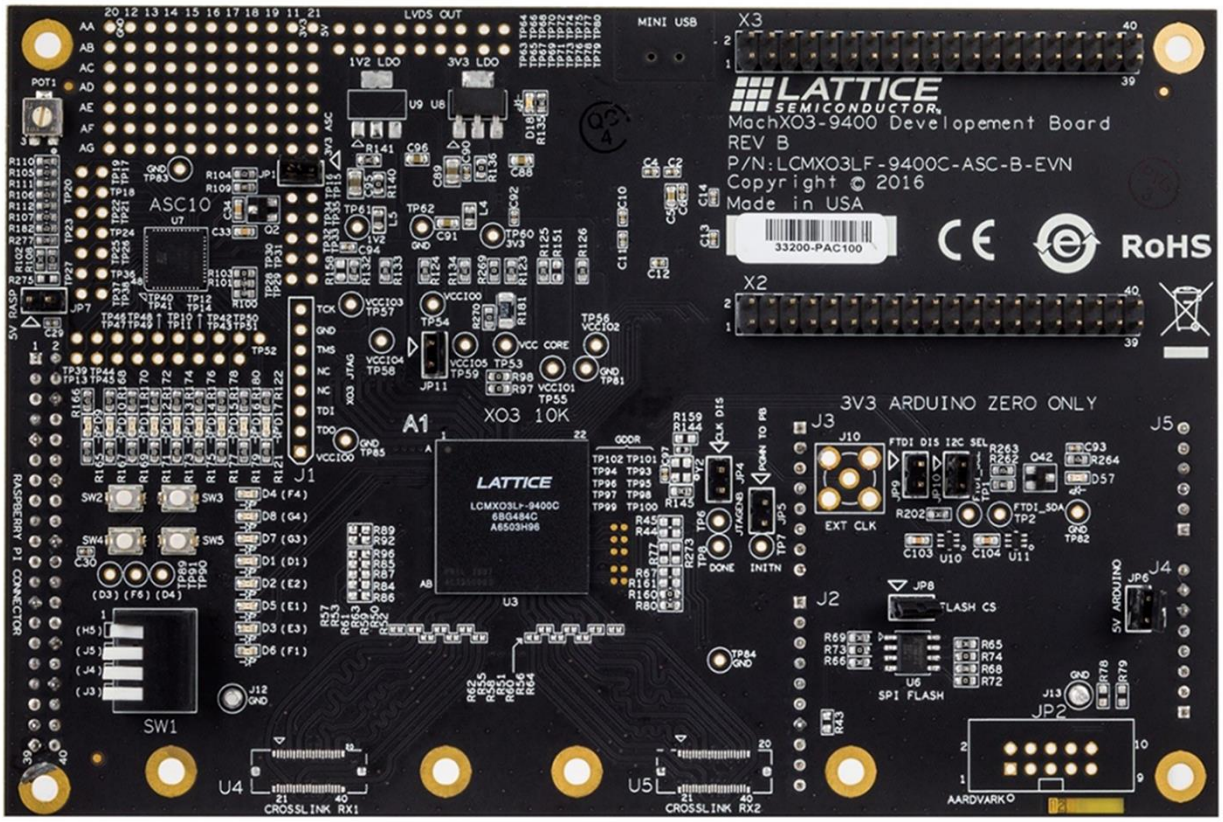


**Figure 1.1. Top View of MachXO3-9400 Development Board**

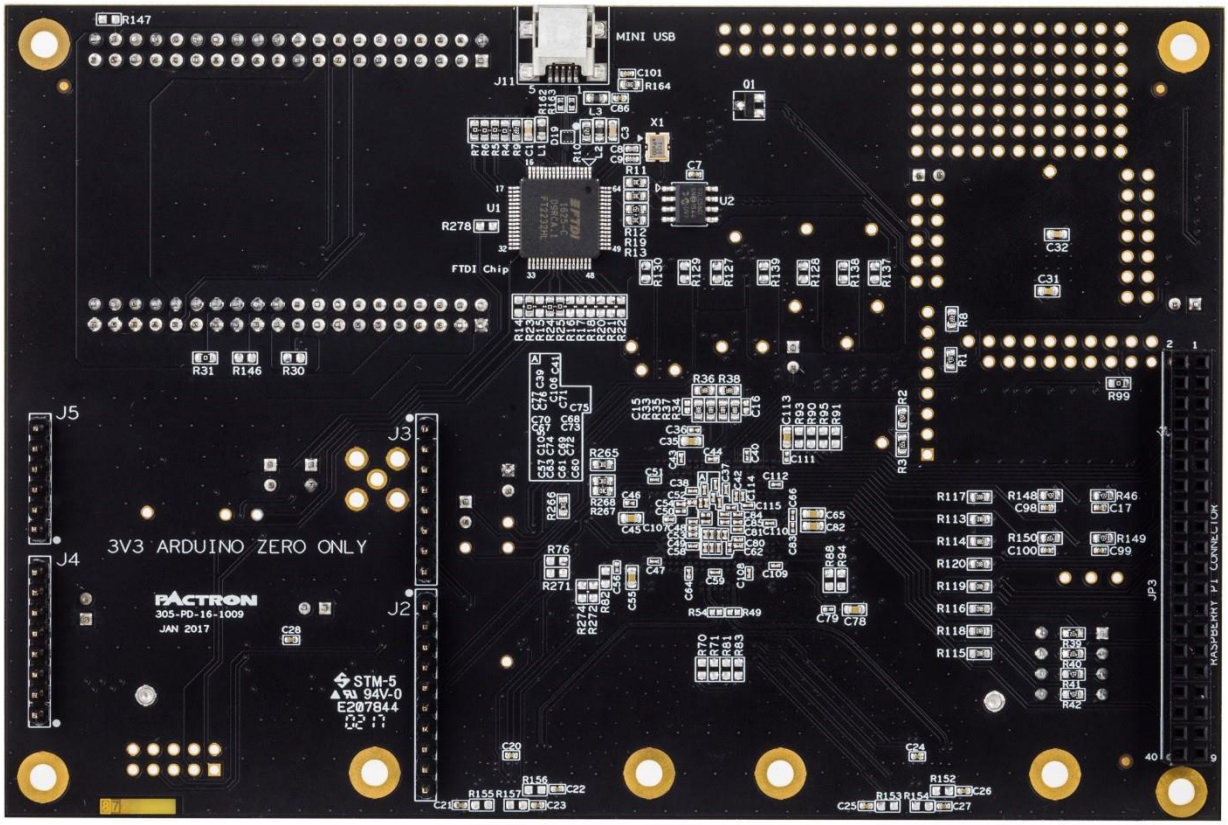


**Figure 1.2. Bottom View of MachXO3-9400 Development Board**

## 1.2. Features

- LCMXO3LF-9400C CPLD demonstration with L-ASC10 for simple hardware management including voltage, current and temperature monitoring
- General Purpose Input/Output (GPIO) interface with Arduino and Raspberry Pi boards
- USB-B connection for device programming and Inter-Integrated Circuit ($I^2C$) utility
- On-board Boot Flash – 16 Mbit Serial Peripheral Interface (SPI) Flash, with Quad read feature for user's application
- 4-position DIP Switches, 4 push buttons and 16 LEDs for demo purposes
- Diamond® programming support
- Multiple reference clock sources
- Two Hirose FX12-40 header positions (DNI)
- Aardvark header (DNI)

**Note:** DNI stands for "Do NOT Install" parts and DI stands for "Do Install" parts for assembly.

**Caution:** The MachXO3-9400 Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

## 1.3. MachXO3LF Device

The MachXO3-9400 Development Board features the MachXO3LF-9400 in 484-ball caBGA package. This MachXO3LF-9400 device (also referred to as LCMXO3LF-9400C) features 9400 LUTs and 432 kbits of embedded block RAM. This device offers a variety of features and programmability. For more information on the capabilities of MachXO3™, see DS1047, MachXO3 Family Data Sheet.

## 1.4. L-ASC10 Device

The L-ASC10 (also referred to as ASC) is a Hardware Management (Power, Thermal, and Control Plane Management) Expander designed to be used with Platform Manager 2 or MachXO2/MachXO3 FPGAs to implement the Hardware Management Control function in a circuit board. The L-ASC10 enables seamless scaling of power supply voltage and current monitoring, temperature monitoring, sequence and margin control channels. ASC includes dedicated interfaces supporting the exchange of monitor signal status and output control signals with centralized hardware management controllers. For more information on the capabilities of ASC device see DS1042, L-ASC10 Data Sheet.

# 2. Applying Power to the Board

The MachXO3-9400 Development Board is ready to power on with onboard Low Dropout (LDO) generators powered by an external 5 V power, as shown in Figure 2.1. The 5 V power can come from a USB connection (J11) and routed to multiple onboard headers listed Table 2.1. Note that the 5 V power path to headers should be manually connected using a zero-ohm resistor or jumper before power is applied to the mated board as outlined in Table 2.1.

**Table 2.1. 5 V Sources and Connections**

| Header (Reference) | 5 V Power Pins | 5 V Power Path (Assembly) |
|---|---|---|
| USB header (J11) | 1 | L3 (DI) |
| FX12 header 1 (U4) | 23, 38 | R153 (DNI) |
| FX12 header 2 (U5) | 23, 38 | R155 (DNI) |
| Aardvark header (JP2) | 4, 6 | R78(DNI), R79 (DNI) |
| Arduino header (J4) | 5 | JP6 (DNI) |
| Raspberry Pi header (JP3) | 2, 4 | JP7 (DNI) |
| Versa header (X2) | 21 | R30 (DNI) |

**Warning:** Avoid power conflict when the 5 V power path is enabled from the MachXO3-9400 Development Board to the mated board, Do Not apply 5V power from both boards when the path is manually shorted.

Conversely, 5 V power can be supplied from onboard headers if J11 is not connected to a USB cable. The power from the headers can be used to drive LDOs and other mated boards.

Aside from the 3.3 V LDO (U8) default power source for MachXO3 device (U3), the board provides additional LDO footprint (U9) for lower power applications. For example, TLV1117LV12DCY can be used for 1.2 V VCCIOs. Other SOT-223 footprint compatible LDOs from 1.2 V to 3.3 V can also be considered. VCCIO1 for Bank 1 and VCCIO3 for Bank 3 can likewise be supplied from mated boards. 3.3 V is used for better GPIO voltage alignment.

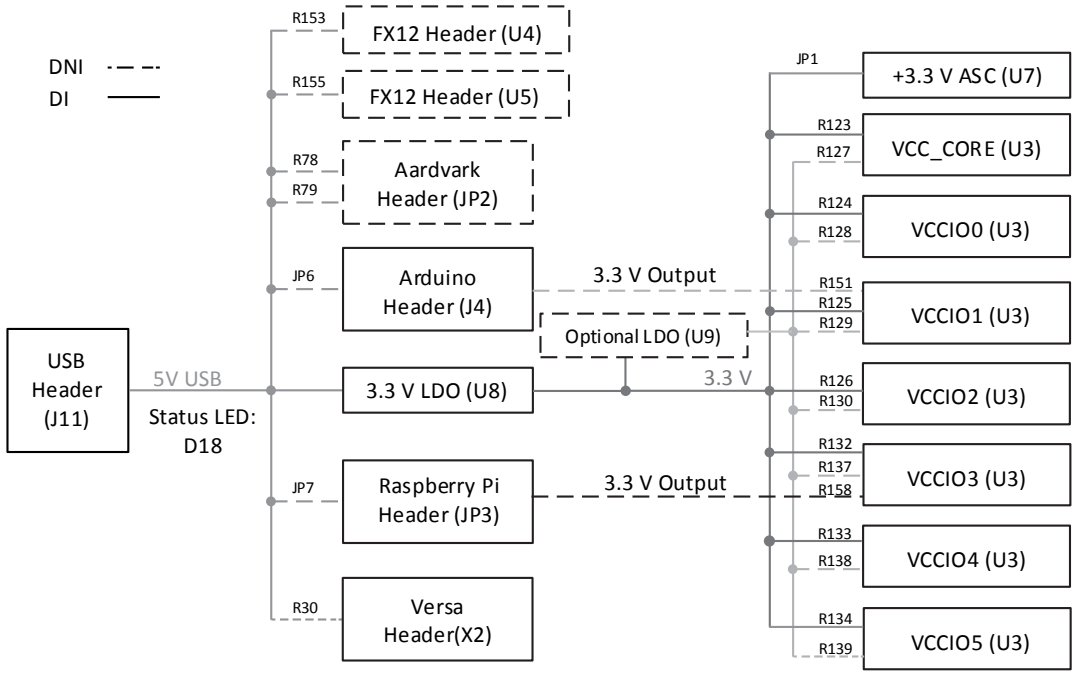


**Figure 2.1. Board Power Supply**

**Table 2.2. MachXO3 Power Rail Options**

| MachXO3 Device Power (U3) | 3.3 V Option (Assembly) | 1.2V~3.3 V Option (Assembly) | Mated Board Option (Assembly) |
|---|---|---|---|
| VCC Core | R123 (DI) | R127 (DNI)* | NA |
| VCCIO0 | R124 (DI) | R128 (DNI) | NA |
| VCCIO1 | R125 (DI) | R129 (DNI) | R151 (DNI) for Arduino |
| VCCIO2 | R126 (DI) | R130 (DNI) | NA |
| VCCIO3 | R132 (DI) | R137 (DNI) | R158 (DNI) for Raspberry Pi |
| VCCIO4 | R133 (DI) | R138 (DNI) | NA |
| VCCIO5 | R134 (DI) | R139 (DNI) | NA |

***Note:** R127 is applicable only in 2.5 V~3.3 V (U9) range for LCMXO3LF-9400C device.

**Warning:** Only one option should be enabled for each MachXO3 device power rail.

The ASC device (U7) acquires power from the 3.3 V LDO only. A jumper (JP1) needs to be installed to provide the power and this can also be used as test point to measure current drawn by the ASC.

**Table 2.3. ASC Power Connections**

| ASC Power | ASC Power Pins | ASC Power Isolation (Assembly) |
|---|---|---|
| 3.3 V VCC | 8, 33 of U7 | JP1 (DI) |

# 3. JTAG/I²C Programming

The JTAG/I²C programming architecture of the MachXO3-9400 Development Board is shown in Figure 3.1.

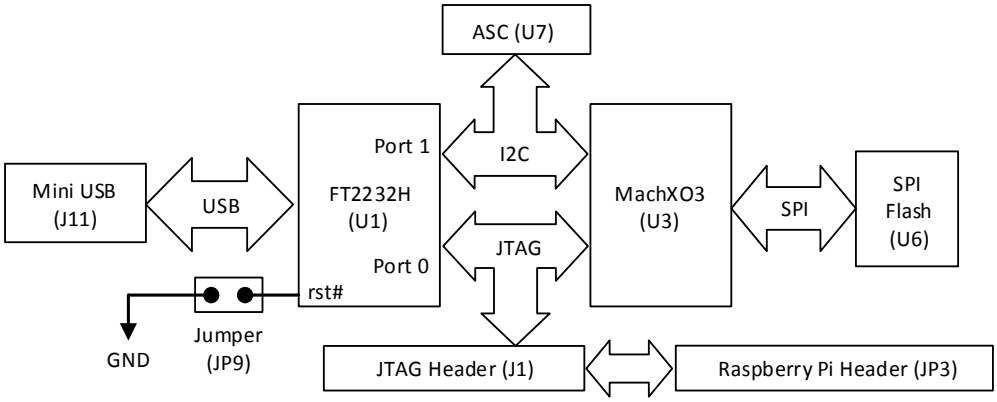


**Figure 3.1. JTAG/I²C Programming Architecture**

## 3.1. JTAG Download Interface

The MachXO3-9400 Development Board has a built-in download controller for programming the MachXO3 device. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download cable, connect the USB cable from J11 to your PC (with Diamond programming software installed). A mini USB to USB-A cable is included in the MarchXO3-9400 Development Kit. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in cable available for use with the Diamond programming software. Use PTM Programming for the Access mode as shown in Figure 3.2.

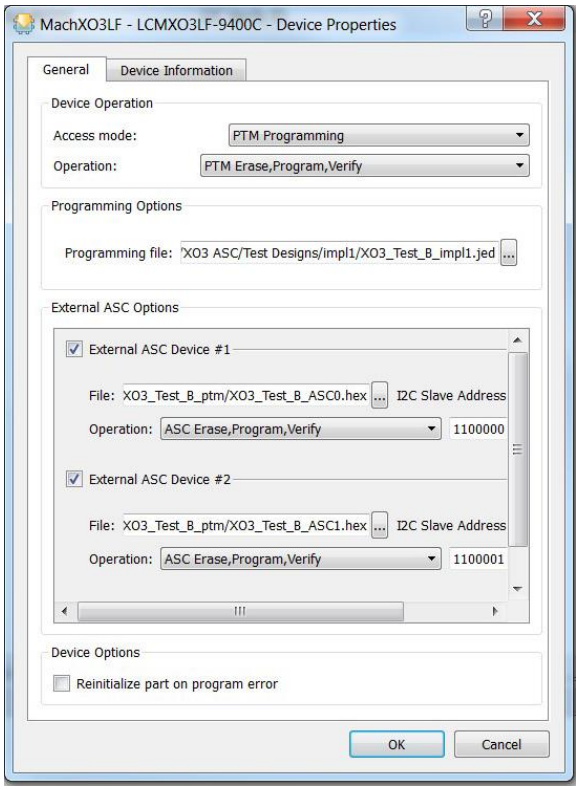


**Figure 3.2. PTM Programming Mode**

## 3.2. I²C Download Interface

The USB hub on the PC can also detect the addition of the USB function on Port 1. Select the port FTUSB-1 on the programmer interface and enable the I²C MUX path from FTDI to the I²C bus. This is done by setting the J10 jumper (D57 red LED is lighted). The I²C interface programming can be also used to configure the MachXO3 and ASC.

## 3.3. Alternate JTAG Download Interface

J1 is an 8-pin standalone JTAG header that is used with an external Lattice download cable (available separately) when the FTDI part is disabled from the JTAG chain after setting JP9. A USB download cable can be attached to the board using J1 to interface with the MachXO3. For details on the connection between the USB download cable and J1, refer to UG48, Programming Cable User's Guide.

J1 can also be used as test point when USB to JTAG is working. Additionally, you can enable the JTAG access path through the Raspberry Pi header (JP3) for customer applications. This is done by connecting the JP3 header to the J1 header through some onboard resistors. The JTAG connections between J1 and JP3 are listed in Table 3.1.

**Table 3.1. JTAG Connections**

| J1 Pin Number | JTAG Signal Name | MachXO3 Ball Location for JTAG | JP3 Pin Number | J1 to JP3 Isolation (Assembly) | Raspberry Pi GPIO |
|---|---|---|---|---|---|
| 1 | VCCIO0 | — | — | — | — |
| 2 | TDO | E8 | 10 | R90 (DNI) | IO15 |
| 3 | TDI | E9 | 11 | R93 (DNI) | IO17 |
| 4 | — | — | — | — | — |
| 5 | — | — | — | — | — |
| 6 | TMS | C10 | 12 | R91 (DNI) | IO18 |
| 7 | GND | — | — | — | — |
| 8 | TCK | D10 | 8 | R95 (DNI) | IO14 |

## 3.4. JTAG to MSPI Pass-through Interface

The download controller can also access the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Diamond Programmer.

## 3.5. Other JTAG Configuration Pins

The MachXO3-9400 Development Board provides test points for other JTAG configuration pins as shown in Table 3.2.

**Table 3.2. Other JTAG Signals**

| Signal Name | MachXO3 Ball Location | Test Point |
|---|---|---|
| JTAGENB | E14 | TP6 |
| PROGRAMN | E15 | Pin 1 of JP5 |
| INITN | F16 | TP7 |
| DONE | E17 | TP8 |

For more information on MachXO3 JTAG/ I²C programming, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

# 4. MachXO3 Clock Sources

The MachXO3-9400 Development Board has four options for the MachXO3 clock sources:

- 12 MHz from U1
- 8 MHz from U7
- User defined frequency by installing an oscillator in the Y2 (DNI) footprint
- Off board clock source from J10 (DNI)

The 8 MHz clock from U7 is the default clock source when building a Platform Manager design. Note that JP1 should be installed to power the ASC device.

The 12 MHz clock from the FT2232H FTDI device is another clock source. Its use requires JP11 to be installed to connect the 12 MHz clock signal to the MachXO3 device I/O. JP9 should not be installed to enable U1.

**Table 4.1. JTAG Connections**

| Clock Frequency | Signal Name | MachXO3 Ball Location | Clock Source | Comments |
|---|---|---|---|---|
| 8 MHz | ASC_CLK | L1 | U7 | JP1 installed, test point TP14 |
| 12 MHz | 12MHz | B10 | U1 | JP11 installed, JP9 removed |
| User defined | OSC_IN | D22 | Y2 (DNI) | JP4 removed and OSC_EN signal (MachXO3 ball L20) Logic 1. |
| User defined | OSC_IN | D22 | J10 (DNI) | Y2 not installed, or OSC_EN signal (MachXO3 ball L20) Logic 0, or JP4 installed. |

Additional information on using optional clock sources:

- The board provides for an optional clock input for the MachXO3 from either the Oscillator (Y2) or the SMA header (J10) as shown in Figure 4.1. Neither of them are populated.
- Y2 should be installed by the end user and it should be a 2.5 mm x 2.0 mm 4-SMD package. This is compatible with the ASDMB serial of the Ultra Miniature Pure Silicon™ Clock Oscillator from Abracon LLC. JP4 can be used to disable Y2 output by pulling down OSC_EN, which can also be controlled by the L20 pin of MachXO3.
- J10 should be installed by the end user. A Complementary Metal-Oxide Semiconductor (CMOS) compatible clock can then be connected with an SMA cable.

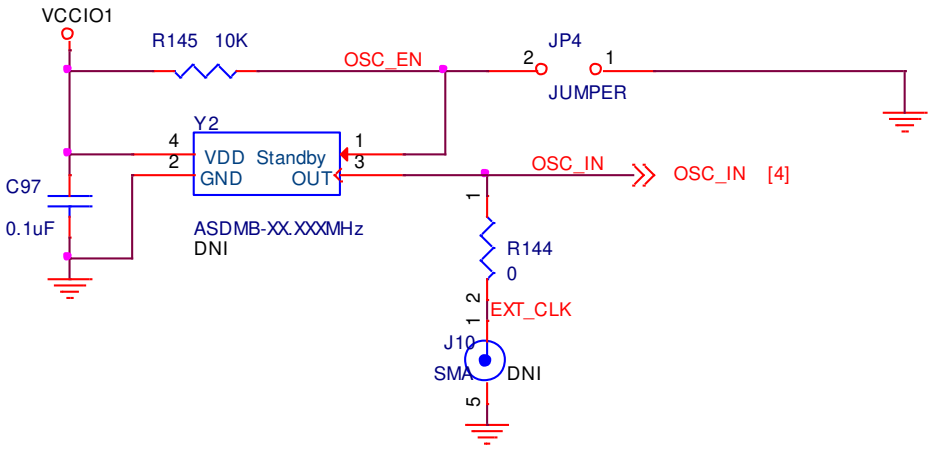


**Figure 4.1. Optional Clock Circuit Design**

# 5. Headers and Test Connections

This section describes the MachXO3-9400 Development Board headers and test connections.

## 5.1. Versa Headers

The board provides two headers – X2 and X3 for expansion purpose.

**Table 5.1. Versa X2 Header Pin Connections**

| X2 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 1 | GND | — |
| 2 | NC | — |
| 3 | EXPCON_2V5* | — |
| 4 | EXPCON_IO29 | E12 |
| 5 | EXPCON_IO30 | D14 |
| 6 | EXPCON_IO31 | C15 |
| 7 | EXPCON_IO32 | C17 |
| 8 | EXPCON_IO33 | D15 |
| 9 | EXPCON_IO34 | C18 |
| 10 | EXPCON_IO35 | D16 |
| 11 | EXPCON_IO36 | C19 |
| 12 | EXPCON_IO37 | D17 |
| 13 | EXPCON_IO38 | D18 |
| 14 | EXPCON_IO39 | C20 |
| 15 | EXPCON_IO40 | E16 |
| 16 | EXPCON_IO41 | E13 |
| 17 | EXPCON_IO42 | F13 |
| 18 | EXPCON_IO43 | F15 |
| 19 | EXPCON_IO44 | G15 |
| 20 | EXPCON_IO45 | G12 |
| 21 | 5VIN* | — |
| 22 | GND | — |
| 23 | EXPCON_2V5* | — |
| 24 | GND | — |
| 25 | VCCIO0 | — |
| 26 | GND | — |
| 27 | VCCIO0 | — |
| 28 | GND | — |
| 29 | EXPCON_OSC* | — |
| 30 | GND | — |
| 31 | EXPCON_CLKIN | A10 |
| 32 | GND | — |
| 33 | EXPCON_CLKOUT | A21 |
| 34 | GND | — |
| 35 | EXPCON_3V3** | — |

**Table 5.1. Versa X2 Header Pin Connections** *(continued)*

| X2 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 36 | GND | — |
| 37 | EXPCON_3V3** | — |
| 38 | GND | — |
| 39 | EXPCON_3V3** | — |
| 40 | GND | — |

**Notes:**

* Signal is optionally connected to power source through resistor; DNI.

** Signal is optionally connected to power source through resistor; DN.

**Table 5.2. Versa X3 Header Pin Connections**

| X3 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 1 | HPE_RESOUT# | G9 |
| 2 | GND | — |
| 3 | EXPCON_IO0 | F8 |
| 4 | EXPCON_IO1 | G8 |
| 5 | EXPCON_IO2 | F9 |
| 6 | EXPCON_IO3 | F7 |
| 7 | EXPCON_IO4 | E7 |
| 8 | EXPCON_IO5 | E6 |
| 9 | EXPCON_IO6 | D5 |
| 10 | EXPCON_IO7 | C3 |
| 11 | EXPCON_IO8 | D6 |
| 12 | EXPCON_IO9 | C4 |
| 13 | EXPCON_IO10 | F10 |
| 14 | EXPCON_IO11 | C5 |
| 15 | EXPCON_IO12 | C6 |
| 16 | EXPCON_IO13 | B12 |
| 17 | EXPCON_IO14 | D7 |
| 18 | EXPCON_IO15 | A12 |
| 19 | GND | — |
| 20 | EXPCON_3V3** | — |
| 21 | EXPCON_IO16 | D8 |
| 22 | GND | — |
| 23 | EXPCON_IO17 | C8 |
| 24 | GND | — |
| 25 | EXPCON_IO18 | D9 |
| 26 | GND | — |
| 27 | EXPCON_IO19 | E10 |
| 28 | EXPCON_IO20 | C9 |
| 29 | EXPCON_IO21 | G11 |
| 30 | GND | — |
| 31 | EXPCON_IO22 | E11 |

**Table 5.2. Versa X3 Header Pin Connections** *(continued)*

| X3 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 32 | EXPCON_IO23 | D11 |
| 33 | EXPCON_IO24 | F11 |
| 34 | GND | — |
| 35 | EXPCON_IO25 | D12 |
| 36 | EXPCON_IO26 | F12 |
| 37 | EXPCON_IO27 | D13 |
| 38 | CARDSEL#* | — |
| 39 | EXPCON_IO28 | C14 |
| 40 | GND | — |

**Notes:**

* Signal is optionally connected to power source through resistor; DNI.

** Signal is optionally connected to power source through resistor; DN.

## 5.2. Arduino Board GPIO Headers

The board provides four headers – J2, J3, J4 and J5 for Arduino Zero board adaption.

**Table 5.3. Arduino J2 Pin Connections**

| J2 Pin Number | Signal Name | Arduino ZERO Board Signal | MachXO3 Ball Location | Comments |
|---|---|---|---|---|
| 1 | AR_IO8 | ~8 | U21 | — |
| 2 | AR_IO9 | ~9 | U22 | — |
| 3 | AR_SS_IO10 | ~10 | W20 | Optional connection to SS through R67 for SPI access, DNI by default. |
| 4 | AR_MOSI_IO 11 | ~11 | V18 | Optional connection to SISPI through R82 for SPI access, DNI by default. |
| 5 | AR_MISO_IO 12 | ~12 | G16 | Optional connection to SPISO through R77 for SPI access, DNI by default. |
| 6 | AR_SCK_IO1 3 | ~13 | F17 | Optional connection to MCLK through R76 for SPI access, DNI by default. |
| 7 | GND | GND | — | — |
| 8 | AR_AREF | AREF | U17 | AR_AREF connection to AREF through R43, DNI by default. |
| 9 | AR_SDA | SDA | U19 | Optional connection to SDA0 through R44, DNI by default. |
| 10 | AR_SCL | SCL | U18 | Optional connection to SCL0 through R45, DNI by default. |

**Table 5.4. Arduino J3 Pin Connections**

| J3 Pin Number | Signal Name | Arduino ZERO Board Signal | MachXO3 Ball Location | Comments |
|---|---|---|---|---|
| 1 | AR_IO0 | RX <- 0 | G19 | — |
| 2 | AR_IO1 | TX -> 1 | G20 | — |
| 3 | AR_IO2 | 2 | G21 | — |
| 4 | AR_IO3 | ~3 | H20 | — |
| 5 | AR_IO4 | ~4 | G18 | — |
| 6 | AR_IO5 | ~5 | L21 | — |
| 7 | AR_IO6 | ~6 | W22 | — |
| 8 | AR_IO7 | 7 | V22 | — |
| 9 | AR_SDA | SDA | U19 | — |
| 10 | AR_SCL | SCL | U18 | — |

**Table 5.5. Arduino J4 Pin Connections**

| J3 Pin Number | Signal Name | Arduino ZERO Board Signal | MachXO3 Ball Location | Comments |
|---|---|---|---|---|
| 1 | AR_IO 14 | ATN | T17 | — |
| 2 | NC | IOREF | — | — |
| 3 | AR_RE SET | RESET | U20 | Pin U20 should be set high by default. Avoid Arduino ZERO board in Reset status when connected. |
| 4 | +3.3V_ AR | 3.3 V | — | 3.3 V power supply from Arduino ZERO board |
| 5 | AR_5V | 5 V | — | Jump to 5 V main power through JP6 |
| 6 | GND | GND | — | — |
| 7 | GND | GND | — | — |
| 8 | +12V | VIN | — | 12 V power supply from Arduino ZERO board |

**Table 5.6. Arduino J5 Pin Connections**

| J3 Pin Number | Signal Name | Arduino ZERO Board Signal | MachXO3 Ball Location | Comments |
|---|---|---|---|---|
| 1 | AR_AD0 | A0 | P19 | Used as GPIO in digital mode |
| 2 | AR_AD1 | A1 | P18 | Used as GPIO in digital mode |
| 3 | AR_AD2 | A2 | P17 | Used as GPIO in digital mode |
| 4 | AR_AD3 | A3 | P16 | Used as GPIO in digital mode |
| 5 | AR_AD4 | A4 | K22 | Used as GPIO in digital mode |
| 6 | AR_AD5 | A5 | G17 | Used as GPIO in digital mode |

**Note:** If JP6 is installed, 5 V power can be supplied from either the Arduino board or the MachXO3-9400 Development Board. With JP6 removed, both boards need their own 5 V power.

## 5.3. FX12 Headers (DNI)

The board provides two headers – U4 and U5 to connect to FX12 compatible boards or cables. Each header has eight pairs of Low-Voltage Differential Signaling (LVDS) signals for high speed data receiver.

**Table 5.7. FX12 U4 Header Pin Connections**

| U4 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 1 | CH0_DCK_P | AA10 |
| 2 | CH0_DCK_N | AB10 |
| 3 | GND | — |
| 4 | CH0_DATA0_P | AA4 |
| 5 | CH0_DATA0_N | AB4 |
| 6 | GND | — |
| 7 | CH0_DATA2_P | AA5 |
| 8 | CH0_DATA2_N | AB5 |
| 9 | GND | — |
| 10 | FX_SN* | — |
| 11 | FX_SCLK* | — |
| 12 | PWR_12V** | — |
| 13 | SDA2 | AB13 |
| 14 | SCL2 | AA13 |
| 15 | GND | — |
| 16 | CH2_DATA0_P | AA6 |
| 17 | CH2_DATA0_N | AB6 |
| 18 | GND | — |
| 19 | CH2_DCK_P | AA7 |
| 20 | CH2_DCK_N | AB7 |
| 21 | PWR_12V** | — |
| 22 | RESETN | AB3 |
| 23 | PWR_5-0V* | — |
| 24 | CH0_DATA1_P | AA2 |
| 25 | CH0_DATA1_N | AB2 |
| 26 | PWR_3-3V* | — |
| 27 | CH0_DATA3_P | AA8 |
| 28 | CH0_DATA3_N | AB8 |
| 29 | PWR_1-8V* | — |
| 30 | FX_MOSI* | — |
| 31 | FX_MISO* | — |
| 32 | PWR_1-8V* | — |
| 33 | GND | — |
| 34 | GND | — |
| 35 | PWR_3-3V* | — |
| 36 | CH2_DATA1_P | AA9 |
| 37 | CH2_DATA1_N | AB9 |

**Table 5.7. FX12 U4 Header Pin Connections** *(continued)*

| U4 Pin Number | | Signal Name | MachXO3 Ball Location |
|---|---|---|---|
| 38 | | PWR_5-0V* | - |
| 39 | | SDA1 | AA11 |
| 40 | | SCL1 | AB11 |

**Notes:**

* Signal is optionally connected to power source through resistor; DNI.

** 12 V power needs external supply from pin 8 of J4.

**Table 5.8. FX12 U5 Header Pin Connections**

| U5 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 1 | CH1_DCK_P | AB12 |
| 2 | CH1_DCK_N | AA12 |
| 3 | GND | — |
| 4 | CH1_DATA0_P | AB16 |
| 5 | CH1_DATA0_N | AA16 |
| 6 | GND | - |
| 7 | CH1_DATA2_P | AB17 |
| 8 | CH1_DATA2_N | AA17 |
| 9 | GND | — |
| 10 | FX_SN* | — |
| 11 | FX_SCLK* | — |
| 12 | PWR_12V** | — |
| 13 | SDA2 | AB13 |
| 14 | SCL2 | AA13 |
| 15 | GND | — - |
| 16 | CH3_DATA0_P | AB18 |
| 17 | CH3_DATA0_N | AA18 |
| 18 | GND | — - |
| 19 | CH3_DCK_P | AB19 |
| 20 | CH3_DCK_N | AA19 |
| 21 | PWR_12V** | — - |
| 22 | RESETN | AB3 |
| 23 | PWR_5-0V* | — - |
| 24 | CH1_DATA1_P | AB14 |
| 25 | CH1_DATA1_N | AA14 |
| 26 | PWR_3-3V* | — - |
| 27 | CH1_DATA3_P | AB15 |
| 28 | CH1_DATA3_N | AA15 |
| 29 | PWR_1-8V | — |
| 30 | FX_MOSI* | — |
| 31 | FX_MISO* | — |
| 32 | PWR_1-8V* | — |
| 33 | GND | — |

**Table 5.8. FX12 U5 Header Pin Connections** *(continued)*

| U5 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 34 | GND | - — |
| 35 | PWR_3-3V* | — - |
| 36 | CH3_DATA1_P | AB20 |
| 37 | CH3_DATA1_N | AA20 |
| 38 | PWR_5-0V* | — - |
| 39 | SDA1 | AA11 |
| 40 | SCL1 | AB11 |

**Notes:**

* Signal is optionally connected to power source through resistor; DNI.

** 12 V power needs external supply from pin 8 of J4.

## 5.4. Aardvark Header (DNI)

The Aardvark I²C /SPI Host Adapter is a fast and powerful I²C bus and SPI bus host adapter through USB. It allows a developer to interface a Windows, Linux, or Mac OS X PC through USB to a downstream embedded system environment and transfer serial messages using the I²C and SPI protocols.

The MachXO3-9400 Development Board provides an Aardvark compatible header for customer applications. The I²C bus is capable of connecting to a global I²C bus on the board if JP10 is NOT set.

**Table 5.9. Aardvark JP2 Header Pin Connections**

| JP2 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 1 | JP2_SCL | To I²C analog switch U10 |
| 2 | — | GND |
| 3 | JP2_SDA | To I²C analog switch U11 |
| 4 | +5V_I2C | To VBUS_5V through R78, DNI |
| 5 | SPISO | To MachXO3 U9 |
| 6 | +5V_SPI | To VBUS_5V through R79, DNI |
| 7 | MCLK | To MachXO3 T9 |
| 8 | SISPI | To MachXO3 AA21 |
| 9 | SS | Multiple options, as shown in Figure 5.1. |
| 10 | — | — |

**Caution:** VCCIO2 should be 3.3 V when connected to Aardvark I²C/SPI Host Adapter.

Pin 9 of the Aardvark header is an SS signal, which is optionally connected to multiple devices or connectors. By default, it can access Slave SPI in the MachXO3 device as the Master SPI through R160. It can access FX12 header, Raspberry Pi header and on-board SPI Flash by enabling R161. It can also access the Arduino header by enabling R67.

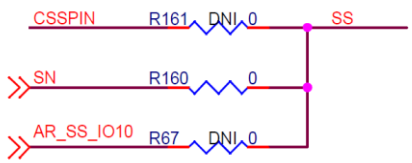


**Figure 5.1. Aardvark SS Pin Connections**

## 5.5. Raspberry Pi Board GPIO Header

The MachXO3-9400 Development Board provides a 40-pin receptacle which is compatible with the GPIO header of Raspberry Pi 2/3 serial models.

**Table 5.10. Raspberry Pi JP3 Header Pin Connections**

| JP3 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 1 | 3.3V_RASP* | — |
| 2 | RASP_5V** | — |
| 3 | RASP_IO02 | T6 |
| 4 | RASP_5V** | — |
| 5 | RASP_IO03 | V1 |
| 6 | GND | — |
| 7 | RASP_IO04 | U2 |
| 8 | RASP_IO14 | P4 |
| 9 | GND | — |
| 10 | RASP_IO15 | N5 |
| 11 | RASP_IO17 | N6 |
| 12 | RASP_IO18 | N7 |
| 13 | RASP_IO27 | P5 |
| 14 | GND | — |
| 15 | RASP_IO22 | P6 |
| 16 | RASP_IO23 | R3 |
| 17 | 3.3V_RASP* | — |
| 18 | RASP_IO24 | R4 |
| 19 | RASP_IO10 | R6 |
| 20 | GND | — |
| 21 | RASP_IO09 | R7 |
| 22 | RASP_IO25 | R5 |
| 23 | RASP_IO11 | T3 |
| 24 | RASP_IO08 | T4 |
| 25 | GND | — |
| 26 | RASP_IO07 | T5 |
| 27 | RASP_ID_SD | V5 |
| 28 | RASP_ID_SC | T7 |
| 29 | RASP_IO05 | U3 |
| 30 | GND | — |
| 31 | RASP_IO06 | U4 |
| 32 | RASP_IO12 | V4 |
| 33 | RASP_IO13 | U5 |
| 34 | GND | — |
| 35 | RASP_IO19 | W3 |
| 36 | RASP_IO16 | W4 |
| 37 | RASP_IO26 | P7 |

**Table 5.10. Raspberry Pi JP3 Header Pin Connections** *(continued)*

| JP3 Pin Number | Signal Name | MachXO3 Ball Location |
|---|---|---|
| 38 | RASP_IO20 | Y2 |
| 39 | GND | — |
| 40 | RASP_IO21 | Y3 |

**Notes:**

* 3.3 V power is supplied from Raspberry Pi board.

** 5 V power can come from either the Raspberry Pi board or the MachXO3-9400 development board when jumper JP7 is installed. When jumper JP7 is not installed, both boards need their own 5 V power.

# 6. I²C and SPI Buses

This section describes the MachXO3-9400 Development Board I²C and SPI topology.

## 6.1. I²C Topology

The MachXO3-9400 Development Board has a flexible I²C bus to support all optional connectors and devices on the board. The global I²C bus has the signal names SDA0 and SCL0 and they are routed close to the devices and headers as shown in Figure 6.1.

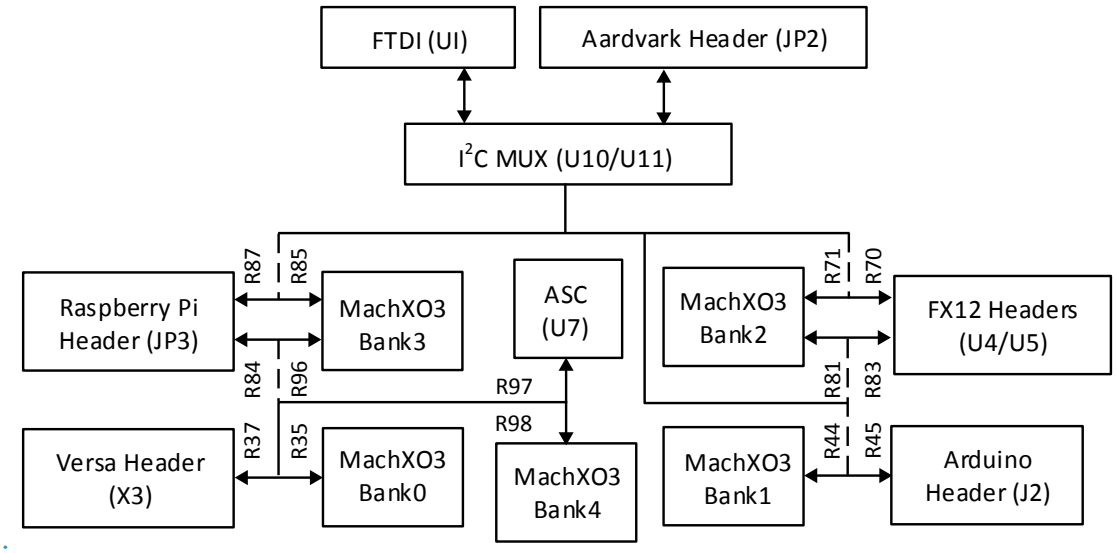


**Figure 6.1. I²C Topology**

The board provides two options for accessing the global I²C bus from external cables. One is from the mini USB cable (J11) through FTDI (U1) and the other is from the Aardvark header (JP2) for an Aardvark cable. Two analog MUXes, as shown in Figure 6.2, are used to select between the USB and Aardvark cables, both MUXes are controlled by the signal USB_I2C_EN.

**Table 6.1. I²C MUX Function**

| Global I²C Controller | USB_I2C_EN Logic Level | FSA4157 MUX Function | SCL0 Test Point | SDA0 Test Point |
|---|---|---|---|---|
| Aardvark Header (JP2) | 0 (JP10 removed) | JP2_SCL <> SCL0<br>JP2_SDA <> SDA0 | Pin1 of JP2 | Pin3 of JP2 |
| USB FTDI (U1) | 1 (JP10 installed) | FTDI_SCL <> SCL0<br>FTDI_SDA <> SDA0 | TP1 | TP2 |

When the jumper JP10 is removed, the USB_I2C_EN signal is low and the Aardvark header JP2 is connected to the global I²C bus. When the jumper JP10 is installed, the USB_I2C_EN signal is high and the USB connector J11 is connected to the global I²C bus through the FTDI device.

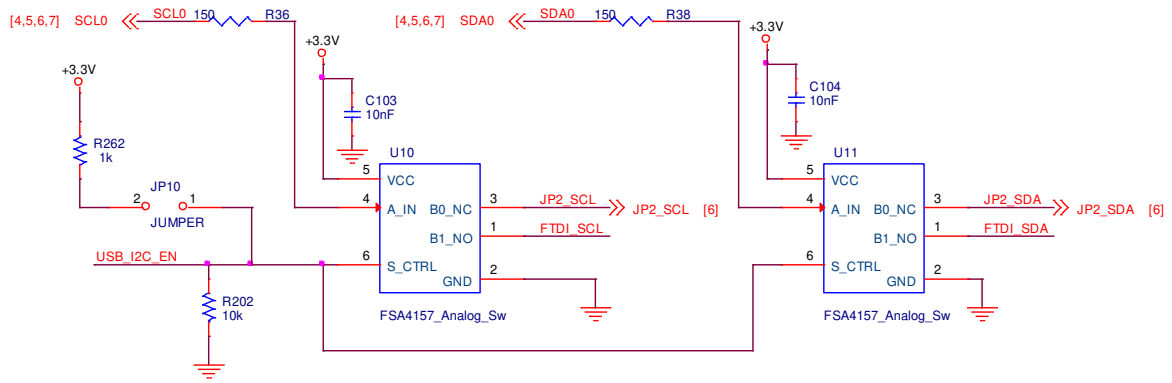


**Figure 6.2. I²C MUX Circuits**

To support a wide variety of I²C applications, each header or device is connected to a dedicated MachXO3 GPIO bank with a direct local I²C bus. Each local I²C bus can optionally connect to the global I²C bus through resistors. The local I²C connections are summarized in Table 6.2.

**Table 6.2. I²C Global Bus Connections**

| MachXO3 Bank | Component (Reference) | Header Pin | MachXO3 Ball | Local Signal Name (Global I²C Signal) | Resistor |
|---|---|---|---|---|---|
| 0 | Versa header (X3) | 18 | A12 | EXPCON_IO15 (SDA0) | R37 (DI)* |
| | | 16 | B12 | EXPCON_IO13 (SCL0) | R35 (DI)* |
| 1 | Arduino header (J2) | 9 | U19 | AR_SDA (SDA0) | R44 (DNI) |
| | | 10 | U18 | AR_SCL (SCL0) | R45 (DNI) |
| 2 | FX12 headers (U4/U5) | 39 | AA11 | SDA1 (SDA0) | R81 (DNI) |
| | | 40 | AB11 | SCL1 (SCL0) | R83 (DNI) |
| | FX12 headers (U4/U5) | 13 | AB13 | SDA2 (SDA0) | R71 (DNI) |
| | | 14 | AA13 | SCL2 (SCL0) | R70 (DNI) |
| 3 | Raspberry Pi header (JP3) | 3 | T6 | RASP_IO02 (SDA0) | R84 (DNI) |
| | | 5 | V1 | RASP_IO03 (SCL0) | R96 (DNI) |
| | | 27 | V5 | RASP_ID_SD (SDA0) | R87 (DNI) |
| | | 28 | T7 | RASP_ID_SC (SCL0) | R85 (DNI) |
| 4 | ASC device (U7) | 14 | K2 | I2C_SDA0 (SDA0) | R97 (DI)* |
| | | 15 | K1 | I2C_SCL0 (SDA0) | R98 (DI)* |

***Note**: The resistor needs to be installed to support programming of the ASC device. Balls K1 and K2 need to be programmed as inputs to support programming of the ASC device. Versa header X3 pins 16 and 18 need to be high-z to support programming of the ASC device. Balls B12 and A12 should be used in Platform Manager designs. Balls K1 and K2 provide a connection for a user instantiated I²C port as part of a separate system to communicate with the ASC device.

## 6.2. SPI Topology

### 6.2.1. SPI Configuration

One of the major functions of SPI connections on the board is to support MachXO3 configuration from SPI ports. The MachXO3-9400 Development Board can support both Master SPI (MSPI) and Slave SPI (SSPI) modes for MachXO3 configuration.

**Table 6.3. MachXO3 SPI Connections**

| Signal Name | MachXO3 Ball Location | MSPI Mode Direction | SSPI Mode Direction |
|---|---|---|---|
| MCLK | T9 | Output | Input |
| SN | AB21 | Input | Input |
| SISPI | AA21 | Output | Input |
| SPISO | U9 | Input | Output |
| CSSPIN | AA3 | Output | Not used |

The MachXO3 can be configured from different ports on the board as listed in Table 6.4. By default, the MachXO3 can boot up from SPI Flash with Master SPI mode.

**Table 6.4. MachXO3 SPI Configuration Options**

| Master SPI Device (Reference) | Master CS (Pin Number of Reference Part) | Slave SPI Device (Reference) | Slave CS (Pin Number of Reference Part) |
|---|---|---|---|
| MachXO3 (U3) | CSSPIN (AA3) | SPI Flash (U6) | CS# (1) |
| MachXO3 (U3) | CSSPIN (AA3) | FX12 (U4, U5) | FX_SN (10) |
| Aardvark (JP2) | SS (9) | MachXO3 (U3) | SN (AB21) |
| Arduino (J2) | AR_SS_IO10 (3) | MachXO3 (U3) | SN (AB21) |
| Raspberry Pi (JP3) | Rasp_IO08 (24) | MachXO3 (U3) | SN (AB21) |

**Note:** Make sure that only one Master SPI and one Slave SPI are working at the same time.

For detailed information on Master SPI and Slave SPI mode configuration, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.

### 6.2.2. SPI Flash Access

Onboard SPI Flash memory can be used to store the MachXO3 configuration data in either External or Dual Boot mode. It can also store customer data in certain applications. The MachXO3 device includes the JTAG to MSPI pass-through circuit that allows the slave SPI Flash to be erased, programmed, and read with Diamond Programmer. For detailed information on JTAG to MSPI pass-through for slave SPI Flash access, refer to TN1279, MachXO3 Programming and Configuration Usage Guide.