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LCP02-150M

Programmable transient voltage suppressor for ringing SLICs

Features

- Protection IC recommended for ringing SLICs
- Wide firing voltage range: from -120 V to + 95 V
- Low gate triggering current
- Peak pulse current: I_{PP} = 100 A (10/1000 µs)
- Holding current: I_H = 150 mA min
- High power dissipation capability
- UL497B approved (file E136224)

Main applications

- Dual battery supply voltage SLICs
  - negative battery supply configuration
  - negative and positive battery supply configuration
- Central Office (CO)
- Private Branch Exchange (PBX)
- Digital Loop Carrier (DLC)
- Asymmetrical Digital Subscriber Line (ADSL)
- Fiber in the Loop (FITL)
- Wireless Local Loop (WLL)
- Hybrid Fiber Coax (HFC)
- ISDN Terminal Adapter
- Cable modem

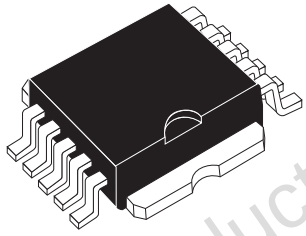
Description

The LCP02-150M has been developed to protect SLICs operating on both negative and positive supplies, as well as on high voltage SLICs. It provides crowbar mode protection for both TIP and RING lines. Surge suppression is assumed for each wire by two thyristor structures, one dedicated to positive surges, the second one to negative surges. Both positive and negative threshold levels are programmable by two gates (Gn and Gp). The use of transistors decreases the battery currents during surge suppression.

The LCP02-150M has high Bellcore Core, ITU-T and FCC Part 68 lightning surge ratings, ensuring rugged performance in the field.

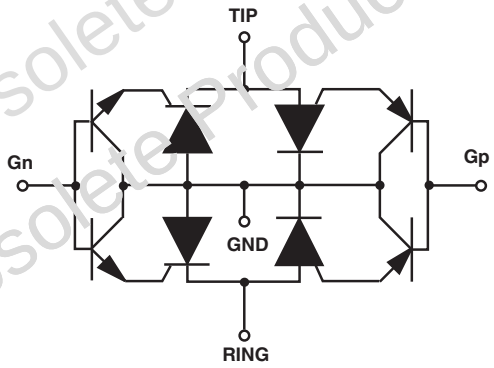
The choice of the PowerSo-10TM package is driven by its high power dissipation capability.

In addition, the LCP02-150M is also specified to assist a designer to comply with UL1950, IEC950 and CSA C22.2. It is UL 497B approved (file E136224), and has UL94-V0 resin approved.

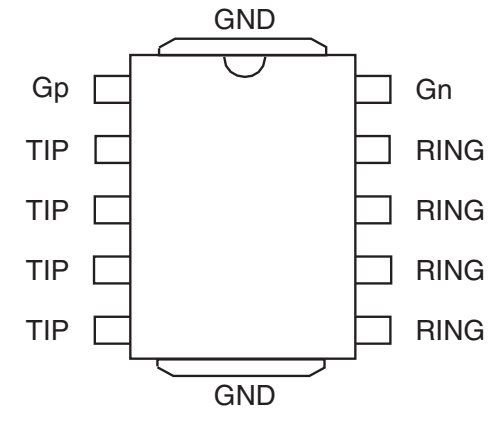


PowerSO-10

Functional diagram



Pin-out configuration



1 Characteristics

Table 1. Complies with the following standards

	Peak surge voltage (V)	Voltage waveform (µs)	Required peak current (A)	Current waveform (µs)	Minimum serial resistor to meet standard (W)
ITU-T K20	6000 1500	10/700 10/700	150 37.5	5/310 5/310	- -
ITU-T K21	6000 1500	10/700 10/700	150 37.5	5/310 5/310	- -
VDE0433	2000	10/700	50	5/310	-
VDE0878	2000	1.2/50	50	1/20	-
IEC61000-4-5	level 4 level 4	10/700 1.2/50	100 100	5/310 8/20	- -
FCC Part 68 lightning surge type A	1500 800	10/160 10/560	200 100	10/160 10/560	- -
FCC Part 68 lightning surge type B	1000	9/720	25	5/320	-
BELLCORE GR-1089-CORE First level	2500 1000	2/10 10/1000	500 100	2/10 10/1000	- -
BELLCORE GR-1089-CORE Second level	5000	2/10	500	2/10	-

Table 2. Absolute ratings (T_{amb} = 25° C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs 10/560 µs 5/310 µs 10/160 µs 1/20 µs 2/10 µs	100 250 120 150 200 250 500	A
I_{TSM}	Non repetitive surge peak on-state current(sinusoidal)	t = 0.2 s t = 1 s t = 15 min	13 10 3.5	A
V_{GN} max V_{GP} maxD V_{bat} max	Maximum negative battery voltage rangeMaximum positivebattery voltage rangeTotal battery supply voltage	See f*Figure 1.*	-120 to 0 0 to + 95 190	V
T_{op}	Operating temperature range (1)		-20 to +85	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_L	Maximum lead temperature for soldering during 10s		260	°C

1. Within the T_{op} range, the LCP02-150M keeps on operating. The impacts of the ambient temperature are given by derating curves.

Figure 1. Test circuit

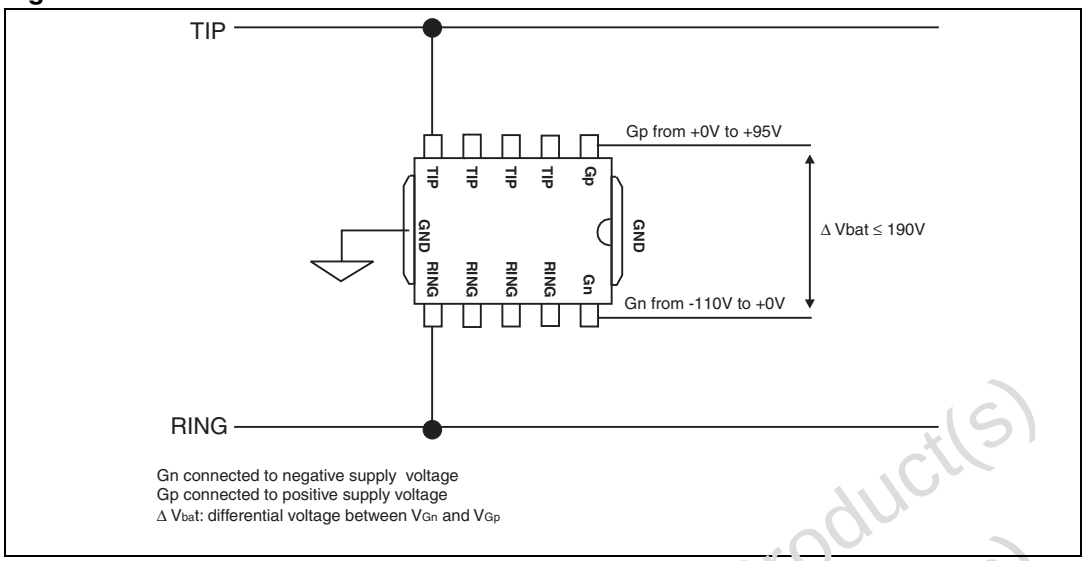


Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction to ambient	60	°C/W

Table 4. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
I_{GP}	Positive gate triggering current
I_{GN}	Negative gate triggering current
I_H	Holding current
I_{RG}	Reverse leakage current GATE / LINE
I_{RM}	Reverse leakage current
V_{RM}	Reverse voltage LINE/ GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{GATE}	GATE / GND voltage
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND

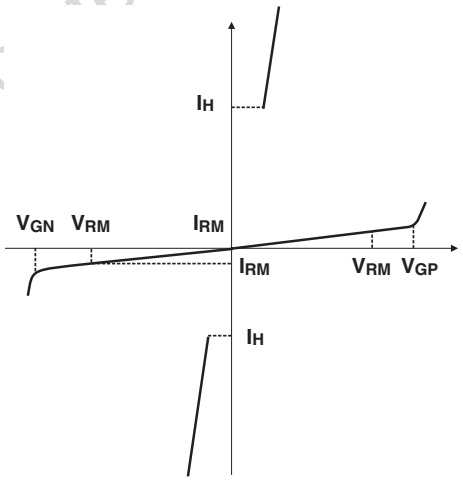


Table 5. Electrical parameters related to the negative suppressor

Symbol	Test conditions	Min.	Max.	Unit
I_{GN}	$V_{GN/GND}$ = -60 V Measured at 50 Hz		5	mA
I_{H-}	Go No-Go test, V_{GN} = -60 V	150		mA
I_{RGL-}	T_j = 25° C, $V_{GN/line}$ = -190 V		5	µA
V_{DGL-}	$V_{GN/GND}$ = -60V 10/1000 µs 1 kV R_P = 25 Ω I_{PP} = 30 A 10/700 µs 2 kV R_P = 25 Ω I_{PP} = 30 A 1.2/50 µs 2 kV R_P = 25 Ω I_{PP} = 30 A		10 6 12	V

Table 6. Electrical parameters related to the positive suppressor

Symbol	Test conditions	Min.	Max.	Unit
I_{GP}	$V_{GP/GND}$ = 60 V Measured at 50 Hz		10	mA
I_{RGL+}	T_j = 25° C, $V_{GP/line}$ = +190 V		5	µA
V_{DGL+}	$V_{GP/GND}$ = +60V 10/1000 µs 1 kV R_P = 25 Ω I_{PP} = 30 A 10/700 µs 2 kV R_P = 25 Ω I_{PP} = 30 A 1.2/50 µs 2 kV R_P = 25 Ω I_{PP} = 30 A		12 8 18	V

Table 7. Electrical parameters related to line/gnd

Symbol	Test conditions	Typ.	Max.	Unit
I_R	T_j = 25° C, V_{LINE} = +90 V, $V_{GP/LINE}$ = +1 V T_j = 25° C, V_{LINE} = -105 V, $V_{GN/LINE}$ = -1 V		5 5	µA
C_{off}	V_R = -2 V, F = 1 MHz, V_{GP} = 60 V, V_{GN} = -60 V	150		pF

Figure 2. Non repetitive surge peak on state current versus overload duration (T_j initial = 25° C)

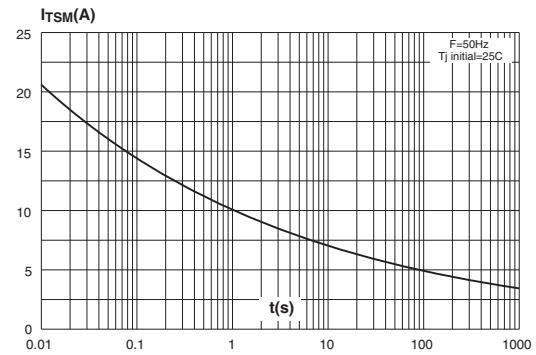


Figure 3. Relative variation of holding current versus junction temperature

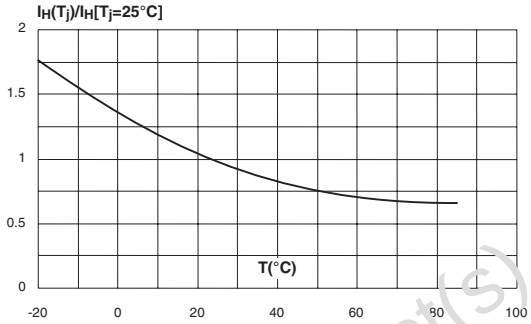
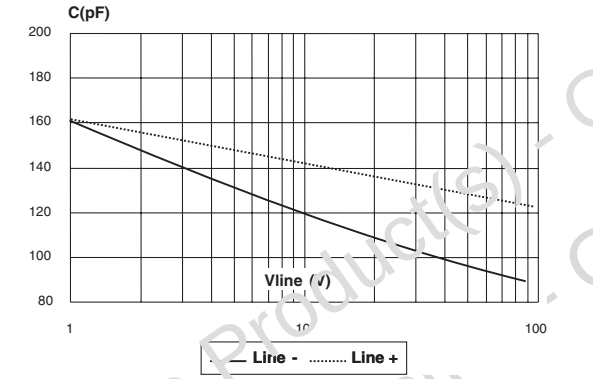


Figure 4. Variation of junction capacitance versus reverse voltage applied (typical calues) with: V_{GN} = -90V and V_{GP} = +90V



2 Technical information

Figure 5. LCP02 concept behavior

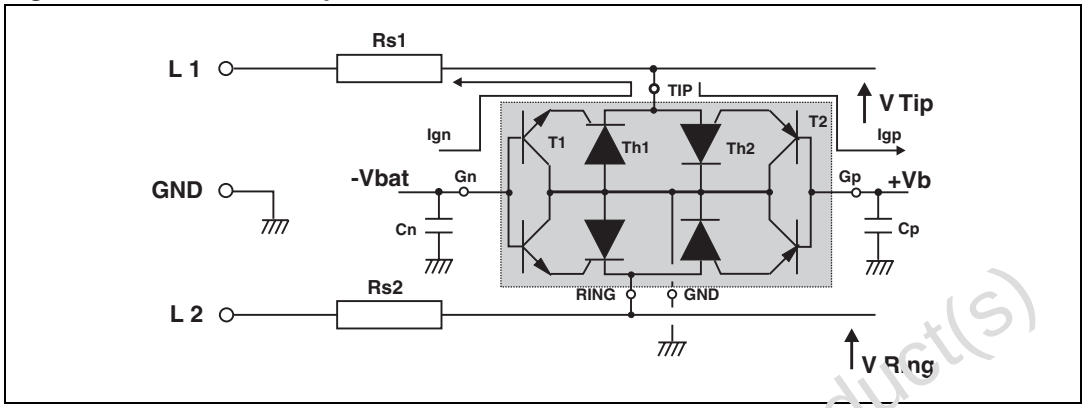


Figure 5. shows the classical protection circuit using the LCP02-150M crowbar concept. This topology has been developped to protect the new two-battery voltage SLICs. It allows both positive and negative firing thresholds to be programmed. The LCP02-150M has two gates (G_N and G_P). Gn is biased to negative battery voltage -Vbat, while G_P is biased to the positive battery voltage +Vb.

When a negative surge occurs on one wire (L1 for example), a current Ign flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1 which fires. The entire surge current flows through the ground. After the surge, when the current flowing through Th1 becomes less negative than the negative holding current, Th1 switches off. This holding current I_{H-} is temperature dependant as per *Figure 2.*

When a positive surge occurs on one wire (L1 for example), a current Igp flows through the base of the transistor T2 and then injects a current in the gate of the thyristor Th2 which fires. The entire surge current flows through the ground. After the surge, when the current flowing through Th2 becomes less positive than the positive holding current I_{H+}, Th2 switches off. This holding current I_{H+} is temperature dependant and is equal to 30 mA at 25° C.

The capacitors C_N and C_P are used to speed up the crowbar structure firing during the fast surge rise or falling edges. This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast surges. Please note that these capacitors are generally available around the SLIC. To be efficient they have to be as close as possible to the LCP02-150M gate pins (G_N and G_P) and to the reference ground track (or plan). The optimized value for C_N and C_P is 220 nF.

The series resistors Rs1 and Rs2 represent the fuse, fuse resistors or the PTCs which are needed to withstand the power contact or the power induction tests imposed by the country standards. Taking this factor into account, the actual lightning surge current flowing through the LCP02-150M is equal to:

I surge = Vsurge / (Rg + Rs)

Where:

Vsurge = peak surge voltage imposed by the standard.

Rg = series resistor of the surge generator

Rs = series resistor of the line card (e.g. PTC)

The LCP02-150M topology is particularly optimized for the new telecom applications such as cable modem, fiber in the loop, WLL systems, and decentralized central office for example. The schematics of *Figure 6.* and *Figure 7.* give the 2 most frequent topologies used for these emergent applications.

Figure 6. Protection of SLIC with positive and negative battery voltages

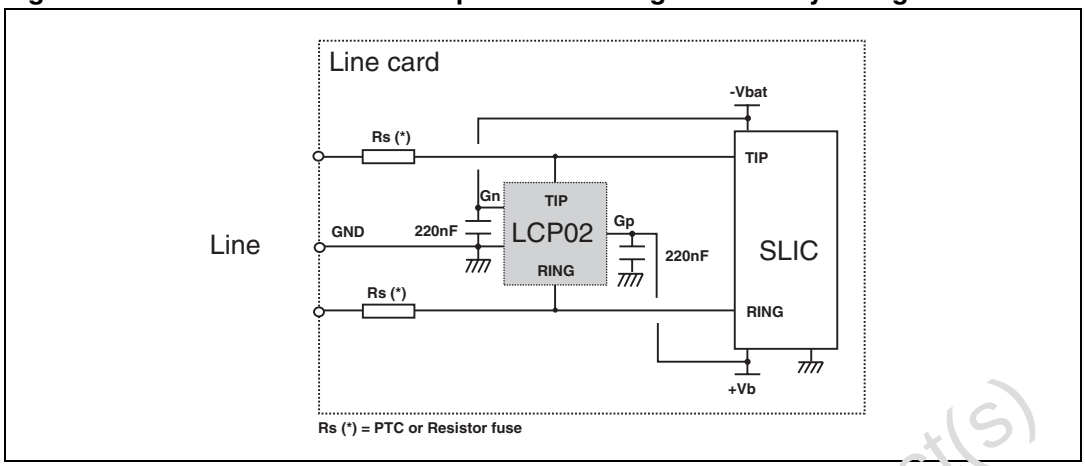


Figure 7. Protection of high voltage SLIC

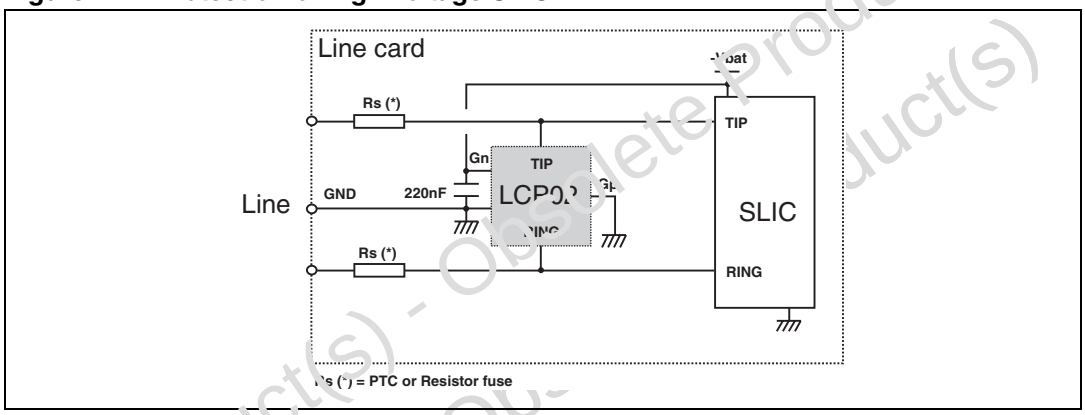
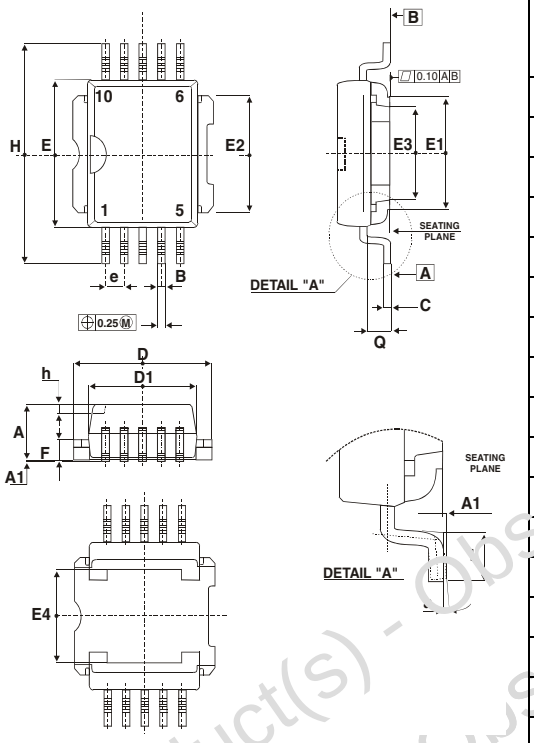


Figure 6. shows the classical protection topology for SLIC using both positive and negative battery voltages. With such a protection the SLIC is protected against surge over +Vb and lower than -Vbat. In this case, +Vb can be programmed up to +95 V while -Vbat can be programmed down to -120 V. Please note that the differential voltage must not exceed -Vbat max at 190V.

Figure 7. gives the protection topology for the new SLIC using high negative voltage down to -120V.

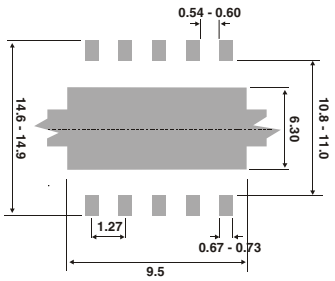
3 Package information

Table 8. PowerSO-10 Dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.35		3.65	0.131		0.143
A1	0.00		0.10	0.00		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.014		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.299
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.299
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.05	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.019	
L	1.20		1.80	0.047		0.071
Q		1.70			0.067	
a	0°		8°	0°		8°

Figure 8. Footprint (dimensions in mm)



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Ordering Type	Marking	Package	Weight	Base qty	Delivery mode
LCP02-150M	LCP02-150M	PowerSO-10	1.02 g	50	Tube
LCP02-150M-TR				600	Tape and Reel

5 Revision history

Date	Revision	Changes
May-2003	4B	Previous release
31-Oct-2006	5	Reformatted to current standards. Negative firing voltage and maximum negative battery voltage changed from -110 V to -120 V throughout the document.

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