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LE25S161

# Serial Flash Memory
16 Mb (2048K x 8)

ON Semiconductor®

1. Overview

The LE25S161 is a SPI bus flash memory device with a 16M bit (2048K × 8-bit) configuration. It uses a single power supply. While making the most of the features inherent to a serial flash memory device, the LE25S161 is housed in an 8-pin ultra-miniature package. All these features make this device ideally suited to storing program in applications such as portable information devices, which are required to have increasingly more compact dimensions.
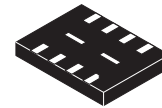
The LE25S161 also has a small sector erase capability which makes the device ideal for storing parameters or data that have fewer rewrite cycles and conventional EEPROMs cannot handle due to insufficient capacity.
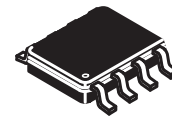
SOIC 8, 150mils
VSOIC8 NB
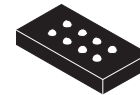
WLCSP8, 2.92x1.53

UDFN8 4x3, 0.8P

2. Features

- Operations power supply : 1.65 to 1.95V supply voltage range
- Operating frequency : 70MHz (max)
- Temperature range : –40 to +90°C
- Serial interface : SPI mode 0, mode 3 supported
- Electronic Identification : JDEC ID, Device ID, Serial Flash Discoverable Parameter (SFDP)
- Sector size : 4K bytes/small sector, 64K bytes/sector
- Erase functions : small sector erase (SSE), sector erase (SE), chip erase (CHE)
- Page program function : 256 bytes/page
- Status functions : Ready/Busy information, protect information
- Low operation current : 5.0mA (Low-power program mode, typ), 3.5mA (Low-Power Read mode, typ)
- Erase time : 10ms (SSE, typ), 15ms (SE, typ), 210ms (CHE, typ)
- Page program time (t_{PP}) : 0.4ms/256 bytes (typ.), 0.7ms/256 bytes (max.)
- Emergency shutdown of the current consumption
  : transition to a standby state in less than 20μs from the active by Write Suspend
  : transition to a standby state in less than 40μs from the active by Software Reset
- High reliability : 100,000 erase/program cycles
  : 20 years data retention period
- Package : LE25S161MDTWG SOIC 8, 150 mils   CASE 751BD
  : LE25S161FDTWG   VSOIC8 NB   CASE 753AA
  : LE25S161XATAG WLCSP8, 2.92×1.53   CASE 567LC
  : LE25S161PCTXG UDFN8 4×3, 0.8P   CASE 506DC
  : KGD   N/A

* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION

See detailed ordering and shipping information on page 54 of this data sheet.

3. Package Types and Pin Configurations

$\overline{CS}$ 1 — 8 V_{DD}
SO (SIO1) 2 — 7 $\overline{HOLD}$
$\overline{WP}$ 3 — 6 SCK
V_{SS} 4 — 5 SI (SIO0)

Top view

SOIC8 (LE25S161MDTWG)
VSOIC8 NB (LE25S161FDTWG)

$\overline{CS}$ 1 — 8 V_{DD}
SO (SIO1) 2 — 7 $\overline{HOLD}$
$\overline{WP}$ 3 — 6 SCK
V_{SS} 4 — 5 SI (SIO0)

Top view

UDFN8 (LE25S161PCTXG)
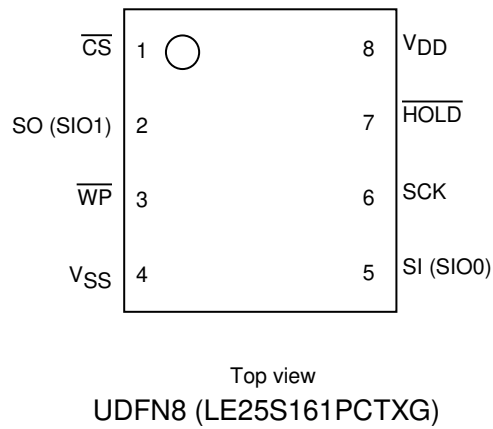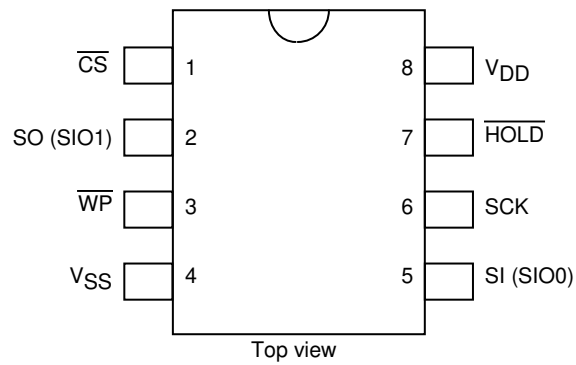
LE25S161

Top View WLCSP8 (LE25S161XATAG)		
	1	**2**
A	VDD	$\overline{CS}$
B	$\overline{HOLD}$	SO/SIO1
C	SCK	$\overline{WP}$
D	SI/SIO0	VSS
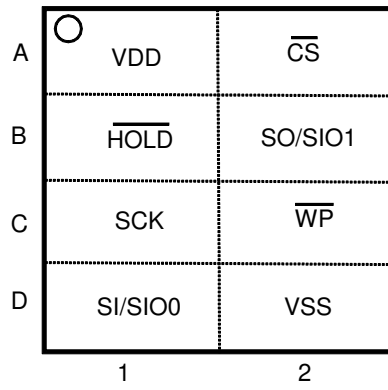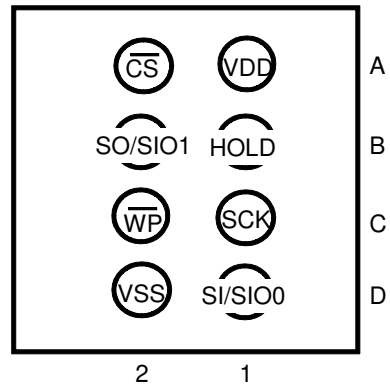
Ball side View WLCSP8 (LE25S161XATAG)		
	2	**1**
A	$\overline{CS}$	VDD
B	SO/SIO1	HOLD
C	$\overline{WP}$	SCK
D	VSS	SI/SIO0

KGD
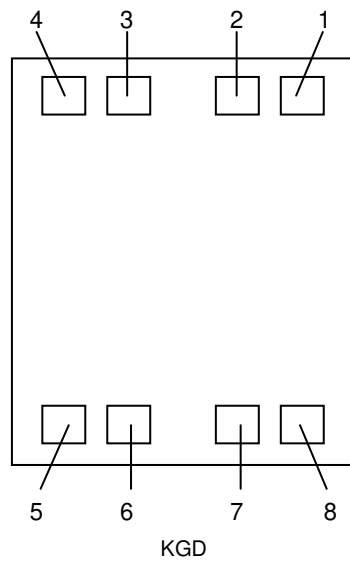
Pad No.	Name
1	$\overline{CS}$
2	SO (SIO1)
3	$\overline{WP}$
4	V_{SS}
5	SI (SIO0)
6	SCK
7	$\overline{HOLD}$
8	V_{DD}

LE25S161

4. Package Dimensions

unit : mm

LE25S161MDTWG

SOIC 8, 150 mils
CASE 751BD-01
ISSUE O
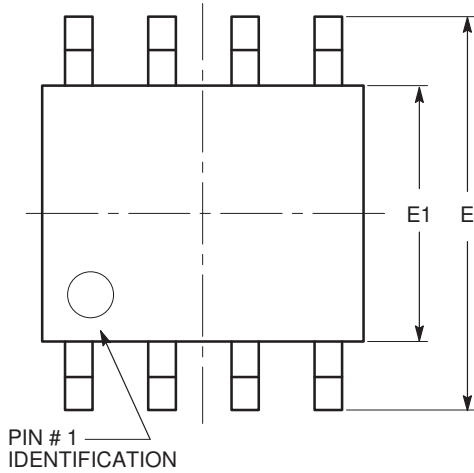
SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º

PIN # 1
IDENTIFICATION

TOP VIEW
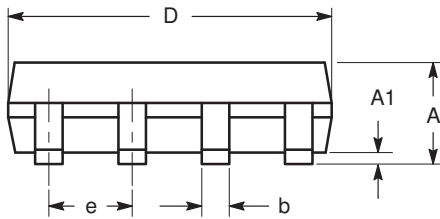
SIDE VIEW
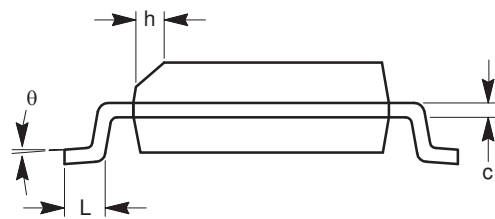
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Package Dimensions

unit : mm

LE25S161FDTWG

VSOIC8 NB
CASE 753AA
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
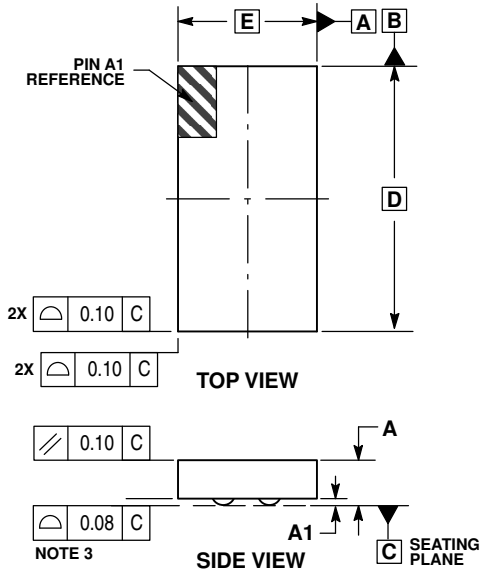6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	0.65	0.85
A1	---	0.05
b	0.31	0.51
c	0.17	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

TOP VIEW

SIDE VIEW

DETAIL A

END VIEW

RECOMMENDED SOLDERING FOOTPRINT*

8X 1.52

7.00

8X 0.60

1.27 PITCH

DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXXXXX
ALYWX■

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

Package Dimensions

unit : mm

LE25S161XATAG

WLCSP8, 2.92x1.53
CASE 567LC
ISSUE A

TOP VIEW

2X | △ | 0.10 | C

2X | △ | 0.10 | C

SIDE VIEW

// | 0.10 | C

△ | 0.08 | C

NOTE 3

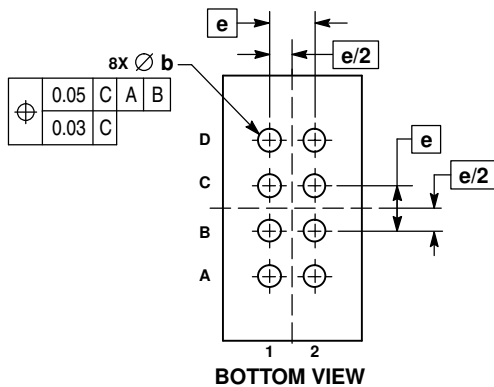C SEATING PLANE
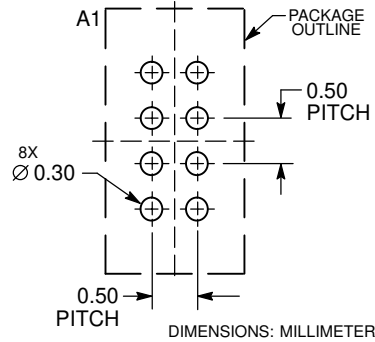
BOTTOM VIEW

8X Ø b

⊕ | 0.05 | C | A | B

| 0.03 | C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	—	0.50
A1	0.03	0.13
b	0.25	0.35
D	2.92 BSC	
E	1.53 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

A1

PACKAGE OUTLINE

0.50 PITCH

8X Ø 0.30

0.50 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
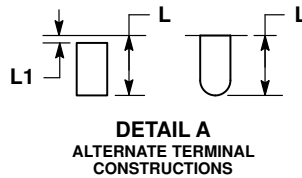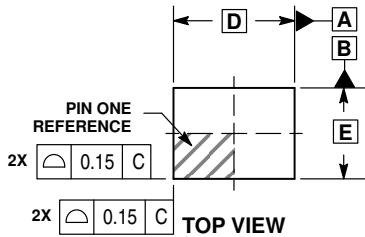
Package Dimensions

unit : mm

LE25S161PCTXG

UDFN8, 4x3, 0.8P
CASE 506DC
ISSUE O

TOP VIEW

PIN ONE REFERENCE

2X ⌒ 0.15 C

2X ⌒ 0.15 C

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

SIDE VIEW

⫽ 0.10 C

DETAIL B

10X ⌒ 0.08 C

NOTE 4

(A3)

A1

C SEATING PLANE

DETAIL B
ALTERNATE CONSTRUCTIONS

EXPOSED Cu   MOLD CMPD

BOTTOM VIEW

DETAIL A

2X D2

⊕ 0.10 Ⓜ C A B

2X E2

⊕ 0.10 Ⓜ C A B

8X L

8X b

⊕ 0.10 Ⓜ C A B
0.05 Ⓜ C NOTE 3

e

e/2

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
A3	0.152 REF	
b	0.25	0.35
D	4.00 BSC	
D2	0.70	0.90
E	3.00 BSC	
E2	0.10	0.30
e	0.80 BSC	
G	1.60 BSC	
L	0.55	0.65
L1	---	0.15

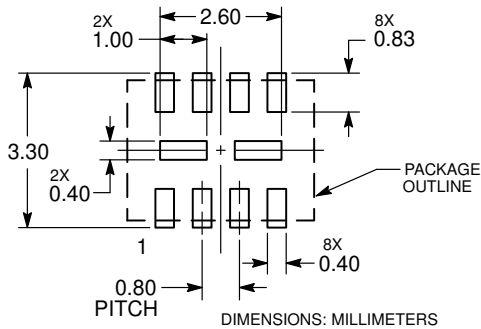**GENERIC MARKING DIAGRAM***

```
○  XXXXX
   XXXXX
   AYWW▪
        ▪
```
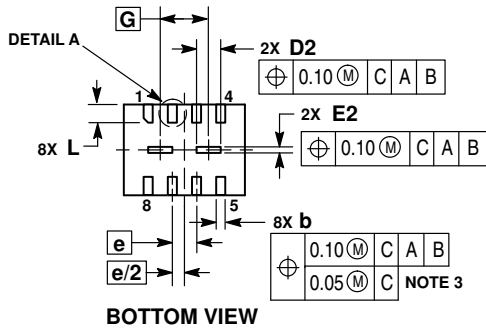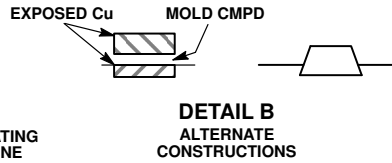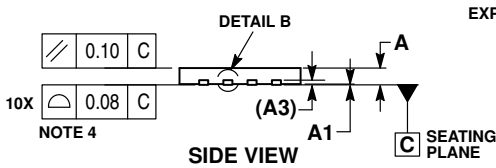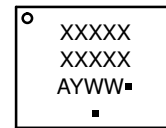
XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ▪ ", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*

2X 1.00   2.60   8X 0.83

3.30

2X 0.40

PACKAGE OUTLINE

1   8X 0.40

0.80 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

5. Pin Description

| Symbol	Pin Name	IO	Description
$\overline{CS}$	Chip select	I	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
SCK	Serial clock	I	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI (SIO0)	Serial data input (Serial data input output)	I/O	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock. (It changes into input/output pin during the Dual operation.)
SO (SIO1)	Serial data output (Serial data input output)	I/O	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock. (It changes into input/output pin during the Dual operation.)
$\overline{WP}$	Write protect	I	The Write Status Register Protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{HOLD}$	Hold	I	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power supply		This pin supplies the 1.65 to 1.95V supply voltage.
V_{SS}	Ground		This pin supplies the 0V supply voltage.

6. Block Diagram
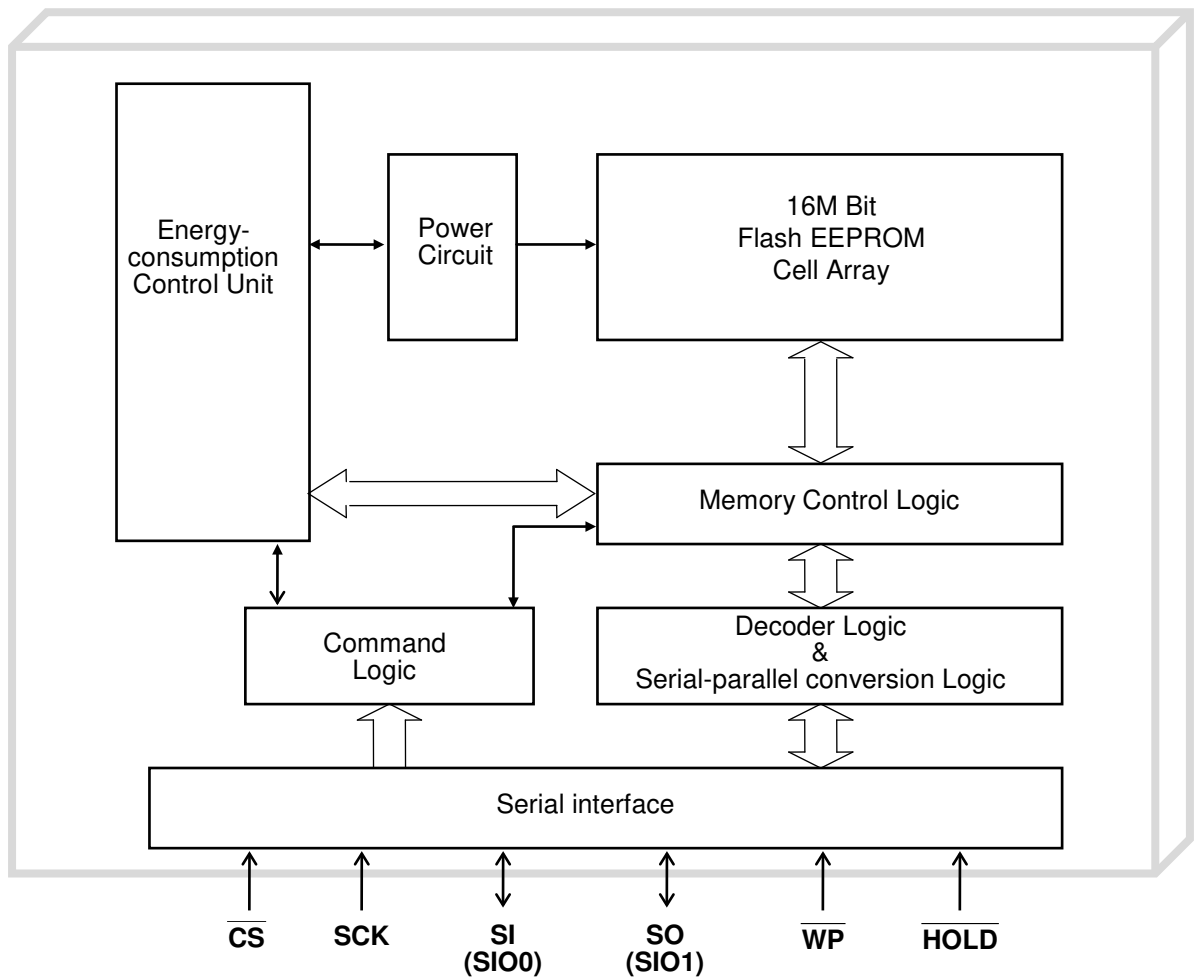
7. Device Operation

7-1. Standard SPI Modes

The read, erase, program and other required functions of the device are executed through the command registers. The serial I/O corrugate is shown in "Figure 1. SPI Modes" and the command list are shown in "Table.1-1. Command Settings (Standard SPI)". At the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are normalized in 8 bit units and taken into the device interior in synchronization with the rising edge of SCK, which causes the device to execute operation according to the command that is input.

The LE25S161 supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 1. SPI Modes
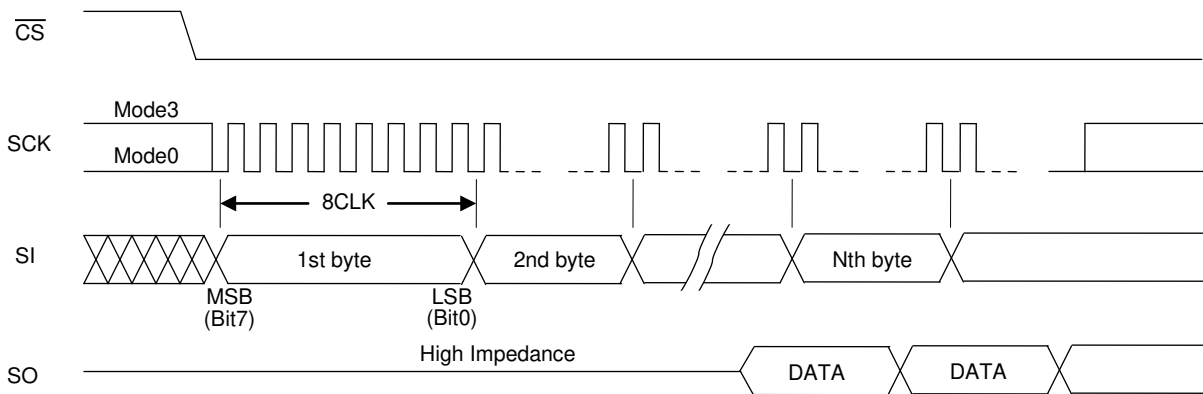
7-2. Dual SPI Modes

The LE25S161 supports Dual SPI operations when using "Dual Output Read (RDDO: 3Bh)", "Dual I/O Read (RDIO: BBh)". The SI and SO pins change into the input/output pin (SIOx) during the Dual SPI modes. The command list is shown in "Table.1-2. Command Settings (Dual SPI)".

Pin Configurations at Dual SPI Mode

Standard SPI		Dual SPI
SI	→	SIO0
SO	→	SIO1

LE25S161

Table 1-1. Command Settings (Standard SPI) --- Max: 70MHz (except RDLP)

Command	Description (clock number)	1st byte (0 - 7)	2nd byte (8 - 15)	3rd byte (16- 23)	4th byte (24 - 31)	5th byte (32 - 39)	6th byte (40 - 47)	Nth byte (8N-8 to 8N-1)
WREN	Write enable	06h						
WRDI	Write disable	04h						
RDSR	Read Status Register	05h						
WRSR	Write Status Register	01h	DATA					
RDLP	Low -Power Read (Max: 33.33MHz)	03h	A23-A16	A15-A8	A7-A0	RD [5]	RD [5]	RD [5]
RDHS	High-Speed Read	0Bh	A23-A16	A15-A8	A7-A0	X	RD [5]	RD [5]
SSE	Small Sector Erase (4KB)	20h / D7h	A23-A16	A15-A8	A7-A0			
SE	Sector Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
CHE	Chip Erase (16M bits)	60h / C7h						
PP	Normal Page Program	02h	A23-A16	A15-A8	A7-A0	PD [7]	PD [7]	PD [7]
PPL	Low-Power Page Program	0Ah						
WSUS	Write Suspend	B0h						
RESM	Resume	30h						
RJID	Read JEDEC ID	9Fh	Manufacture (62h)	Memory Type (16h)	Capacity (15h)			
RID	Read Device ID (Exit power down mode)	ABh	X	X	X	Device ID (88h)		
RSFDP	Read SFDP	5Ah	A23-A16	A15-A8	A7-A0	X	RD [5]	RD [5]
DP	Deep Power down	B9h						
EDP	Exit Deep Power down	ABh						
RSTEN	Reset Enable	66h						
RST	Reset	99h						

Table 1-2. Command Settings (Dual SPI) --- Max: 50MHz

Command	Description (clock number)	1st byte (0 - 7)	2nd byte (8 - 15)	3rd byte (16- 23)	4th byte (24 - 31)	5th byte (32 - 39)	6th byte (40 - 47)	Nth byte (8N-8 to 8N-1)
RDDO	Dual Output Read	3Bh	A23-A16	A15-A8	A7-A0	Z	RDD [6]	RDD [6]
RDIO	Dual I/O Read	BBh	A23-A8 [8]	A7-A0 [8], X, Z	RDD [6]	RDD [6]	RDD [6]	RDD [6]

Note:

1. "X" signifies "don't care" (that is to say, any value may be input).
2. "Z" signifies "high-impedance".
3. The "h" following each code indicates that the number given is in hexadecimal notation.
4. Addresses A23 to A21 for all commands are "Don't care".
5. "RD"   Read data on SO.
6. "RDD"   Dual Read data:

    SIO0=(Bit6, Bit4, Bit2, Bit0)
    SIO1=(Bit7, Bit5, Bit3, Bit1)

7. "PD"   Page Program data on SO.
8. Dual SPI address input from SIO0 and SIO1:

    SIO0=(A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0)
    SIO1=(A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1)

8. Memory Organization

Table 2. Memory Organization

16M bits

Sector (64KB) Symbol :SE	small sector (4KB) Symbol :SSE	address space (A23 to A0)	
31	SSE[511]	1FF000h	1FFFFFh
	to		
	SSE[496]	1F0000h	1F0FFFh
30 to 6	SSE[495]	1EF000h	1EFFFFh
	to		
	SSE[96]	060000h	060FFFh
5	SSE[95]	05F000h	05FFFFh
	to		
	SSE[80]	050000h	050FFFh
4	SSE[79]	04F000h	04FFFFh
	to		
	SSE[64]	040000h	040FFFh
3	SSE[63]	03F000h	03FFFFh
	to		
	SSE[48]	030000h	030FFFh
2	SSE[47]	02F000h	02FFFFh
	to		
	SSE[32]	020000h	020FFFh
1	SSE[31]	01F000h	01FFFFh
	to		
	SSE[16]	010000h	010FFFh
0	SSE[15]	00F000h	00FFFFh
	to		
	SSE[4]	004000h	004FFFh
	SSE[3]	003800h	003FFFh
		003000h	0037FFh
	SSE[2]	002800h	002FFFh
		002000h	0027FFh
	SSE[1]	001800h	001FFFh
		001000h	0017FFh
	SSE[0]	000800h	000FFFh
		000000h	0007FFh

9. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read by Read Status Register (RDSR) and the protect information can be rewritten by Write Status Register (WRSR). There are 8 bits in total, and "Table 3. Status registers" gives the significance of each bit.

Table 3. Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{RDY}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0		Nonvolatile information
		1		
Bit3	BP1	0	Block protect information	
		1	Protected area switch	
Bit4	BP2	0		
		1		
Bit5	TB	0	Block protect	Nonvolatile information
		1	Upper side/Lower side switch	
Bit6	SUS	0	Erase/Program is not suspended	0
		1	Erase/Program suspended	
Bit7	SRWP	0	Write Status Register enabled	Nonvolatile information
		1	Write Status Register disabled	

Note: All non-volatile bits of the status registers-1 are set "0" in the factory.

9-1. Contents of each status register

9-1-1. $\overline{\text{RDY}}$ (bit 0)

The $\overline{\text{RDY}}$ register is for detecting the write (Program, Erase and Write Status Register) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

9-1-2. WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.

WEN can be controlled using the write enable (WREN) and write disable (WRDI). By inputting the write enable (WREN: 06h), WEN can be set to "1" by inputting the write disable (WRDI: 04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.
- At power-on
- Upon completion of Erase (SSE, SE, or CHE)
- Upon completion of Page Program (PP or PPL)
- Upon completion of Write Status Register (WRSR)

* If a write operation has not been performed inside the LE25S161 because, for instance, the command input for any of the write operations (SSE, SE, CHE, PP, PPL or WRSR) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

9-1-3. BP0, BP1, BP2, TB (bits 2, 3, 4, 5)

Block Protect: BP0, BP1, BP2 and TB are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 4. Protected Level Setting Conditions".
BP0, BP1, and BP2 are used to select the protected area and TB to allocate the protected area to the higher-order address area or lower-order address area.

Table 4. Protection Level Setting Conditions

Protected Level	Protected Block	Status Register Bits				Protected Area
		TB	BP2	BP1	BP0	
0	Whole area unprotected	X	0	0	0	None
T1	Upper side 1/32 protected	0	0	0	1	1F0000h to 1FFFFFh
T2	Upper side 1/16 protected	0	0	1	0	1E0000h to 1FFFFFh
T3	Upper side 1/8 protected	0	0	1	1	1C0000h to 1FFFFFh
T4	Upper side 1/4 protected	0	1	0	0	180000h to 1FFFFFh
T5	Upper side 1/2 protected	0	1	0	1	100000h to 1FFFFFh
B1	Lower side 1/32 protected	1	0	0	1	000000h to 00FFFFh
B2	Lower side 1/16 protected	1	0	1	0	000000h to 01FFFFh
B3	Lower side 1/8 protected	1	0	1	1	000000h to 03FFFFh
B4	Lower side 1/4 protected	1	1	0	0	000000h to 07FFFFh
B5	Lower side 1/2 protected	1	1	0	1	000000h to 0FFFFFh
6	Whole area protected	X	1	1	X	000000h to 1FFFFFh

Note: Chip Erase is enabled only when the protection level is 0.

9-1-4. SUS (bit 6)

The SUS register indicates when Erase/Program operation has been suspended. The SUS becomes "1" when the Erase/Program operation has been suspended (WSUS: B0h). The SUS is cleared to"0" by Resume (RESM:30h) or re-erase/program (SSE, SE, CHE, PP, PPL).

9-1-5. SRWP (bit 7)

Write Status Register protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the $\overline{WP}$ pin is low, the Write Status Register (WRSR: 01h) is ignored, and status registers BP0, BP1, BP2, TB and SRWP are protected. When the logic level of the $\overline{WP}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 5. SRWP Setting Conditions".

Table 5. SRWP Setting Conditions

$\overline{WP}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

10. Description of Commands and Operations

A detailed description of the functions and operations corresponding to each command is presented below.

10-1. Read Status Register (RDSR)

The contents of the status registers can be read using the Read Status Register (RDSR). This command can be executed even during the following operations.

- Erase (SSE, SE or CHE)
- Page Program (PP or PPL)
- Write Status Register (WRSR)

"Figure 2. Read Status Register (RDSR)" shows the timing waveforms.

> The sequence of RDSR operation :
> $\overline{CS}$ goes to low → input RDSR command (05h)
> → Status Register data (SRWP, SUS, TB, BP2, BP1, BP0,WEN, $\overline{RDY}$) out on SO →→
> →completed by $\overline{CS}$=high
>
> * The data output starts from the falling edge of SCK(7th clock)

This command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK).
If the clock input is continued after bit0 ($\overline{RDY}$) has been output, the data is output by returning to bit7 (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by this command at any time (even during a program, erase cycle). By setting $\overline{CS}$ to high, the device is deselected, and Read JEDEC ID cycle is completed. While the device is deselected, the output pin SO is in a high-impedance state

Figure 2. Read Status Register (RDSR)
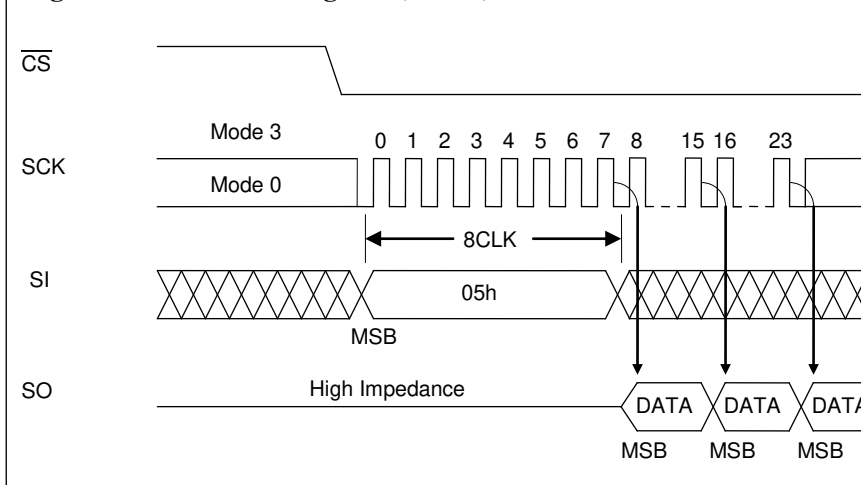
● DATA: Status Resister, "Table 3 Status Register"

10-2. Write Status Register (WRSR)

The information in status registers BP0, BP1, BP2, TB and SRWP can be rewritten using this command. bit0 ($\overline{\text{RDY}}$), bit1 (WEN) and bit6 (SUS) are read-only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, TB and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down.

"Figure 3. Write Status Register (WRSR)" shows the timing waveforms.
"Figure 31. Write Status Register Flowcharts" shows the flowcharts.

> The sequence of WRSR operation :
> $\overline{\text{CS}}$ goes to low → input WRSR command (01h)
> → Status Register data input on SI
> → $\overline{\text{CS}}$ goes to high (be executed by the rising $\overline{\text{CS}}$ edge)

Erase and program are performed automatically inside the device by Write Status Register. So that erasing or other processing is unnecessary before executing the command. By the operation of this command, the information in bits BP0, BP1, BP2, TB and SRWP can be rewritten. Since bits bit0 ($\overline{\text{RDY}}$), bit1 (WEN), bit 6 (SUS) of the status register cannot be written, no problem will arise if an attempt is made to set them to any value when rewriting the status register. Write Status Register ends can be detected by $\overline{\text{RDY}}$ of Read Status Register (RDSR). To initiate Write Status Register, the logic level of the $\overline{\text{WP}}$ pin must be set high and status register WEN must be set to "1".

Figure 3. Write Status Register (WRSR)
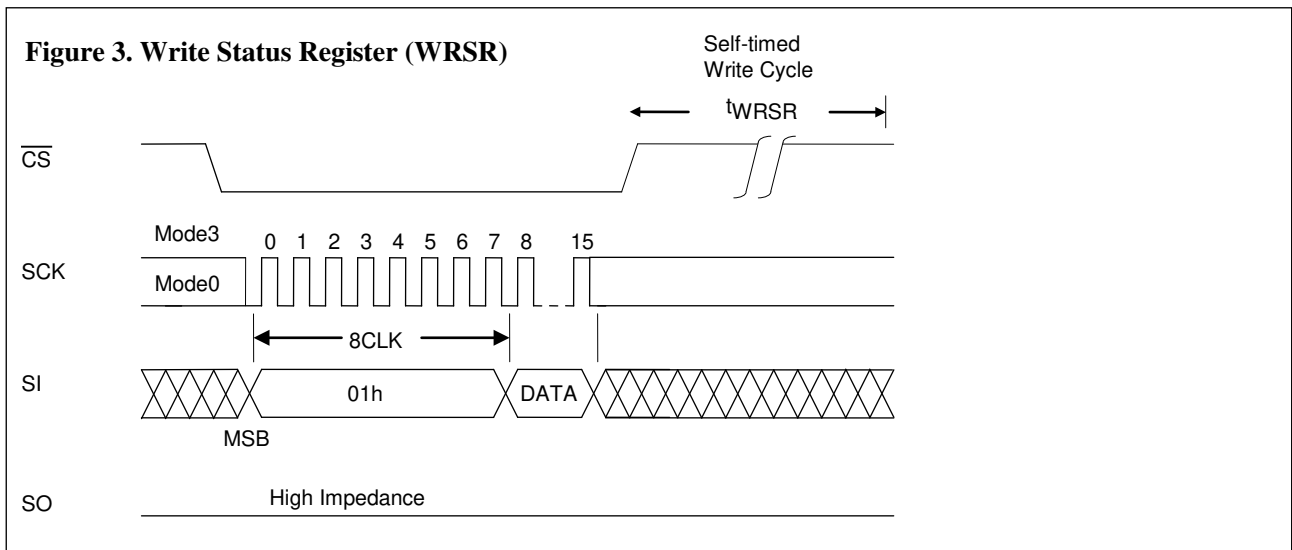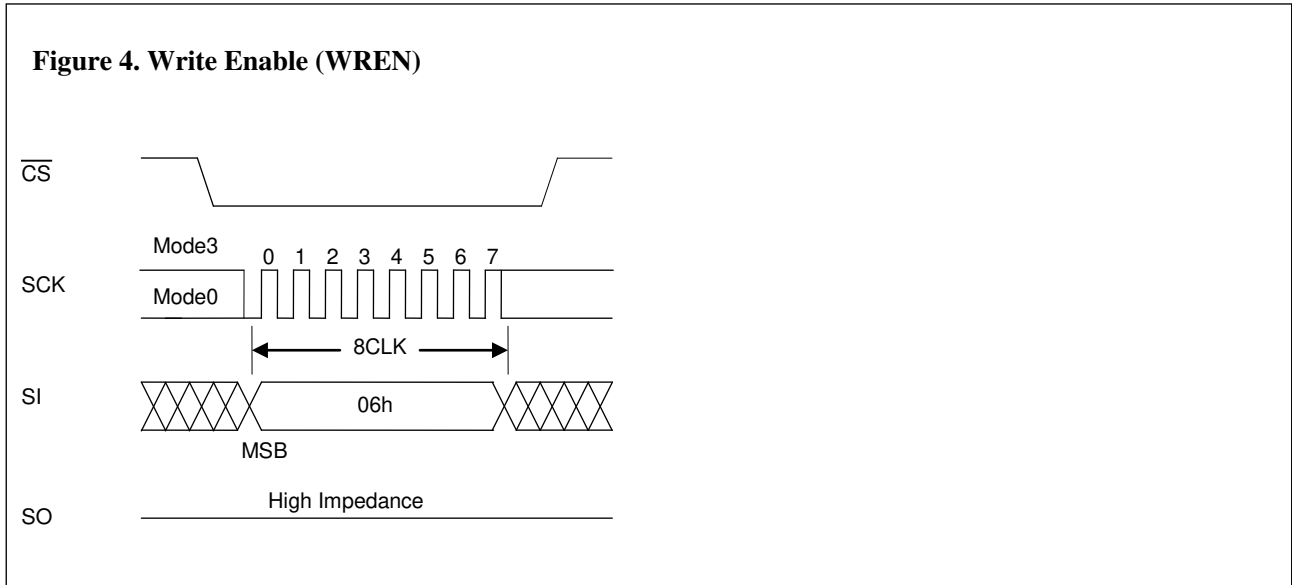
10-3. Write Enable (WREN)

Before performing any of the operations listed below, the device must be placed in the write enable state.

- Erase (SSE, SE, CHE or CHE)
- Page Program (PP or PPL)
- Write Status Register (WRSR)

Operation is the same as for setting status register WEN to "1", and the state is enabled by this command.

"Figure 4. Write Enable (WREN)" shows the timing waveforms.

The sequence of WREN operation :
$\overline{CS}$ goes to low → input WREN command (06h)
→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)


Figure 4. Write Enable (WREN)

10-4. Write Disable (WRDI)

This command sets status register WEN to "0" to prohibit unintentional writing. The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable (WREN: 06h).

"Figure 5. Write Disable (WRDI)" shows the timing waveforms.

The sequence of WRDI operation :
$\overline{CS}$ goes to low → input WRDI command (04h)
→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

Figure 5. Write Disable (WRDI)
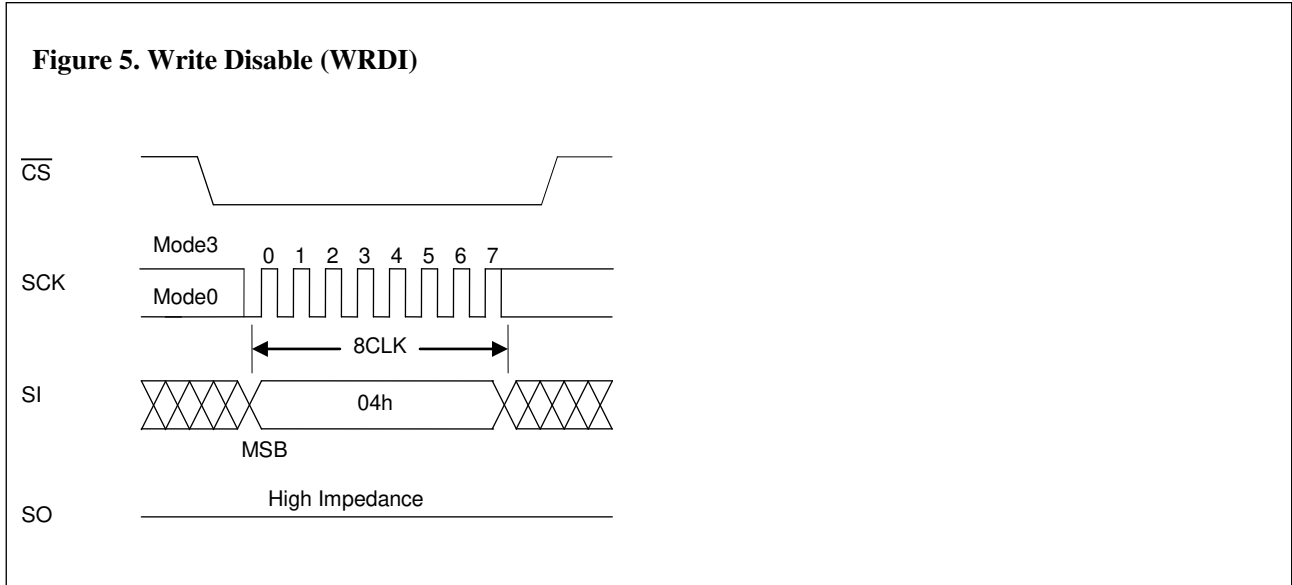
Standard SPI Read

There are two Read commands, "Low-Power Read (RDLP: 03h)" and "High-Speed Read (RDHS: 0Bh)".

10-5. Standard SPI Read

There are two Read commands, Low-Power Read (RDLP) and High-Speed Read (RDHS).

10-5-1. Low-Power Read command (RDLP) _____ Maximum Clock frequency: 33.33MHz
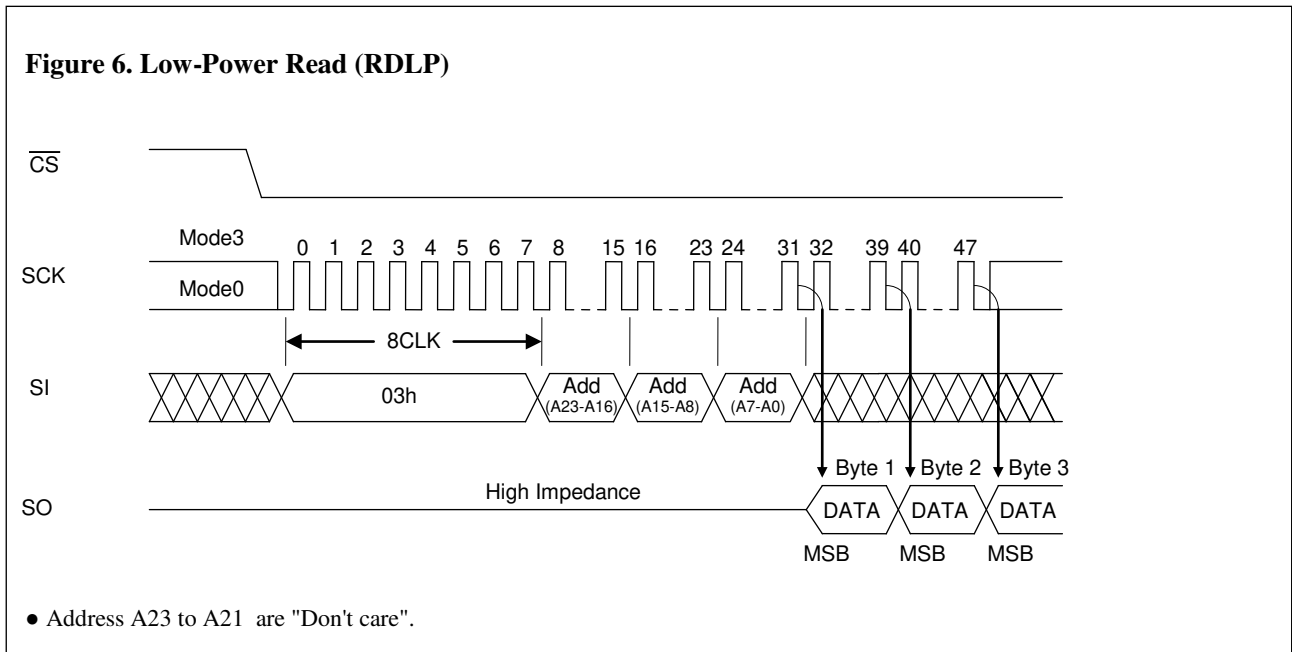
This command is for reading data out.

"Figure 6. Low-Power Read (RDLP)" shows the timing waveforms.

The sequence of RDLP operation :
$\overline{CS}$ goes to low → input RDLP command (03h) → 3 Byte address (A23-A0) input on SI
→ the corresponding data out on SO
→ continuous data out (n-byte) →→
→ completed by $\overline{CS}$=high

* The data output starts from the falling edge of SCK(31th clock)

The Address is latched on rising edge of SCK, and the corresponding data is shifted out on SO by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 6. Low-Power Read (RDLP)

● Address A23 to A21 are "Don't care".

10-5-2. High-Speed Read command (RDHS) _____ Maximum Clock frequency: 70MHz

This command is for reading data out at the high frequency operation.

"Figure 7. High-Speed Read (RDHS)" shows the timing waveforms.

The sequence of RDHS operation :
$\overline{CS}$ goes to low → input RDHS command (0Bh) → 3 Byte address (A23-A0) input on SI
→ 1 byte dummy cycle → the corresponding data out on SO
→ continuous data out (n-byte) →→
→ completed by $\overline{CS}$=high

* The data output starts from the falling edge of SCK(39th clock)

The Address is latched on rising edge of SCK. It is necessary to add 1 dummy byte cycle after address is latched, and the corresponding data is shifted out on SO by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 7. High-Speed Read (RDHS)
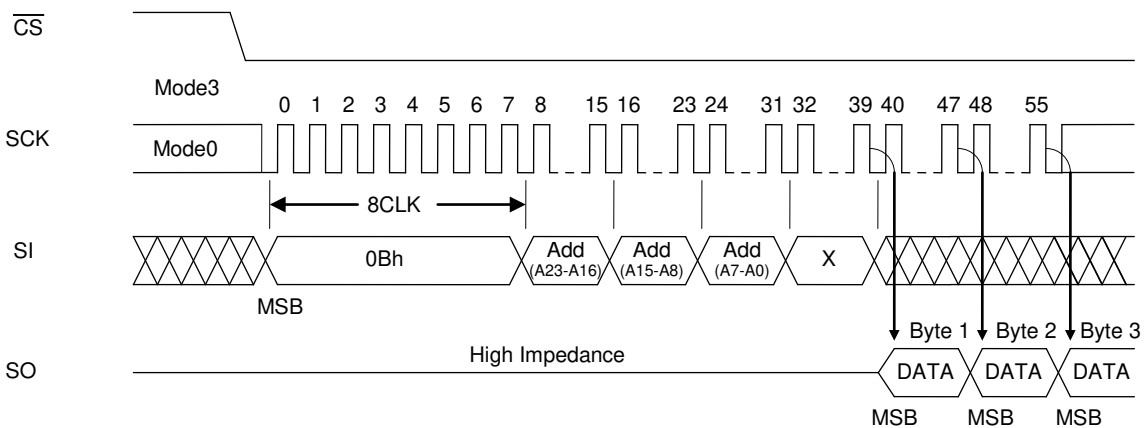
● Address A23 to A21 are "Don't care".

10-6. Dual read

There are two Dual read commands, the Dual Output Read (RDDO) and the Dual I/O Read (RDIO).
They achieve the twice speed-up from "High-Speed Read (RDHS: 0Bh)". The command list is shown in "Table.1-2.
Command Settings (Dual SPI)"

Pin Configurations at Dual SPI Mode

Standard SPI		Dual SPI
SI	→	SIO0
SO	→	SIO1

10-6-1. Dual Output Read command (RDDO)‾‾‾‾‾ Maximum Clock frequency: 50MHz

The SI and SO pins change into the input/output pin (SIOx) during this operation. It makes the data output x2 bit and has achieved a high-speed output. bit7, 5, 3 and bit1are output from SIO0. bit6, 4, 2 and bit0 are output from SIO1.

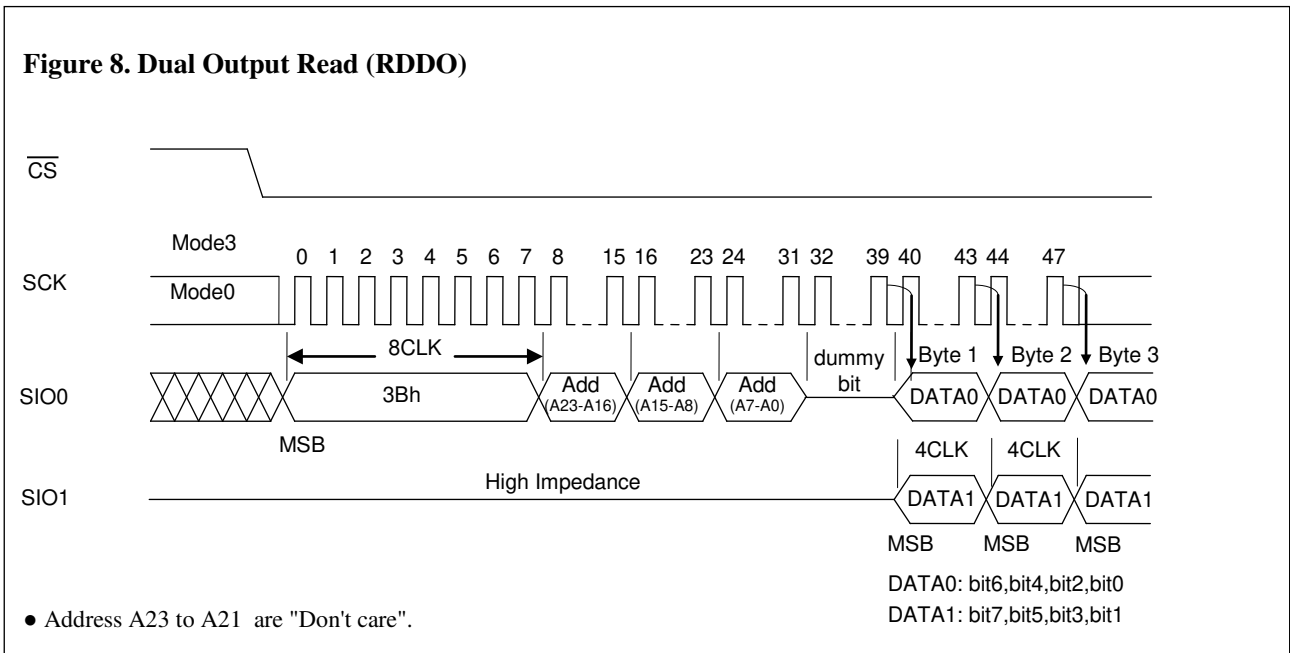"Figure 8. Dual Output Read (RDDO)" shows the timing waveforms.

The sequence of RDDO operation :
$\overline{CS}$ goes to low → input RDDO command (3Bh) → 3 Byte address (A23-A0) input on SI
→ 1 byte dummy cycle → the corresponding data out on SI/SIO0 and SO/SIO1
→ continuous data out (n-byte) per 4clock →→
→ completed by $\overline{CS}$=high

* The data output starts from the falling edge of SCK(39th clock)

	Output Data
SI/SIO0	bit6,4,2,0
SO/SIO1	bit7,5,3,1

The Address is latched on rising edge of SCK. It is necessary to add 1 dummy byte cycle after address is latched, and the corresponding data is shifted out on SI/SIO0 and SO/SIO1 by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data (4 clock cycles) is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 8. Dual Output Read (RDDO)

- Address A23 to A21 are "Don't care".

DATA0: bit6,bit4,bit2,bit0
DATA1: bit7,bit5,bit3,bit1

10-6-2. Dual I/O Read command (RDIO)_____ Maximum Clock frequency: 50MHz

The SI and SO pins change into the input/output pin (SIOx) during this operation. It makes the address input and data output x2 bit and has achieved a high-speed output. Add1 (A23, A21, -, A3 and A1) is input from SIO1 and Add0 (A22, A20, -, A2 and A0) is input from SIO0. bit7, 5, 3 and bit1are output from SIO0. bit6, 4, 2 and bit0 are output from SIO1.

"Figure 9. Dual I/O Read (RDIO)" shows the timing waveforms.

The sequence of RDIO operation :

$\overline{CS}$ goes to low → input RDIO command (BBh)
→ 3 Byte address (A23-A0) input on SI/SIO0 and SO/SIO1 by 12 clock cycle
→ 2 dummy clock (SI/SIO0 and SO/SIO1 are don't care)
 + 2 dummy clock (must set SI/SIO0 and SO/SIO1 high impedance)
→ the corresponding data out on SI/SIO0 and SO/SIO
→ continuous data out (n-byte) per 4clock →→
→ completed by $\overline{CS}$=high

* The data output starts from the falling edge of SCK(23th clock)

	Input Address	Output Data
SI/SIO0	A22,20,18 --,A2,A0	bit6,4,2,0
SO/SIO1	A23,21,19 --,A3,A1	bit7,5,3,1

The Address is latched on rising edge of SCK. It is necessary to add 4 dummy clocks after address is latched, 2CLK of the latter half of the dummy clock is in the state of high impedance, the controller can switch I/O for this period. The corresponding data is shifted out on SI/SIO0 and SO/SIO1 by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data (4 clock cycles) is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high-impedance state.

Figure 9. Dual I/O Read (RDIO)
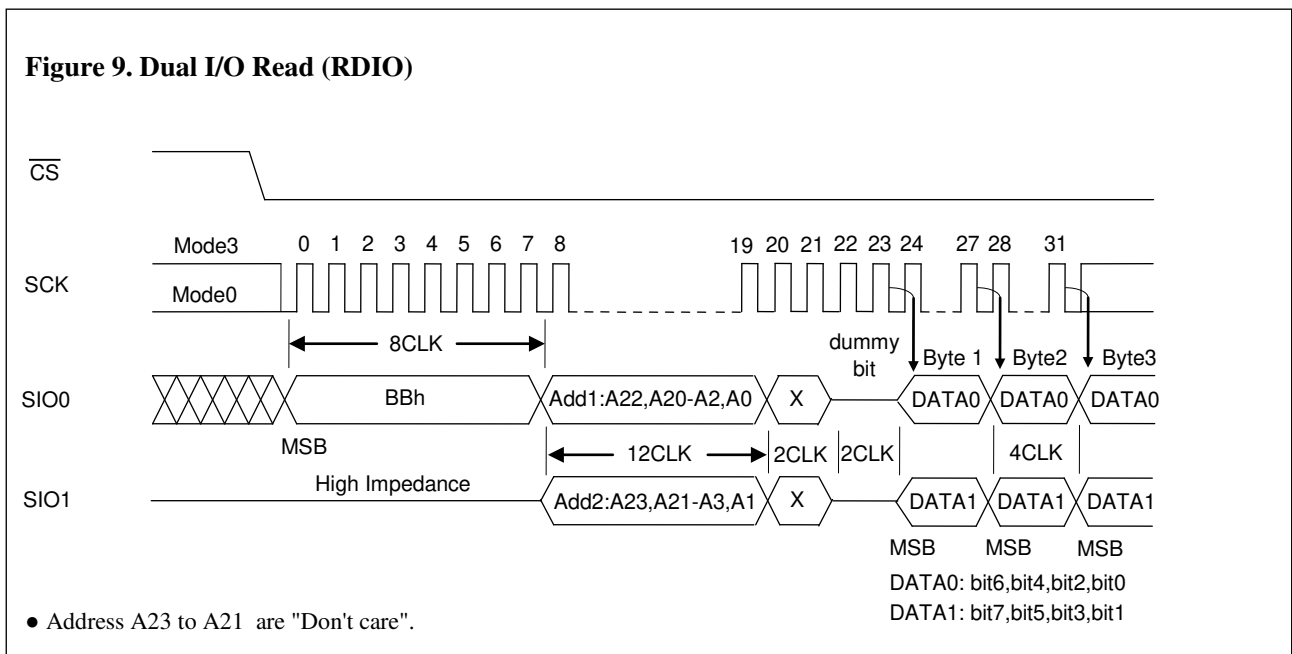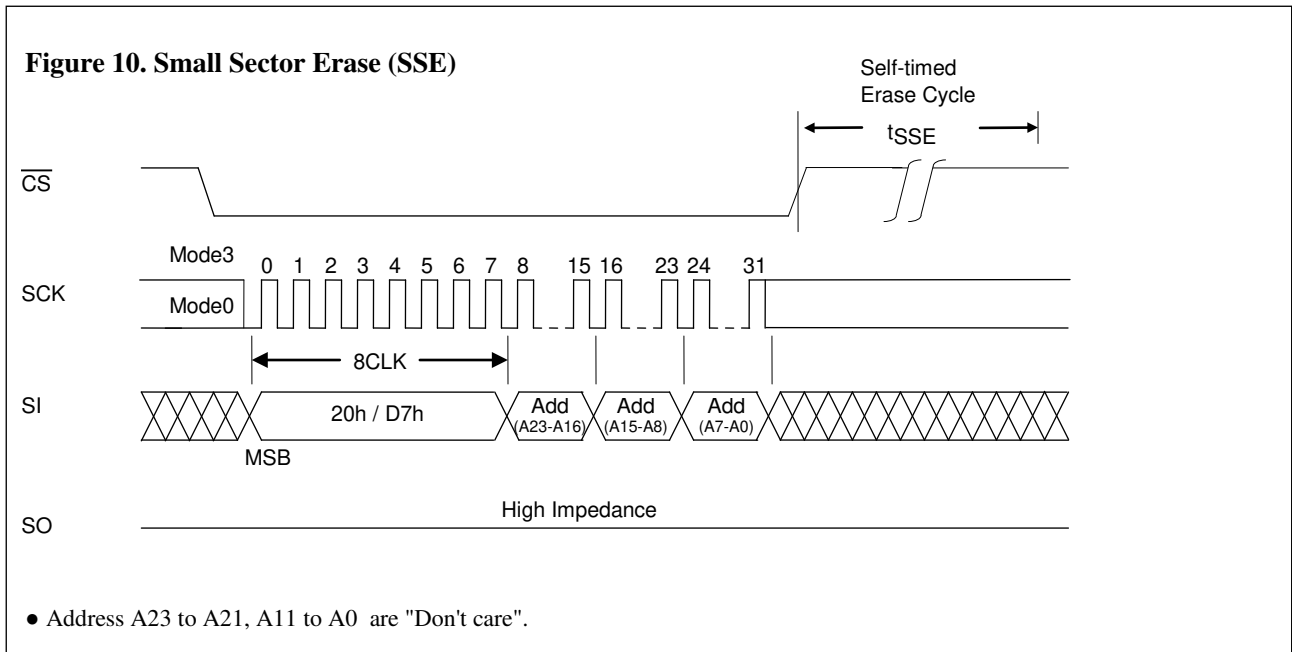
10-7. Small Sector Erase (SSE)

Small Sector Erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 4Kbytes.

"Figure 10. Small Sector Erase (SSE)" shows the timing waveforms.
"Figure 32. Small Sector Erase Flowcharts" shows the flowcharts.

> The sequence of SSE operation :
> $\overline{\text{CS}}$ goes to low → input SSE command (20h or D7h) → 3 Byte address (A23-A0) input on SI
> → $\overline{\text{CS}}$ goes to high (be executed by the rising $\overline{\text{CS}}$ edge)
> * A20 to A12 are valid address

After the correct input sequence the internal erase operation is executed by the rising $\overline{\text{CS}}$ edge, and it is completed automatically by the control exercised by the internal timer (tSSE). The end of erase operation can also be detected by status register (RDY).

Figure 10. Small Sector Erase (SSE)

● Address A23 to A21, A11 to A0 are "Don't care".

10-8. Sector Erase (SE)

Sector Erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64Kbytes.

"Figure 11. Sector Erase (SE)" shows the timing waveforms.
"Figure 33. Sector Erase Flowcharts" shows the flowcharts.

> The sequence of SE operation :
> $\overline{CS}$ goes to low → input SE command (D8h) → 3 Byte address (A23-A0) input on SI
> → $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)
> * A20 to A16 are valid address

After the correct input sequence the internal erase operation is executed by the rising $\overline{CS}$ edge, and it is completed automatically by the control exercised by the internal timer (tSE). The end of erase operation can also be detected by status register (RDY).

Figure 11. Sector Erase (SE)

● Address A23 to A21 , A15 to A0 are "Don't care.