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ZARLINK SEMICONDUCTOR™

VoiceEdge

# Le58083

## *Low Voltage Subscriber Line Audio-processing Circuit*
## VE580 Series

## APPLICATIONS

- **Codec function on telephone switch line cards**

## FEATURES

- **Low-power, 3.3 V CMOS technology with 5 V tolerant digital inputs**
- **Pin programmable PCM/MPI or GCI interface**
- **Software and coefficient compatible to the VE580 series QLSLAC™ devices**
- **Standard PCM/microprocessor interface (PCM/MPI mode)**
  - Single or Dual PCM ports available
  - Time slot assigner (up to 128 channels per port)
  - Clock slot and transmit clock edge options
  - Optional supervision on the PCM highway
  - 1.536, 1.544, 2.048, 3.072, 3.088, 4.096, 6.144, 6.176, or 8.192 MHz master clock derived from MCLK or PCLK
  - µP access to PCM data
  - Real Time Data with interrupt (open drain or TTL)
  - Broadcast mode
- **General Circuit Interface (GCI mode)**
  - Control and PCM data on a single port
  - 2.048 Mbits/s data rate
  - 2.048 MHz or 4.096 MHz clock option
- **Performs the functions of eight codec/filters**
- **Software programmable:**
  - SLIC device input impedance and Transhybrid balance
  - Transmit and receive gains and Equalization
  - Programmable Digital I/O pins with debouncing
- **A-law, µ-law, or linear coding**
- **Built-in test modes with loopback, tone generation, and µP access to PCM data**
- **Mixed state (analog and digital) impedance scaling**
- **Performance guaranteed over a 12 dB gain range**
- **Supports multiplexed SLIC device outputs**
- **256 kHz or 293 kHz chopper clock for Zarlink SLIC devices with switching regulator**
- **Maximum channel bandwidth for V.90 modems**

## ORDERING INFORMATION

| Device | Package |
|---|---|
| Le58083ABGC | 121-pin BGA (Green package)* |

**Green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*

## RELATED LITERATURE

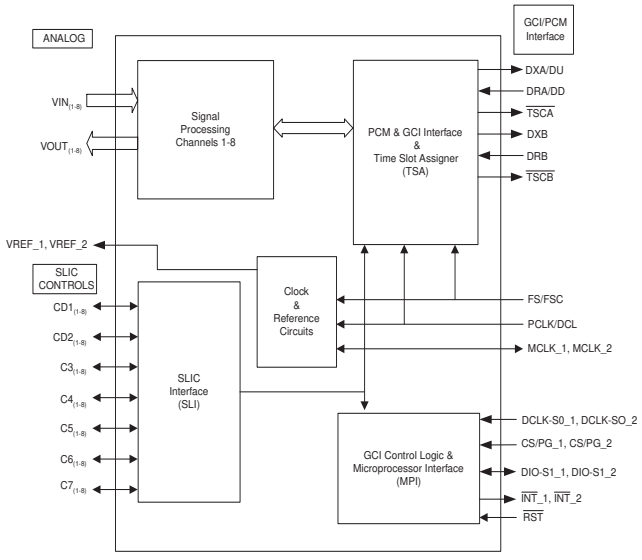
- **080753 Le58QL02/021/031 QLSLAC™ Data Sheet**
- **080754 Le58QL061/063 QLSLAC™ Data Sheet**
- **080761 QSLAC™ to QLSLAC™ Design Conversion Guide**
- **080758 QSLAC™ to QLSLAC™ Guide to New Designs**

## DESCRIPTION

The Le58083 Octal Low Voltage Subscriber Line Audio-Processing Circuit (Octal SLAC™) devices integrate the key functions of analog line cards into high-performance, very-programmable, eight-channel codec-filter devices. The Le58083 Octal SLAC devices are based on the proven design of Zarlink's reliable SLAC device families. The advanced architecture of the Le58083 Octal SLAC devices implements eight independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the audio-processing function of programmable line cards. The Le58083 Octal SLAC devices are software and coefficient compatible to the VE580 series QLSLAC™ devices.

Advanced submicron CMOS technology makes the Le58083 Octal SLAC devices economical, with both the functionality and the low power consumption needed in line card designs to maximize line card density at minimum cost. When used with multiple Zarlink SLIC devices, an Le58083 Octal SLAC device provides a complete software-configurable solution to the BORSCHT functions.

## BLOCK DIAGRAM





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## TABLE OF CONTENTS

## LIST OF FIGURES

## LIST OF TABLES

## PRODUCT DESCRIPTION

The Le58083 Octal SLAC device performs the codec/filter and two-to-four-wire conversion functions required of the subscriber line interface circuitry in telecommunications equipment. These functions involve converting audio signals into digital PCM samples and converting digital PCM samples back into audio signals. During conversion, digital filters are used to band limit the voice signals. All of the digital filtering is performed in digital signal processors operating from a master clock, which can be derived either from PCLK or MCLK in the PCM/MPI mode and DCL in the GCI mode.

The Le58083 Octal SLAC device is configured as two four-channel groups that share a common reset and PCM/GCI interface. Each four-channel group has its own chip select for individual programming. The signal names for each four-channel SLAC device are differentiated by _1 or _2. Generic naming of each signal is $_C$_X, where the subscript $_C$ equals the channel number 1 through 4 and the _X equals the four-channel group number 1 or 2. For example, $VIN_3$_2 would identify channel 3 of the second four-channel group.

Eight independent channels allow the Le58083 Octal SLAC device to function as eight SLAC devices. In PCM/MPI mode, each channel has its own enable bit (EC1, EC2, EC3, etc.) to allow individual channel programming. If more than one Channel Enable bit is High or if all Channel Enable bits are High, all channels enabled will receive the programming information written; therefore, a Broadcast mode can be implemented by simply enabling all channels in the device to receive the information and enabling both chip selects. The Channel Enable bits are contained in the Channel Enable (EC) register, which is written and read using Commands 4A/4Bh. The Broadcast mode is useful in initializing Le58083 Octal SLAC devices in a large system.

In GCI mode, one GCI channel controls two channels of the Le58083 Octal SLAC device. The Monitor channel and SC channel within the GCI channel are used to read/write filter coefficient data, read/write operating conditions and to read/write data to/from the programmable I/O ports of the two channels. Two pairs of GCI channels control the two four-channel groups in the Le58083 Octal SLAC device. The four GCI channels used, of the eight total available, are determined by S0 and S1 inputs.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance, and provide equalization of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the WinSLAC™ software.

In PCM/MPI mode, Data transmitted or received on the PCM highway can be 8-bit companded code (with an optional 8-bit signaling byte in the transmit direction) or 16-bit linear code. The 8-bit codes appear 1 byte per time slot, while the 16-bit code appears in two consecutive time slots. The compressed PCM codes can be either 8-bit companded A-law or µ-law. The PCM data is read from and written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The transmit clock edge and clock slot can be selected for compatibility with other devices that can be connected to the PCM highway.

In GCI mode, two 8-bit companded codes are received or transmitted per GCI channel. The compressed PCM codes can be either 8-bit companded A-law or µ-law. There is no Signaling or Linear mode available when GCI mode is selected.

The programming software is backward compatible to the Zarlink Le58000 SLAC family of devices.

## DEVICE DESCRIPTION

| PCM/GCI Highway | Programmable I/O per Channel | Chopper Clock | Package | Part Number |
|---|---|---|---|---|
| Dual/single | Five I/O<br>Two Output | Yes | BGA | Le58083GC |

## BLOCK DESCRIPTIONS

### Clock and Reference Circuits

This block generates a master clock and a frame sync signal for the digital circuits. It also generates an analog reference voltage for the analog circuits.

### Microprocessor Interface (MPI)

This block communicates with the external control microprocessor over a serial interface. It passes user control information to the other blocks, and it passes status information from the blocks to the user. In addition, this block contains the reset circuitry. When GCI is selected, this block is combined with the TSA block.

### Time Slot Assigner (TSA)

This block communicates with the PCM highway, where the PCM highway is a time division mutiplexed bus carrying the digitized voice samples. The block implements programmable time slots and clocking arrangements in order to achieve a first layer of switching. Internally, this block communicates with the Signal Processing Channels (CHx). When GCI is selected, this block is combined with the TSA block.

## Signal Processing Channels (CHx)

These blocks do the transmission processing for the voice channels. Part of the processing is analog and is interfaced to the VIN and VOUT pins. The remainder of the processing is digital and is interfaced to the Time Slot Assigner (TSA) block.

## SLIC Device Interface (SLI)

This block communicates digitally with the SLIC device circuits. It sends control bits to the SLIC devices to control modes and to operate LEDs and optocouplers. It also accepts supervision information from the SLIC devices and performs some filtering.

## CONNECTION DIAGRAM

## 121-Pin BGA

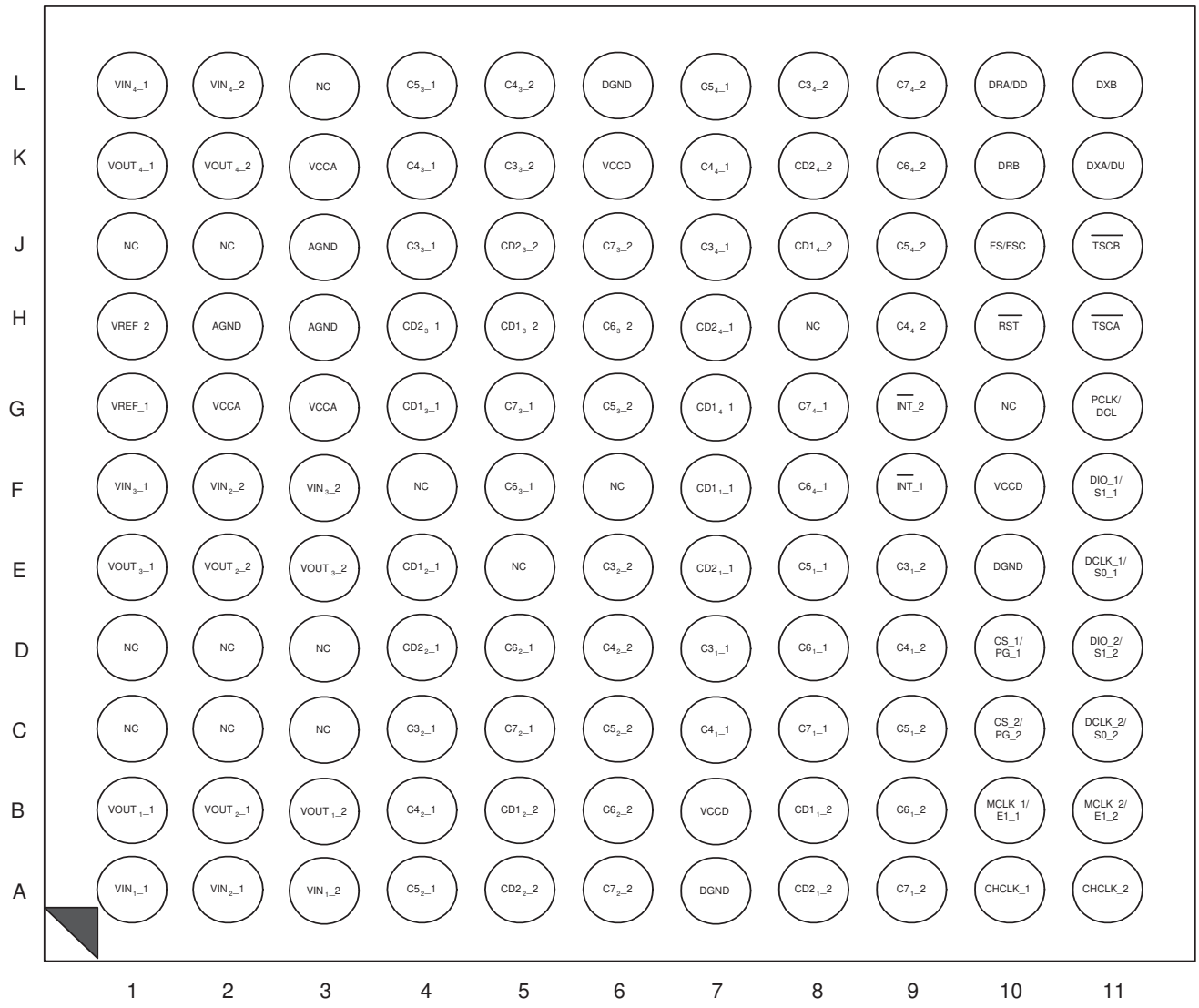


**Table 1. Le58083 Octal SLAC™ Device Pin Names and Numbers**

| Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # |
|---|---|---|---|---|---|---|---|---|---|
| $VIN_1$_1 | A1 | $CD1_4$_2 | J8 | $C5_1$_1 | E8 | CHCLK_1 | A10 | VCCD | B7 |
| $VIN_2$_1 | A2 | $CD2_1$_1 | E7 | $C5_2$_1 | A4 | CHCLK_2 | A11 | VCCD | F10 |
| $VIN_3$_1 | F1 | $CD2_2$_1 | D4 | $C5_3$_1 | L4 | MCLK_1/E1_1 | B10 | AGND | H2 |
| $VIN_4$_1 | L1 | $CD2_3$_1 | H4 | $C5_4$_1 | L7 | MCLK_2/E1_2 | B11 | AGND | H3 |
| $VIN_1$_2 | A3 | $CD2_4$_1 | H7 | $C5_1$_2 | C9 | $\overline{CS}$_1/PG_1 | D10 | AGND | J3 |
| $VIN_2$_2 | F2 | $CD2_1$_2 | A8 | $C5_2$_2 | C6 | $\overline{CS}$_2/PG_2 | C10 | DGND | L6 |
| $VIN_3$_2 | F3 | $CD2_2$_2 | A5 | $C5_3$_2 | G6 | DCLK_1/S0_1 | E11 | DGND | A7 |
| $VIN_4$_2 | L2 | $CD2_3$_2 | J5 | $C5_4$_2 | J9 | DCLK_2/S0_2 | C11 | DGND | E10 |
| $VOUT_1$_1 | B1 | $CD2_4$_2 | K8 | $C6_1$_1 | D8 | DIO_1/S1_1 | F11 | NC | C1 |
| $VOUT_2$_1 | B2 | $C3_1$_1 | D7 | $C6_2$_1 | D5 | DIO_2/S1_2 | D11 | NC | C2 |
| $VOUT_3$_1 | E1 | $C3_2$_1 | C4 | $C6_3$_1 | F5 | $\overline{INT}$_1 | F9 | NC | C3 |
| $VOUT_4$_1 | K1 | $C3_3$_1 | J4 | $C6_4$_1 | F8 | $\overline{INT}$_2 | G9 | NC | D1 |
| $VOUT_1$_2 | B3 | $C3_4$_1 | J7 | $C6_1$_2 | B9 | PCLK/DCL | G11 | NC | D2 |
| $VOUT_2$_2 | E2 | $C3_1$_2 | E9 | $C6_2$_2 | B6 | FS/FSC | J10 | NC | D3 |
| $VOUT_3$_2 | E3 | $C3_2$_2 | E6 | $C6_3$_2 | H6 | DRA/DD | L10 | NC | J1 |
| $VOUT_4$_2 | K2 | $C3_3$_2 | K5 | $C6_4$_2 | K9 | DRB | K10 | NC | J2 |
| VREF_1 | G1 | $C3_4$_2 | L8 | $C7_1$_1 | C8 | DXA/DU | K11 | NC | L3 |
| VREF_2 | H1 | $C4_1$_1 | C7 | $C7_2$_1 | C5 | DXB | L11 | NC | F4 |
| $CD1_1$_1 | F7 | $C4_2$_1 | B4 | $C7_3$_1 | G5 | $\overline{TSCA}$ | H11 | NC | E5 |
| $CD1_2$_1 | E4 | $C4_3$_1 | K4 | $C7_4$_1 | G8 | $\overline{TSCB}$ | J11 | NC | F6 |
| $CD1_3$_1 | G4 | $C4_4$_1 | K7 | $C7_1$_2 | A9 | $\overline{RST}$ | H10 | NC | H8 |
| $CD1_4$_1 | G7 | $C4_1$_2 | D9 | $C7_2$_2 | A6 | VCCA | G2 | NC | G10 |
| $CD1_1$_2 | B8 | $C4_2$_2 | D6 | $C7_3$_2 | J6 | VCCA | G3 | | |
| $CD1_2$_2 | B5 | $C4_3$_2 | L5 | $C7_4$_2 | L9 | VCCA | K3 | | |
| $CD1_3$_2 | H5 | $C4_4$_2 | H9 | | | VCCD | K6 | | |

## PIN DESCRIPTIONS

| Pin Names | Type | Description |
|---|---|---|
| AGND, DGND | Power | Separate analog and digital grounds are provided to allow noise isolation; however, the two grounds are connected inside the part, and the grounds must also be connected together on the circuit board. |
| CD1**C_**X,<br>CD2**C_**X | Inputs/Outputs | Control and Data. CD1 and CD2 are TTL compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of SLIC device or any other device associated with the subscriber line interface. The direction, input or output, is programmed using MPI Command 54/55h or GCI Command SOP 8. As outputs, CD1 and CD2 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. In PCM/MPI mode, the output state of CD1 and CD2 is written using MPI Command 52h. In GCI mode, the output state of CD1 and CD2 is determined by the C1 and C2 bits contained in the down stream C/I channel for the respective channel. As inputs, CD1 and CD2 can be processed by the Le58083 Octal SLAC device (if programmed to do so). CD1 can be debounced before it is made available to the system. The debounce time is programmable from 0 to 15 ms in 1 ms increments using MPI Command C8/C9h and GCI Command SOP 11. CD2 can be filtered using the up/down counter facility and programming the sampling interval using MPI Command E8/E9h or GCI Command SOP 12.<br>Additionally, CD1 can be demultiplexed into two separate inputs using the E1 demultiplexing function. The E1 demultiplexing function of the Le58083 Octal SLAC device was designed to interface directly to Zarlink SLIC devices supporting the ground key function. With the proper Zarlink SLIC device and the E1 function of the Le58083 Octal SLAC device enabled, the CD1 bit can be demultiplexed into an Off-Hook/Ring Trip signal and Ground Key signal. In the demultiplex mode, the second bit, Ground Key, takes the place of the CD2 as an input. The demultiplexed bits can be debounced (CD1) or filtered (CD2) as explained previously. A more complete description of CD1, CD2, debouncing, and filtering functions is contained in the *Operating the Le58083 Octal SLAC Device* section on page 30.<br>Once the CD1 and CD2 inputs are processed (Debounced, Filtered and/or Demultiplexed) by the Le58083 Octal SLAC device, the information can be accessed by the system in two ways in the PCM/MPI mode: 1) on a per channel basis along with C3, C4, and C5 of the specific channel using MPI Command 53h, or 2) by using MPI Command 4D/4Fh, which obtain the CD1 and CD2 bits from all four channels, of a selected four-channel, simultaneously. This feature reduces the processor overhead and the time required to retrieve time-critical signals from the line circuits, such as off-hook and ring trip. With this feature, hookswitch status and ring trip information, for example, can be obtained from four channels of a Le58083 Octal SLAC device with one read command.<br>In the GCI mode, the processed CD1 and CD2 inputs are transmitted upstream on the CD1 and CD2 bits for the respective analog channel, 1 or 2, using the C/I channel. |
| C3**C_**X,<br>C4**C_**X,<br>C5**C_**X | Inputs/Outputs | Control. C3, C4, and C5 are TTL-compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of the SLIC device or any other device associated with subscriber line interface. The direction, input or output, is programmed using MPI Command 54/55h or GCI Command SOP 8. As outputs, C3, C4, and C5 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. In PCM/MPI mode, the output state of C3, C4, and C5 is written using MPI Command 52h. In GCI mode, the output state of C3, C4, and C5 is determined by the C3, C4, and C5 bits contained in the down stream C/I channel for the respective analog channel. As inputs, C3, C4, and C5 can be accessed by the system in PCM/MPI mode by using MPI Command 53h. In GCI mode, C3 is transmitted upstream, along with CD1 and CD2, for the respective analog channel using C3 of the C/I channel. Also, in GCI mode, C3, C4, and C5 can be read along with CD1 and CD2 using GCI Command SOP 10. |
| C6**C_**X,<br>C7**C_**X | Outputs | Additional Control outputs. |
| CHCLK_X | Output | Chopper Clock. This output provides a 256 kHz or a 292.57 kHz, 50% duty cycle, TTL-compatible clock for use by up to four SLIC devices with built-in switching regulators. The CHCLK frequency is synchronous to the master clock, but the phase relationship to the master clock is random. |

| Pin Names | Type | Description |
|---|---|---|
| $\overline{CS}$_X/PG_X | Input | Chip Select/PCM-GCI. The $\overline{CS}$/PG input along with the DCLK/S0 input are used to determine the operating state of the programmable PCM/GCI interface. On power up, the Le58083 Octal SLAC device will initialize to GCI mode if $\overline{CS}$/PG is low *and* there is no toggling (no high to low or low to high transitions) of the DCLK/S0 input. The device will initialize to the PCM/MPI mode if either $\overline{CS}$ is high *or* DCLK is toggling.<br>Once the device is in PCM/MPI mode, it is ready to receive commands through its serial interface pins, DIO and DCLK. Once a valid command has been sent through the MPI serial interface, GCI mode cannot be entered unless a hardware reset is asserted or power is removed from the part. If a valid command has not been sent since the last hardware reset or power up, then GCI mode can be re-entered (after a delay of one PCM frame) by holding $\overline{CS}$/PG low and keeping DCLK static. While the part is in GCI mode, then $\overline{CS}$/PG going high or DCLK toggling will immediately place the device in PCM/MPI mode.<br>In the PCM/MPI mode, the Chip Select input (active Low) enables the device so that control data can be written to or read from the part. The channels selected for the write or read operation are enabled by writing 1s to the appropriate bits in the Channel Enable Registers of the Le58083 Octal SLAC device prior to the command. See EC1, EC2, EC3, EC4. of the Channel Enable Register and Command 4A/4Bh for more information. If Chip Select is held Low for 16 rising edges of DCLK, a hardware reset is executed when Chip Select returns High. |
| DCLK_X/S0_X | Input | Data Clock. In addition to providing both a data clock input and an S0 GCI address input, DCLK/S0 acts in conjunction with $\overline{CS}$/PG to determine the operational mode of the system interface, PCM/MPI or GCI. See $\overline{CS}$/PG for details.<br>In the PCM/MPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the Le58083 Octal SLAC device. The maximum clock rate is 8.192 MHz. |
| | Input | Select Bit 0. In GCI mode, S0 is one of two inputs (S0, S1) that is decoded to determine on which GCI channel pair a four-channel group of the Le58083 Octal SLAC device transmits and receives data. |
| DIO_X/S1_X | Input/Output | Data Input/Output. In the PCM/MPI mode, control data is serially written into and read out of the Le58083 Octal SLAC device via the DIO pin, most significant bit first. The Data Clock determines the data rate. DIO is high impedance except when data is being transmitted from the Le58083 Octal SLAC device. |
| | Input | Select Bit 1. In GCI mode, S1 is the second of two inputs (S0, S1) that is decoded to determine on which GCI channel pair a four-channel group of the Le58083 Octal SLAC device transmits and receives data. |
| DRA/DD, DRB | Inputs | PCM Data Receive (A/B). In the PCM/MPI mode, the PCM data is serially received on either the DRA or DRB port during user-programmed time slots. Data is always received with the most significant bit first. For compressed signals, 1 byte of data for each channel is received every 125 µs at the PCLK rate. In the Linear mode, 2 consecutive bytes of data for each channel are received every 125 µs at the PCLK rate. |
| | Input | GCI Data Downstream. In GCI mode, the B1, B2, Monitor and SC channel data is serially received, from the individual channels, on the Data Downstream input for all four channels of the Le58083 Octal SLAC device. The Le58083 Octal SLAC device requires four of the eight GCI channels for operation. The four GCI Channels, out of the eight possible, are determined by the S0 and S1 inputs. Data is always received with the most significant bit first. 4 bytes of data for each GCI channel is received every 125 µs at the 2.048 Mbit/s data rate. |
| DXA/DU, DXB | Outputs | PCM Data Transmit. In the PCM/MPI mode, the transmit data, from the individual channels, is sent serially out on either the DXA or DXB port or on both ports during user-programmed time slots. Data is always transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit (16-bit in Linear or PCM Signaling mode) bursts at the PCLK rate. DXA and DXB are High impedance between time slots, while the device is in the Inactive mode with no PCM signaling, or while the Cutoff Transmit Path bit (CTP) is on. |
| | Output | GCI Data Upstream. In the GCI mode, the B1, B2, Monitor and SC channel data is serially transmitted on the Data Upstream output of the Le58083 Octal SLAC device. Which GCI channels the device uses is determined by the S0 and S1 inputs. Data is always transmitted with the most significant bit first. 4 bytes of data for each GCI channel is transmitted every 125 µs at the DCL rate. |
| FS/FSC | Input | Frame Sync. In the PCM/MPI mode, the Frame Sync (FS) pulse is an 8 kHz signal that identifies Time Slot 0 and Clock Slot 0 of a system's PCM frame. The Le58083 Octal SLAC device references individual time slots with respect to this input, which must be synchronized to PCLK. |
| | Input | Frame Sync. In GCI mode, the Frame Sync (FSC) pulse is an 8 kHz signal that identifies the beginning of GCI channel 0 of a system's GCI frame. The Le58083 Octal SLAC device references individual GCI channels with respect to this input, which must be synchronized to DCL. |

| Pin Names | Type | Description |
|---|---|---|
| $\overline{INT}$_X | Output | Interrupt. $\overline{INT}$ is an active Low output signal, which is programmable as either TTL-compatible or open drain. The $\overline{INT}$ output goes Low any time one of the input bits in the Real Time Data register changes state and is not masked. It also goes Low any time new transmit data appears if this interrupt is armed. $\overline{INT}$ remains Low until the appropriate register is read via the microprocessor interface, or the Le58083 Octal SLAC device receives either a software or hardware reset. The individual $CDx_C$ bits in the Real Time Data register can be masked from causing an interrupt by using MPI Command 6C/6Dh or GCI Command SOP 14. The transmit data interrupt must be armed with a bit in the Operating Conditions Register. |
| MCLK_X/E1_X | Input/Output | Master Clock/Enable CD1 Multiplex. In PCM/MPI mode only, the Master Clock can be a 1.536 MHz, 1.544 MHz, or 2.048 MHz (times 1, 2, or 4) clock for use by the digital signal processor. If the internal clock is derived from the PCM Clock Input (PCLK) or if GCI mode is selected, this pin can be used as an E1 output to control Zarlink SLIC devices having multiplexed hook switch and ground key detector outputs. |
| NC | — | No connect. This pin is not internally connected. |
| PCLK/DCL | Input | PCM Clock. In the PCM/MPI mode, the PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz for dual PCM highway versions and 256 kHz for single PCM highway versions. The minimum clock rate must be doubled if Linear mode or PCM signaling is used. PCLK frequencies between 1.03 MHz and 1.53 MHz are not allowed. Optionally, the digital signal processor clock can be derived from PCLK rather than MCLK. In PCM/MPI mode, PCLK can be operated at twice the PCM data rate in the Double PCLK mode (bit 1 of PCM/MPI Command C8/C9h). |
| | Input | GCI Data Clock. In GCI mode, DCL is either 2.048 MHz or 4.096 MHz, which is an integer multiple of the frame sync frequency. Circuitry internal to the Le58083 Octal SLAC device monitors this input to determine which frequency is being used, 2.048 MHz or 4.096 MHz. When 4.096 MHz clock operation is detected, internal timing is adjusted so that DU and DD operate at the 2.048 Mbit/s rate. |
| $\overline{RST}$ | Input | Reset. A logic Low signal at this pin resets both four-channel groups of the Le58083 Octal SLAC device to their default state. |
| $\overline{TSCA}$, $\overline{TSCB}$ | Outputs | Time Slot Control. The Time Slot Control outputs are open-drain outputs (requiring pull-up resistors to VCCD) and are normally inactive (high impedance). In the PCM/MPI mode, $\overline{TSCA}$ or $\overline{TSCB}$ is active (low) when PCM data is transmitted on the DXA or DXB pin, respectively. In GCI mode, $\overline{TSCA}$ is active (low) during the two GCI time slots selected by the S1 and S0. |
| VCCA, VCCD | Power | Analog and digital power supply inputs. VCCA and VCCD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VCC power supply pins should be connected together at the connector of the printed circuit board. |
| $VIN_C$_X | Inputs | Analog Input. The analog voice band signal is applied to the VIN input of the Le58083 Octal SLAC device. The VIN input is biased at VREF by a large internal resistor. The audio signal is sampled, digitally processed and encoded, and then made available at the TTL-compatible PCM output (DXA or DXB) or in the B1 and B2 of the GCI channel. If the digitizer saturates in the positive or negative direction, VIN is pulled by a reduced resistance toward AGND or VCCD, respectively. |
| $VOUT_C$_X | Outputs | Analog Output. The received digital data at DRA/DRB or DD (GCI mode) is processed and converted to an analog signal at the VOUT pin.The VOUT voltages are referenced to VREF. |
| VREF_X | Output | Analog Voltage Reference. The VREF output is provided in order for an external capacitor to be connected from VREF to ground, filtering noise present on the internal voltage reference. VREF is buffered before it is used by internal circuitry. The voltage on VREF and the output resistance are given in *Electrical Characteristics*, on page 13. The leakage current in the capacitor must be low. |

## ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

| | |
|---|---|
| Storage Temperature | –60° C < $T_A$ < +125° C |
| Ambient Temperature, under Bias | –40° C < $T_A$ < +85° C |
| Ambient relative humidity (non condensing) | 5 to 95% |
| $V_{CCA}$ with respect to AGND | –0.4 to + 4.0 V |
| $V_{CCA}$ with respect to VCCD | ±0.4 V |
| $V_{CCD}$ with respect to DGND | –0.4 to + 4.0 V |
| $V_{IN}$ with respect to AGND | –0.4 V to ($V_{CCA}$ + 0.4 V) |
| AGND with respect to DGND | ±50 mV |
| Digital pins with respect to DGND | –0.4 to 5.5 V or VCCD + 2.37 V, whichever is smaller |
| Total combined CD1–C7 current for each four-channel group:<br>Source from VCCD<br>Sink into DGND | <br>40 mA<br>40 mA |
| Latch up immunity (any pin) | ± 100 mA |
| Total VCC current if rise rate of VCC > 0.4 V/µs | 1.0 A |

### Package Assembly

The green package devices are assembled with enhanced environmental, compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

## OPERATING RANGES

Zarlink guarantees the performance of this device over commercial (0º C to 70º C) and industrial (–40º C to 85º C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment

### Environmental Ranges

| | |
|---|---|
| Ambient Temperature | –40° C < $T_A$ < +85° C |
| Ambient Relative Humidity | 15 to 85% |

### Electrical Ranges

| | |
|---|---|
| Analog Supply $V_{CCA}$ | +3.3 V ± 5%<br>$V_{CCD}$ ± 50 mV |
| Digital Supply $V_{CCD}$ | +3.3 V ± 5% |
| DGND | 0 V |
| AGND | ±10 mV |
| CFIL Capacitance: VREF_X to AGND | 0.1 µF ± 20% |
| Digital Pins | DGND to +5.25 V |

## ELECTRICAL CHARACTERISTICS

Typical values are for TA = 25º C and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in Operating Ranges, except where noted.

| Symbol | Parameter Descriptions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Digital Input Low voltage | | | 0.8 | V | |
| $V_{IH}$ | Digital Input High voltage | 2.0 | | | | |
| $I_{IL}$ | Digital Input leakage current<br>Pins connected to one channel group<br>0 < V < VCCD<br>Otherwise<br>Pins connected to both channel groups<br>0 < V < VCCD<br>Otherwise | <br><br><br>–7<br>–120<br><br>–14<br>–240 | | <br><br><br>+7<br>+180<br><br>+14<br>+360 | µA | 6 |
| $V_{HYS}$ | Digital Input hysteresis | 0.16 | 0.25 | 0.34 | V | |
| $V_{OL}$ | Digital Output Low voltage<br>CD1–C7 ($I_{OL}$ = 4 mA)<br>CD1–C7 ($I_{OL}$ = 8 mA)<br>$\overline{TSCA}$/ $\overline{TSCB}$ ($I_{OL}$ =14 mA)<br>Other digital outputs ($I_{OL}$ = 2 mA) | | | <br>0.4<br>0.8<br>0.4<br>0.4 | V | 1 |
| $V_{OH}$ | Digital Output High voltage<br>CD1–C7 ($I_{OH}$ = 4 mA)<br>CD1–C7 ($I_{OH}$ = 8 mA)<br>Other digital outputs ($I_{OH}$ = 400 µA) | <br>$V_{CCD}$ – 0.4 V<br>$V_{CCD}$ – 0.8 V<br>2.4 | | | V | 1 |
| $I_{OL}$ | Digital Output leakage current (Hi-Z state)<br>Pins connected to one channel group<br>0 < V < VCCD<br>Otherwise<br>Pins connected to both channel groups<br>0 < V < VCCD<br>Otherwise | <br><br><br>–7<br>–120<br><br>–14<br>–240 | | <br><br><br>+7<br>+180<br><br>+14<br>+360 | µA | 6 |
| GIN | Input attenuator gain<br>DGIN = 0<br>DGIN = 1 | | <br>0.6438<br>1 | | V/V | |
| $V_{IR}$ | Analog input voltage range (Relative to VREF)<br>AX = 0 dB, attenuator on (DGIN = 0)<br>AX = 6.02 dB, attenuator on (DGIN = 0)<br>AX = 0 dB, attenuator off (DGIN = 1)<br>AX = 6.02 dB, attenuator off (DGIN = 1) | | <br>±1.584<br>±0.792<br>±1.02<br>±0.51 | | Vpk | |
| $V_{IOS}$ | Offset voltage allowed on VIN | –50 | | 50 | mV | |
| $Z_{IN}$ | Analog input impedance to VREF, 300 to 3400 Hz | 600 | | 1400 | kΩ | |
| $I_{IP}$ | Current into analog input for an input voltage of 3.3 V | 50 | | 115 | µA | 2 |
| $I_{IN}$ | Current out of analog input for an input voltage of –0.3 V | 50 | | 130 | | 2 |
| $Z_{OUT}$ | VOUT output impedance | | 1 | 10 | Ω | |
| $CL_{OUT}$ | Allowable capacitance, $V_{OUT}$ to AGND | | | 500 | pF | |
| $I_{OUT}$ | VOUT output current (F< 3400 Hz) | –4 | | 4 | mApk | 3 |
| $V_{REF}$ | VREF_X output open circuit voltage (leakage < 20 nA) | 1.43 | 1.5 | 1.57 | V | |
| $Z_{REF}$ | VREF_X output impedance (F <3400 Hz) | 70 | | 130 | kΩ | |
| $V_{OR}$ | VOUT analog output voltage range (Relative to VREF)<br>AR = 0 dB<br>AR = –6.02 dB | | <br>±1.02<br>±0.51 | | Vpk | |
| $V_{OOS}$ | VOUT offset voltage (AISN off) | –40 | | 40 | mV | 4 |
| $V_{OOSA}$ | VOUT offset voltage (AISN on) | –80 | | 80 | | |
| $G_{AISN}$ | AISN gain - expected gain (input = 0 dBm0, 1014 Hz)<br>Attenuator on (DGIN = 0)<br>Attenuator off (DGIN = 1) | <br>–0.010<br>–0.016 | | <br>0.010<br>0.016 | V/V | |
| PD | Power dissipation<br>All channels active<br>1 channel active<br>All channels inactive | | <br>260<br>55<br>26 | <br>340<br>100<br>36 | mW | 5 |

| Symbol | Parameter Descriptions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $C_I$ | Digital Input capacitance<br>Pins connected to one channel group<br>Pins connected to both channel groups | | | <br>10<br>20 | pF | <br>6 |
| $C_O$ | Digital Output capacitance<br>Pins connected to one channel group<br>Pins connected to both channel groups | | | <br>10<br>20 | | <br>6 |
| PSRR | Power supply rejection ratio (1.02 kHz, 100 $mV_{RMS}$, either path, GX = GR = 0 dB) | 40 | | | dB | |

***Notes:***

1. *The CD1, CD2, C3–C7 outputs are resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.*
2. *When the digitizer saturates, a resistor of 50 kΩ ± 20 kΩ is connected either to AGND or to VCCA as appropriate to discharge the coupling capacitor.*
3. *When the Le58083 Octal SLAC device is in the Inactive state, the analog output will present either a VREF DC output level through a 15 kΩ resistor (VMODE = 0) or a high impedance (VMODE = 1).*
4. *If there is an external DC path from VOUT to VIN with a gain of $G_{DC}$ and the AISN has a gain of $h_{AISN}$, then the output offset will be multiplied by 1 / [1 – ($h_{AISN}$ • $G_{DC}$)].*
5. *Power dissipation in the Inactive state is measured with all digital inputs at $V_{IH}$ = VCCD and $V_{IL}$ = DGND and with no load connected to $VOUT_{C_}$X pins.*
6. *The PCM/GCI pins (DRA/DD, DRB, DXA/DU, DXB, FS/FSC, PCLK/DCL, $\overline{TSCA}$ and $\overline{TSCB}$) connect to both four-channel groups and have double the capacitance and leakage. Also, $\overline{RST}$ is in this category.*

## Transmission Characteristics

### Table 2. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

| Signal at Digital Interface | Transmit (DGIN = 0) | Transmit (DGIN = 1) | Receive | Unit |
|---|---|---|---|---|
| A-law digital mW or equivalent (0 dBm0) | 0.7804 | 0.5024 | 0.5024 | Vrms |
| μ-law digital mW or equivalent (0 dBm0) | 0.7746 | 0.4987 | 0.4987 | |
| ±22,827 peak linear coded sine wave | 0.7804 | 0.5024 | 0.5024 | |

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the GX gain from 0 dB to 12 dB, the GR loss from 0 dB to 12 dB, and the input attenuator (GIN) on or off.

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz<br>AX = AR = 0 dB<br>0 to 85° C<br>–40° C<br>AX = +6.02 dB and/or<br>AR = –6.02 dB<br>0 to 85° C<br>–40° C | <br><br>–0.25<br>–0.30<br><br><br>–0.30<br>–0.40 | | <br><br>+0.25<br>+0.30<br><br><br>+0.30<br>+0.40 | dB | |
| Gain accuracy digital-to-digital | | –0.25 | | +0.25 | | |
| Gain accuracy analog-to-analog | | –0.25 | | +0.25 | | |
| Attenuation distortion | 300 Hz to 3 kHz | –0.125 | | +0.125 | | 1 |
| Single frequency distortion | | | | –46 | | 2 |
| Second harmonic distortion, D/A | GR = 0 dB | | | –55 | | |
| Idle channel noise<br>Analog out<br><br><br><br><br>Digital out | <br>Digital looped backweighted<br>unweighted<br>Digital input = 0 A-law<br>Digital input = 0 μ-law<br>Analog $V_{IN}$ = 0 VACA-law<br>Analog $V_{IN}$ = 0 VAC μ-law | | <br><br><br><br>0<br><br>0 | <br>–68<br>–55<br>–78<br>12<br>–68<br>16 | <br>dBm0p<br>dBm0<br>dBm0p<br>dBrnc0<br>dBm0p<br>dBrnc0 | <br>3<br>3<br>3<br>3, 6<br>3<br>3, 6 |
| Crosstalk TX to RX<br>same channel RX to TX | 0 dBm0 300 to 3400 Hz<br>0 dBm0 300 to 3400 Hz | | | –75<br>–75 | dBm0 | |
| Crosstalk between channels<br><br>TX or RX to TX<br>TX or RX to RX | 0 dBm0<br>SLIC device imped. < 5000 Ω<br>1014 Hz, Average<br>1014 Hz, Average | | | <br><br>–76<br>–78 | dBm0 | 4 |
| End-to-end group delay | B = Z = 0; X = R = 1 | | | 678 | μs | 5 |

***Notes:***

1. *See Figure 1 and Figure 2.*
2. *0 dBm0 input signal, 300 Hz to 3400 Hz; measurement at any other frequency, 300 Hz to 3400 Hz.*
3. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
4. *The weighted average of the crosstalk is defined by the following equation, where C(f) is the crosstalk in dB as a function of frequency, $f_N$ = 3300 Hz, $f_1$ = 300 Hz, and the frequency points ($f_J$, j = 2..N) are closely spaced:*

$$\text{Average} = 20 \bullet \log \left[ \frac{\sum_{j} \frac{10^{\frac{1}{20} \bullet C(f_j)} + 10^{\frac{1}{20} \bullet C(f_{j-1})}}{2} \bullet \log \left( \frac{f_j}{f_{j-1}} \right)}{\log \left( \frac{f_N}{f_1} \right)} \right]$$

5. *The End-to-End Group Delay is the sum of the transmit and receive group delays (both measured using the same time and clock slot).*
6. *Typical values not tested in production.*

## Attenuation Distortion

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 1 and Figure 2. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

**Figure 1. Transmit Path Attenuation vs. Frequency**

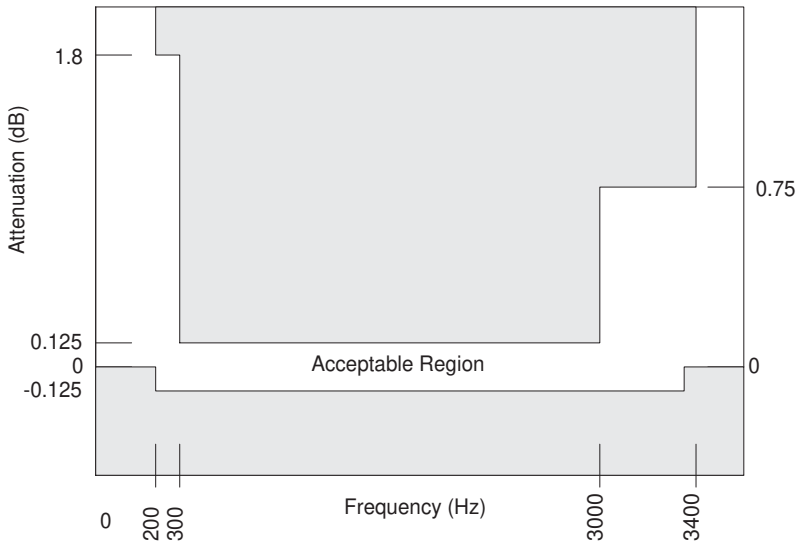
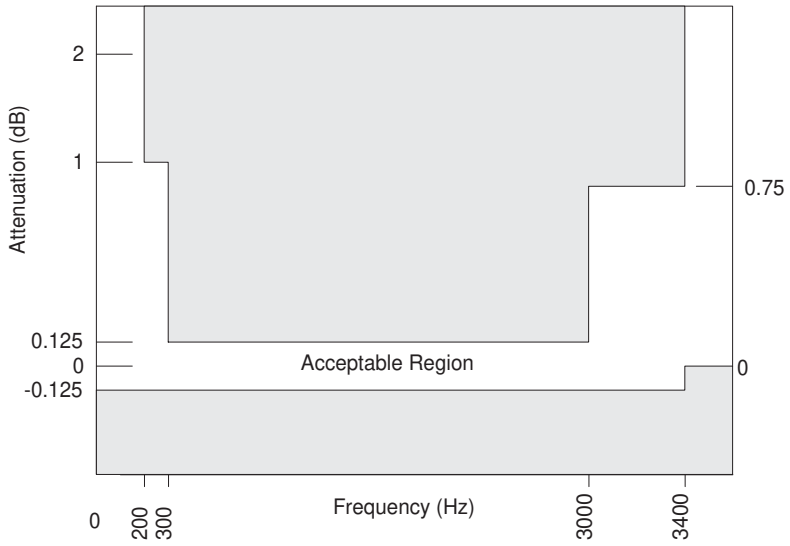


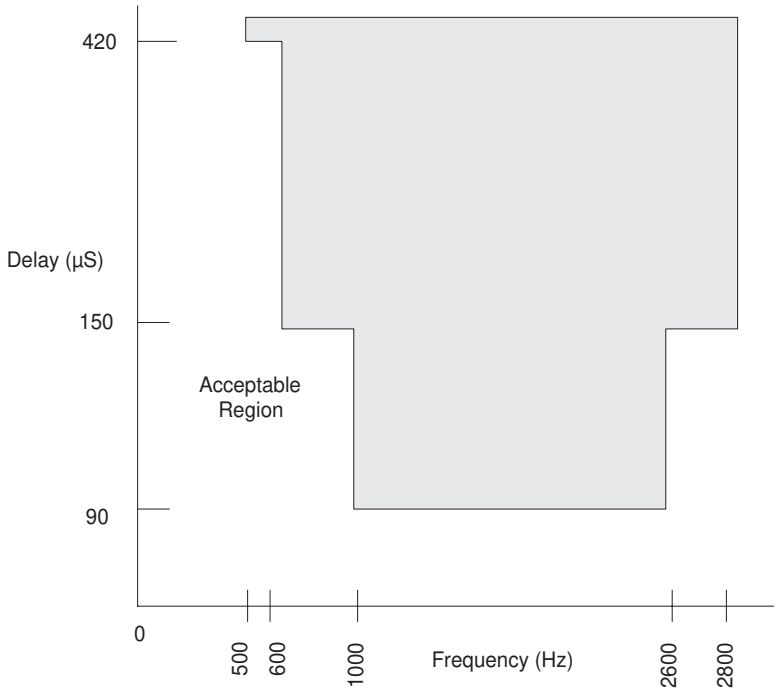
**Figure 2. Receive Path Attenuation vs. Frequency**




## Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 3. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

**Figure 3. Group Delay Distortion**




## Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 4 (A-law) and Figure 5 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

**Figure 4. A-law Gain Linearity with Tone Input (Both Paths)**

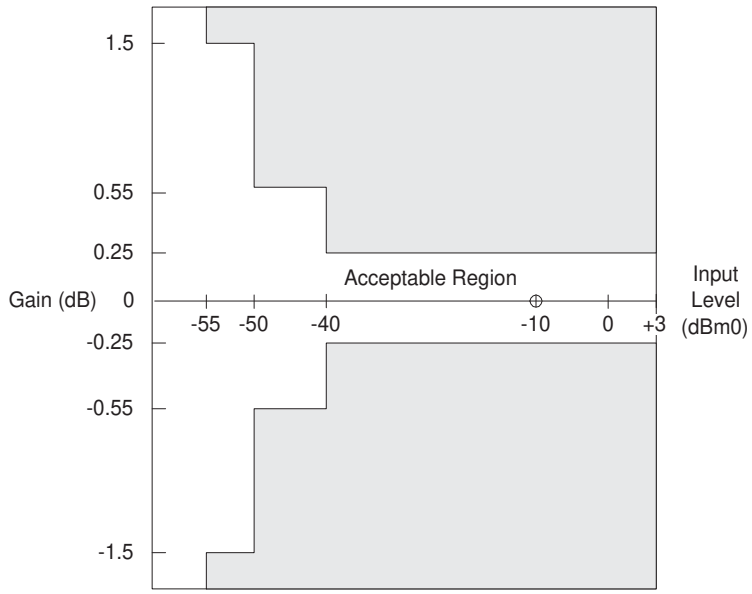
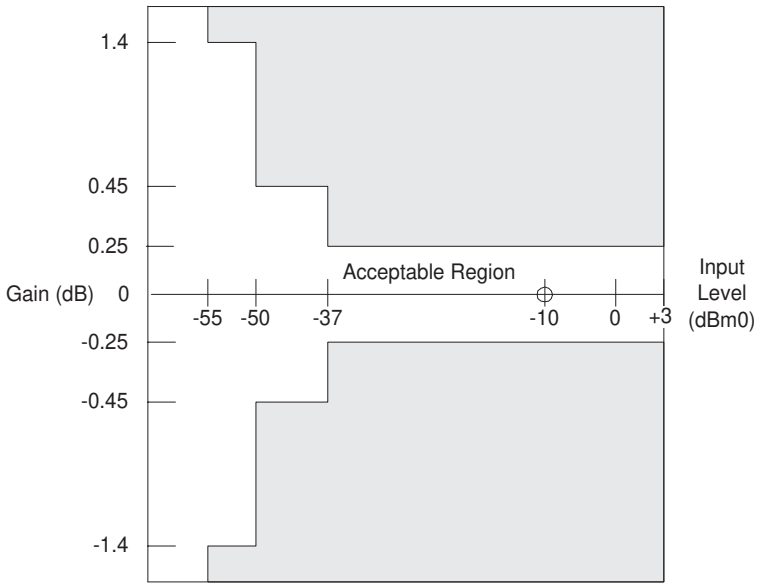


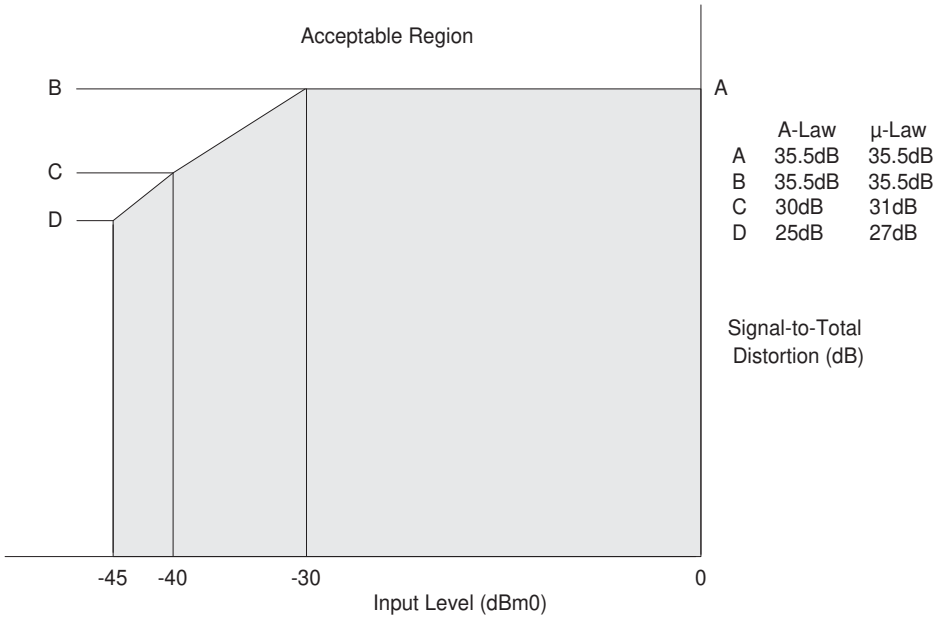

**Figure 5. µ-law Gain Linearity with Tone Input (Both Paths)**



## Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 6 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

**Figure 6. Total Distortion with Tone Input (Both Paths)**

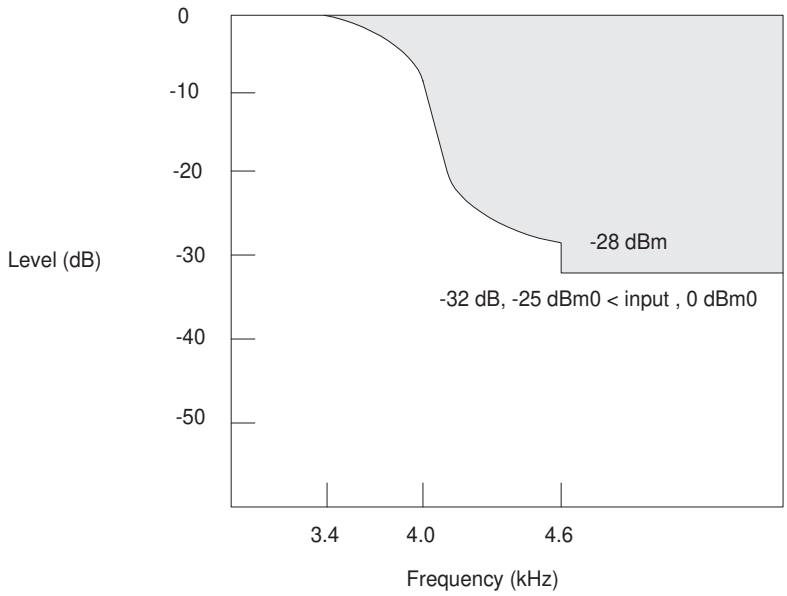



## Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table.

| Frequency of Out-of-Band Signal | Amplitude of Out-of-Band Signal | Level below A |
|---|---|---|
| 16.6 Hz < f < 45 Hz | –25 dBm0 < A ≤ 0 dBm0 | 18 dB |
| 45 Hz < f < 65 Hz | –25 dBm0 < A ≤ 0 dBm0 | 25 dB |
| 65 Hz < f < 100 Hz | –25 dBm0 < A ≤ 0 dBm0 | 10 dB |
| 3400 Hz < f < 4600 Hz | –25 dBm0 < A ≤ 0 dBm0 | see Figure 7 |
| 4600 Hz < f < 100 kHz | –25 dBm0 < A ≤ 0 dBm0 | 32 dB |

**Figure 7. Discrimination Against Out-of-Band Signals**




***Note:***

*The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:*

$$\text{Attenuation (db)} = 14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)$$

## Discrimination Against 12- and 16-kHz Metering Signals

If the Le58083 Octal SLAC device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones also may appear at the VIN terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the analog input voltage range.

## Spurious Out-of-Band Signals at the Analog Output

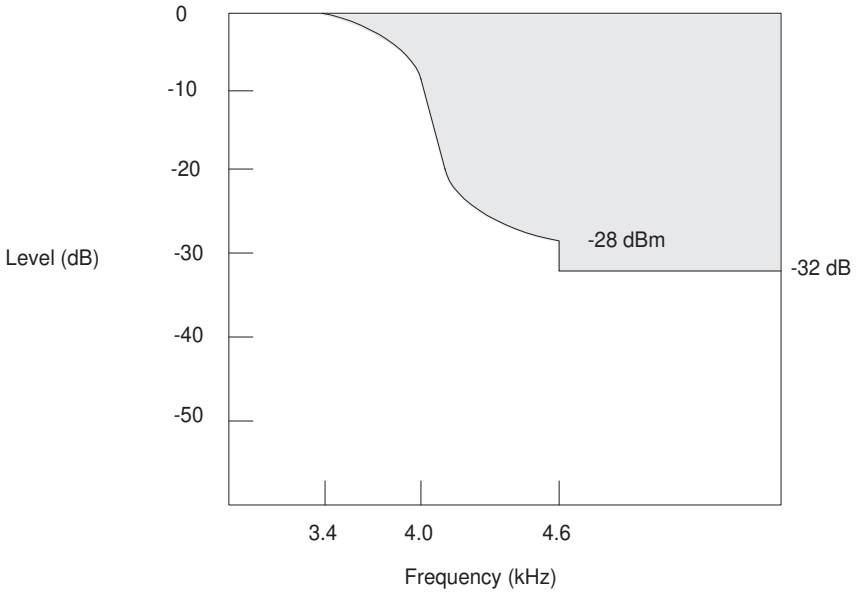
With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

| Frequency | Level |
|---|---|
| 4.6 kHz to 40 kHz | –32 dBm0 |
| 40 kHz to 240 kHz | –46 dBm0 |
| 240 kHz to 1 MHz | –36 dBm0 |

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 8. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14\sin\left(\frac{\pi(f - 4000)}{1200}\right)\right] \text{dBm0}$$

**Figure 8. Spurious Out-of-Band Signals**

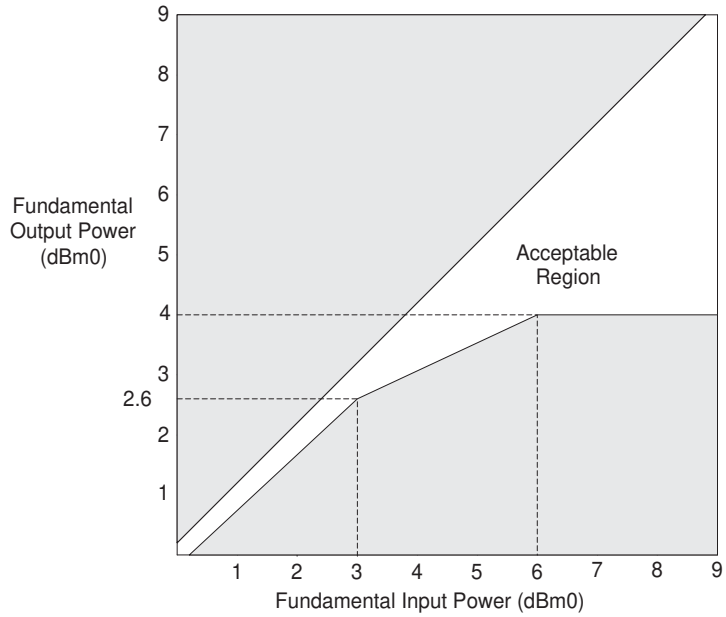



## Overload Compression

Figure 9 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. 1.2 dB < GX ≤ + 12 dB
2. –12 dB ≤ GR < –1.2 dB
3. Digital voice output connected to digital voice input.
4. Measurement analog-to-analog.

**Figure 9. Analog-to-Analog Overload Compression**



## SWITCHING CHARACTERISTICS

The following are the switching characteristics over operating range (unless otherwise noted). Min and max values are valid for all digital outputs with a 115 pF load, except CD1–C7 with a 30 pF load. (See Figure 11 and Figure 12 for the microprocessor interface timing diagrams.)

### Microprocessor Interface

| No. | Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | $t_{DCY}$ | Data clock period | 122 | | | ns | |
| 2 | $t_{DCH}$ | Data clock HIGH pulse width | 48 | | | | |
| 3 | $t_{DCL}$ | Data clock LOW pulse width | 48 | | | | |
| 4 | $t_{DCR}$ | Rise time of clock | | | 25 | | |
| 5 | $t_{DCF}$ | Fall time of clock | | | 25 | | |
| 6 | $t_{ICSS}$ | Chip select setup time, Input mode | 30 | | $t_{DCY}$ –10 | | |
| 7 | $t_{ICSH}$ | Chip select hold time, Input mode | 0 | | $t_{DCH}$ –20 | | |
| 8 | $t_{ICSL}$ | Chip select pulse width, Input mode | | $8t_{DCY}$ | | | |
| 9 | $t_{ICSO}$ | Chip select off time, Input mode | 2500 | | | | 1 |
| 10 | $t_{IDS}$ | Input data setup time | 25 | | | | |
| 11 | $t_{IDH}$ | Input data hold time | 30 | | | | |
| 12 | $t_{OLH}$ | SLIC device output latch valid | | | 2500 | | |
| 13 | $t_{OCSS}$ | Chip select setup time, Output mode | 30 | | $t_{DCY}$ –10 | | |
| 14 | $t_{OCSH}$ | Chip select hold time, Output mode | 0 | | $t_{DCH}$ –20 | | |
| 15 | $t_{OCSL}$ | Chip select pulse width, Output mode | | $8t_{DCY}$ | | | |
| 16 | $t_{OCSO}$ | Chip select off time, Output mode | 2500 | | | | 1 |
| 17 | $t_{ODD}$ | Output data turn on delay | | | 50 | | 2 |
| 18 | $t_{ODH}$ | Output data hold time | 3 | | | | |
| 19 | $t_{ODOF}$ | Output data turn off delay | | | 50 | | |
| 20 | $t_{ODC}$ | Output data valid | | | 50 | | |
| 21 | $t_{RST}$ | Reset pulse width | 50 | | | µs | |

### PCM Interface

PCLK not to exceed 8.192 MHz.

Pull-up resistors to $V_{CCD}$ of 240 Ω are attached to $\overline{TSCA}$ and $\overline{TSCB}$. (See Figure 13 through Figure 15 for the PCM interface timing diagrams.)

| No. | Symbol | Parameter | Min. | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 22 | $t_{PCY}$ | PCM clock period | 122 | | | ns | 3 |
| 23 | $t_{PCH}$ | PCM clock HIGH pulse width | 48 | | | | |
| 24 | $t_{PCL}$ | PCM clock LOW pulse width | 48 | | | | |
| 25 | $t_{PCF}$ | Fall time of clock | | | 15 | | |
| 26 | $t_{PCR}$ | Rise time of clock | | | 15 | | |
| 27 | $t_{FSS}$ | FS setup time | 25 | | $t_{PCY}$–30 | | |
| 28 | $t_{FSH}$ | FS hold time | 50 | | | | |
| 30 | $t_{TSD}$ | Delay to $\overline{TSC}$ valid | 5 | | 80 | | 4 |
| 31 | $t_{TSO}$ | Delay to $\overline{TSC}$ off | 5 | | 80 | | 4,5 |
| 32 | $t_{DXD}$ | PCM data output delay | 5 | | 70 | | |
| 33 | $t_{DXH}$ | PCM data output hold time | 5 | | 70 | | |
| 34 | $t_{DXZ}$ | PCM data output delay to High-Z | 5 | | 70 | | |
| 35 | $t_{DRS}$ | PCM data input setup time | 25 | | | | |
| 36 | $t_{DRH}$ | PCM data input hold time | 5 | | | | |

### Master Clock

(See Figure 16 for the Master Clock timing diagram.)

| No. | Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| 37 | $J_{MCY}$ | Master clock jitter | | | 50 | ns | 6 |
| 38 | $t_{MCR}$ | Rise time of clock | | | 15 | | |
| 39 | $t_{MCF}$ | Fall time of clock | | | 15 | | |
| 40 | $t_{MCH}$ | MCLK HIGH pulse width | 48 | | | | |
| 41 | $t_{MCL}$ | MCLK LOW pulse width | 48 | | | | |

### Auxiliary Output Clocks

| No. | Symbol | Parameter | Min | Typ | Max | Unit | |
|---|---|---|---|---|---|---|---|
| 42 | $f_{CHP}$ | Chopper clock frequency CHP = 0<br>CHP = 1 | | 256<br>292.57 | | kHz | 7 |
| 42A | $DC_{CHP}$ | Chopper clock duty cycle | | 50 | | % | 7 |
| 43 | $f_{E1}$ | E1 output frequency (CMODE = EE1 = 1) | | 4.923 | | kHz | 7 |
| 44 | $t_{E1}$ | E1 pulse width (CMODE = EE1 = 1) | | 31.25 | | µs | 7 |

***Notes:***

1. *If CFAIL = 1 (Command 55h), GX, GR, Z, B1, X, R, and B2 coefficients must not be written or read without first deactivating all channels or switching them to default coefficients; otherwise, a chip select off time of 25 µs is required.*
2. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
3. *The PCM clock frequency must be an integer multiple of the frame sync frequency. The maximum allowable PCM clock frequency is 8.192 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz in Companded state and 256 kHz in Linear state, PCM Signaling state, or double PCLK state. The minimum PCM clock rates should be doubled for parts with only one PCM highway in order to allow simultaneous access to all four channels.*
4. *$\overline{TSC}$ is delayed from FS by a typical value of $N \bullet t_{PCY}$, where N is the value stored in the time/clock-slot register.*
5. *$t_{TSO}$ is defined as the time at which the output achieves the Open Circuit state.*
6. *PCLK and MCLK are required to be integer multiples of the frame sync (FS) frequency. Frame sync is expected to be an accurate 8 kHz pulse train. If PCLK or MCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*
7. *Phase jumps of 81 ns will be present when the master clock frequency is a multiple of 1.544 MHz.*

## SWITCHING WAVEFORMS

**Figure 10. Input and Output Waveforms for AC Tests**

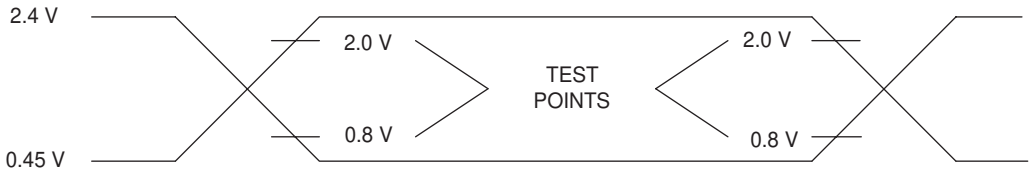



**Figure 11. Microprocessor Interface (Input Mode)**

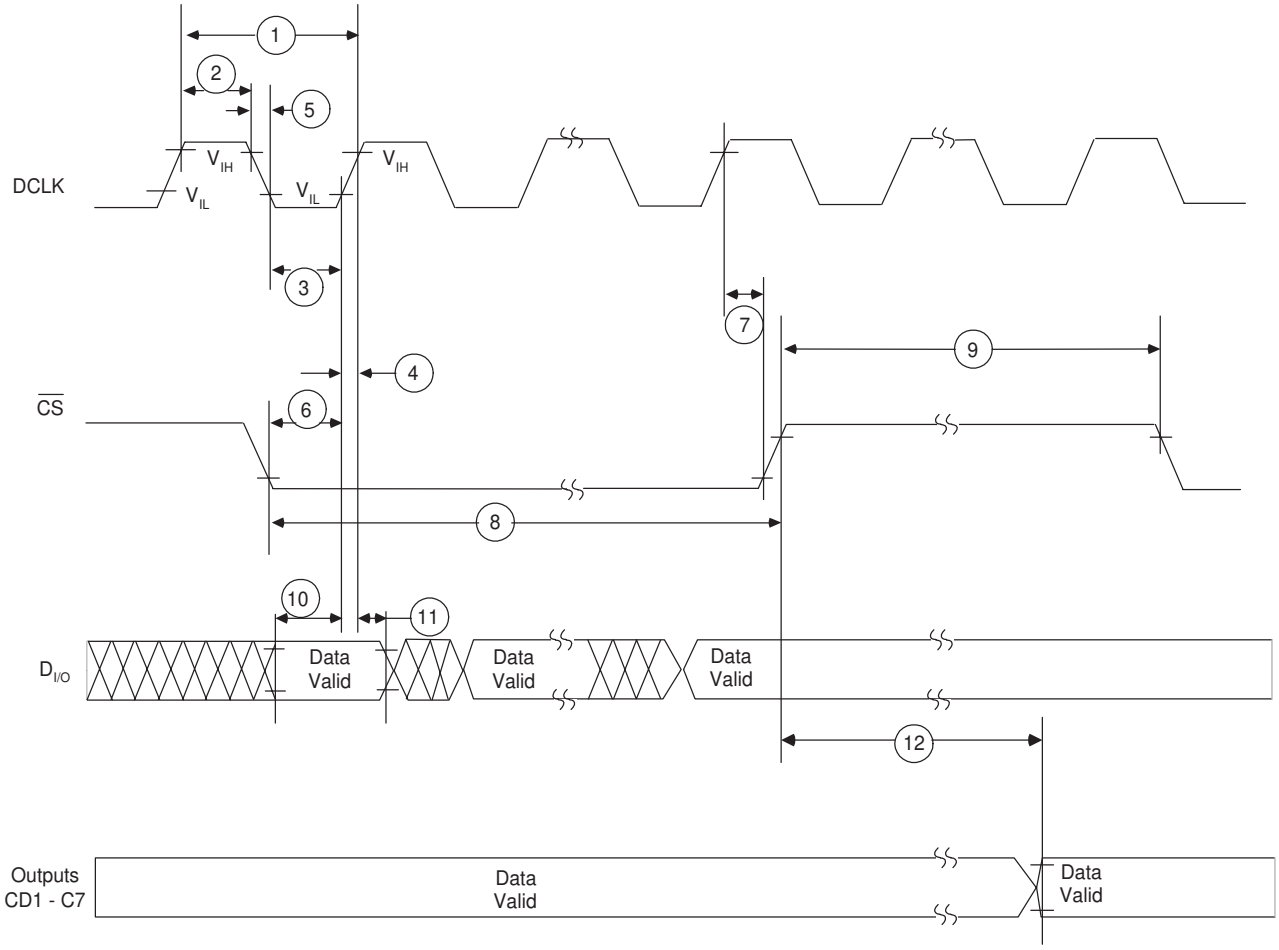


**Figure 12. Microprocessor Interface (Output Mode)**

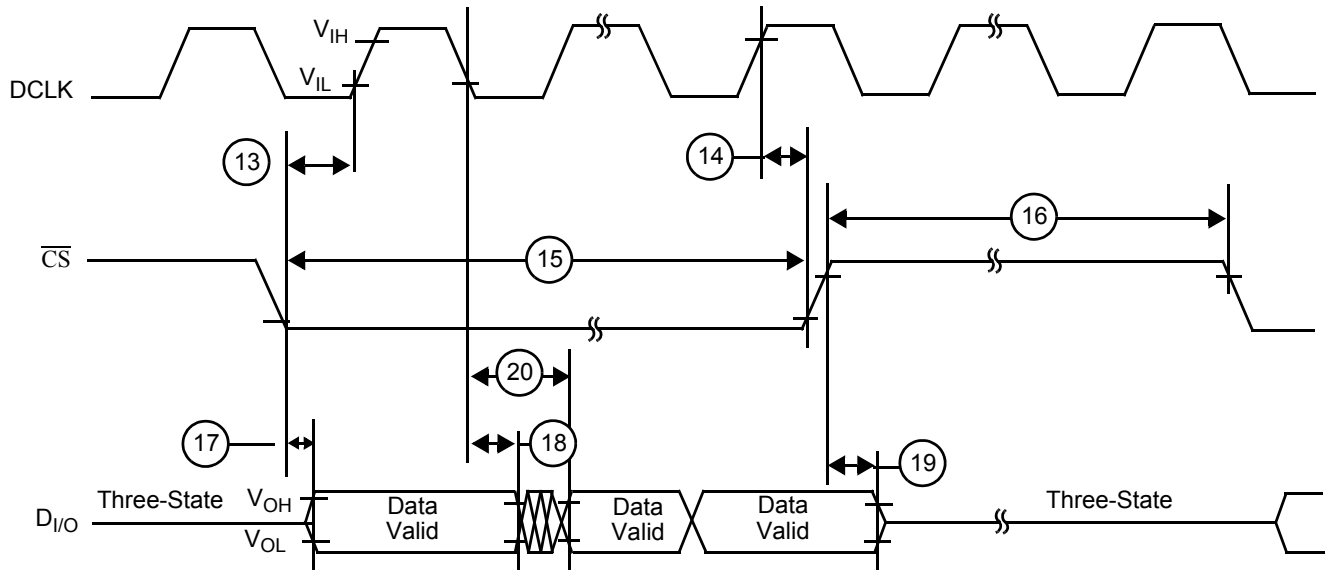



**Figure 13. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)**

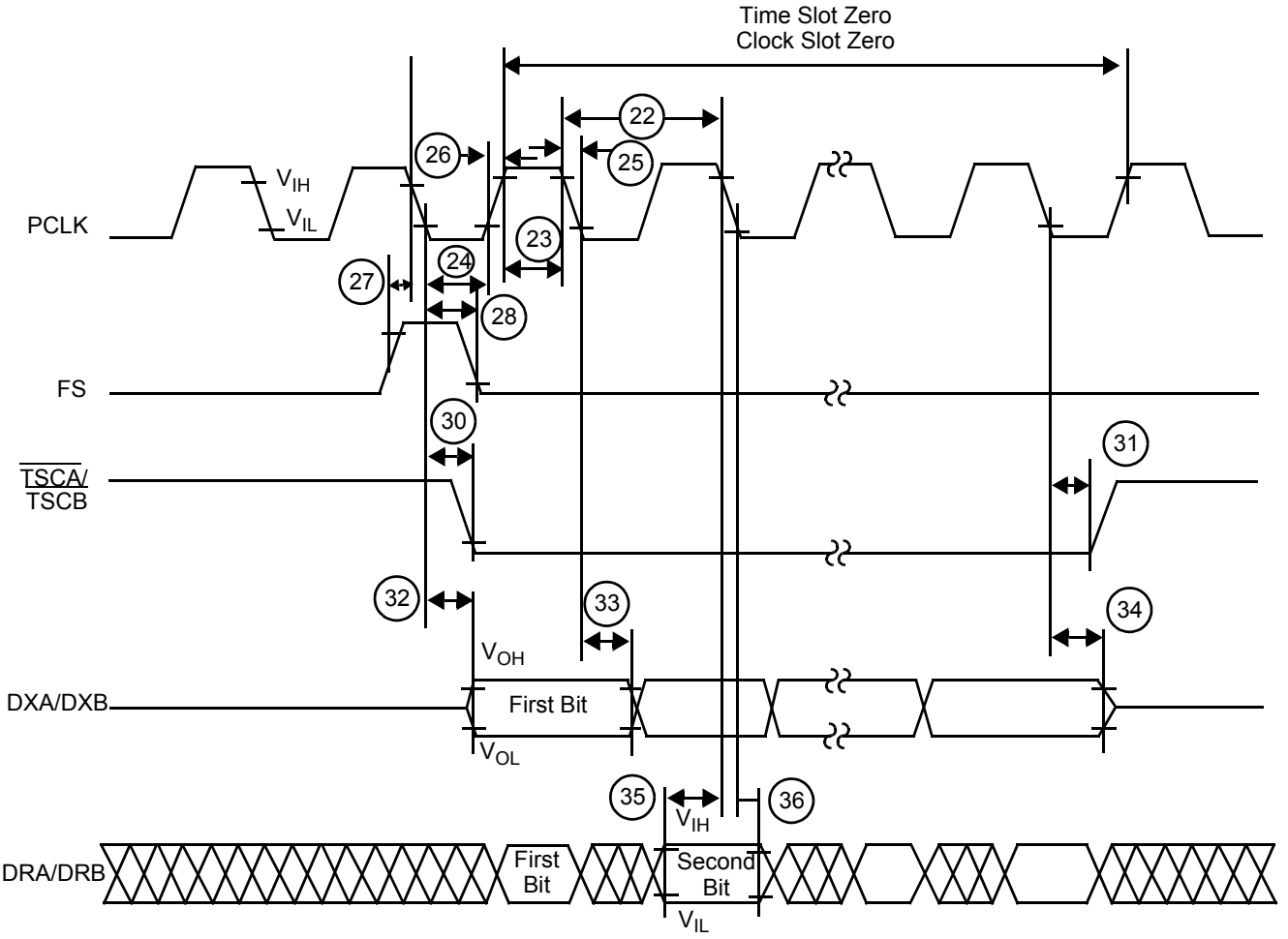


**Figure 14. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)**