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Le58QL02/021/031

Quad Low Voltage Subscriber Line Audio-Processing Circuit

VE580 Series

APPLICATIONS

- **Codec function on telephone switch line cards**

FEATURES

- **Low-power, 3.3 V CMOS technology with 5-V tolerant digital inputs**
- **Software and coefficient compatible to the Le79Q02/ 021/031 QSLAC™ device**
- **Performs the functions of four codec/filters**
- **Software programmable:**
  - SLIC device input impedance
  - Transhybrid balance
  - Transmit and receive gains
  - Equalization (frequency response)
  - Digital I/O pins
  - Programmable debouncing on one input
  - Time slot assigner
  - Programmable clock slot and PCM transmit clock edge options
- **Standard microprocessor interface**
- **A-law, µ-law, or linear coding**
- **Single or Dual PCM ports available**
  - Up to 128 channels (PCLK at 8.192 MHz) per PCM port
  - Optional supervision on the PCM highway
- **1.536, 1.544, 2.048, 3.072, 3.088, 4.096, 6.144, 6.176, or 8.192 MHz master clock derived from MCLK or PCLK**
- **Built-in test modes with loopback, tone generation, and µP access to PCM data**
- **Mixed state (analog and digital) impedance scaling**
- **Performance guaranteed over a 12 dB gain range**
- **Real Time Data register with interrupt (open drain or TTL output)**
- **Supports multiplexed SLIC device outputs**
- **Broadcast state**
- **256 kHz or 293 kHz chopper clock for Legerity SLIC devices with switching regulator**
- **Maximum channel bandwidth for V.90 modems**

RELATED LITERATURE

- **080754 Le58QL061/063 QLSLAC™ Device Data Sheet**
- **080761 QSLAC™ to QLSLAC™ Device Design Conversion Guide**
- **080758 QSLAC™ to QLSLAC™ Guide to New Designs**

ORDERING INFORMATION

Device	Package (Green)[1]	Packing[2]
Le58QL02FJC	44-pin PLCC	Tube
Le58QL021FJC	44-pin PLCC	Tube
Le58QL021BVC	44-pin TQFP	Tray
Le58QL031DJC	32-pin PLCC	Tube

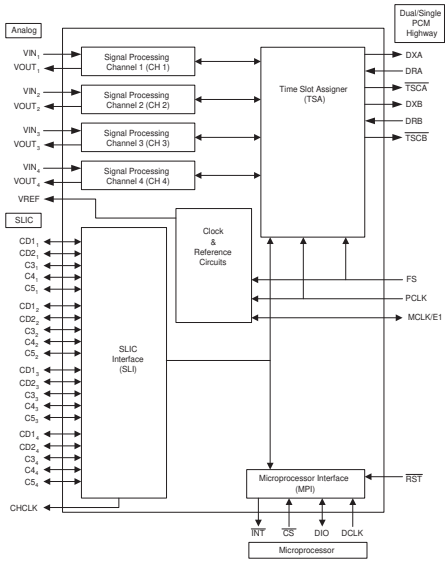
1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

The Le58QL02/021/031 Quad Low Voltage Subscriber Line Audio-Processing Circuit (QLSLAC™) devices integrate the key functions of analog line cards into high-performance, very-programmable, four-channel codec-filter devices. The QLSLAC devices are based on the proven design of Legerity's reliable SLAC™ device families. The advanced architecture of the QLSLAC devices implements four independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the audio-processing function of programmable line cards. The QLSLAC devices are software and coefficient compatible to the QSLAC devices.

Advanced submicron CMOS technology makes the Le58QL02/ 021/031 QLSLAC devices economical, with both the functionality and the low power consumption needed in line card designs to maximize line card density at minimum cost. When used with four Legerity SLIC devices, a QLSLAC device provides a complete software-configurable solution to the BORSCHT functions.

BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The QLSLAC device performs the codec/filter and two-to-four-wire conversion functions required of the subscriber line interface circuitry in telecommunications equipment. These functions involve converting audio signals into digital PCM samples and converting digital PCM samples back into audio signals. During conversion, digital filters are used to band limit the voice signals. All of the digital filtering is performed in digital signal processors operating from a master clock, which can be derived either from PCLK or MCLK.

Four independent channels allow the QLSLAC device to function as four SLAC™ devices. For programming information, each channel has its own enable bit (EC1, EC2, EC3, and EC4) to allow individual channel programming. If more than one Channel Enable bit is High or if all Channel Enable bits are High, all channels enabled will receive the programming information written; therefore, a Broadcast mode can be implemented by simply enabling all channels in the device to receive the information. The Channel Enable bits are contained in the Channel Enable (EC) register, which is written and read using Command 4A/4Bh. The Broadcast mode is useful in initializing QLSLAC devices in a large system.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance, and provide equalization of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the WinSLAC™ software.

Data transmitted or received on the PCM highway can be 8-bit companded code (with an optional 8-bit signaling byte in the transmit direction) or 16-bit linear code. The 8-bit codes appear 1 byte per time slot, while the 16-bit code appears in two consecutive time slots. The compressed PCM codes can be either 8-bit companded A-law or μ-law. The PCM data is read from and written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The transmit clock edge and clock slot can be selected for compatibility with other devices that can be connected to the PCM highway.

Three configurations of the QLSLAC device are offered with single or dual PCM highways. The Le58QL02 and Le58QL021 QLSLAC devices with dual and single PCM highways respectively are available in the 44-pin packages. The Le58QL031JC QLSLAC device is a single PCM highway version in a 32-pin PLCC package.

Table 1. QLSLAC Device Configurations

PCM Highway	Programmable I/O per Channel	Chopper Clock	Package	Part Number
Dual	Four I/O	Yes	44 PLCC	Le58QL02JC
Single	Five I/O	No	44 PLCC/TQFP	Le58QL021JC (or VC)
Single	Two I/O	No	32 PLCC	Le58QL031JC

BLOCK DESCRIPTIONS

Clock and Reference Circuits

This block generates a master clock and a frame sync signal for the digital circuits. It also generates an analog reference voltage for the analog circuits.

Microprocessor Interface (MPI)

This block communicates with the external control microprocessor over a serial interface. It passes user control information to the other blocks, and it passes status information from the blocks to the user. In addition, this block contains the reset circuitry.

Time Slot Assigner (TSA)

This block communicates with the PCM highway, where the PCM highway is a time division mutiplexed bus carrying the digitized voice samples. The block implements programmable time slots and clocking arrangements in order to achieve a first layer of switching. Internally, this block communicates with the Signal Processing Channels (CHx).

Signal Processing Channels (CHx)

These blocks do the transmission processing for the voice channels. Part of the processing is analog and is interfaced to the VIN and VOUT pins. The remainder of the processing is digital and is interfaced to the Time Slot Assigner (TSA) block.

SLIC Device Interface (SLI)

This block communicates digitally with the SLIC device circuits. It sends control bits to the SLIC devices to control modes and to operate LEDs and optocouplers. It also accepts supervision information from the SLIC devices and performs some filtering.

CONNECTION DIAGRAMS

Figure 1. Le58QL02JC 44-Pin PLCC

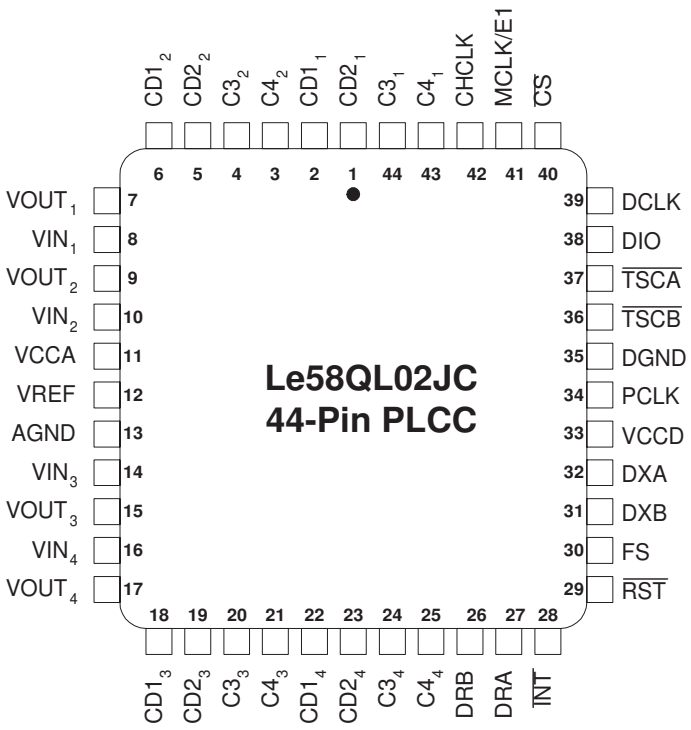


Figure 2. Le58QL021JC 44-Pin PLCC

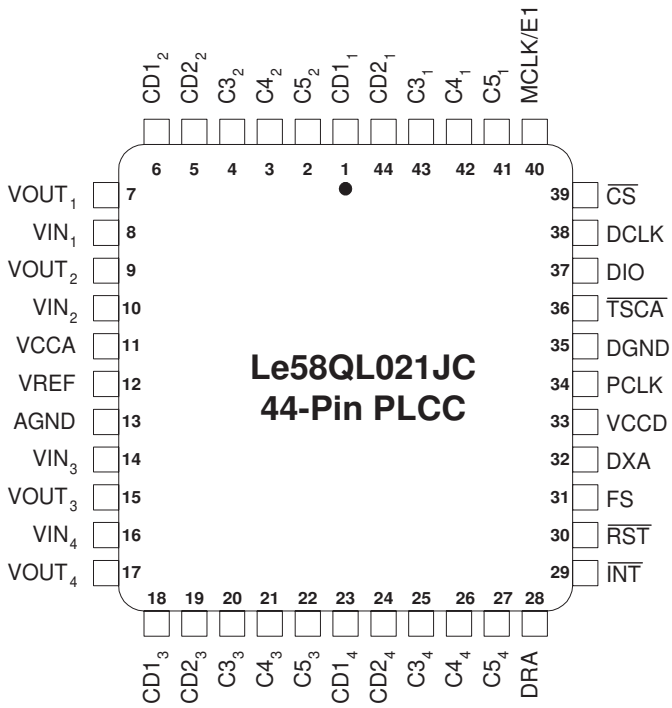


Figure 3. Le58QL031JC 32-Pin PLCC

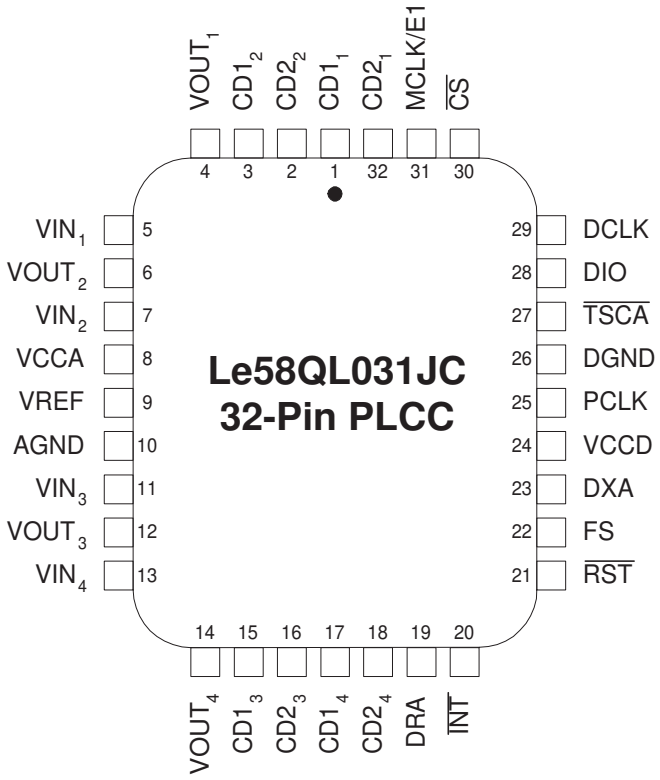
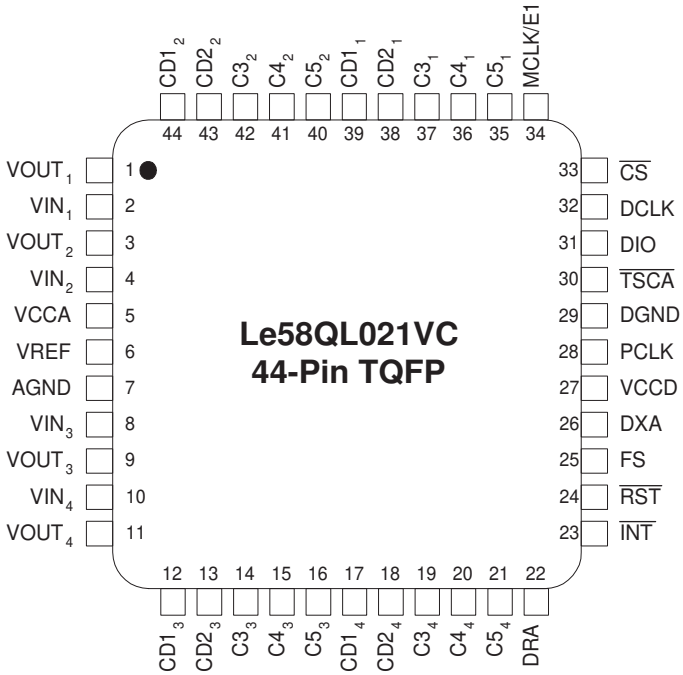


Figure 4. Le58QL021VC 44-Pin PLCC



PIN DESCRIPTIONS

Pin Names	Type	Description
AGND, DGND	Power	Separate analog and digital grounds are provided to allow noise isolation; however, the two grounds are connected inside the part, and the grounds must also be connected together on the circuit board.
$CD1_1$–$CD1_4$, $CD2_1$–$CD2_4$	Inputs/Outputs	Control and Data. CD1 and CD2 are TTL compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of the SLIC drivce or any other device associated with the subscriber line interface. The direction, input or output, is programmed using MPI Command 54/55h. As outputs, CD1 and CD2 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. The output state of CD1 and CD2 is written using MPI Command 52h. As inputs, CD1 and CD2 can be processed by the QLSLAC device (if programmed to do so). CD1 can be debounced before it is made available to the system. The debounce time is programmable from 0 to 15 ms in 1 ms increments using MPI Command C8/C9h. CD2 can be filtered using the up/down counter facility and programming the sampling interval using MPI Command E8/E9h. Additionally, CD1 can be demultiplexed into two separate inputs using the E1 demultiplexing function. The E1 demultiplexing function of the QLSLAC device was designed to interface directly to Legerity SLIC devices supporting the ground key function. With the proper Legerity SLIC device and the E1 function of the QLSLAC device enabled, the CD1 bit can be demultiplexed into an Off-Hook/Ring Trip signal and Ground Key signal. In the demultiplex mode, the second bit, Ground Key, takes the place of the CD2 as an input. The demultiplexed bits can be debounced (CD1) or filtered (CD2) as explained previously. A more complete description of CD1, CD2, debouncing, and filtering functions is contained in *Operating the QLSLAC Device*, on page 27. Once the CD1 and CD2 inputs are processed (Debounced, Filtered and/or Demultiplexed) by the QLSLAC device, the information can be accessed by the system in two ways: 1) on a per channel basis along with C3, C4, and C5 of the specific channel using MPI Command 53h, or 2) by using MPI Command 4D/4Fh, which obtain the CD1 and CD2 bits from all four channels simultaneously. This feature reduces the processor overhead and the time required to retrieve time-critical signals from the line circuits, such as off-hook and ring trip. With this feature, hookswitch status and ring trip information, for example, can be obtained from all four channels of a QLSLAC device with one read command.
$C3_1$–$C3_4$, $C4_1$–$C4_4$, $C5_1$–$C5_4$	Inputs/Outputs	Control. C3, C4, and C5 are TTL-compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of the SLIC device or any other device associated with subscriber line interface. The direction, input or output, is programmed using MPI Command 54/55h. As outputs, C3, C4, and C5 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. The output state of C3, C4, and C5 is written using MPI Command 52h. As inputs, C3, C4, and C5 can be accessed by the system by using MPI Command 53h. The Le58QL021 QLSLAC device contains a single PCM highway and five programmable I/Os per channel (CD1, CD2, C3, C4, and C5) in a 44-pin PLCC or TQFP package. In the Le58QL02 QLSLAC device, the $C5_1$, $C5_2$, $C5_3$, and $C5_4$ I/Os are eliminated, enabling dual PCM highways and a chopper clock output in a 44-pin PLCC or TQFP package. In the Le58QL031 QLSLAC device, the $C3_1$–$C5_1$, $C3_2$–$C5_2$, $C3_3$–$C5_3$, and $C3_4$–$C5_4$ I/Os are eliminated, enabling a single PCM highway and two control and data I/Os (CD1, CD2) per channel in a 32-pin PLCC package.
CHCLK	Output	Chopper Clock. This output provides a 256 kHz or a 292.57 kHz, 50% duty cycle, TTL-compatible clock for use by up to four SLIC devices with built-in switching regulators. The CHCLK frequency is synchronous to the master clock, but the phase relationship to the master clock is random. The chopper clock is not available in all package types.
$\overline{CS}$	Input	Chip Select. The Chip Select input (active Low) enables the device so that control data can be written to or read from the part. The channels selected for the write or read operation are enabled by writing 1 s to the appropriate bits in the Channel Enable Register of the QLSLAC device prior to the command. See EC1, EC2, EC3, and EC4 of the Command *4A/4Bh Write/Read Channel Enable and Operating Mode Register*, on page 44 for more information. If Chip Select is held Low for 16 rising edges of DCLK, a hardware reset is executed when Chip Select returns High.
DCLK	Input	Data Clock. The Data Clock input shifts data into and out of the microprocessor interface of the QLSLAC device. The maximum clock rate is 8.192 MHz.
DIO	Input/Output	Data. Control data is serially written into and read out of the QLSLAC device via the DIO pin, with the most significant bit first. The Data Clock determines the data rate. DIO is high impedance except when data is being transmitted from the QLSLAC device.

Pin Names	Type	Description
DRA, DRB	Inputs	PCM Data Receive A/B. The PCM data for channels 1, 2, 3, and 4 is serially received on either the DRA or DRB port during user-programmed time slots. Data is always received with the most significant bit first. For compressed signals, 1 byte of data for each channel is received every 125 µs at the PCLK rate. In the Linear state, two consecutive bytes of data for each channel are received every 125 µs at the PCLK rate. DRB is not available on all package types.
DXA, DXB	Outputs	PCM Data Transmit. The transmit data from channels 1, 2, 3, and 4 is sent serially out on either the DXA or DXB port or both ports during user-programmed time slots. Data is always transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit (16-bit in Linear or PCM Signaling state) bursts at the PCLK rate. DXA and DXB are High impedance between time slots, while the device is in the Inactive state with no PCM signaling, or while the Cutoff Transmit Path bit (CTP) is on. DXB is not available on all package types.
FS	Input	Frame Sync. The Frame Sync pulse is an 8 kHz signal that identifies Time Slot 0, Clock Slot 0 of a system's PCM frame. The QLSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.
$\overline{INT}$	Output	Interrupt. $\overline{INT}$ is an active Low output signal which is programmable as either TTL compatible or open drain. The $\overline{INT}$ output goes Low any time one of the input bits in the Real Time Data register changes state and is not masked. It also goes Low any time new transmit data appears if this interrupt is armed. $\overline{INT}$ remains Low until the appropriate register is read via the microprocessor interface, or the QLSLAC device receives either a software or hardware reset. The individual CD_{xy} bits in the Real Time Data register can be masked from causing an interrupt by using MPI Command 6C/6Dh. The transmit data interrupt must be armed with a bit in the Operating Conditions register.
MCLK/E1	Input/Output	Master Clock (Input)/Enable CD1 Multiplex (Output). The Master Clock can be a 1.536 MHz, 1.544 MHz, or 2.048 MHz (times 1, 2, or 4) clock for use by the digital signal processor. If the internal clock is derived from the PCM Clock Input (PCLK), this pin can be used as an E1 output to control Legerity SLIC devices having multiplexed hookswitch and ground-key detector outputs.
PCLK	Input	PCM Clock. The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz for dual PCM highway versions and 256 kHz for single PCM highway versions. The minimum clock rate must be doubled if Linear state or PCM signaling is used. PCLK frequencies between 1.03 MHz and 1.53 MHz are not allowed. Optionally, the digital signal processor clock can be derived from PCLK rather than MCLK.
$\overline{RST}$	Input	Reset. A logic Low signal at this pin resets the QLSLAC device to its default state. The $\overline{RST}$ pin may be tied to VCCD if it is not needed in the system.
$\overline{TSCA}$, $\overline{TSCB}$	Outputs	Time Slot Control. The Time Slot Control outputs are open drain outputs (requiring pull-up resistors to VCCD) and are normally inactive (High impedance). $\overline{TSCA}$ or $\overline{TSCB}$ is active (Low) when PCM data is transmitted on the DXA or DXB pin respectively.
VCCA, VCCD	Power	Analog and digital power supply inputs. VCCA and VCCD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VCC power supply pins should be connected together at the connector of the printed circuit board.
VIN_1–VIN_4	Inputs	Analog Input. The analog voice band signal is applied to the VIN input of the QLSLAC device. The VIN input is biased at VREF by a large internal resistor. The audio signal is sampled, digitally processed and encoded, and then made available at the TTL-compatible PCM output (DXA or DXB). If the digitizer saturates in the positive or negative direction, VIN is pulled by a reduced resistance toward AGND or VCCD, respectively. VIN_1 is the input for channel 1, VIN_2 is the input for channel 2, VIN_3 is the input for channel 3, and VIN_4 is the input for channel 4.
$VOUT_1$–$VOUT_4$	Outputs	Analog Output. The received digital data at DRA or DRB is processed and converted to an analog signal at the VOUT pin. $VOUT_1$ is the output from channel 1, $VOUT_2$ is the output for channel 2, $VOUT_3$ is the output from channel 3, and $VOUT_4$ is the output for channel 4. The VOUT voltages are referenced to VREF.
VREF	Output	Analog Voltage Reference. The VREF output is provided in order for an external capacitor to be connected from VREF to ground, filtering noise present on the internal voltage reference. VREF is buffered before it is used by internal circuitry. The voltage on VREF and the output resistance are given in *Electrical Characteristics*, on page 13. The leakage current in the capacitor must be low.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Storage Temperature	–60° C < T_A < +125° C
Ambient Temperature, under Bias	–40° C < T_A < +85° C
Ambient relative humidity (non condensing)	5 to 95%
V_{CCA} with respect to AGND	–0.4 to + 4.0 V
V_{CCA} with respect to VCCD	±0.4 V
V_{CCD} with respect to DGND	–0.4 to + 4.0 V
V_{IN} with respect to AGND	–0.4 V to (V_{CCA} + 0.4 V)
AGND with respect to DGND	±50 mV
Digital pins with respect to DGND	–0.4 to 5.5 V or VCCD + 2.37 V, whichever is smaller
Total combined CD1–C5 current per device: Source from VCCD Sink into DGND	 40 mA 40 mA
Latch up immunity (any pin)	± 100 mA
Total VCC current if rise rate of VCC > 0.4 V/µs	0.5 A

Package Assembly

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 Table 4-2 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Legerity guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40° C < T_A < +85° C
Ambient Relative Humidity	15 to 85%

Electrical Ranges

Analog Supply V_{CCA}	+3.3 V ± 5% V_{CCD} ± 50 mV
Digital Supply V_{CCD}	+3.3 V ± 5%
DGND	0 V
AGND	±10 mV
CFIL Capacitance: VREF to AGND	0.1 µF ± 20%
Digital Pins	DGND to +5.25 V

ELECTRICAL CHARACTERISTICS

Typical values are for TA = 25º C and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in Operating Ranges, except where noted.

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
V_{IL}	Digital Input Low voltage			0.8	V	
V_{IH}	Digital Input High voltage	2.0				
I_{IL}	Digital Input leakage current 0 < V < VCCD Otherwise	 –7 –120		 +7 +180	µA	
V_{HYS}	Digital Input hysteresis	0.16	0.25	0.34	V	
V_{OL}	Digital Output Low voltage CD1–C5 (I_{OL} = 4 mA) CD1–C5 (I_{OL} = 8 mA) $\overline{TSCA}$, $\overline{TSCB}$ (I_{OL} =14 mA) Other digital outputs (I_{OL} = 2 mA)			 0.4 0.8 0.4 0.4	V	1
V_{OH}	Digital Output High voltage CD1–C5 (I_{OH} = 4 mA) CD1–C5 (I_{OH} = 8 mA) Other digital outputs (I_{OH} = 400 µA)	 V_{CCD} – 0.4 V V_{CCD} – 0.8 V 2.4			V	1
I_{OL}	Digital Output leakage current (H_I Z state) 0 < V < VCCD Otherwise	 –7 –120		 +7 +180	µA	
GIN	Input attenuator gain DGIN = 0 DGIN = 1		 0.6438 1		V/V	
V_{IR}	Analog input voltage range (Relative to VREF) AX = 0 dB, attenuator on (DGIN = 0) AX = 6.02 dB, attenuator on (DGIN = 0) AX = 0 dB, attenuator off (DGIN = 1) AX = 6.02 dB, attenuator off (DGIN = 1)		 ±1.584 ±0.792 ±1.02 ±0.51		Vpk	
V_{IOS}	Offset voltage allowed on VIN	–50		50	mV	
Z_{IN}	Analog input impedance to VREF, 300 to 3400 Hz	600		1400	kΩ	
I_{IP}	Current into analog input for an input voltage of 3.3 V	50		115	µA	2
I_{IN}	Current out of analog input for an input voltage of –0.3 V	50		130		2
Z_{OUT}	VOUT output impedance		1	10	Ω	
CL_{OUT}	Allowable capacitance, V_{OUT} to AGND			500	pF	
I_{OUT}	VOUT output current (F< 3400 Hz)	–4		4	mApk	3
V_{REF}	VREF output open circuit voltage (leakage < 20 nA)	1.43	1.5	1.57	V	
Z_{REF}	VREF output impedance (F < 3400 Hz)	70		130	kΩ	
V_{OR}	VOUT voltage range(AR = 0 dB) (Relative to VREF)(AR = 6.02 dB)		 ±1.02 ±0.51		Vpk	
V_{OOS}	VOUT offset voltage (AISN off)	–40		40	mV	4
V_{OOSA}	VOUT offset voltage (AISN on)	–80		80		
G_{AISN}	AISN gain - expected gain (input = 0 dBm0, 1014 Hz) Attenuator on (DGIN = 0) Attenuator off (DGIN = 1)	 –0.016 –0.024		 0.016 0.024	V/V	
PD	Power dissipation All channels active 1 channel active All channels inactive		 130 40 13	 170 80 18	mW	
C_I	Digital Input capacitance			10	pF	
C_O	Digital Output capacitance			10		
PSRR	Power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	40			dB	

Notes:

1. *The CD1, CD2, C3–C5 outputs are resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.*
2. *When the digitizer saturates, a resistor of 50 kΩ ±20 kΩ is connected either to AGND or to VCCA as appropriate to discharge the coupling capacitor.*
3. *When the QLSLAC device is in the Inactive state, the analog output will present either a VREF DC output level through a 15 kΩ resistor (VMODE = 0) or a high impedance (VMODE = 1).*
4. *If there is an external DC path from VOUT to VIN with a gain of G_{DC} and the AISN has a gain of h_{AISN}, then the output offset will be multiplied by 1 / [1 – (h_{AISN} • G_{DC})].*
5. *Power dissipation in the Inactive state is measured with all digital inputs at VIH = VCCD and VIL = DGND and with no load connected to VOUT1, VOUT2, VOUT3, or VOUT4.*

Transmission Characteristics

Table 2. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit (DGIN = 0)	Transmit (DGIN = 1)	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.7804	0.5024	0.5024	Vrms
μ-law digital mW or equivalent (0 dBm0)	0.7746	0.4987	0.4987	
±22,827 peak linear coded sine wave	0.7804	0.5024	0.5024	

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the GX gain from 0 dB to 12 dB, the GR loss from 0 dB to 12 dB, and the input attenuator (GIN) on or off.

Description	Test Conditions		Min	Typ	Max	Unit	Note
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz AX = AR = 0 dB 0 to 85° C –40° C AX = +6.02 dB and/or AR = –6.02 dB 0 to 85° C –40° C		 –0.25 –0.30 –0.30 –0.40		 +0.25 +0.30 +0.30 +0.40	dB	
Gain accuracy digital-to-digital			–0.25		+0.25		
Gain accuracy analog-to-analog			–0.25		+0.25		
Attenuation distortion	300 Hz to 3 kHz		–0.125		+0.125		1
Single frequency distortion					–46		2
Second harmonic distortion, D-A	GR = 0 dB				–55		
Idle channel noise Analog out Digital out	Digital looped back Digital input = 0 Digital input = 0 Analog V_{IN} = 0 VAC Analog V_{IN} = 0 VAC	weighted unweighted A-law μ-law A-law μ-law		 0 0	–68 –55 –78 12 –68 16	dBm0p dBm0 dBm0p dBrnc0 dBm0p dBrnc0	3 3 3 3, 6 3 3, 6
Crosstalk TX to RX same channel RX to TX	0 dBm0 0 dBm0	300 to 3400 Hz 300 to 3400 Hz			–75 –75	dBm0	
Crosstalk between channels TX or RX to TX TX or RX to RX	0 dBm0 SLIC imped. < 300 Ω	 1014 Hz, Average 1014 Hz, Average			 –76 –78	dBm0	4
End-to-end group delay	B = Z = 0; X = R = 1				678	μs	5

Notes:

1. *See Figure 5 and Figure 6.*
2. *0 dBm0 input signal, 300 Hz to 3400 Hz; measurement at any other frequency, 300 Hz to 3400 Hz.*
3. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
4. *The weighted average of the crosstalk is defined by the following equation, where C(f) is the crosstalk in dB as a function of frequency, f_N = 3300 Hz, f_1 = 300 Hz, and the frequency points (f_j, j = 2..N) are closely spaced:*

$$\text{Average} = 20 \bullet \log \left[\frac{\sum_{j} \frac{10^{\frac{1}{20} \bullet C(f_j)} + 10^{\frac{1}{20} \bullet C(f_{j-1})}}{2} \bullet \log \left(\frac{f_j}{f_{j-1}} \right)}{\log \left(\frac{f_N}{f_1} \right)} \right]$$

5. *The End-to-End Group Delay is the sum of the transmit and receive group delays (both measured using the same time and clock slot).*
6. *Typical values not tested in production.*

Attenuation Distortion

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 5 and Figure 6. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

Figure 5. Transmit Path Attenuation vs. Frequency

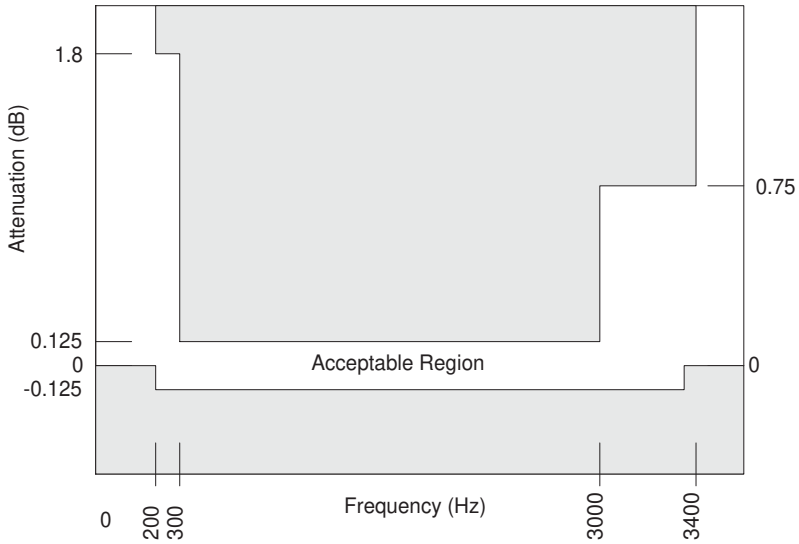
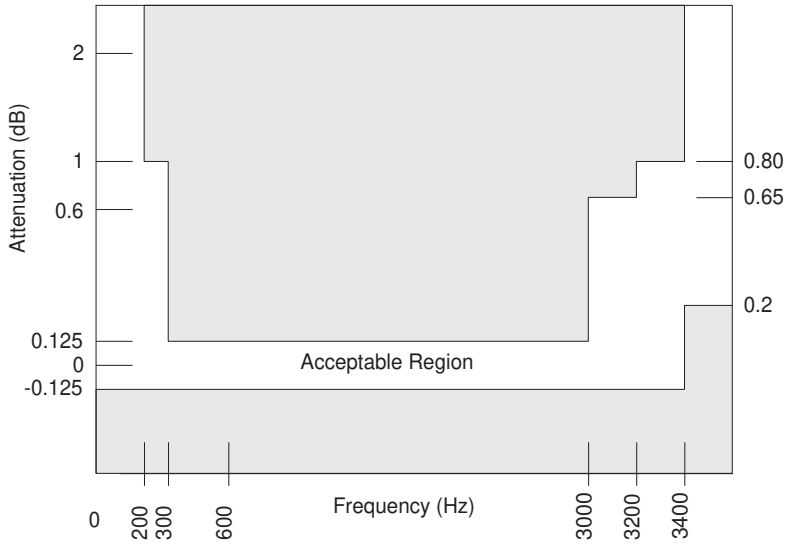


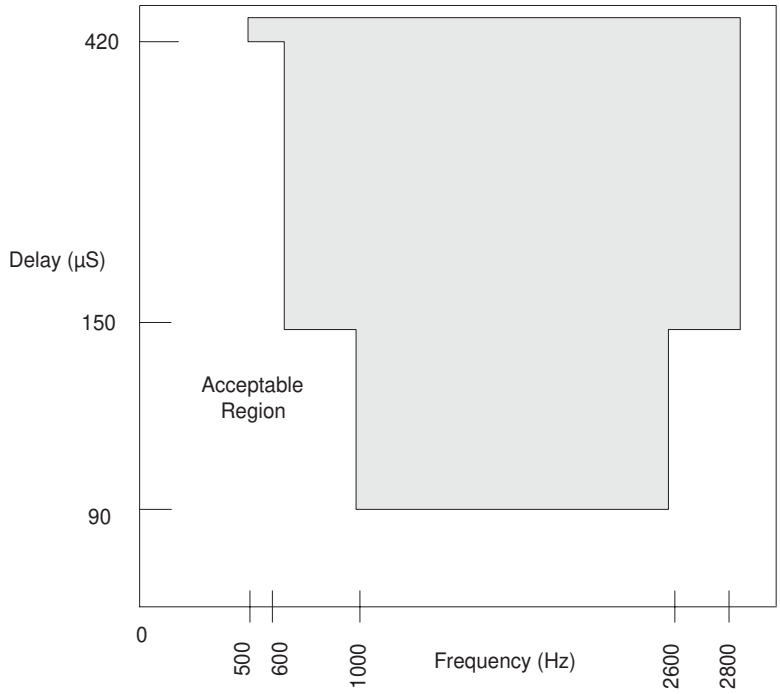
Figure 6. Receive Path Attenuation vs. Frequency



Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 7. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

Figure 7. Group Delay Distortion



Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 8 (A-law) and Figure 9 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 8. A-law Gain Linearity with Tone Input (Both Paths)

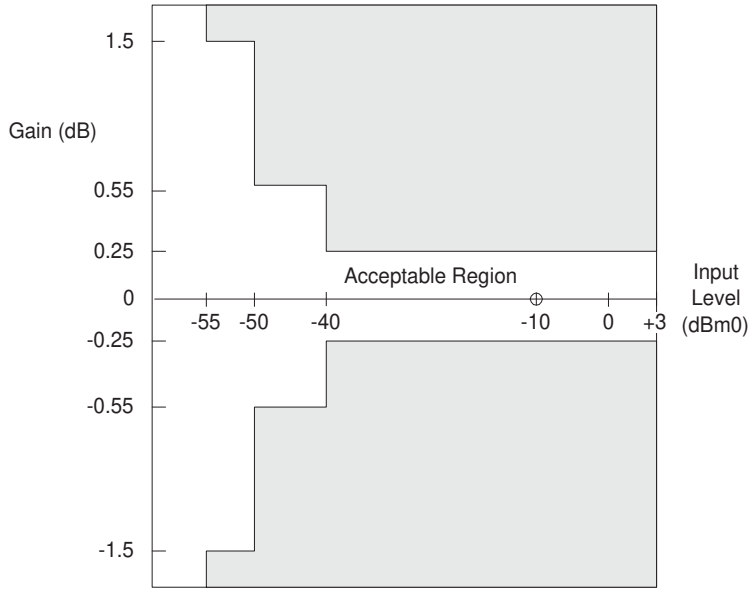
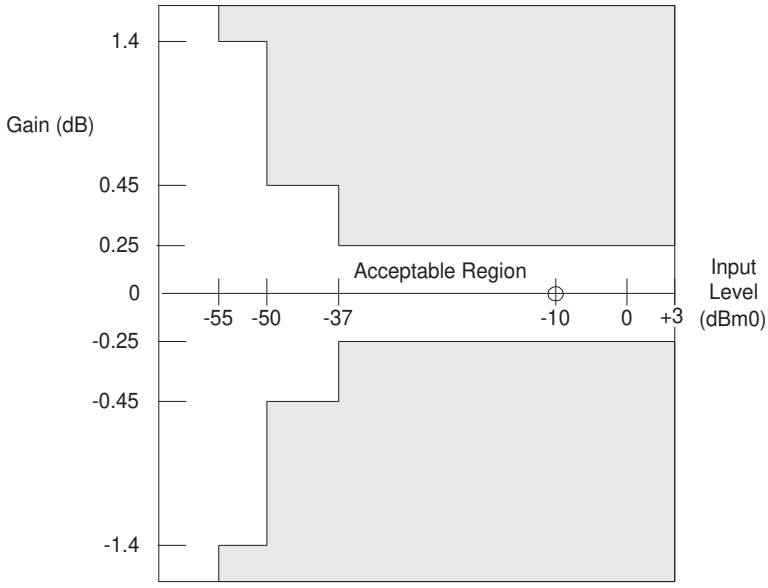


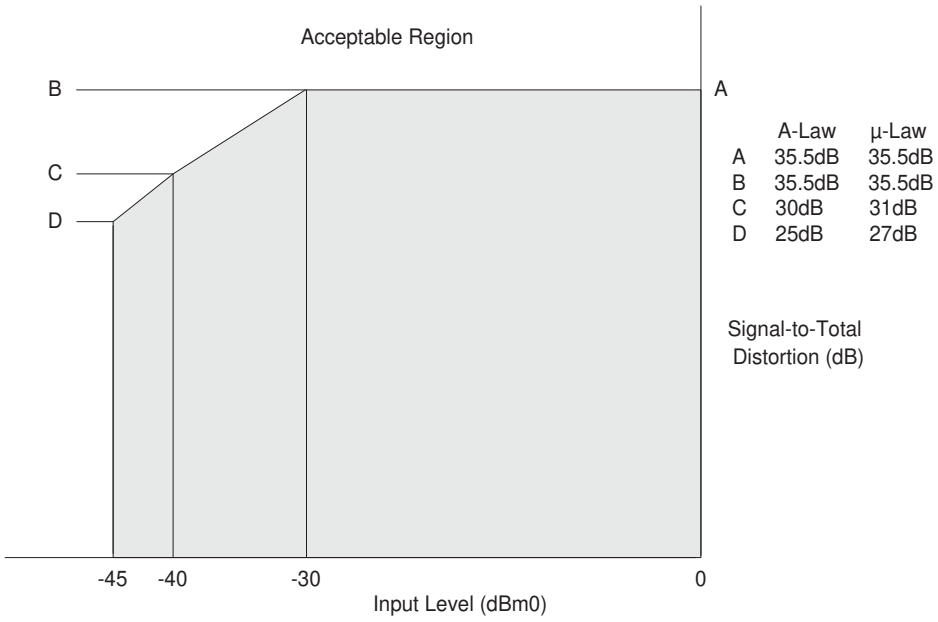
Figure 9. µ-law Gain Linearity with Tone Input (Both Paths)



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 10 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Figure 10. Total Distortion with Tone Input (Both Paths)



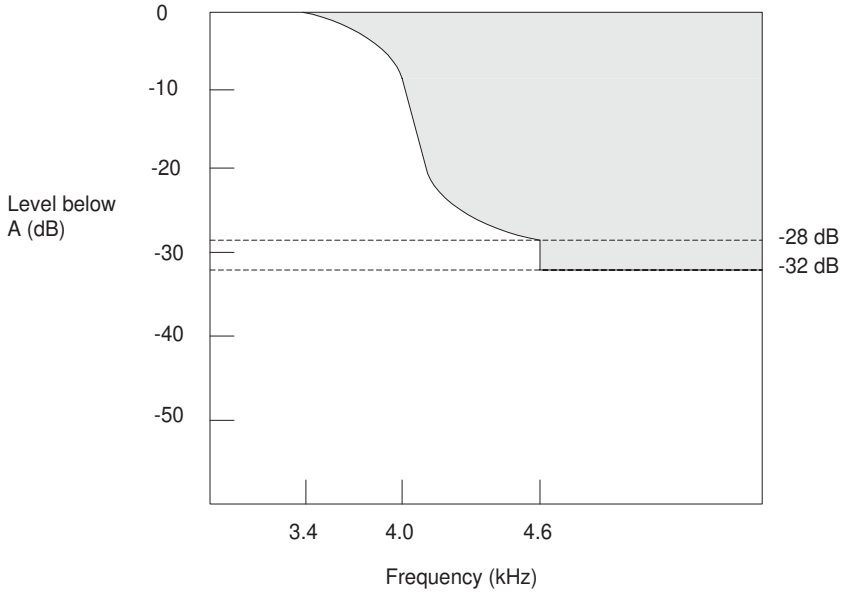
	A-Law	µ-Law
A	35.5dB	35.5dB
B	35.5dB	35.5dB
C	30dB	31dB
D	25dB	27dB

Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 11
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB

Figure 11. Discrimination Against Out-of-Band Signals



Note:

The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)$$

Discrimination Against 12- and 16-kHz Metering Signals

If the QLSLAC device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones also may appear at the VIN terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the analog input voltage range.

Spurious Out-of-Band Signals at the Analog Output

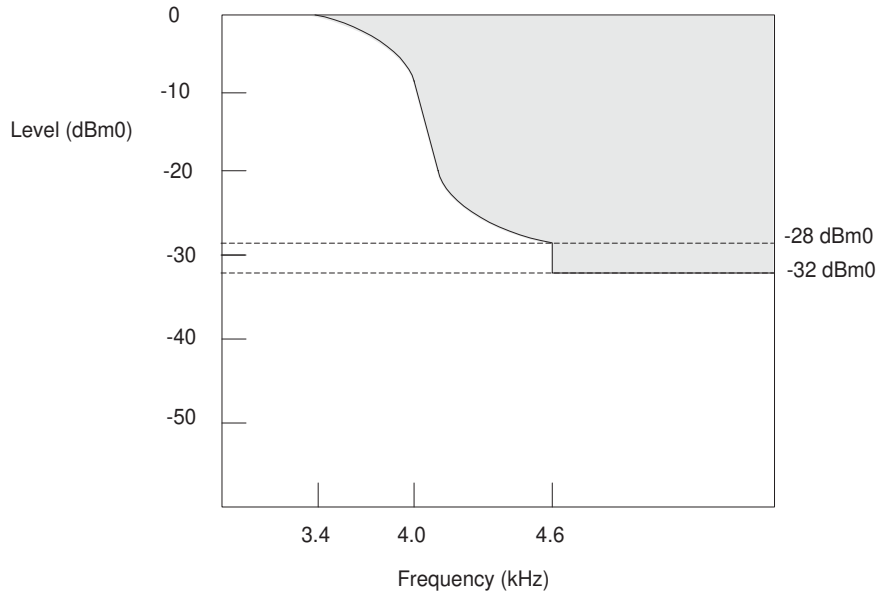
With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 12. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

Figure 12. Spurious Out-of-Band Signals

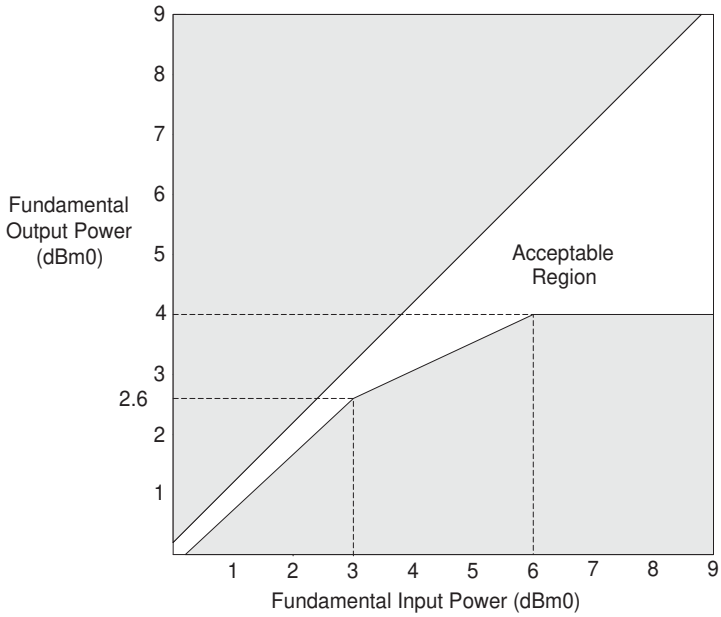


Overload Compression

Figure 13 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. 1.2 dB < GX ≤ + 12 dB
2. –12 dB ≤ GR < –1.2 dB
3. Digital voice output connected to digital voice input.
4. Measurement analog-to-analog.

Figure 13. Analog-to-Analog Overload Compression



SWITCHING CHARACTERISTICS

The following are the switching characteristics over operating range (unless otherwise noted). Min and max values are valid for all digital outputs with a 115 pF load, except CD1–C5 with a 30 pF load. (See Figure 15 and Figure 16 for the microprocessor interface timing diagrams.)

Microprocessor Interface

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122			ns	
2	t_{DCH}	Data clock HIGH pulse width	48				
3	t_{DCL}	Data clock LOW pulse width	48				
4	t_{DCR}	Rise time of clock			25		
5	t_{DCF}	Fall time of clock			25		
6	t_{ICSS}	Chip select setup time, Input mode	30		t_{DCY}–10		
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH}–20		
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$			
9	t_{ICSO}	Chip select off time, Input mode	2500				1
10	t_{IDS}	Input data setup time	25				
11	t_{IDH}	Input data hold time	30				
12	t_{OLH}	SLIC device output latch valid			2500		
13	t_{OCSS}	Chip select setup time, Output mode	30		t_{DCY}–10		
14	t_{OCSH}	Chip select hold time, Output mode	0		t_{DCH}–20		
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$			
16	t_{OCSO}	Chip select off time, Output mode	2500				1
17	t_{ODD}	Output data turn on delay			50		2
18	t_{ODH}	Output data hold time	3				
19	t_{ODOF}	Output data turn off delay			50		
20	t_{ODC}	Output data valid			50		
21	t_{RST}	Reset pulse width	50			µs	

PCM Interface

PCLK not to exceed 8.192 MHz.

Pull-up resistors to V_{CCD} of 240 Ω are attached to $\overline{TSCA}$ and $\overline{TSCB}$. (See Figure 17 and Figure 18 for the PCM interface timing diagrams.)

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	122			ns	3
23	t_{PCH}	PCM clock HIGH pulse width	48				
24	t_{PCL}	PCM clock LOW pulse width	48				
25	t_{PCF}	Fall time of clock			15		
26	t_{PCR}	Rise time of clock			15		
27	t_{FSS}	FS setup time	25		t_{PCY}–30		
28	t_{FSH}	FS hold time	50				
30	t_{TSD}	Delay to $\overline{TSC}$ valid	5		80		4
31	t_{TSO}	Delay to $\overline{TSC}$ off	5		80		4, 5
32	t_{DXD}	PCM data output delay	5		70		
33	t_{DXH}	PCM data output hold time	5		70		
34	t_{DXZ}	PCM data output delay to High-Z	5		70		
35	t_{DRS}	PCM data input setup time	25				
36	t_{DRH}	PCM data input hold time	5				

Master Clock

(See Figure 19, *Master Clock Timing*, on page 26.)

No.	Symbol	Parameter	Min	Typ	Max	Unit	Notes
37	J_{MCY}	Master clock jitter			50	ns	6
38	t_{MCR}	Rise time of clock			15		
39	t_{MCF}	Fall time of clock			15		
40	t_{MCH}	MCLK HIGH pulse width	48				
41	t_{MCL}	MCLK LOW pulse width	48				

Auxiliary Output Clocks

No.	Symbol	Parameter	Min	Typ	Max	Unit	Notes
42	f_{CHP}	Chopper clock frequency CHP = 0 CHP = 1		256 292.57		kHz	7
42A	DC_{CHP}	Chopper click duty cycle		50		%	7
43	f_{E1}	E1 output frequency (CMODE = EE1 = 1)		4.923		kHz	7
44	t_{E1}	E1 pulse width (CMODE = EE1 = 1)		31.25		µs	7

Notes:

1. *If CFAIL = 1 (Command 55h), GX, GR, Z, B1, X, R, and B2 coefficients must not be written or read without first deactivating all channels or switching them to default coefficients; otherwise, a chip select off time of 25 µs is required.*
2. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
3. *The PCM clock frequency must be an integer multiple of the frame sync frequency. The maximum allowable PCM clock frequency is 8.192 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz in Companded state and 256 kHz in Linear state, PCM Signaling state, or double PCLK state. The minimum PCM clock rates should be doubled for parts with only one PCM highway in order to allow simultaneous access to all four channels.*
4. *$\overline{TSC}$ is delayed from FS by a typical value of $N \bullet t_{PCY}$, where N is the value stored in the time/clock-slot register.*
5. *t_{TSO} is defined as the time at which the output achieves the Open Circuit state.*
6. *PCLK and MCLK are required to be integer multiples of the frame sync (FS) frequency. Frame sync is expected to be an accurate 8 kHz pulse train. If PCLK or MCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*
7. *Phase jumps of 81 nS will be present when the master clock frequency is a multiple of 1.544 MHz.*

SWITCHING WAVEFORMS

Figure 14. Input and Output Waveforms for AC Tests

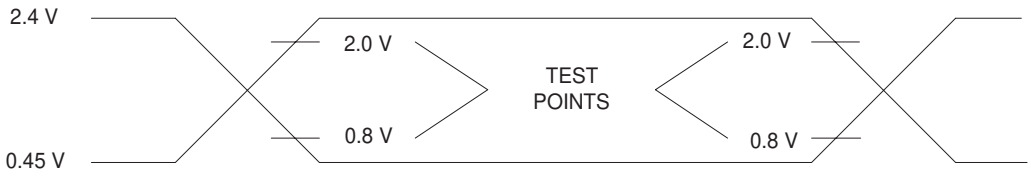


Figure 15. Microprocessor Interface (Input Mode)

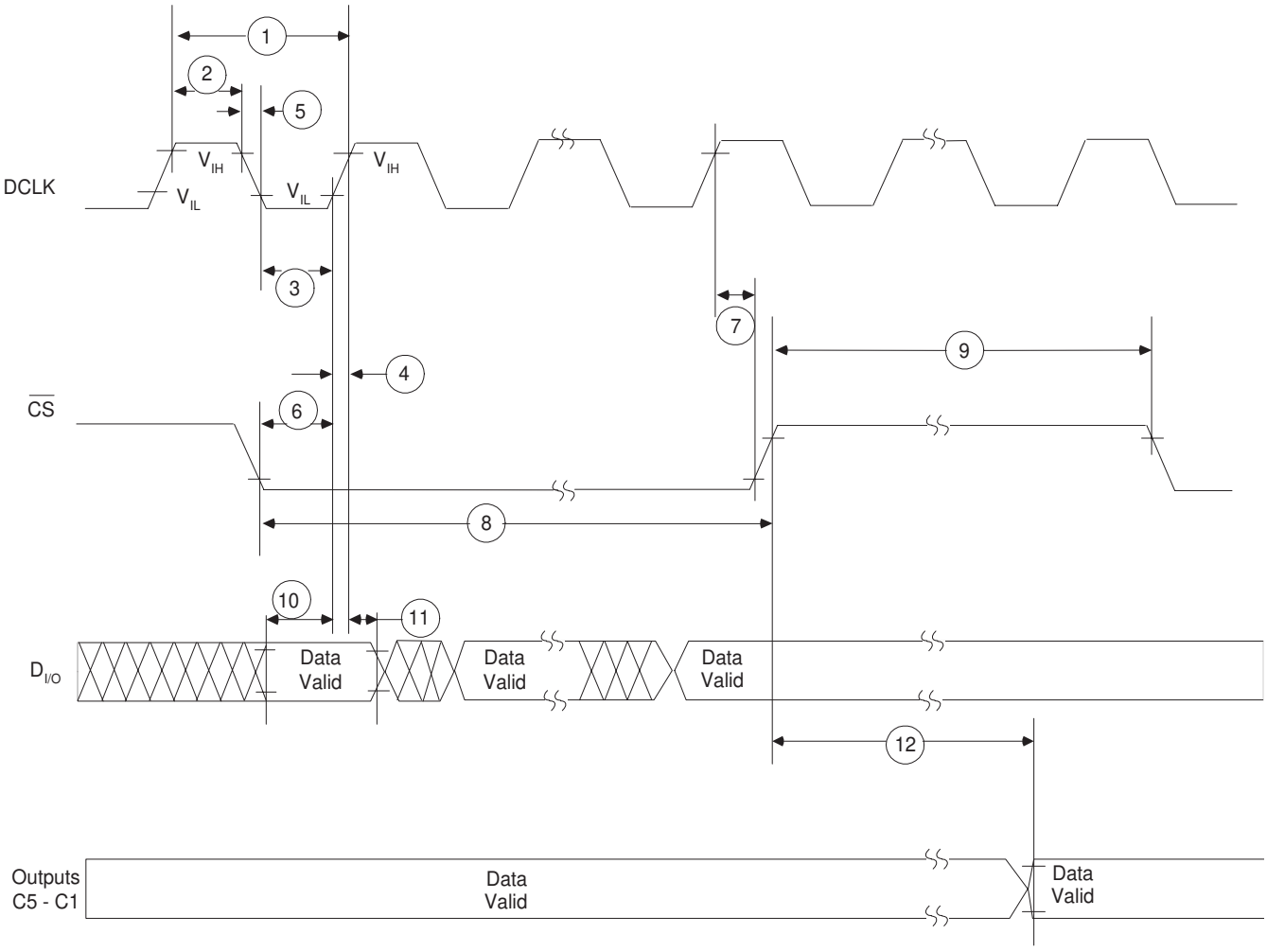


Figure 16. Microprocessor Interface (Output Mode)

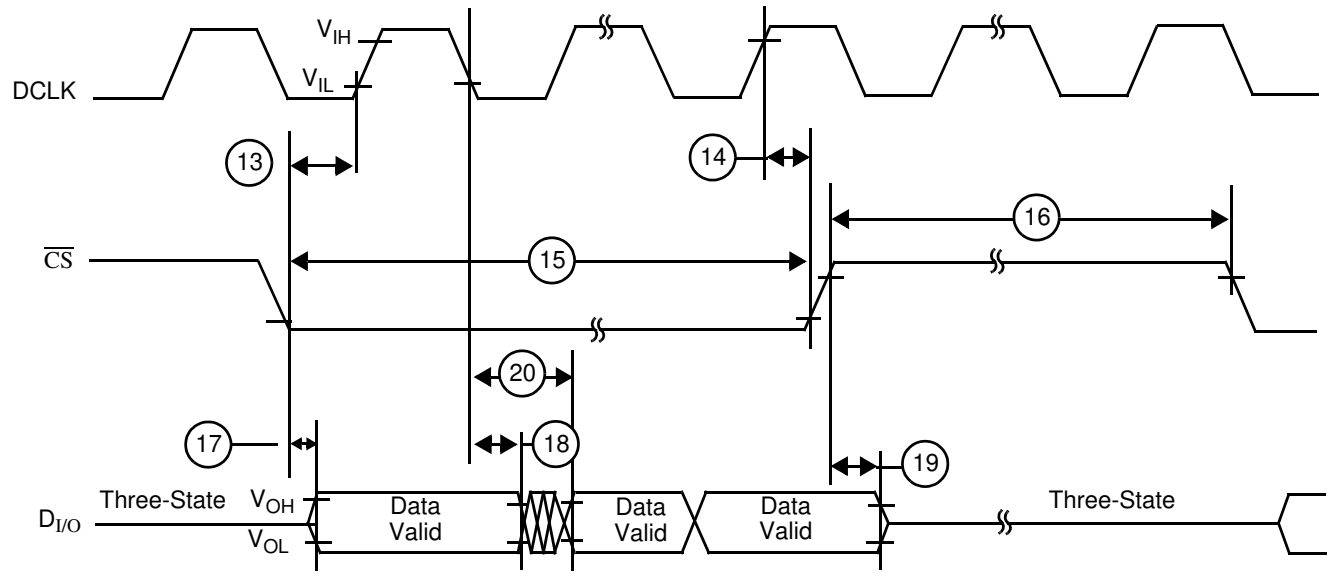


Figure 17. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)