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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## Features

- Low-power, 3.3 V CMOS technology with 5 V tolerant digital inputs
- Pin programmable PCM/MPI or GCI interface
- Software and coefficient compatible to the Le79Q061/063 QSLAC device
- Standard PCM/microprocessor interface (PCM/MPI mode)
  - Single or Dual PCM ports available
  - Time slot assigner (up to 128 channels per port)
  - Clock slot and transmit clock edge options
  - Optional supervision on the PCM highway
  - 1.536, 1.544, 2.048, 3.072, 3.088, 4.096, 6.144, 6.176, or 8.192 MHz master clock derived from MCLK or PCLK
  - $\mu$ P access to PCM data
  - Real Time Data with interrupt (open drain or TTL)
- Broadcast mode
- General Circuit Interface (GCI mode)
  - Control and PCM data on a single port
  - 2.048 Mbits/s data rate
  - 2.048 MHz or 4.096 MHz clock option
- Performs the functions of four codec/filters
- Software programmable:
  - SLIC device input impedance and Transhybrid balance
  - Transmit and receive gains and Equalization
  - Programmable Digital I/O pins with debouncing
- A-law,  $\mu$ -law, or linear coding
- Built-in test modes with loopback, tone generation, and  $\mu$ P access to PCM data
- Mixed state (analog and digital) impedance scaling
- Performance guaranteed over a 12 dB gain range
- Supports multiplexed SLIC device outputs

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<b>Ordering Information</b>		
Device	Package <sup>1</sup> (Green)	Packing <sup>2</sup>
Le58QL061BVC	44-pin TQFP	Trays
Le58QL063HVC	64-pin LQFP	Trays

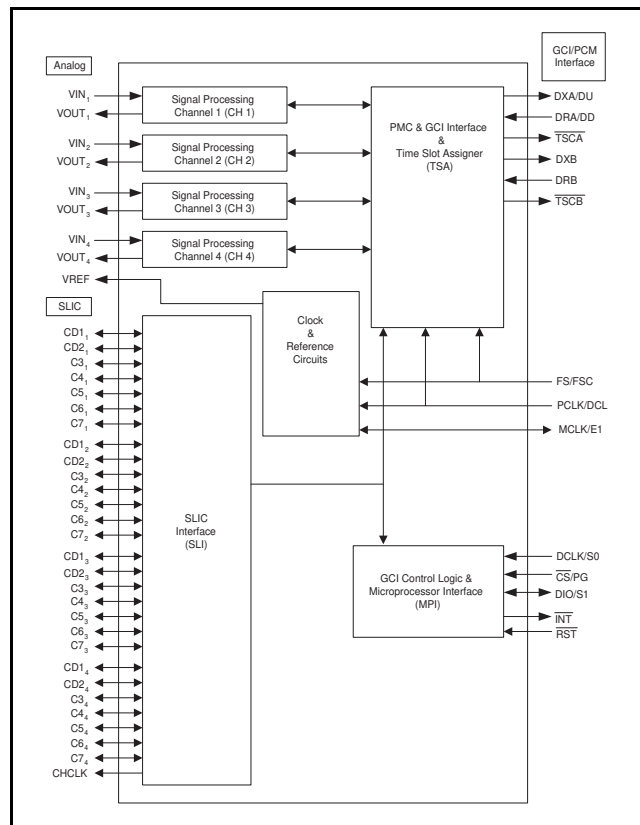
1. The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

2. For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.

- 256 kHz or 293 kHz chopper clock for Zarlink SLIC devices with switching regulator
- Maximum channel bandwidth for V.90 modems

## Applications

- Codec function on telephone switch line cards



**Figure 1 - Block Diagram**

## Description

The Le58QL061/063 Quad Low Voltage Subscriber Line Audio-Processing Circuit (QLSLAC™) devices integrate the key functions of analog line cards into high-performance, very-programmable, four-channel codec-filter devices. The QLSLAC devices are based on the proven design of Zarlink's reliable SLAC™ device families. The advanced architecture of the QLSLAC devices implements four independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the audio-processing function of programmable line cards. The QLSLAC devices are software and coefficient compatible to the QSLAC devices.

Advanced submicron CMOS technology makes the Le58QL061/063 QLSLAC devices economical, with both the functionality and the low power consumption needed in line card designs to maximize line card density at minimum cost. When used with four Zarlink SLIC devices, a QLSLAC device provides a complete software-configurable solution to the BORSCHT functions.

The Le58QL061/063 device supports the feature set of the Le58QL02/021/031 device and provides a General Circuit Interface as a programmable mode.

## Related Literature

- 080753 Le58QL02/021/031 QLSLAC™ Data Sheet
- 080761 QSLAC™ to QLSLAC™ Design Conversion Guide
- 080758 QSLAC™ to QLSLAC™ Guide to New Designs

## Revision History

Below are the changes from the September 2007 version to the June 2011 version.

Page	Item	Description
1	Ordering Information	Obsoleted Le58QL061FJC package.
32	9.1, "GCI Timing Specifications"	Corrected $t_{SD}$ Data Setup Min. to 20.



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## 1.0 Product Description

The QLSLAC device performs the codec/filter and two-to-four-wire conversion functions required of the subscriber line interface circuitry in telecommunications equipment. These functions involve converting audio signals into digital PCM samples and converting digital PCM samples back into audio signals. During conversion, digital filters are used to band limit the voice signals. All of the digital filtering is performed in digital signal processors operating from a master clock, which can be derived either from PCLK or MCLK in the PCM/MPI mode and DCL in the GCI mode.

Four independent channels allow the QLSLAC device to function as four SLAC™ devices. In PCM/MPI mode, each channel has its own enable bit (EC1, EC2, EC3, and EC4) to allow individual channel programming. If more than one Channel Enable bit is High or if all Channel Enable bits are High, all channels enabled will receive the programming information written; therefore, a Broadcast mode can be implemented by simply enabling all channels in the device to receive the information. The Channel Enable bits are contained in the Channel Enable (EC) register, which is written and read using Commands 4A/4Bh. The Broadcast mode is useful in initializing QLSLAC devices in a large system.

In GCI mode, one GCI channel controls two channels of the QLSLAC device. The Monitor channel and SC channel within the GCI channel are used to read/write filter coefficient data, read/write operating conditions and to read/write data to/from the programmable I/O ports of the two channels. Two consecutive GCI channels control all four channels of the QLSLAC device. The two GCI channels used, of the eight total available, are determined by S0 and S1 inputs.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance, and provide equalization of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the WinSLAC™ device software.

In PCM/MPI mode, Data transmitted or received on the PCM highway can be 8-bit companded code (with an optional 8-bit signaling byte in the transmit direction) or 16-bit linear code. The 8-bit codes appear 1 byte per time slot, while the 16-bit code appears in two consecutive time slots. The compressed PCM codes can be either 8-bit companded A-law or  $\mu$ -law. The PCM data is read from and written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The transmit clock edge and clock slot can be selected for compatibility with other devices that can be connected to the PCM highway.

In GCI mode, two 8-bit companded codes are received or transmitted per GCI channel. The compressed PCM codes can be either 8-bit companded A-law or  $\mu$ -law. There is no Signaling or Linear mode available when GCI mode is selected.

Table 1 lists the features available for each device.

Part Number	PCM/GCI Highway	Programmable I/O per Channel	Chopper Clock	Package
Le58QL061BVC	Single/Single	Five I/O	No	44-Pin TQFP
Le58QL063HVC	Dual/Single	Five I/O Two Output	Yes	64-Pin LQFP

**Table 1 - QLSLAC Device Features**

## 2.0 Block Descriptions

### 2.1 Clock and Reference Circuits

This block generates a master clock and a frame sync signal for the digital circuits. It also generates an analog reference voltage for the analog circuits.

### 2.2 Microprocessor Interface (MPI)

This block communicates with the external control microprocessor over a serial interface. It passes user control information to the other blocks, and it passes status information from the blocks to the user. In addition, this block contains the reset circuitry. When GCI is selected, this block is combined with the TSA block.

### 2.3 Time Slot Assigner (TSA)

This block communicates with the PCM highway, where the PCM highway is a time division multiplexed bus carrying the digitized voice samples. The block implements programmable time slots and clocking arrangements in order to achieve a first layer of switching. Internally, this block communicates with the Signal Processing Channels (CHx). When GCI is selected, this block is combined with the TSA block.

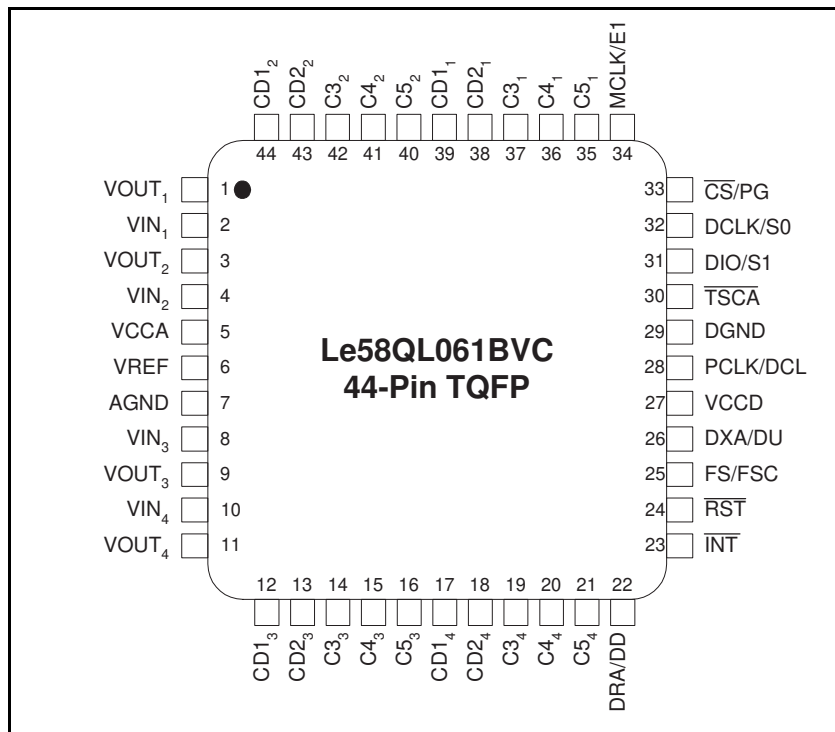
### 2.4 Signal Processing Channels (CHx)

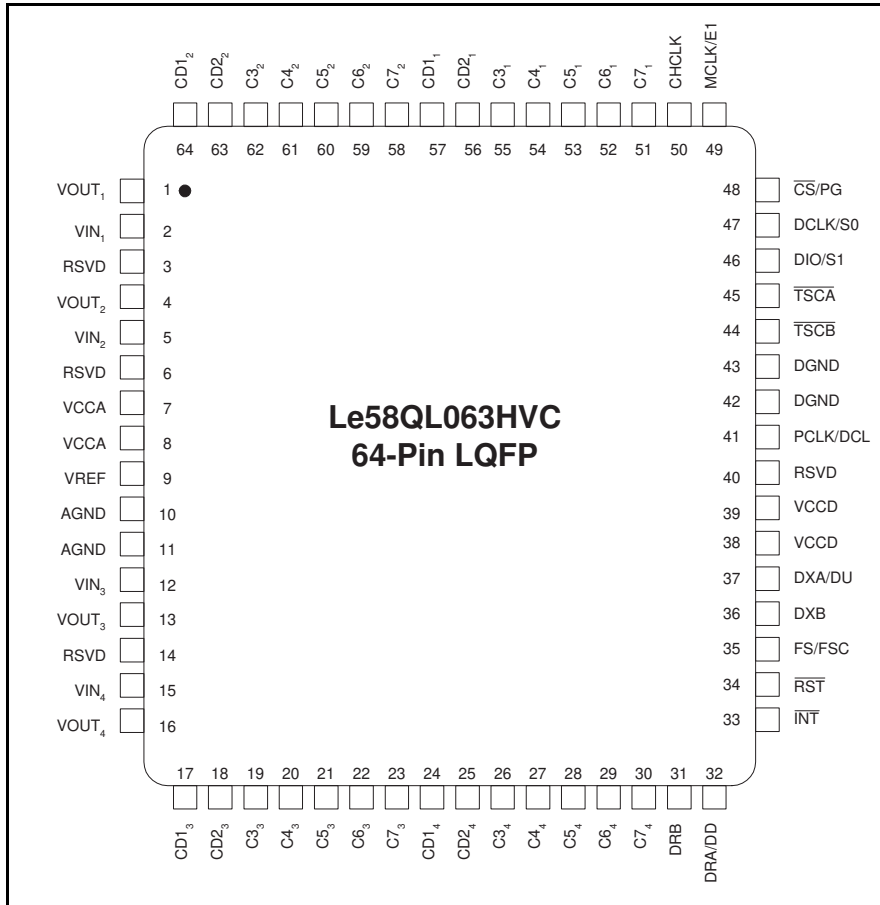
These blocks do the transmission processing for the voice channels. Part of the processing is analog and is interfaced to the VIN and VOUT pins. The remainder of the processing is digital and is interfaced to the Time Slot Assigner (TSA) block.

### 2.5 SLIC Device Interface (SLI)

This block communicates digitally with the SLIC device circuits. It sends control bits to the SLIC devices to control modes and to operate LEDs and optocouplers. It also accepts supervision information from the SLIC devices and performs some filtering.

### 3.0 Connection Diagrams





**Notes:**

1. NC= No connect. Pins 3 and 14 on the Le58QL063HVC device should be grounded if the inputs to VIN<sub>1</sub> and VIN<sub>4</sub> have an impedance larger than 300 Ω.
2. Pins of same name on the Le58QL063HVC device are internally connected (AGND, pins 10, 11; VCCA, pins 7, 8; VCCD, pins 38, 39; DGND, pins 42, 43).

## 4.0 Pin Descriptions

Pin Names	Type	Description
AGND, DGND	Power	Separate analog and digital grounds are provided to allow noise isolation; however, the two grounds are connected inside the part, and the grounds must also be connected together on the circuit board.
CD1 <sub>1</sub> –CD1 <sub>4</sub> , CD2 <sub>1</sub> –CD2 <sub>4</sub>	Inputs/Outputs	<p>Control and Data. CD1 and CD2 are TTL compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of SLIC device or any other device associated with the subscriber line interface. The direction, input or output, is programmed using MPI Command 54/55h or GCI Command SOP 8. As outputs, CD1 and CD2 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. In PCM/MPI mode, the output state of CD1 and CD2 is written using MPI Command 52h. In GCI mode, the output state of CD1 and CD2 is determined by the C1 and C2 bits contained in the down stream C/I channel for the respective channel. As inputs, CD1 and CD2 can be processed by the QLSLAC device (if programmed to do so). CD1 can be debounced before it is made available to the system. The debounce time is programmable from 0 to 15 ms in 1 ms increments using MPI Command C8/C9h and GCI Command SOP 11. CD2 can be filtered using the up/down counter facility and programming the sampling interval using MPI Command E8/E9h or GCI Command SOP 12.</p> <p>Additionally, CD1 can be demultiplexed into two separate inputs using the E1 demultiplexing function. The E1 demultiplexing function of the QLSLAC device was designed to interface directly to Zarlink SLIC devices supporting the ground key function. With the proper Zarlink SLIC device and the E1 function of the QLSLAC device enabled, the CD1 bit can be demultiplexed into an Off-Hook/Ring Trip signal and Ground Key signal. In the demultiplex mode, the second bit, Ground Key, takes the place of the CD2 as an input. The demultiplexed bits can be debounced (CD1) or filtered (CD2) as explained previously. A more complete description of CD1, CD2, debouncing, and filtering functions is contained in the <i>Operating the QLSLAC Device</i> section on page 35.</p> <p>Once the CD1 and CD2 inputs are processed (Debounced, Filtered and/or Demultiplexed) by the QLSLAC device, the information can be accessed by the system in two ways in the PCM/MPI mode: 1) on a per channel basis along with C3, C4, and C5 of the specific channel using MPI Command 53h, or 2) by using MPI Command 4D/4Fh, which obtain the CD1 and CD2 bits from all four channels simultaneously. This feature reduces the processor overhead and the time required to retrieve time-critical signals from the line circuits, such as off-hook and ring trip. With this feature, hookswitch status and ring trip information, for example, can be obtained from all four channels of a QLSLAC device with one read command.</p> <p>In the GCI mode, the processed CD1 and CD2 inputs are transmitted upstream on the CD1 and CD2 bits for the respective analog channel, 1 or 2, using the C/I channel.</p>
C3 <sub>1</sub> –C3 <sub>4</sub> , C4 <sub>1</sub> –C4 <sub>4</sub> , C5 <sub>1</sub> –C5 <sub>4</sub>	Inputs/Outputs	<p>Control. C3, C4, and C5 are TTL-compatible programmable Input or Output (I/O) ports. They can be used to monitor or control the state of the SLIC device or any other device associated with subscriber line interface. The direction, input or output, is programmed using MPI Command 54/55h or GCI Command SOP 8. As outputs, C3, C4, and C5 can be used to control relays, illuminate LEDs, or perform any other function requiring a latched TTL compatible signal for control. In PCM/MPI mode, the output state of C3, C4, and C5 is written using MPI Command 52h. In GCI mode, the output state of C3, C4, and C5 is determined by the C3, C4, and C5 bits contained in the down stream C/I channel for the respective analog channel. As inputs, C3, C4, and C5 can be accessed by the system in PCM/MPI mode by using MPI Command 53h. In GCI mode, C3 is transmitted upstream, along with CD1 and CD2, for the respective analog channel using C3 of the C/I channel. Also, in GCI mode, C3, C4, and C5 can be read along with CD1 and CD2 using GCI Command SOP 10.</p> <p>The Le58QL061 QLSLAC device contains a single PCM highway or GCI Interface and five programmable I/Os per channel (CD1, CD2, C3, C4, and C5) in a TQFP package.</p>
C6 <sub>1</sub> –C6 <sub>4</sub> , C7 <sub>1</sub> –C7 <sub>4</sub>	Outputs	Control. Two additional outputs per channel are available on the Le58QL063HVC device.
CHCLK	Output	Chopper Clock. This output provides a 256 kHz or a 292.57 kHz, 50% duty cycle, TTL-compatible clock for use by up to four SLIC devices with built-in switching regulators. The CHCLK frequency is synchronous to the master clock, but the phase relationship to the master clock is random. The chopper clock is not available in all package types.

Pin Names	Type	Description
$\overline{\text{CS}}/\text{PG}$	Input	<p>Chip Select/PCM-GCI. The <math>\overline{\text{CS}}/\text{PG}</math> input along with the DCLK/S0 input are used to determine the operating state of the programmable PCM/GCI interface. On power up, the QLSLAC device will initialize to GCI mode if <math>\overline{\text{CS}}/\text{PG}</math> is low <i>and</i> there is no toggling (no high to low or low to high transitions) of the DCLK/S0 input. The device will initialize to the PCM/MPI mode if either <math>\overline{\text{CS}}</math> is high <i>or</i> DCLK is toggling.</p> <p>Once the device is in PCM/MPI mode, it is ready to receive commands through its serial interface pins, DIO and DCLK. Once a valid command has been sent through the MPI serial interface, GCI mode cannot be entered unless a hardware reset is asserted or power is removed from the part. If a valid command has not been sent since the last hardware reset or power up, then GCI mode can be re-entered (after a delay of one PCM frame) by holding <math>\overline{\text{CS}}/\text{PG}</math> low and keeping DCLK static. While the part is in GCI mode, then <math>\overline{\text{CS}}/\text{PG}</math> going high or DCLK toggling will immediately place the device in PCM/MPI mode.</p> <p>In the PCM/MPI mode, the Chip Select input (active Low) enables the device so that control data can be written to or read from the part. The channels selected for the write or read operation are enabled by writing 1s to the appropriate bits in the Channel Enable Register of the QLSLAC device prior to the command. See EC1, EC2, EC3, and EC4 of the Channel Enable Register and Command 4A/4Bh for more information. If Chip Select is held Low for 16 rising edges of DCLK, a hardware reset is executed when Chip Select returns High.</p>
DCLK/S0	Input	<p>Data Clock. In addition to providing both a data clock input and an S0 GCI address input, DCLK/S0 acts in conjunction with <math>\overline{\text{CS}}/\text{PG}</math> to determine the operational mode of the system interface, PCM/MPI or GCI. See <math>\overline{\text{CS}}/\text{PG}</math> for details.</p> <p>In the PCM/MPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the QLSLAC device. The maximum clock rate is 8.192 MHz.</p>
	Input	Select Bit 0. In GCI mode, S0 is one of two inputs (S0, S1) that is decoded to determine on which GCI channels the QLSLAC device transmit and receives data.
DIO/S1	Input/Output	Data Input/Output. In the PCM/MPI mode, control data is serially written into and read out of the QLSLAC device via the DIO pin, most significant bit first. The Data Clock determines the data rate. DIO is high impedance except when data is being transmitted from the QLSLAC device.
	Input	Select Bit 1. In GCI mode, S1 is the second of two inputs (S0, S1) that is decoded to determine on which GCI channels the QLSLAC device transmits and receives data.
DRA/DD, DRB	Inputs	PCM Data Receive (A/B). In the PCM/MPI mode, the PCM data for channels 1, 2, 3, and 4 is serially received on either the DRA or DRB port during user-programmed time slots. Data is always received with the most significant bit first. For compressed signals, 1 byte of data for each channel is received every 125 $\mu\text{s}$ at the PCLK rate. In the Linear mode, 2 consecutive bytes of data for each channel are received every 125 $\mu\text{s}$ at the PCLK rate. DRB is not available on all package types.
	Input	GCI Data Downstream. In GCI mode, the B1, B2, Monitor and SC channel data is serially received on the Data Downstream input for all four channels of the QLSLAC device. The QLSLAC device requires two of the eight GCI channels for operation. The two GCI Channels, out of the eight possible, are determined by the S0 and S1 inputs. Data is always received with the most significant bit first. 4 bytes of data for each GCI channel is received every 125 $\mu\text{s}$ at the 2.048 Mbit/s data rate.
DXA/DU, DXB	Outputs	PCM Data Transmit. In the PCM/MPI mode, the transmit data from channels 1, 2, 3, and 4 is sent serially out on either the DXA or DXB port or on both ports during user-programmed time slots. Data is always transmitted with the most significant bit first. The output is available every 125 $\mu\text{s}$ and the data is shifted out in 8-bit (16-bit in Linear or PCM Signaling mode) bursts at the PCLK rate. DXA and DXB are High impedance between time slots, while the device is in the Inactive mode with no PCM signaling, or while the Cutoff Transmit Path bit (CTP) is on. DXB is not available on all package types.
	Output	GCI Data Upstream. In the GCI mode, the B1, B2, Monitor and SC channel data is serially transmitted on the Data Upstream output for all four channels of the QLSLAC device. Which GCI channels the device uses is determined by the S0 and S1 inputs. Data is always transmitted with the most significant bit first. 4 bytes of data for each GCI channel is transmitted every 125 $\mu\text{s}$ at the DCL rate.
FS/FSC	Input	Frame Sync. In the PCM/MPI mode, the Frame Sync (FS) pulse is an 8 kHz signal that identifies Time Slot 0 and Clock Slot 0 of a system's PCM frame. The QLSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.
	Input	Frame Sync. In GCI mode, the Frame Sync (FSC) pulse is an 8 kHz signal that identifies the beginning of GCI channel 0 of a system's GCI frame. The QLSLAC device references individual GCI channels with respect to this input, which must be synchronized to DCL.

Pin Names	Type	Description
$\overline{\text{INT}}$	Output	Interrupt. $\overline{\text{INT}}$ is an active Low output signal, which is programmable as either TTL-compatible or open drain. The $\overline{\text{INT}}$ output goes Low any time one of the input bits in the Real Time Data register changes state and is not masked. It also goes Low any time new transmit data appears if this interrupt is armed. $\overline{\text{INT}}$ remains Low until the appropriate register is read via the microprocessor interface, or the QLSLAC device receives either a software or hardware reset. The individual $\text{CDx}_C$ bits in the Real Time Data register can be masked from causing an interrupt by using MPI Command 6C/6Dh or GCI Command SOP 14. The transmit data interrupt must be armed with a bit in the Operating Conditions Register.
MCLK/E1	Input/Output	Master Clock/Enable CD1 Multiplex. In PCM/MPI mode only, the Master Clock can be a 1.536 MHz, 1.544 MHz, or 2.048 MHz (times 1, 2, or 4) clock for use by the digital signal processor. If the internal clock is derived from the PCM Clock Input (PCLK) or if GCI mode is selected, this pin can be used as an E1 output to control Zarlink SLIC devices having multiplexed hook switch and ground key detector outputs.
NC	—	No connect. This pin is not internally connected.
PCLK/DCL	Input	PCM Clock. In the PCM/MPI mode, the PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz for dual PCM highway versions and 256 kHz for single PCM highway versions. The minimum clock rate must be doubled if Linear mode or PCM signaling is used. PCLK frequencies between 1.03 MHz and 1.53 MHz are not allowed. Optionally, the digital signal processor clock can be derived from PCLK rather than MCLK. In PCM/MPI mode, PCLK can be operated at twice the PCM data rate in the Double PCLK mode (bit 1 of PCM/MPI Command C8/C9h).
	Input	GCI Data Clock. In GCI mode, DCL is either 2.048 MHz or 4.096 MHz, which is an integer multiple of the frame sync frequency. Circuitry internal to the QLSLAC device monitors this input to determine which frequency is being used, 2.048 MHz or 4.096 MHz. When 4.096 MHz clock operation is detected, internal timing is adjusted so that DU and DD operate at the 2.048 Mbit/s rate.
$\overline{\text{RST}}$	Input	Reset. A logic Low signal at this pin resets the QLSLAC device to its default state.
$\overline{\text{TSCA}}$ , $\overline{\text{TSCB}}$	Outputs	Time Slot Control. The Time Slot Control outputs are open-drain outputs (requiring pull-up resistors to VCCD) and are normally inactive (high impedance). In the PCM/MPI mode, $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is active (low) when PCM data is transmitted on the DXA or DXB pin, respectively. In GCI mode, $\overline{\text{TSCA}}$ is active (low) during the two GCI time slots selected by the S1 and S0. $\overline{\text{TSCB}}$ is not available on all package types.
VCCA, VCCD	Power	Analog and digital power supply inputs. VCCA and VCCD are provided to allow for noise isolation and proper power supply decoupling techniques. For best performance, all of the VCC power supply pins should be connected together at the connector of the printed circuit board.
VIN <sub>1</sub> –VIN <sub>4</sub>	Inputs	Analog Input. The analog voice band signal is applied to the VIN input of the QLSLAC device. The VIN input is biased at VREF by a large internal resistor. The audio signal is sampled, digitally processed and encoded, and then made available at the TTL-compatible PCM output (DXA or DXB) or in the B1 and B2 of the GCI channel. If the digitizer saturates in the positive or negative direction, VIN is pulled by a reduced resistance toward AGND or VCCD, respectively. VIN <sub>1</sub> is the input for channel 1, VIN <sub>2</sub> is the input for channel 2, VIN <sub>3</sub> is the input for channel 3, and VIN <sub>4</sub> is the input for channel 4.
VOUT <sub>1</sub> – VOUT <sub>4</sub>	Outputs	Analog Output. The received digital data at DRA/DRB or DD (GCI mode) is processed and converted to an analog signal at the VOUT pin. VOUT <sub>1</sub> is the output from channel 1, VOUT <sub>2</sub> is the output for channel 2, VOUT <sub>3</sub> is the output from channel 3, and VOUT <sub>4</sub> is the output for channel 4. The VOUT voltages are referenced to VREF.
VREF	Output	Analog Voltage Reference. The VREF output is provided in order for an external capacitor to be connected from VREF to ground, filtering noise present on the internal voltage reference. VREF is buffered before it is used by internal circuitry. The voltage on VREF and the output resistance are given in “Electrical Characteristics” on page 16. The leakage current in the capacitor must be low.



## 5.0 Absolute Maximum Ratings

Stresses above those listed under "Absolute Maximum Ratings" can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	$-60^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$
Ambient Temperature, under Bias	$-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$
Ambient relative humidity (non condensing)	5 to 95%
$V_{CCA}$ with respect to AGND	-0.4 to + 4.0 V
$V_{CCA}$ with respect to VCCD	$\pm 0.4\text{ V}$
$V_{CCD}$ with respect to DGND	-0.4 to + 4.0 V
$V_{IN}$ with respect to AGND	-0.4 V to ( $V_{CCA} + 0.4\text{ V}$ )
AGND with respect to DGND	$\pm 50\text{ mV}$
Digital pins with respect to DGND	-0.4 to 5.5 V or $V_{CCD} + 2.37\text{ V}$ , whichever is smaller
Total combined CD1–C7 current per device:	
Source from VCCD	40 mA
Sink into DGND	40 mA
Latch up immunity (any pin)	$\pm 100\text{ mA}$
Total VCC current if rise rate of VCC > 0.4 V/ $\mu\text{s}$	0.5 A

## 5.1 Package Assembly

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 Table 4-2 for recommended peak soldering temperature and Table 5-2 for the recommended solder reflow temperature profile.

## 6.0 Operating Ranges

Zarlink guarantees the performance of this device over commercial (0 to 70° C) and industrial (-40 to 85° C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

### 6.1 Environmental Ranges

Ambient Temperature	$-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$
Ambient Relative Humidity	15 to 85%

### 6.2 Electrical Ranges

Analog Supply $V_{CCA}$	$+3.3\text{ V} \pm 5\%$ $V_{CCD} \pm 50\text{ mV}$
Digital Supply $V_{CCD}$	$+3.3\text{ V} \pm 5\%$
DGND	0 V
AGND	$\pm 10\text{ mV}$
CFIL Capacitance: VREF to AGND	$0.1\ \mu\text{F} \pm 20\%$
Digital Pins	DGND to +5.25 V

## 7.0 Electrical Characteristics

Typical values are for TA = 25° C and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in Operating Ranges, except where noted.

Symbol	Parameter Descriptions	Min.	Typ.	Max.	Unit	Note
V <sub>IL</sub>	Digital Input Low voltage			0.8	V	
V <sub>IH</sub>	Digital Input High voltage	2.0				
I <sub>IL</sub>	Digital Input leakage current 0 < V < V <sub>CCD</sub>	-7		+7	μA	
	Otherwise	-120		+180		
V <sub>HYS</sub>	Digital Input hysteresis	0.16	0.25	0.34	V	
V <sub>OL</sub>	Digital Output Low voltage				V	1
	CD1-C7 (I <sub>OL</sub> = 4 mA)			0.4		
	CD1-C7 (I <sub>OL</sub> = 8 mA)			0.8		
	TSCA/ TSCB (I <sub>OL</sub> = 14 mA)			0.4		
	Other digital outputs (I <sub>OL</sub> = 2 mA)			0.4		
V <sub>OH</sub>	Digital Output High voltage				V	1
	CD1-C7 (I <sub>OH</sub> = 4 mA)	V <sub>CCD</sub> - 0.4 V				
	CD1-C7 (I <sub>OH</sub> = 8 mA)	V <sub>CCD</sub> - 0.8 V				
	Other digital outputs (I <sub>OH</sub> = 400 μA)	2.4				
I <sub>OL</sub>	Digital Output leakage current (Hi-Z state) 0 < V < V <sub>CCD</sub>	-7		+7	μA	
	Otherwise	-120		+180		
G <sub>IN</sub>	Input attenuator gain				V/V	
	DGIN = 0 DGIN = 1		0.6438 1			
V <sub>IR</sub>	Analog input voltage range (Relative to VREF)				V <sub>pk</sub>	
	AX = 0 dB, attenuator on (DGIN = 0)		±1.584			
	AX = 6.02 dB, attenuator on (DGIN = 0)		±0.792			
	AX = 0 dB, attenuator off (DGIN = 1)		±1.02			
	AX = 6.02 dB, attenuator off (DGIN = 1)		±0.51			
V <sub>IOS</sub>	Offset voltage allowed on VIN	-50		50	mV	
Z <sub>IN</sub>	Analog input impedance to VREF, 300 to 3400 Hz	600		1400	kΩ	
I <sub>IP</sub>	Current into analog input for an input voltage of 3.3 V	50		115	μA	2
I <sub>IN</sub>	Current out of analog input for an input voltage of -0.3 V	50		130		2
Z <sub>OUT</sub>	VOUT output impedance		1	10	Ω	
CL <sub>OUT</sub>	Allowable capacitance, V <sub>OUT</sub> to AGND			500	pF	
I <sub>OUT</sub>	VOUT output current (F < 3400 Hz)	-4		4	mA <sub>pk</sub>	3
V <sub>REF</sub>	VREF output open circuit voltage (leakage < 20 nA)	1.43	1.5	1.57	V	
Z <sub>REF</sub>	VREF output impedance (F < 3400 Hz)	70		130	kΩ	
V <sub>OR</sub>	VOUT analog output voltage range (Relative to VREF)				V <sub>pk</sub>	
	AR = 0 dB AR = -6.02 dB		±1.02 ±0.51			
V <sub>OOS</sub>	VOUT offset voltage (AISN off)	-40		40	mV	4
V <sub>OOSA</sub>	VOUT offset voltage (AISN on)	-80		80		

Symbol	Parameter Descriptions	Min.	Typ.	Max.	Unit	Note
$G_{AISN}$	AISN gain - expected gain (input = 0 dBm0, 1014 Hz) Attenuator on (DGIN = 0) Attenuator off (DGIN = 1)	-0.016 -0.024		0.016 0.024	V/V	
PD	Power dissipation All channels active 1 channel active All channels inactive		130 40 13	170 80 18	mW	
$C_I$	Digital Input capacitance			4	pF	
$C_O$	Digital Output capacitance			4		
PSRR	Power supply rejection ratio (1.02 kHz, 100 mV <sub>RMS</sub> , either path, GX = GR = 0 dB)	40			dB	

**Notes:**

1. The CD1, CD2, C3–C7 outputs are resistive for less than a 0.8 V drop. Total current must not exceed absolute maximum ratings.
2. When the digitizer saturates, a resistor of  $50\text{ k}\Omega \pm 20\text{ k}\Omega$  is connected either to AGND or to VCCA as appropriate to discharge the coupling capacitor.
3. When the QLSLAC device is in the Inactive state, the analog output will present either a VREF DC output level through a  $15\text{ k}\Omega$  resistor (VMODE = 0) or a high impedance (VMODE = 1).
4. If there is an external DC path from VOUT to VIN with a gain of  $G_{DC}$  and the AISN has a gain of  $h_{AISN}$ , then the output offset will be multiplied by  $1 / [1 - (h_{AISN} \cdot G_{DC})]$ .
5. Power dissipation in the Inactive state is measured with all digital inputs at  $V_{IH} = V_{CCD}$  and  $V_{IL} = DGND$  and with no load connected to VOUT<sub>1</sub>, VOUT<sub>2</sub>, VOUT<sub>3</sub>, or VOUT<sub>4</sub>.

## 7.1 Transmission Characteristics

Signal at Digital Interface	Transmit (DGIN = 0)	Transmit (DGIN = 1)	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.7804	0.5024	0.5024	Vrms
$\mu$ -law digital mW or equivalent (0 dBm0)	0.7746	0.4987	0.4987	
$\pm 22,827$ peak linear coded sine wave	0.7804	0.5024	0.5024	

**Table 2 - 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX and AR**

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the GX gain from 0 dB to 12 dB, the GR loss from 0 dB to 12 dB, and the input attenuator (GIN) on or off.

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz AX = AR = 0 dB 0 to 85° C -40° C AX = +6.02 dB and/or AR = -6.02 dB 0 to 85° C -40° C	-0.25 -0.30		+0.25 +0.30	dB	
Gain accuracy digital-to-digital		-0.25		+0.25		
Gain accuracy analog-to-analog		-0.25		+0.25		
Attenuation distortion	300 Hz to 3 kHz	- 0.125		+0.125		1
Single frequency distortion				-46		2
Second harmonic distortion, D/A	GR = 0 dB			-55		
Idle channel noise Analog out	Digital looped backweighted unweighted			-68 -55	dBm0p dBm0	3 3
Digital out	Digital input = 0 A-law Digital input = 0 $\mu$ -law Analog $V_{IN}$ = 0 VACA-law Analog $V_{IN}$ = 0 VAC $\mu$ -law		0 0	12 16	dBrnc0 dBrnc0	3, 6 3, 6
Crosstalk TX to RX same channel RX to TX	0 dBm0 300 to 3400 Hz 0 dBm0 300 to 3400 Hz			-75 -75	dBm0	
Crosstalk between channels TX or RX to TX TX or RX to RX	0 dBm0 SLIC imped. <300 $\Omega$ (Le58QL061), <5000 $\Omega$ (Le58QL063) 1014 Hz, Average 1014 Hz, Average			-76 -78	dBm0	4
End-to-end group delay	B = Z = 0; X = R = 1			678	$\mu$ s	5

### Notes:

- See Figure 2 and Figure 3.
- 0 dBm0 input signal, 300 Hz to 3400 Hz; measurement at any other frequency, 300 Hz to 3400 Hz.
- No single frequency component in the range above 3800 Hz may exceed a level of -55 dBm0.
- The weighted average of the crosstalk is defined by the following equation, where  $C(f)$  is the crosstalk in dB as a function of frequency,  $f_N =$

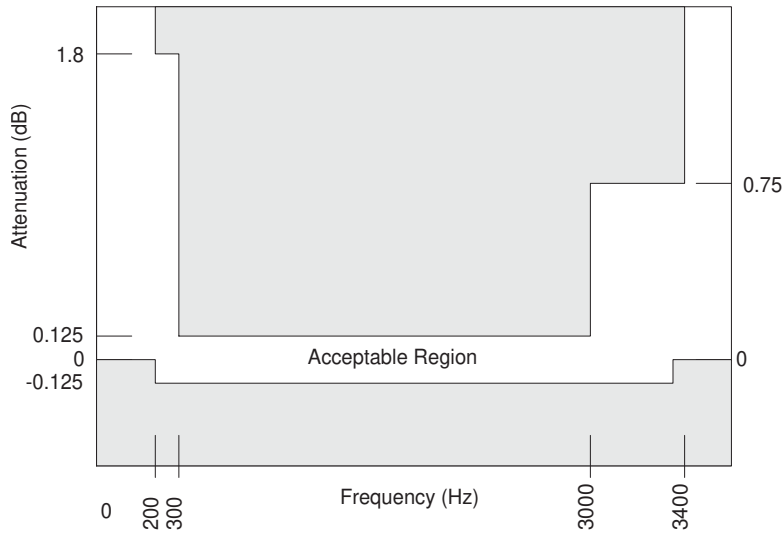
3300 Hz,  $f_1 = 300$  Hz, and the frequency points ( $f_j, j = 2..N$ ) are closely spaced:

$$\text{Average} = 20 \cdot \log \left[ \frac{\sum_j \frac{10^{\frac{1}{20} \cdot C(f_j)} + 10^{\frac{1}{20} \cdot C(f_{j-1})}}{2} \cdot \log \left( \frac{f_j}{f_{j-1}} \right)}{\log \left( \frac{f_N}{f_1} \right)} \right]$$

- 5. The End-to-End Group Delay is the sum of the transmit and receive group delays (both measured using the same time and clock slot).
- 6. Typical values not tested in production.

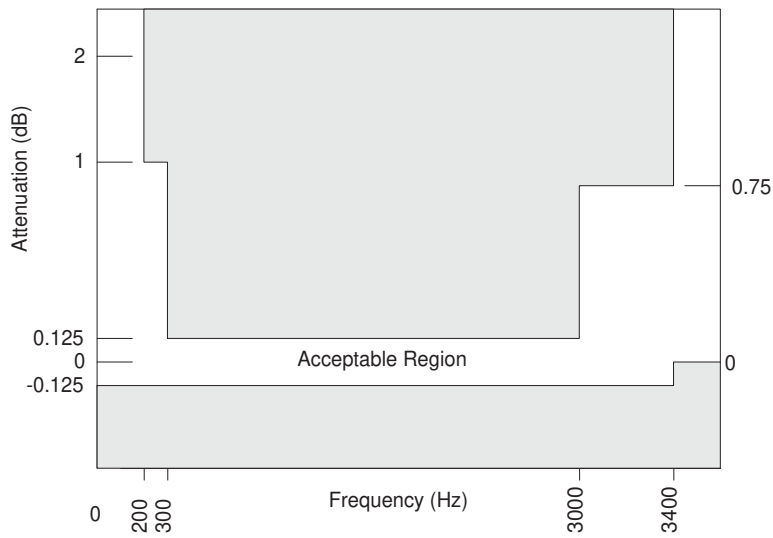
### 7.2 Attenuation Distortion

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 2 and Figure 3. The reference frequency is 1014 Hz and the signal level is -10 dBm0.



**Figure 2 - Transmit Path Attenuation vs. Frequency**

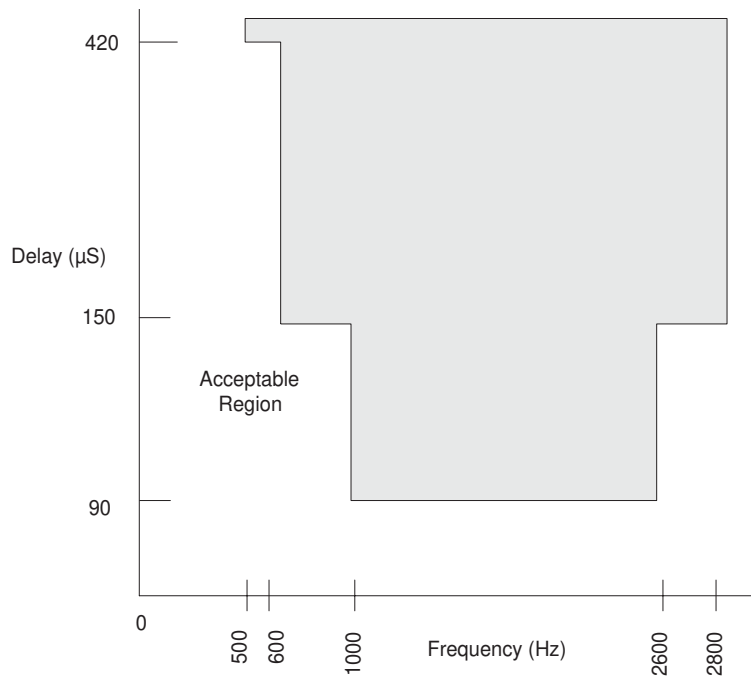




**Figure 3 - Receive Path Attenuation vs. Frequency**

### 7.3 Group Delay Distortion

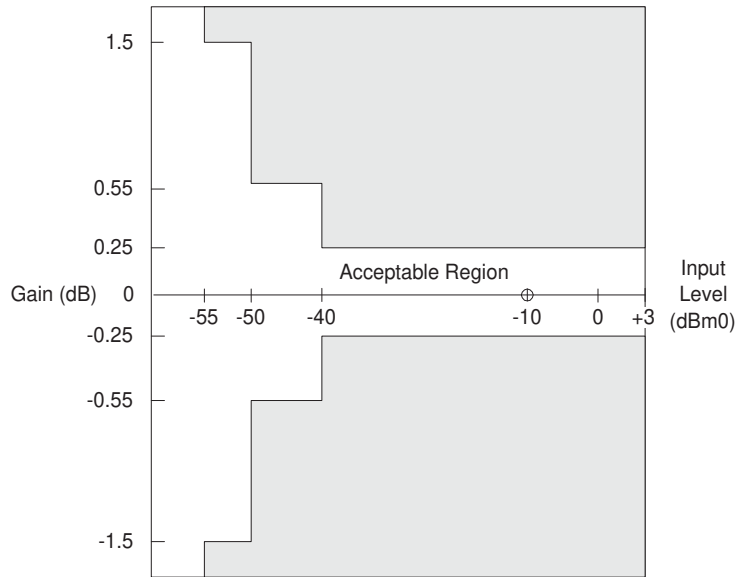
For either transmission path, the group delay distortion is within the limits shown in Figure 4. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.



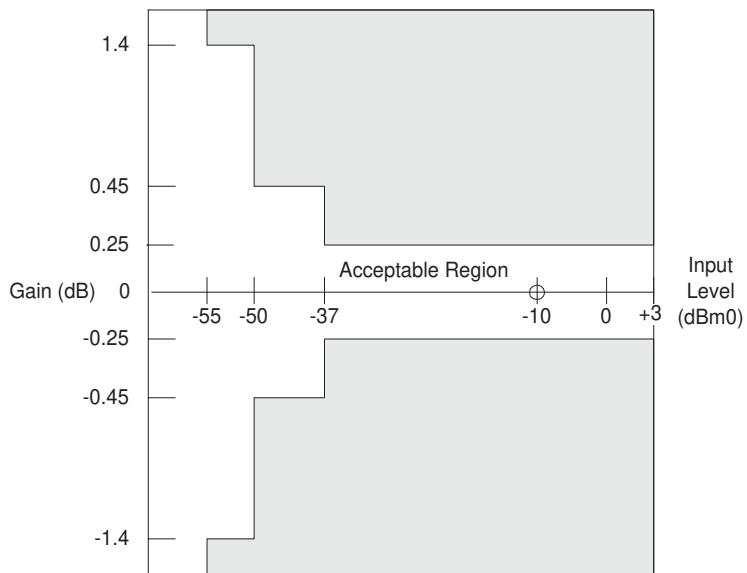
**Figure 4 - Group Delay Distortion**

### 7.4 Gain Linearity

The gain deviation relative to the gain at  $-10$  dBm<sub>0</sub> is within the limits shown in Figure 5 (A-law) and Figure 6 ( $\mu$ -law) for either transmission path when the input is a sine wave signal of 1014 Hz.



**Figure 5 - A-law Gain Linearity with Tone Input (Both Paths)**



**Figure 6 -  $\mu$ -law Gain Linearity with Tone Input (Both Paths)**

## 7.5 Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 7 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

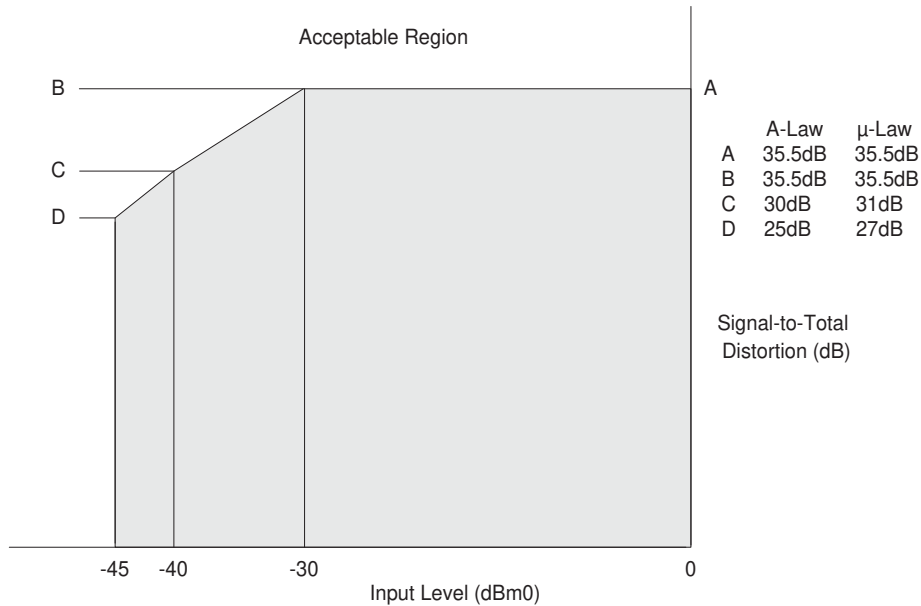
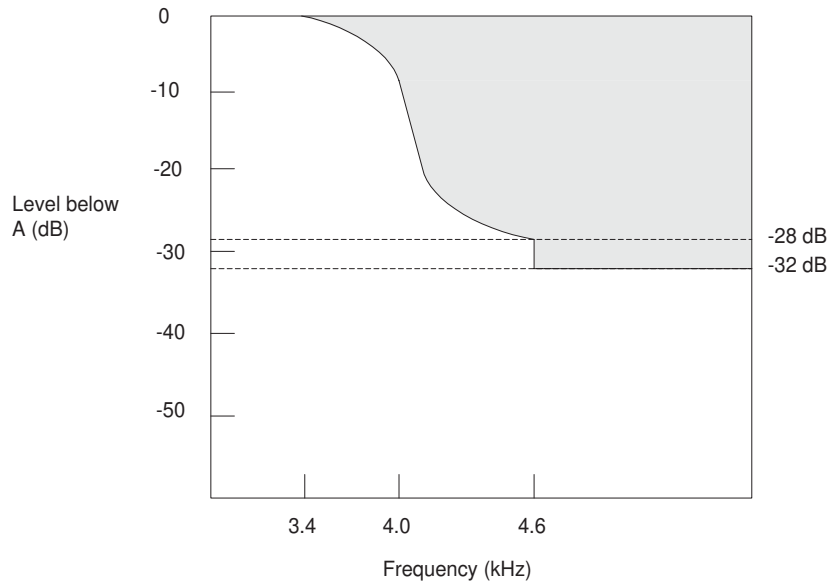


Figure 7 - Total Distortion with Tone Input (Both Paths)

## 7.6 Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal of frequency  $f$ , and level  $A$  is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of  $A$  dBm0 also applied to the analog input. The minimum specifications are shown in the following table.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < $f$ < 45 Hz	-25 dBm0 < $A$ ≤ 0 dBm0	18 dB
45 Hz < $f$ < 65 Hz	-25 dBm0 < $A$ ≤ 0 dBm0	25 dB
65 Hz < $f$ < 100 Hz	-25 dBm0 < $A$ ≤ 0 dBm0	10 dB
3400 Hz < $f$ < 4600 Hz	-25 dBm0 < $A$ ≤ 0 dBm0	see Figure 8
4600 Hz < $f$ < 100 kHz	-25 dBm0 < $A$ ≤ 0 dBm0	32 dB



**Figure 8 - Discrimination Against Out-of-Band Signals**

**Note:**

The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation (db)} = 14 - 14 \sin\left(\frac{\pi(4000 - f)}{1200}\right)$$

### 7.7 Discrimination Against 12- and 16-kHz Metering Signals

If the QLSLAC device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones also may appear at the VIN terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz or 16 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the analog input voltage range.

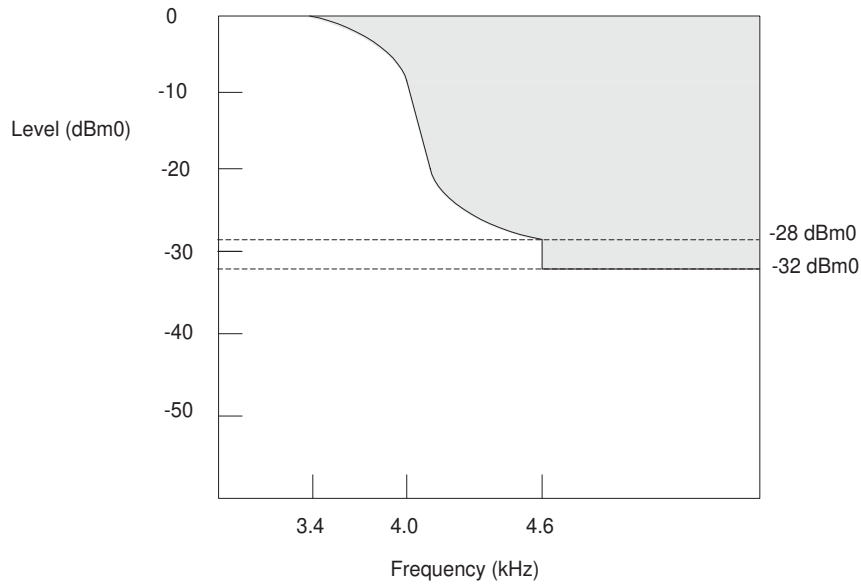
### 7.8 Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	-32 dBm0
40 kHz to 240 kHz	-46 dBm0
240 kHz to 1 MHz	-36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 9. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[ -14 - 14 \sin\left(\frac{\pi(f - 4000)}{1200}\right) \right] \text{dBm0}$$

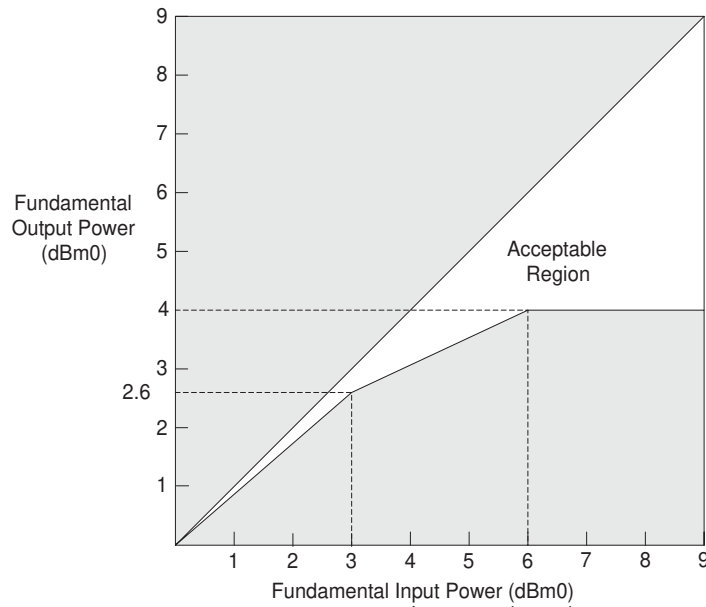


**Figure 9 - Spurious Out-of-Band Signals**

**7.9 Overload Compression**

Figure 10 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1.  $1.2 \text{ dB} < GX \leq + 12 \text{ dB}$
2.  $-12 \text{ dB} \leq GR < -1.2 \text{ dB}$
3. Digital voice output connected to digital voice input.
4. Measurement analog-to-analog.



**Figure 10 - Analog-to-Analog Overload Compression**

## 8.0 Switching Characteristics

The following are the switching characteristics over operating range (unless otherwise noted). Min and max values are valid for all digital outputs with a 115 pF load, except CD1–C7 with a 30 pF load. (See Figure 12 and Figure 13 for the microprocessor interface timing diagrams.)

### Microprocessor Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
1	$t_{DCY}$	Data clock period	122			ns	
2	$t_{DCH}$	Data clock HIGH pulse width	48				
3	$t_{DCL}$	Data clock LOW pulse width	48				
4	$t_{DCR}$	Rise time of clock			25		
5	$t_{DCF}$	Fall time of clock			25		
6	$t_{ICSS}$	Chip select setup time, Input mode	30		$t_{DCY} - 10$		
7	$t_{ICSH}$	Chip select hold time, Input mode	0		$t_{DCH} - 20$		
8	$t_{ICSL}$	Chip select pulse width, Input mode		$8t_{DCY}$			
9	$t_{ICSO}$	Chip select off time, Input mode	2500				1
10	$t_{IDS}$	Input data setup time	25				
11	$t_{IDH}$	Input data hold time	30				
12	$t_{OLH}$	SLIC device output latch valid			2500		
13	$t_{OCSS}$	Chip select setup time, Output mode	30		$t_{DCY} - 10$		
14	$t_{OCSH}$	Chip select hold time, Output mode	0		$t_{DCH} - 20$		
15	$t_{OCSL}$	Chip select pulse width, Output mode		$8t_{DCY}$			
16	$t_{OCSO}$	Chip select off time, Output mode	2500				1
17	$t_{ODD}$	Output data turn on delay			36		2
18	$t_{ODH}$	Output data hold time	3				
19	$t_{ODOF}$	Output data turn off delay			36		
20	$t_{ODC}$	Output data valid			36		
21	$t_{RST}$	Reset pulse width	50			$\mu s$	