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# Le71HR0021

# Le58QL021/Le79R79
# Line Module Reference Design Guide

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# OVERVIEW

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## 1.1 INTRODUCTION

This document describes one of the series of Zarlink line module reference designs. Each Zarlink line module is a complete standalone line card solution applicable to specific target market segments. When used with the Zarlink's VoicePath software and the VoicePath™ demo board, this module provides a complete voice solution requiring only a power supply to operate.

This line module demonstrates all of the powerful features of the Zarlink Le58QL021 QLSLAC and the Le79R79 devices. The QLSLAC device includes A-law/μ-law and linear coding. Transmit and receive gain, two-wire AC port impedance, transhybrid balance, equalization, and hybrid balance. The Le79R79 SLIC device provides internal ring generation and ring trip detection, battery switching, programmable open circuit voltage, and a programmable loop detect threshold. Together, these devices form a complete line card solution.

## 1.2 SCOPE

This document describes the Le71HR0021 line module only. For information regarding the VoicePath software, the WinSLAC™ software, or the VP demo board please see their respective user's guides.

## 1.3 REFERENCES

The following documents are referred to in this document and may be helpful.

- *Le79R79 Data Sheet*, document ID# 080125
- *Le58QL021 Data Sheet*, document ID# 080753
- *Le79R79 Ringing SLIC Device User's Guide*, document ID# 080194
- *VoicePath Demo Board User's Guide*, document ID# 080756
- *Mini-PBX Demo Application User's Guide*, document ID# 080722

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# CHAPTER

# 2 LINE MODULE DESCRIP-TION

## 2.1 OVERVIEW

This chapter describes the features of the Le71HR0021 line module.

## 2.2 INTERFACE CONNECTORS

Zarlink line modules have three connectors to interface the QLSLAC device and SLIC devices to a customer's main board or the Zarlink's VP demo board. These connectors are mounted on the bottom of the Line Module PCB. In this implementation, the larger connector (J3) interfaces the Tip and Ring leads of each line to the VP demo board. This connector also provides a means of supplying external battery supplies to the line module SLIC devices. To use external batteries, it is necessary to break off the on board DC-DC converter so that contention does not occur.

The two smaller connectors are used to interface the low-level digital signals and the low voltage power sources to the Line Module (+3.3 V, +5 V, and +12 V). These are deliberately spaced apart from the SLIC device area where higher voltages and lightning surges are possible. The MPI and power connector (J2) provide connections for the control interface (MPI Bus) and the 3.3 VDC power to the QLSLAC device, and the +12 V for an on-board switching power supply.

The PCM and power connector (J1) provides the interface to the PCM highway, and the master clock for the QLSLAC device. In addition, the SLIC device 5-V VCC supply enters the line module through this connector. The MPI and PCM signals are split on separate connectors deliberately. The PCM connector has extra ground connections to isolate critical clock signals on the connector.

## 2.3 ON BOARD POWER CONVERTER

The on board DC-DC power converter is used to create the required SLIC device battery voltages. In the case of the Le79R79 device, two battery voltages are required. On this line module, a $-63$ V, and a $-21$ V supply are created with the on board DC-DC converter. These voltages were chosen so that the On-Hook Tip/Ring voltage would not exceed the UL1950 requirement of 56 V. The on board converter is capable of delivering up to approximately 9 W total to the SLIC devices. This provides enough power to ring 5 REN at 0 loop length on all four lines simultaneously.

## 2.4 LINE INTERFACE CIRCUITS

The line interface circuit consists of a fuse for each of Tip and Ring, a sidactor for shunting over-voltages on Tip and Ring to ground, and 50-$\Omega$ current limiting fuse resistors. See Chapter 3 *Surge Protection,* on page 7 for more information regarding the line protection circuits.

## 2.5 TRANSMISSION

### 2.5.1 Two-Wire Impedance

The QLSLAC device can modify the two-wire "desired" port impedance ($Z_D$) by programming the AISN and the Z-filter of the SLAC device and/or by changing the Line impedance setting resistor RTX. All complex impedance subscriber line terminations such as those found in China, Europe, Middle East, Africa, South America and North America can be achieved. The achievable two-wire return loss for these terminations is higher than any country's required value for subscriber lines. The Zarlink VoicePath Mini-PBX application provides a 600-$\Omega$ resistive, 900-$\Omega$ resistive, and German Complex impedance for demonstration purposes. Other line impedances can be supported in the Mini-PBX application by downloading the WinSLAC coefficient file generated by the WinSLAC coefficient generation software. For more information on downloading custom coefficient files see the Mini-PBX User's Guide. For this line module the two-wire impedance is nominally set to be 600 $\Omega$.

### 2.5.2 Four-Wire Return Loss or Transhybrid Balance Impedance

The QLSLAC device can modify the four-wire port balance or line impedance ($Z_L$) by programming the B-filter. All of the complex balance impedance for subscriber lines from areas like China, Europe, Middle East, Africa, South America and North America can be achieved with no hardware changes. The achievable four-wire return loss for these terminations is higher than any country's required value for subscriber lines. The Zarlink VoicePath Mini-PBX software provides a 600-$\Omega$ resistive, 900-$\Omega$ resistive, and German Complex impedance for demonstration purposes. Other line impedances can be supported in the Mini-PBX application by downloading the WinSLAC coefficient file generated by the WinSLAC coefficient generation software. For more information on downloading custom coefficient files see the Mini-PBX User's Guide.

### 2.5.3 Equalization

The QLSLAC device is capable of applying equalization to either the transmit direction (into the PSTN) or the receive direction (from the PSTN). The equalization can provide compensation for attenuation distortion caused by the line. The equalization for attenuation distortion caused by complex two-wire port impedance is automatically done in the Zarlink WinSLAC software. Other equalization can be applied with the WinSLAC software if special needs exist. See the *WinSLAC User's Guide* for information on the WinSLAC Software.

### 2.5.4 Transmit Gain (AX/GX)

The transmit gain of the SLIC/SLAC device system is determined by the two-to-four-wire gain through the SLIC device ($G_{24}$) and the gain of the QLSLAC device in the transmit direction. For the Le79R79 device, $G_{24}$ is equal to $-6.02$ dB and the QLSLAC transmit gain can be adjusted from 0 dB to +18 dB. It is important to point out that with the QLSLAC transmit gain set to unity, a 0.5 VRMS signal presented to its analog input will produce a 0 dBm0 on the PCM highway (A-Law). When using the QSLAC device, or if the internal attenuator of the QLSLAC device is enabled a 0.775 VRMS signal at the analog input will produce a 0 dBm0 signal on the PCM highway. As an example, suppose a system gain of 0 dB is desired and that the SLIC device presents a 600-$\Omega$ termination to the line. This implies that a 0 dBm signal on the two wire side of the SLIC device will have a voltage of 0.775 VRMS. Since the voltage gain through the SLIC device is -6.02 dB, the voltage presented to the SLAC device's analog input will be 0.388 VRMS. This voltage will give a -6 dBm0 signal on the PCM highway if the internal attenuator is enabled. Therefore it is necessary to set the QLSLAC device gain to +6 dB to achieve the desired 0 dBm0 signal on the PCM highway. The system transmit gain is set in the WinSLAC program. For more information on setting the transmit gain, please refer to the *Le79R79 Ringing SLIC User's Guide* and the *QLSLAC Data Sheet*.

### 2.5.5 Receive Gain (AR/GR)

The system receive gain is determined by the QLSLAC device receive gain, and the four-to-two-wire gain ($G_{42}$) through the SLIC device. The QLSLAC device receive gain ranges from 0 dB to $-18$ dB. The magnitude of $G_{42}$, the gain through the SLIC device, is determined by the RTX and RRX resistors. For this line module, $G_{42}$ has be set to unity when the load presented to the SLIC device is 600 $\Omega$. It is important to note that $G_{42}$ is a function of the load presented to the SLIC device. For more information on setting the receive gain, please refer to the *Le79R79 Ringing SLIC User's Guide* and the *QLSLAC Data Sheet*.

### 2.5.6 Longitudinal Balance

This reference design hardware utilizes 1% 50-$\Omega$ resistors for current limiting in the surge protection circuit. The longitudinal balance is determined by how well these resistors are matched.

## 2.6 SIGNALING

### 2.6.1 Loop Supervision

The switch hook detect is accomplished by comparing the loop resistance to a loop threshold programming resistor $R_D$. When the loop resistance is less than the programmed resistance set by $R_D$, the loop detect pin of the SLIC device is pulled Low to indicate an off-hook condition. In the Active and OHT states loop threshold resistance is set to 5.4 k$\Omega$ when operating from of low battery ($V_{BAT2}$) or 6.0 k$\Omega$ when operating off of high battery (VBAT1). In the Standby state the threshold

resistance is set to 3.5 k$\Omega$ These loop thresholds include 50-$\Omega$ fuse resistors and any line resistance. For more information on setting the loop detect threshold, refer to the *Le79R79 Ringing SLIC User's Guide*.

### 2.6.2      Ring Trip

The line module is set up for short loop ring trip detection (no DC offset) and uses AC detection of the ring trip condition. Ring trip is detected by sensing the AC resistance of the line. A threshold resistance is set using an external resistor. When the AC impedance drops below the threshold resistance, ring trip occurs. Since this line module is designed to ring a 5REN load at zero loop length, a threshold resistance of less then 1400 $\Omega$ must be selected. For this application the ring trip threshold resistance is set to approximately 650 $\Omega$. For complete details on setting the ring trip threshold, refer to the *Le79R79 Ringing SLIC User's Guide*.

## 2.7      DC FEED

The DC feed curve for the Le79R79 device consists of an amplifier anti-saturation region and a constant current region. Under normal short loop conditions, the Le79R79 device generally operates as constant current source in the Off-hook state. As the loop length increases so does the loop resistance, thereby requiring a higher Tip/Ring voltage to maintain a constant current. At a given Tip/Ring threshold voltage the device switches into its anti-saturation region to prevent saturation and clipping of the amplifiers. For the Le79R79 device, this threshold voltage is set to 12.5 V when operating from $V_{BAT2}$ (low battery) and 44 V when operating from $V_{BAT1}$ (high battery). The anti-saturation region for the Le79R79 device looks like a voltage feed with a fairly high series feed resistance. For this application, the feed resistance in the anti-saturation region is about 168 $\Omega$.

### 2.7.1      Loop Range

The loop range is determined by the apparent Tip/Ring voltage at zero loop current ($V_{APP}$), the line impedance, and the current requirements of the CPE equipment. The maximum loop length is achieved when running from $V_{BAT1}$ where $V_{APP}$ is equal to 48.2 V. For example, if we assume a 250-$\Omega$ phone, a minimum loop current of 18 mA, 26 AWG wire (24.5 ft/$\Omega$), and two 50-$\Omega$ fuse resistors, then the line resistance (Tip + Ring) can be as high as 2159 $\Omega$ when running from the -63 V ($V_{BAT1}$). This is equivalent to about a 26 kft loop. Ringing, of course, will not accommodate out to this distance. When running from the $-21$ V supply ($V_{BAT2}$) this feed range drops to about 5 kft. Note that fully serviceable loop length is dictated by the ringing range. See below for a discussion of the ringing range.

### 2.7.2      Loop Current Range

The loop current of this design is limited to 25 mA.

### 2.7.3      Power Supplies

The most negative power supply for this design was selected such that the UL1950 requirements for the maximum voltage of an open circuit loop would be met. This specification requires that no open circuit voltage greater than 56.5 V shall be present. This requirement does not apply during ringing. In the Le79R79 device, the magnitude of the open circuit voltage at tip and ring is between 8 V and 10 V less than the magnitude of $V_{BAT1}$ when in the Standby state. To meet the UL1950 specification $V_{BAT1}$ was chosen to be 63 V, thus giving an open circuit voltage of about 55 V. The topology of the power supply used on this reference design dictated that $V_{BAT2}$ be 1/3 of $V_{BAT1}$ or 21 V.

### 2.7.4      Ringing Range

The ringing range is set by five factors: the number of Ringer Equivalences desired to ring per line, the ringing waveform, the available battery voltage, the required ringing voltage presented to the ringer, and the ring source series resistance. REN, or Ringer Equivalence Number, is a measure of ringer load or how many standard electro-mechanical ringers can be rung. One REN is generally thought to be about 6800 $\Omega$ at a 20-Hz ringer frequency. The required ringer voltage should be about 40 VRMS at the CPE.

This design uses trapezoidal ringing waveform with a crest factor (CF) equal to 1.21, and a ring source series resistance of 187 $\Omega$. The Le79R79 device generates a ringing voltage equal to

($V_{BAT1}$ − 2.5) VPK or approximately 50 VRMS when $V_{BAT1}$ is set to 63 V and the crest factor is set to 1.21. For this design, 5 REN can be rung at 0 loop and 2.5 REN can be rung out to approximately 3.9 kft. The design's loop range is limited by the ringing capability.

## 3.1      CURRENT AND VOLTAGE LIMITING

This line module design has series current limiting and shunt voltage limiting for lightning and surge protection. The protection design utilizes a Teccor F1250T fuse device in series with 50-$\Omega$ fuse resistors on tip and ring to limit surge current.

Voltage limiting in the line circuit is provided by a Teccor PO641SC Sidactor. This device is a solid state crowbar device that is designed to protect the line circuit during dangerous transient conditions. These devices are triggered upon application of a voltage that exceeds its triggering voltage. For the PO641SC, a voltage greater than 58 V will trigger the device. Once the device has been triggered, it will appear as a short circuit to ground until a minimum holding current is reached. When this holding current is reached the device will reset and return to its transparent open circuit state. In the triggered state, the voltage across it will not exceed 5 V. These devices also contain an integrated diode that will clamp any positive going voltages presented on tip or ring. There are two devices used for each line circuit, one for the tip and one for ring. Current limiting into the tip and ring leads of the Le79R79 device is accomplished by the 50-$\Omega$ series resistors.

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# 4    LINE CIRCUIT IDENTIFICATION MEMORY

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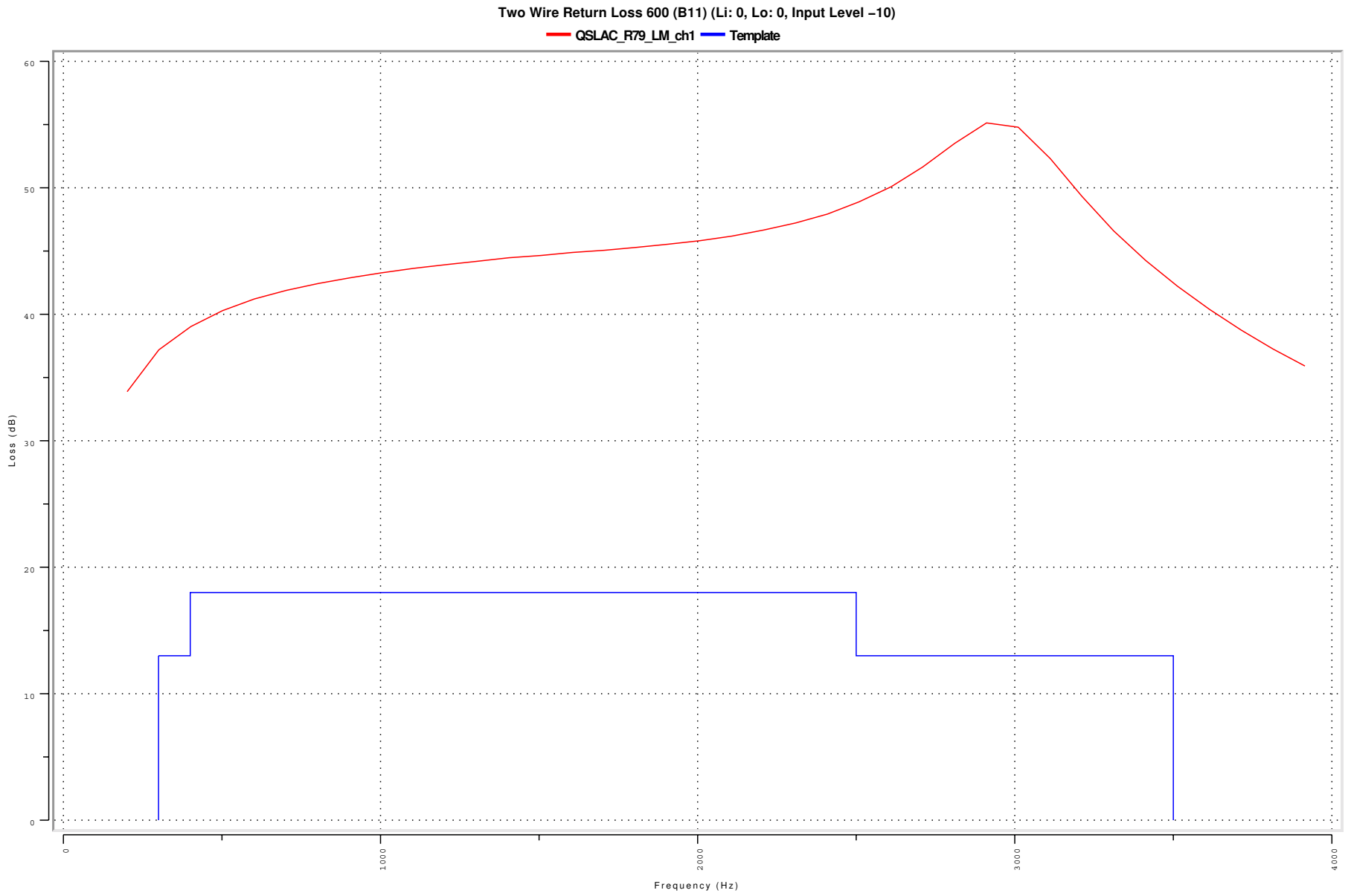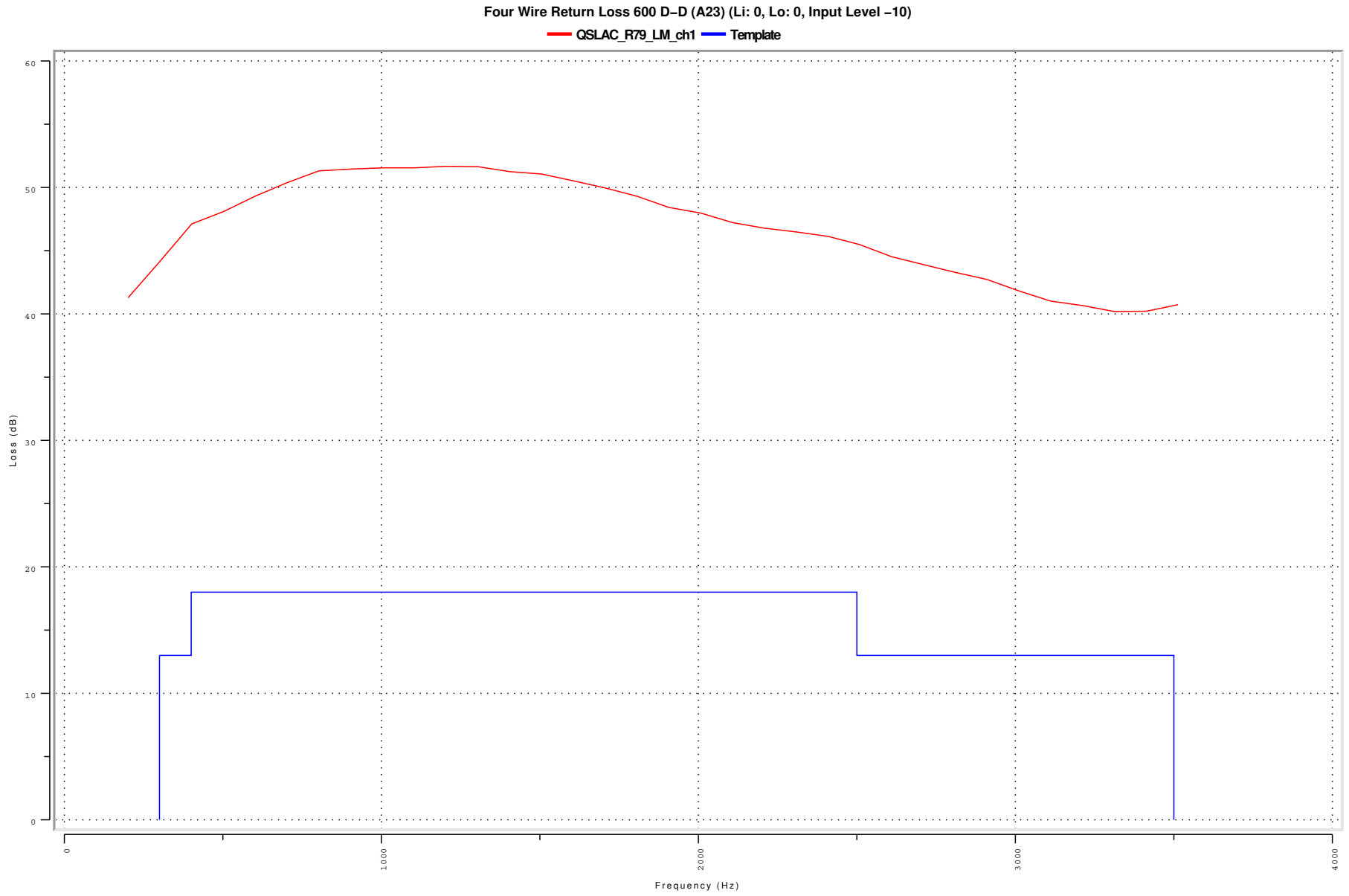## 4.1    ID EEPROM

The line module has a Dallas Semiconductor DS2433 EEPROM on the PCB. This is a 4 kbit one-wire EEPROM memory which, while not crucial to module operation, is essential to the demonstration system. This memory is factory loaded with a line module design identification, a serial number, and various control coefficient sets. These coefficient sets provide the user with differing AC transmission characteristics for this market segment. Of course a user is not limited to these coefficient sets. Zarlink provides a tool chain to enable the line module user to program their own desired coefficient set. The line module user can remove the ID EEPROM from their custom design by using their own coefficients contained in their own software code. This ID EEPROM might be replaced by a smaller EEPROM in the user design. This could contain the recommended or required Telecordia "CLEI" code information.

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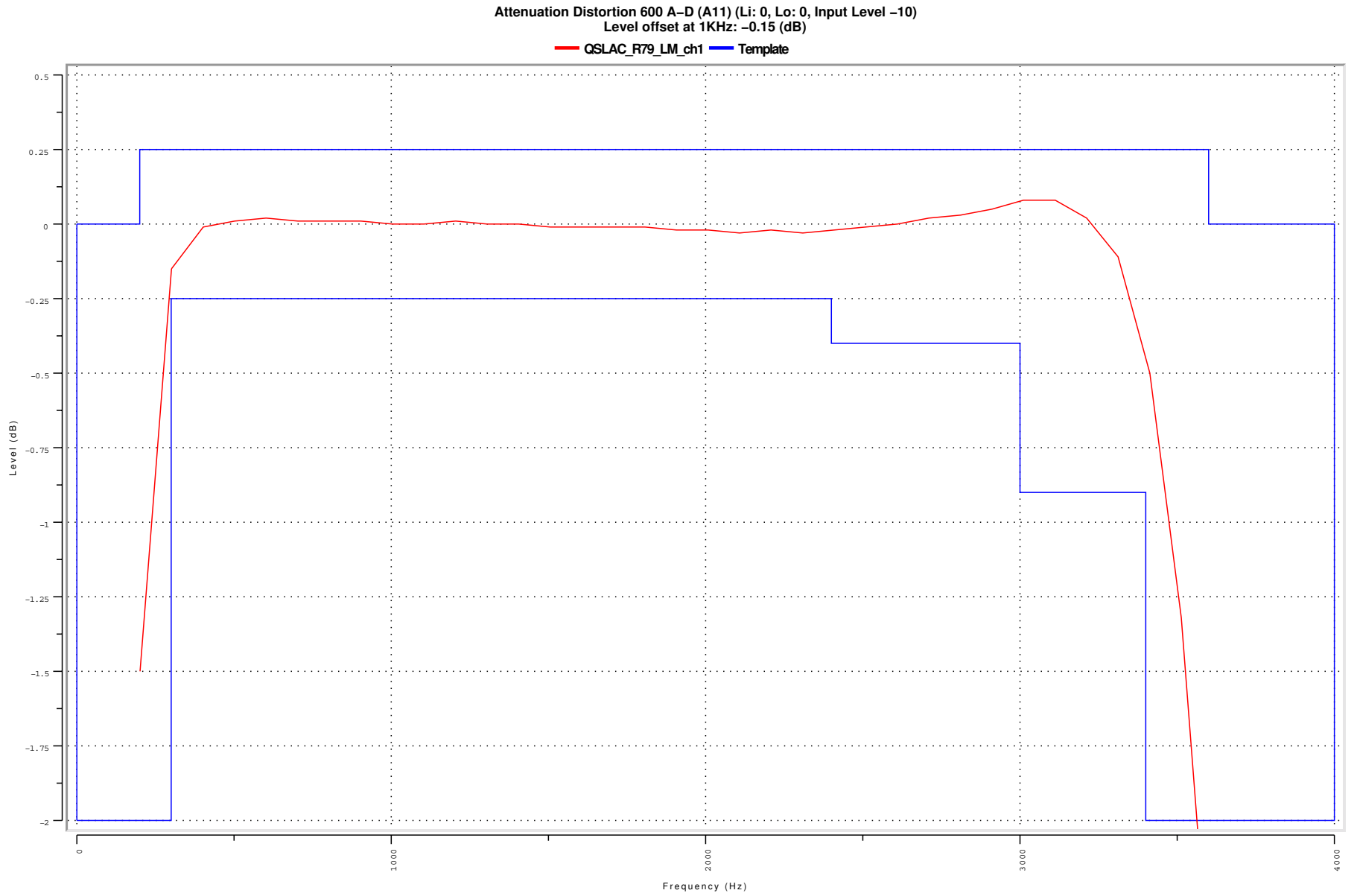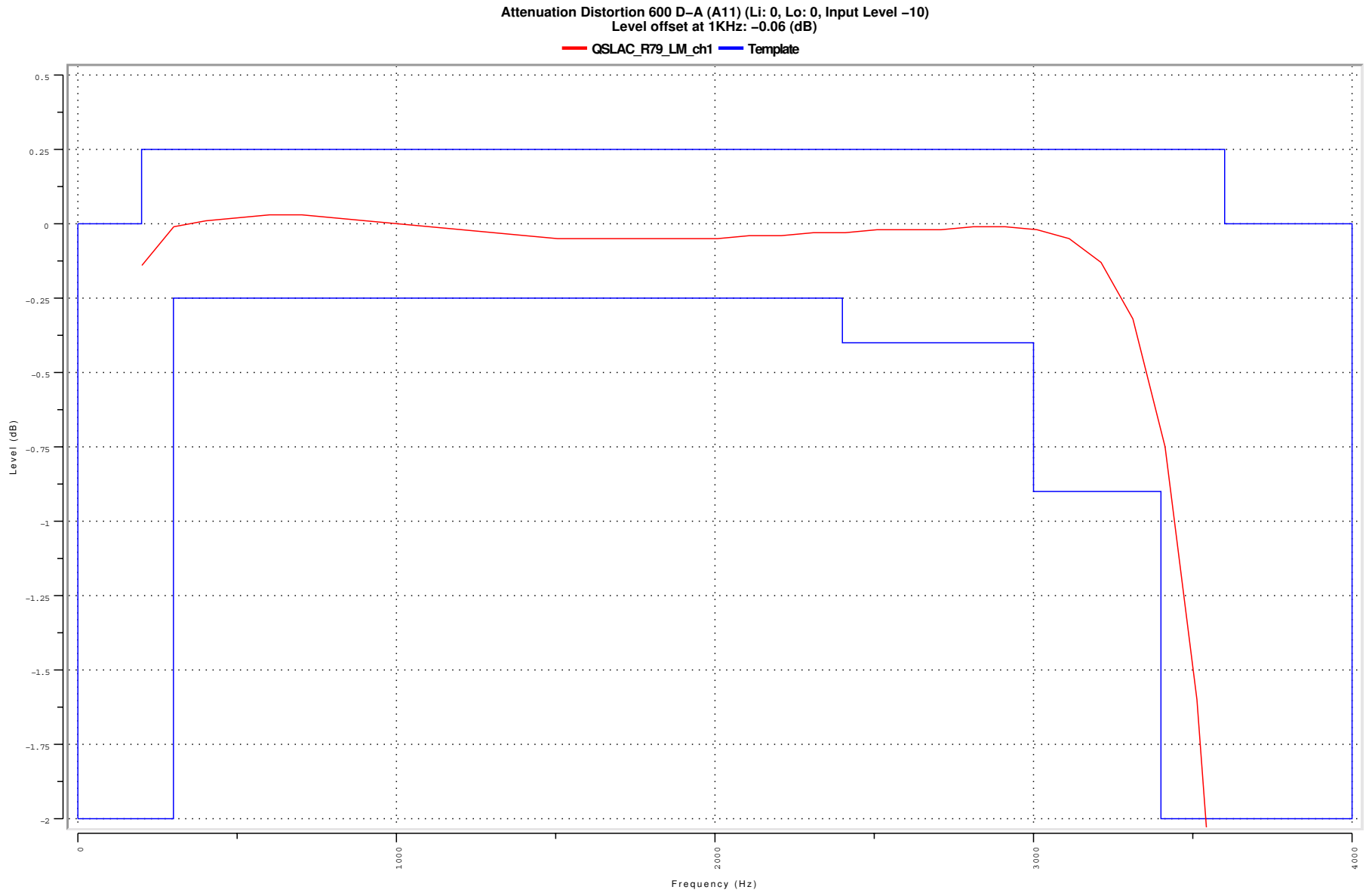
# 5 LINE MODULE PERFOR-MANCE DATA

## 5.1 PERFORMANCE DATA GRAPHS

The graphs on the following pages provide typical performance data for this line module.

**Two Wire Return Loss 600 (B11) (Li: 0, Lo: 0, Input Level –10)**

QSLAC_R79_LM_ch1     Template

**Four Wire Return Loss 600 D–D (A23) (Li: 0, Lo: 0, Input Level –10)**

QSLAC_R79_LM_ch1 ————    Template ————

**Attenuation Distortion 600 A–D (A11) (Li: 0, Lo: 0, Input Level –10)**
**Level offset at 1KHz: –0.15 (dB)**

━━ QSLAC_R79_LM_ch1    ━━ Template

**Attenuation Distortion 600 D–A (A11) (Li: 0, Lo: 0, Input Level –10)**
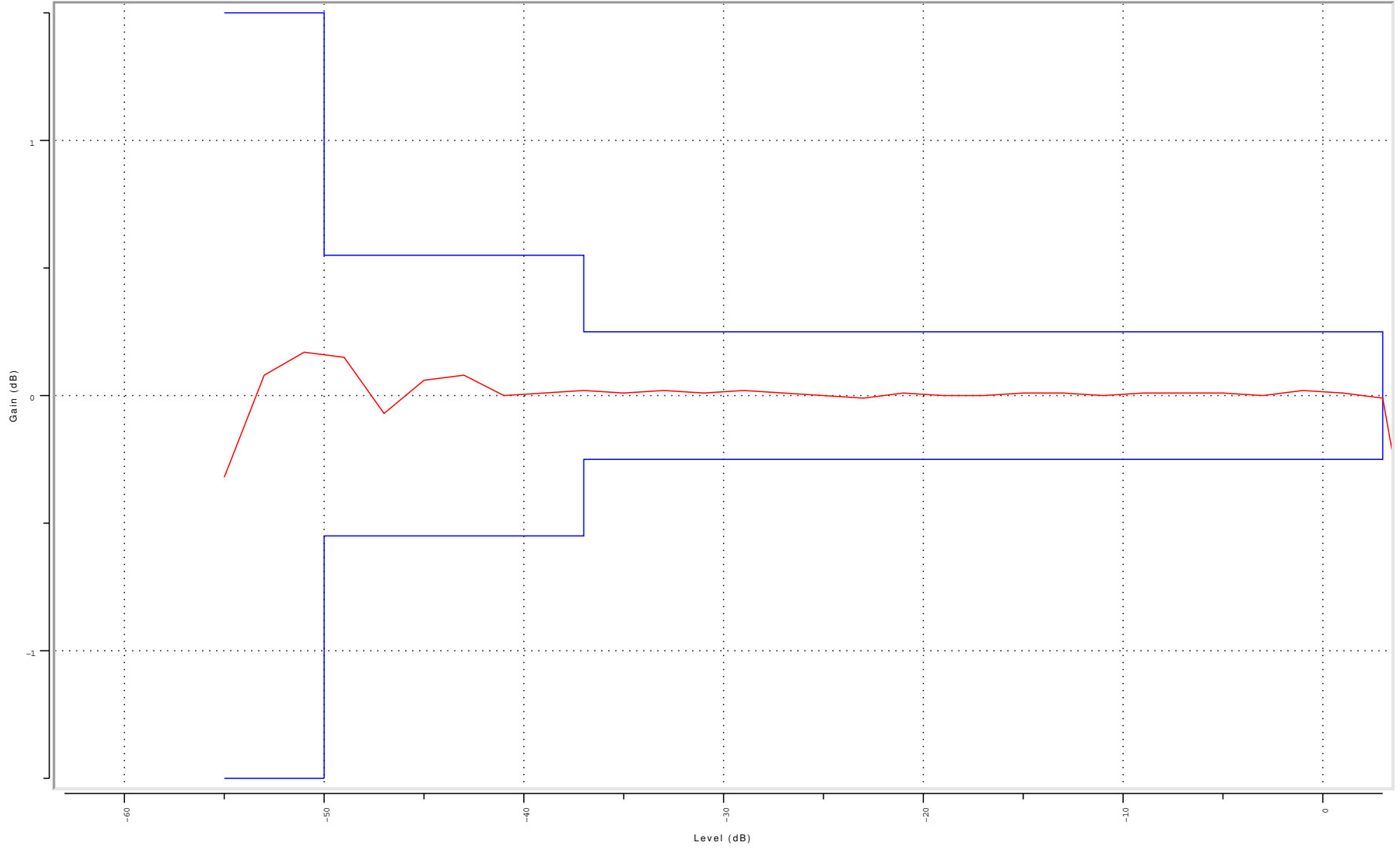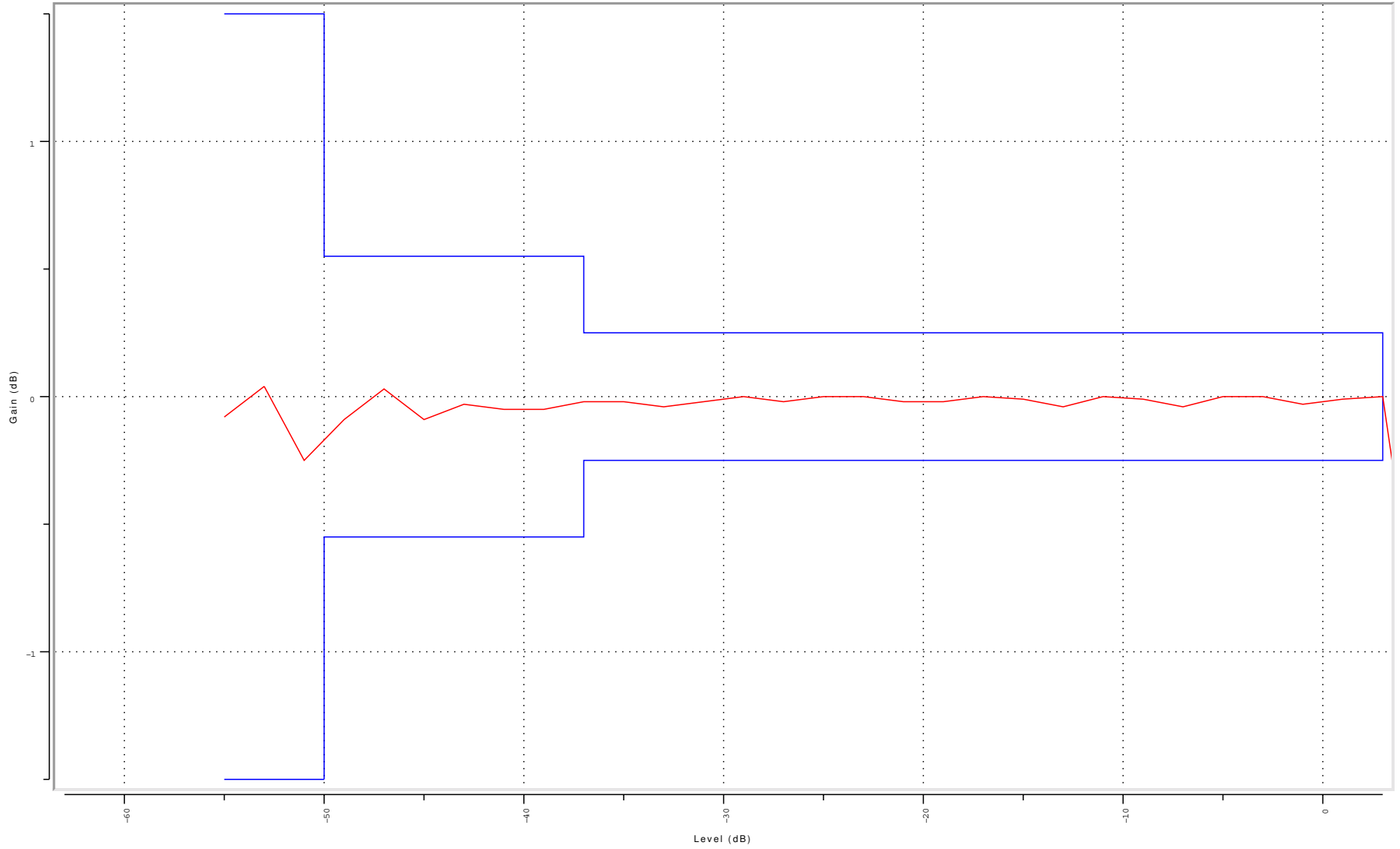**Level offset at 1KHz: –0.06 (dB)**

**Gain Tracking 600 A–D (A43) (Li: 0, Lo: 0, Input Level –10)**
**ICN: PSOPH (A61) –99.81, C–Message (A62) –96.30 (dBm0)**
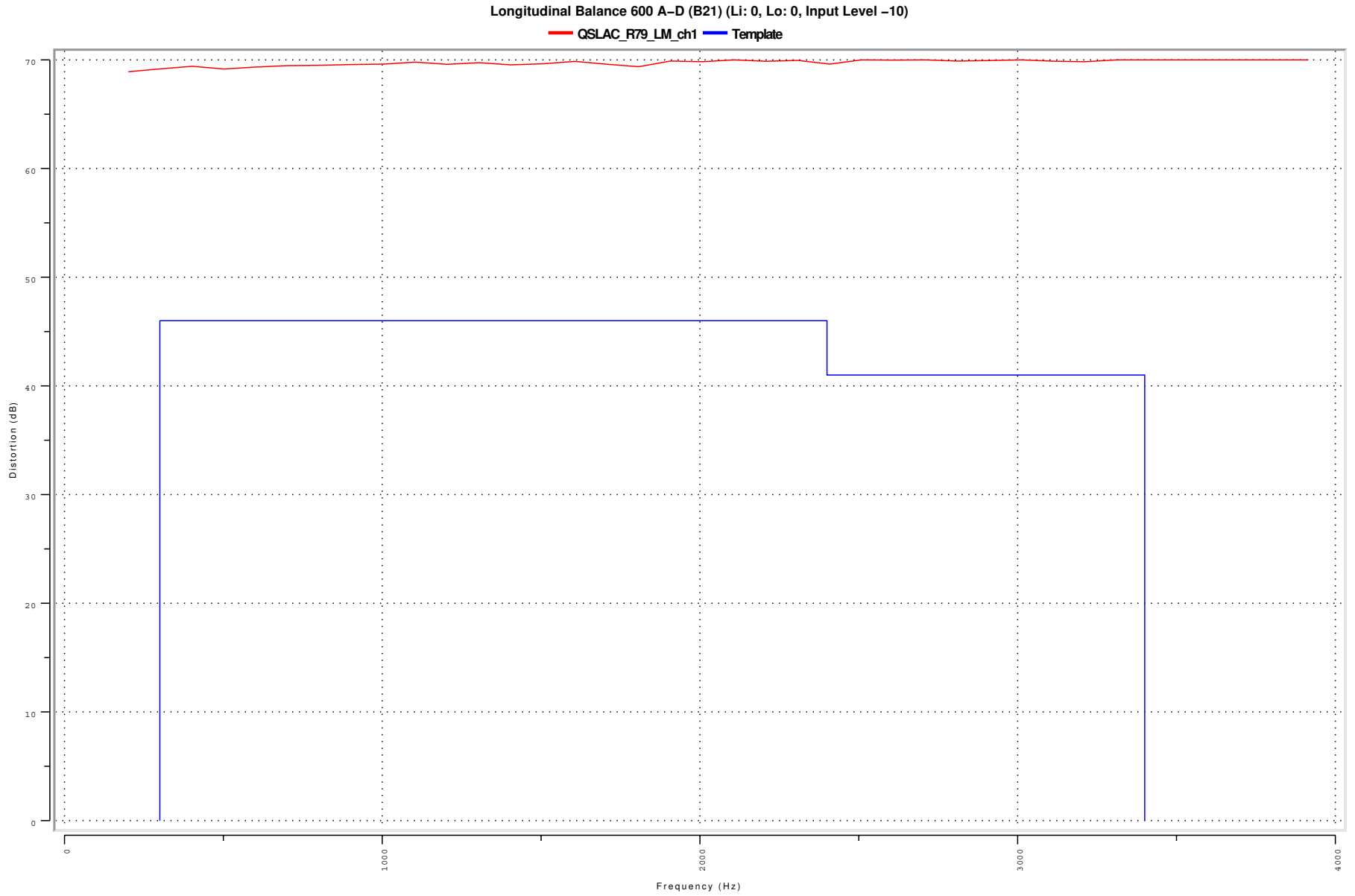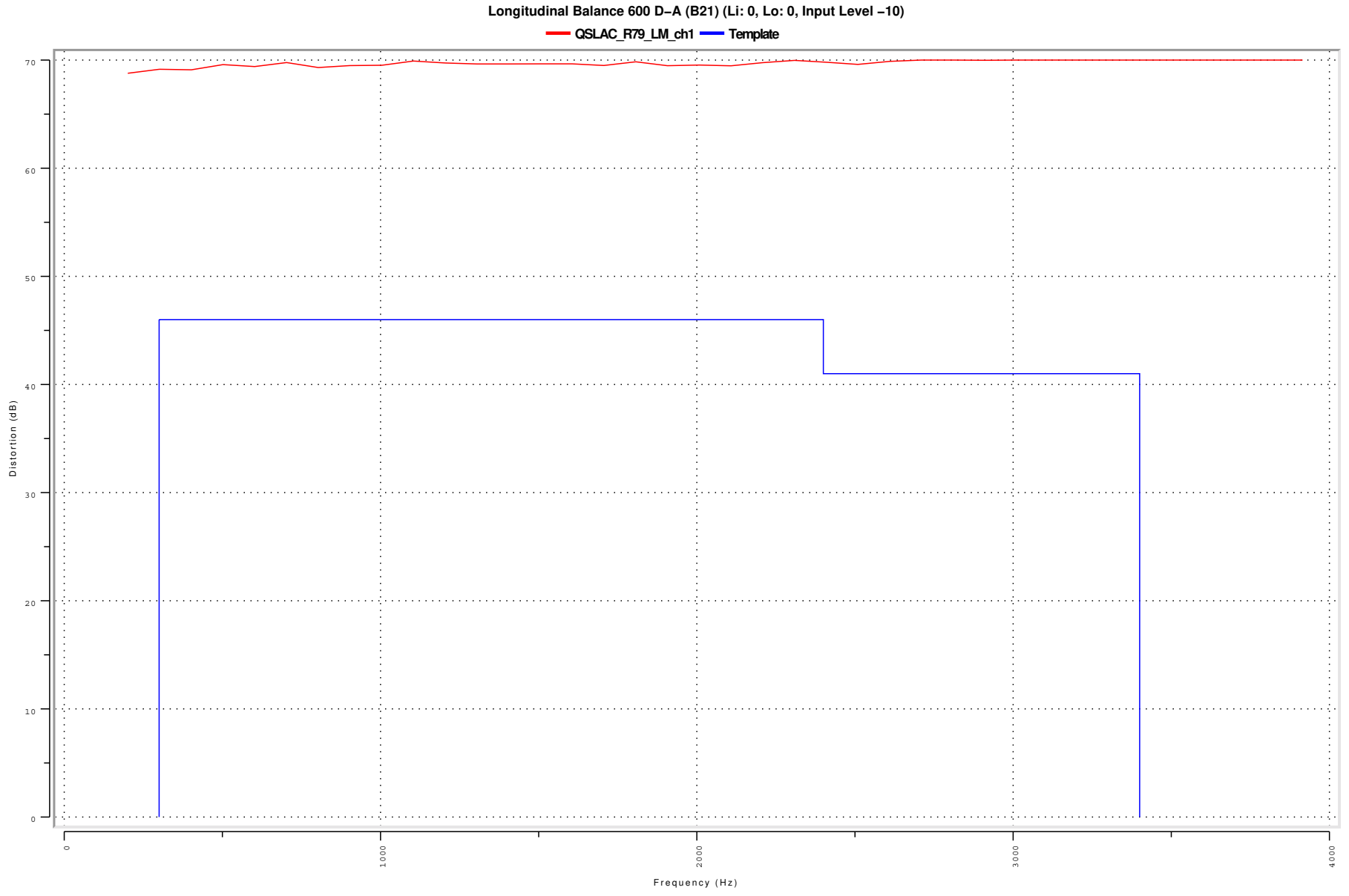**300Hz...3350Hz (A63) –94.29 (dBm0)**

**Gain Tracking 600 D–A (A43) (Li: 0, Lo: 0, Input Level –10)**
**ICN: PSOPH (A61) –84.85, C–Message (A62) –84.38 (dBm0)**
**300Hz...3350Hz (A63) –82.20 (dBm0)**

━━ QSLAC_R79_LM_ch1    ━━ Template

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**Longitudinal Balance 600 A–D (B21) (Li: 0, Lo: 0, Input Level –10)**

═══ QSLAC_R79_LM_ch1   ═══ Template

**Longitudinal Balance 600 D–A (B21) (Li: 0, Lo: 0, Input Level –10)**
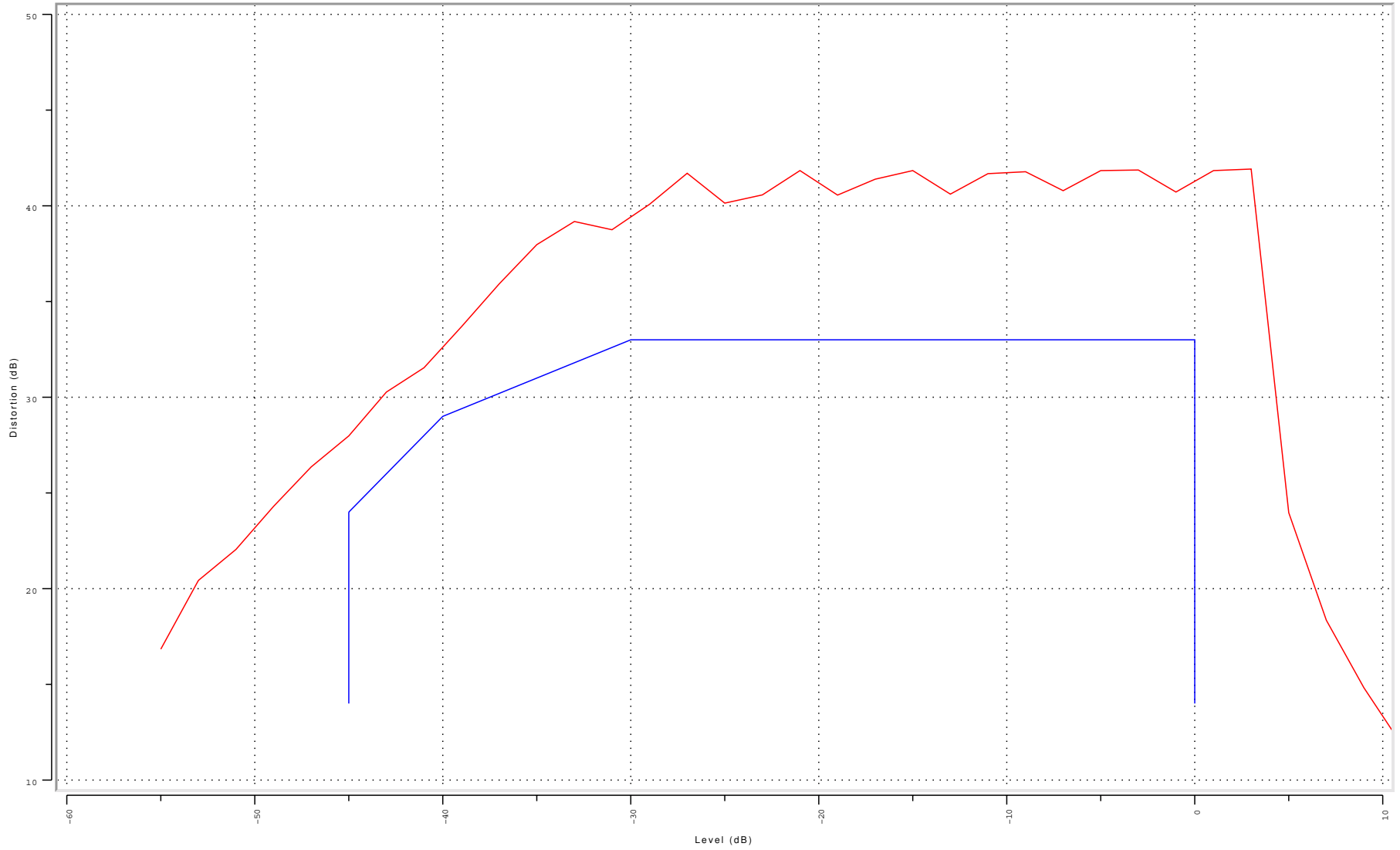
QSLAC_R79_LM_ch1    Template

**Total Distortion 600 A–D (A56) (Li: 0, Lo: 0, Input Level –10)**
**Harmonic Dis 2nd (A91): +56.38, 3rd (A92): +56.38 (dB)**
**Intermod. Dis 2nd (A93): +53.82, 3rd (A94): +55.10 (dB)**

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**Total Distortion 600 D–A (A56) (Li: 0, Lo: 0, Input Level –10)**
**Harmonic Dis 2nd (A91): +52.10, 3rd (A92): +53.98 (dB)**
**Intermod. Dis 2nd (A93): +53.62, 3rd (A94): +52.32 (dB)**

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