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ZARLINK SEMICONDUCTOR

VoiceEdge

# Le75282

## *Dual Intelligent Line Card Access Switch*
## VE750 Series

## APPLICATIONS

- **Central office**
- **DLC**
- **PBX**
- **DAML**
- **HFC/FITL**

## FEATURES

- **Small size/surface-mount packaging**
- **Monolithic IC reliability**
- **Low impulse noise**
- **Make-before-break, break-before-make operation**
- **Clean, bounce-free switching**
- **Low, matched ON-resistance**
- **Built-in current limiting, thermal shutdown, and SLIC device protection**
- **5-V operation, very low power consumption**
- **Battery monitor, All Off state upon loss of battery**
- **No EMI**
- **Latched logic level inputs, no drive circuitry**
- **Only one external protector required per channel**

## RELATED LITERATURE

- **081065 Le79228 Quad ISLAC™ Device Data Sheet**
- **081190 Le792288 Octal ISLAC™ Device Data Sheet**
- **081143 Le79232 Dual ISLIC™ Device Data Sheet**
- **081144 Le79252 Dual ISLIC™ Device Data Sheet**
- **080923 Le792x2/Le79228 Chip Set User's Guide**

## ORDERING INFORMATION

| Device | Package Type[1] | Packing[2] |
|---|---|---|
| Le75282BBVC | 44-pin TQFP (Green) | Tray |

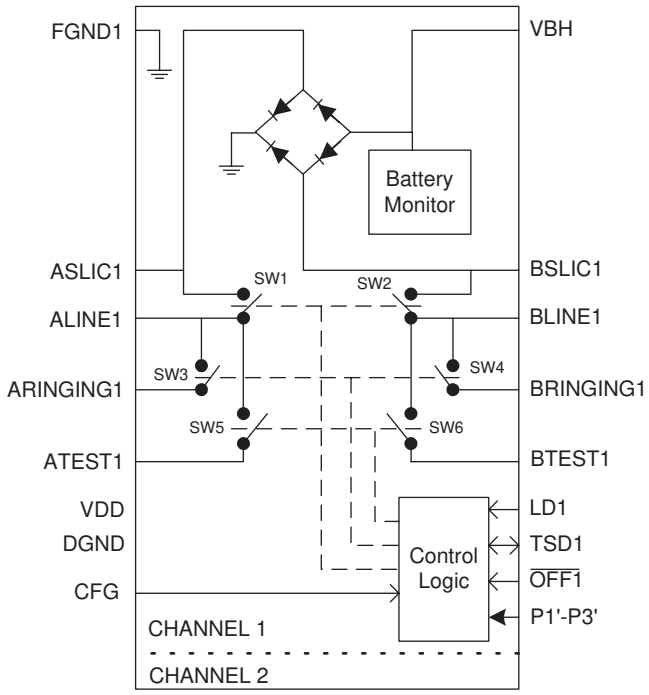
1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

## DESCRIPTION

The Le75282 Dual Intelligent Line Card Access Switch (LCAS) device is a monolithic solid-state device that provides the switching functionality of *four* 2 Form C relays in one economical small package.

The Le75282 Dual LCAS device is designed to provide power ringing access to a telephone loop in central office, digital loop carrier, private branch exchange, digitally added main line, and hybrid fiber coax/fiber-in-the-loop analog line card applications. An additional pair of solid-state contacts provides access to the telephone loop for line test access or message waiting in the PBX application.

## BLOCK DIAGRAM



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## PRODUCT DESCRIPTION

The Le75282 Dual LCAS device has six operating states:

- **Idle/Talk** — Line break switches closed, ringing and test access switches open.
- **Ringing** — Ringing access switches closed, line break and test access switches open.
- **Test** — Test access switches closed, line break and ringing access switches open.
- **Test/Monitor** — Test access and line break switches closed, ringing access switches open.
- **Test Ringing** — Test and ringing access switches closed, line break switches open.
- **All Off** — Line break and ringing and test access switches open.

Control is provided by an Intelligent Subscriber Line Audio-processing Circuit (ISLAC), such as the Le79228 codec, or any microcontroller. See *Applications*. on page 14 for proper connection of the control bus (P-bus).

The Le75282 Dual LCAS device offers break-before-make or make-before-break switching, with simple logic level input control. Because of the solid-state construction, voltage transients generated when switching into an inductive ringing load during ring cadence or ring trip are minimized, possibly eliminating the need for external zero cross switching circuitry. State control is via logic level inputs so no additional driver circuitry is required.

The line break switch is a linear switch that has exceptionally low ON-resistance and an excellent ON-resistance matching characteristic. The ringing access switch has a breakdown voltage rating > 320 V which is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Incorporated into the Le75282 Dual LCAS device is a diode bridge, current-limiting circuitry, and a thermal shutdown mechanism to provide protection to the SLIC device and subsequent circuitry during fault conditions. Positive faults are directed to ground and negative faults to battery. In either polarity, faults are reduced by the built-in current-limit and/or thermal shutdown mechanisms.

To protect the Le75282 Dual LCAS device from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the A (Tip)/B (Ring) terminals to prevent the breakdown voltage of the switches from being exceeded. To minimize stress on the solid-state contacts, use of a foldback- or crowbar- type secondary protector is recommended. With proper choice of secondary protection, a line card using the Le75282 device will meet all relevant ITU-T, LSSGR, FCC, or UL protection requirements.

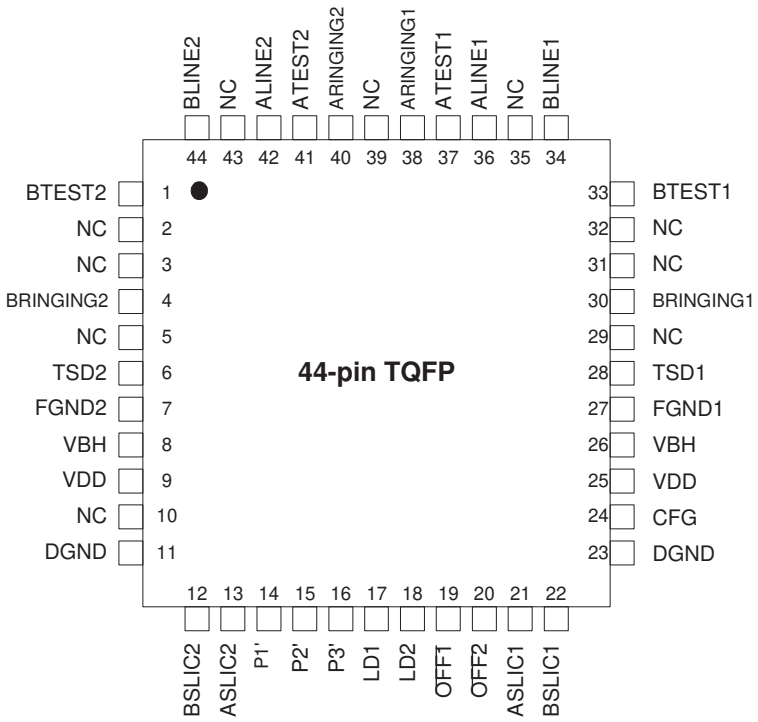
The Le75282 Dual LCAS device provides extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. This makes the Le75282 Dual LCAS device especially appropriate for remote power applications such as DAML or FOC/FITL or other Bellcore TA 909 applications where power dissipation is particularly critical.

Battery voltage is monitored by the control circuitry and used as a reference for the integrated protection circuit. The Le75282 device will enter an All Off state upon loss of battery.

During ringing, to turn on and maintain the ON state, the ringing access switch will draw a nominal 2 mA from the ring generator.

The Le75282 Dual LCAS device is packaged in a 44-pin TQFP package.

## CONNECTION DIAGRAM




## Pin Descriptions

| CH1 | CH2 | Pin Name | Description | CH1 | CH2 | Pin Name | Description |
|---|---|---|---|---|---|---|---|
| 27 | 7 | FGNDx | Fault ground. | 8, 26 | | VBH | High-battery voltage. Used as a reference for protection circuit. |
| 21 | 13 | $ASLIC_x$ | Connect to A lead on SLIC side. | 22 | 12 | BSLICx | Connect to B lead on SLIC side. |
| 36 | 42 | ALINEx | Connect to A lead on line side. | 34 | 44 | BLINEx | Connect to B lead on line side. |
| 38 | 40 | ARINGINGx | Connect to return ground of ringing generator. | 30 | 4 | BRINGINGx | Connect to ringing generator. |
| 37 | 41 | $ATEST_x$ | A lead test access. | 33 | 1 | BTESTx | B lead test access. |
| 9, 25 | | VDD | 5 V supply. | 17 | 18 | LDx | Data latch channel control, active low. |
| 28 | 6 | TSDx | Temperature shutdown flags. Read VDD potential when device is in its operational mode and 0 V when device is in the thermal shutdown mode. | 14 | | P1' | Logic level input switch control. Connect to P-bus. See *Applications*, on page 14 for proper connection. |
| 11, 23 | | DGND | Digital ground. | 15 | | P2' | Logic level input switch control. Connect to P-bus. See *Applications*, on page 14 for proper connection. |
| 19 | 20 | $\overline{OFF}$x* | All Off logic level input switch control. A pull-down device is included, setting All Off as the power-up default state. These pins can also be used as a device reset. **If these pins are not to be used, they must be tied to VDD.** | 16 | | P3' | Logic level input switch control. Connect to P-bus. See *Applications*, on page 14 for proper connection. |
| 2, 3, 5, 10, 29, 31, 32, 35, 39, 43 | | NC | No Connect. This pin is not internally connected. | 24 | | CFG | Operating states configuration. Tie to DGND to select operating states as defined in Table 9. Tie to VDD for operating states as defined in Table 10. |

***Notes:***

*"x" denotes channel number.*

** Internal pull down on this node.*

## ABSOLUTE MAXIMUM RATING

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Operating Temperature Range | –40 | 110 | °C |
| Storage Temperature Range | –40 | 150 | °C |
| Relative Humidity Range | 5 | 95 | % |
| Pin Soldering Temperature (t=10 s max) | — | 260 | °C |
| 5-V Power Supply | -0.3 | 7 | V |
| Battery Supply | — | –85 | V |
| Logic Input Voltage | -0.3 | $V_{DD}$+0.3 | V |
| Input-to-output Isolation | — | 330 | V |
| Pole-to-pole Isolation | — | 330 | V |
| ESD Immunity (Human Body Model) | JESD22 Class 1C compliant | | |

### Package Assembly

Green package devices are assembled with enhanced, environmental, compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

## OPERATING RANGES

### Environmental Ranges

Zarlink guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment

.

| | |
|---|---|
| Ambient Temperature | 0 to 70°C Commercial |
| | –40 to +85 °C extended temperature |
| Ambient Relative Humidity | 15 to 85% |

### Electrical Ranges

| | |
|---|---|
| $V_{DD}$ | +4.75 V to +5.25 V |
| $V_{BH}$ | –19 V to –72 V |

## ELECTRICAL CHARACTERISTICS

$T_A$ = –40 °C to +85 °C, unless otherwise specified.

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

**Table 1. Break Switches, SW1x (A lead) and SW2x (B lead)** (Refer to Figure 2, on page 12)

| Parameter | Test Condition | Measure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OFF-state Leakage Current: | | | | | | |
| +25 °C | Vswitch (differential) = –320 V to Gnd<br>Vswitch (differential) = –60 V to +260 V | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (differential) = –330 V to Gnd<br>Vswitch (differential) = –60 V to +270 V | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (differential) = –310 V to Gnd<br>Vswitch (differential) = –60 V to +250 V | Iswitch | — | — | 1 | µA |
| ON-resistance: | $A_{LINE}$ = ±10 mA, ±40 mA, $A_{SLIC}$ = –2 V<br>$B_{LINE}$ = ±10 mA, ±40 mA, $B_{SLIC}$ = –2 V | | | | | |
| +25 °C | | Δ VON | — | 19 | — | Ω |
| +85 °C | | Δ VON | — | — | 31 | Ω |
| –40 °C | | Δ VON | — | 14 | — | Ω |
| ON-resistance Match | Per ON-resistance test condition of SW1, SW2 | Magnitude RON SW1 – RON SW2 | — | 0.02 | 1.0 | Ω |
| ON-state Voltage[1] | Maximum Differential Voltage ($V_{max}$) | VON | — | — | 320 | V |
| | Foldback Voltage Breakpoint 1 ($V_1$) | VON | 60 | — | — | |
| | Foldback Voltage Breakpoint 2 ($V_2$) | VON | $V_1$ + 0.5 | — | — | |
| DC Current Limit | $I_{LIM1}$ | Iswitch | 85 | 145 | 300 | mA |
| | $I_{LIM2}$ | Iswitch | 1 | — | — | |
| Dynamic Current Limit[2] (t = < 0.5 µs) | Break switches in ON state; ringing switches off; apply ±1000 V (Source impedance 10 Ω) unipolar double exponential 10/1000 µs pulse with appropriate secondary protection in place | Iswitch | — | 2.5 | — | A |
| Isolation: | | | | | | |
| +25 °C | Vswitch (both poles) = ±320 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (both poles) = ±330 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (both poles) = ±310 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| dV/dt Sensitivity[3] | — | — | — | 200 | — | V/µs |

*1. Choice of secondary protector should ensure this rating is not exceeded.*

*2. This parameter is not tested in production.*

*3. Applied voltage is 100 Vp-p square wave at 100 Hz.*

**Table 2. Ringing Return Switch, SW3x** (Refer to Figure 2, on page 12)

| Parameter | Test Condition | Measure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OFF-state Leakage Current: | | | | | | |
| +25 °C | Vswitch (differential) = –320 V to Gnd<br>Vswitch (differential) = –60 V to +260 V | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (differential) = –330 V to Gnd<br>Vswitch (differential) = –60 V to +270 V | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (differential) = –310 V to Gnd<br>Vswitch (differential) = –60 V to +250 V | Iswitch | — | — | 1 | µA |
| ON-resistance | Iswitch (on) = ±0 mA, ±10 mA | Δ VON | — | 26 | 110 | Ω |
| ON-state Voltage[1] | Maximum Differential Voltage ($V_{max}$) | VON | — | — | 320 | V |
| | Foldback Voltage Breakpoint 1 ($V_1$) | VON | 200 | — | — | |
| | Foldback Voltage Breakpoint 2 ($V_2$) | VON | $V_1$ + 0.5 | — | — | |
| dc Current Limit | $I_{LIM1}$ | Iswitch | 70 | — | — | mA |
| | $I_{LIM2}$ | Iswitch | 1 | — | — | |
| Isolation: | | | | | | |
| +25 °C | Vswitch (both poles) = ±320 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (both poles) = ±330 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (both poles) = ±310 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| dV/dt Sensitivity[2] | — | — | — | 200 | — | V/µs |

*1. This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

*2. Applied voltage is 100 Vp-p square wave at 100 Hz.*

**Table 3. Ringing Access Switch, SW4x** (Refer to Figure 3, on page 12)

| Parameter | Test Condition | Measure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OFF-state Leakage Current (SW4): | | | | | | |
| +25 °C | Vswitch (differential) = –255 V to +210 V<br>Vswitch (differential) = +255 V to –210 V | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (differential) = –270 V to +210 V<br>Vswitch (differential) = +270 V to –210 V | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (differential) = –245 V to +210 V<br>Vswitch (differential) = +245 V to –210 V | Iswitch | — | — | 1 | µA |
| ON-resistance | Iswitch (on) = ±70 mA, ±80 mA | Δ VON | — | 6 | 20 | Ω |
| Crossover Offset Voltage | Iswitch (on) = ±1 mA | VOS | — | — | 3 | V |
| Ring Generator Current During Ring | VCC = 5 V | IRING-SOURCE | — | 2 | — | mA |
| Steady-state Current[1] | — | — | — | — | 150 | mA |
| Surge Current[1] | Ringing access switch on; apply unipolar double exponential 10/1000 µs pulse | — | — | — | 2 | A |
| Release Current | — | — | — | 500 | — | µA |
| Isolation: | | | | | | |
| +25 °C | Vswitch (both poles) = ±320 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (both poles) = ±330 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (both poles) = ±310 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| dV/dt Sensitivity[2] | — | — | — | 200 | — | V/µs |

*1. This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

*2. Applied voltage is 100 Vp-p square wave at 100 Hz.*

**Table 4. Test Access Switches, SW5x and SW6x** (Refer to Figure 4, on page 13)

| Parameter | Test Condition | Measure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OFF-state Leakage Current: | | | | | | |
| +25 °C | Vswitch (differential) = –320 V to Gnd<br>Vswitch (differential) = –60 V to +260 V | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (differential) = –330 V to Gnd<br>Vswitch (differential) = –60 V to +270 V | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (differential) = –310 V to Gnd<br>Vswitch (differential) = –60 V to +250 V | Iswitch | — | — | 1 | µA |
| ON-resistance: | | | | | | |
| +25 °C | Iswitch (on) = ±10 mA, ±40 mA | Δ VON | — | 34 | — | Ω |
| +85 °C | Iswitch (on) = ±10 mA, ±40 mA | Δ VON | — | — | 77 | Ω |
| –40 °C | Iswitch (on) = ±10 mA, ±40 mA | Δ VON | — | 24 | — | Ω |
| ON-state Voltage[1] | Iswitch = ILIMIT @ 50 Hz/60 Hz | VON | — | — | 130 | V |
| dc Current Limit: | $I_{LIMIT}$: | | | | | |
| +85 °C | Vswitch (on) = ±20 V | Iswitch | 80 | — | — | mA |
| –40 °C | Vswitch (on) = ±20 V | Iswitch | — | — | 250 | mA |
| Isolation: | | | | | | |
| +25 °C | Vswitch (both poles) = ±320 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| +85 °C | Vswitch (both poles) = ±330 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| –40 °C | Vswitch (both poles) = ±310 V, $\overline{OFFx}$ = 0 | Iswitch | — | — | 1 | µA |
| dV/dt Sensitivity[2] | — | — | — | 200 | — | V/µs |

*1. This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

*2. Applied voltage is 100 Vp-p square wave at 100 Hz.*

**Table 5. Diode Bridge**

| Parameter | Test Condition | Measure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Voltage Drop @ Continuous Current (50 Hz/60 Hz) | Apply ± DC current limit of break switches | Forward Voltage | — | — | 3.5 | V |
| Voltage Drop @ Surge Current | Apply ± dynamic current limit of break switches | Forward Voltage | — | 5 | — | V |

**Table 6. Additional Electrical Characteristics**

| Parameter | Test Condition | Measure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital Input Characteristics: | | | | | | |
| Input Low Voltage (P1'-P3', $\overline{OFFx}$, CFG) | — | — | — | — | 0.8 | V |
| Input Low Voltage (LDx) | — | — | — | — | 0.6 | |
| Input High Voltage (P1'-P3', $\overline{OFFx}$) | — | — | 2.0 | — | — | V |
| Input High Voltage (CFG) | — | — | 3.0 | — | — | V |
| Input High Voltage (LDx) | — | — | 1.1 | — | — | V |
| Input Leakage Current (High): ($\overline{OFFx}$) | $V_{DD}$ = 5.25 V, VBH = –72 V, Vlogic-in = 5 V | Ilogic-in | — | — | 500 | µA |
| Input Leakage Current (High): (P1'-P3', LDx, CFG) | $V_{DD}$ = 5.25 V, VBH = –72 V, Vlogic-in = 5 V | Ilogic-in | — | — | 20 | µA |
| Input Leakage Current (Low): (P1'-P3', LDx, $\overline{OFFx}$, CFG) | $V_{DD}$ = 5.25 V, VBH = –72 V, Vlogic-in = 0 V | Ilogic-in | — | — | 20 | µA |

**Table 6. Additional Electrical Characteristics (Continued)**

| | | | | | | |
|---|---|---|---|---|---|---|
| Power Requirements[1]: | $V_{DD}$ = 5 V, VBH = –48 V, | | | | | |
| Power Dissipation | Idle/Talk state | $I_{DD}$, $I_{VBH}$ | — | — | 10 | mW |
| | All Off state | $I_{DD}$, $I_{VBH}$ | — | — | 7.5 | mW |
| | Ringing or Test Access state | $I_{DD}$, $I_{VBH}$ | — | — | 20 | mW |
| $V_{DD}$ Current | $V_{DD}$ = 5 V, | | | | | |
| | Idle/Talk state | $I_{DD}$ | — | — | 2.0 | mA |
| | All Off state[2] | $I_{DD}$ | — | — | 1.5 | mA |
| | Ringing or Test Access state | $I_{DD}$ | — | — | 4.0 | mA |
| $V_{BH}$ Current | $V_{BH}$ = –48 V, All states | $I_{VBH}$ | — | 4 | 10 | µA |
| Temperature Shutdown Requirements[3]: | | | | | | |
| Shutdown Activation Temperature | — | — | 110 | 125 | 150 | °C |
| Shutdown Circuit Hysteresis | — | — | 10 | — | 25 | °C |
| Loss of Battery Detector Threshold: | | | | | | |
| Loss of Battery | — | — | –19 | –12 | –5 | V |
| Resumption of Battery | — | — | –19 | –14 | –5 | V |

*1. Combined power or current of both channels, both channels in same state.*
*2. Controlled via $\overline{OFFx}$ pin.*
*3. Temperature shutdown flag (TSDx) will be high during normal operation and low during temperature shutdown state.*

## ZERO CROSS CURRENT TURN OFF

The ringing access switch (SW4x) is designed to turn off on the next zero current crossing after application of the appropriate logic input control. This switch requires a current zero cross to turn off. This switch, once on, will remain in the ON state (regardless of logic input) until a current zero cross. Therefore, to ensure proper operation, this switch should be connected, via proper impedance, to the ringing generator or some other ac source. Do not attempt to switch pure dc with the ringing access switch.

## SWITCHING BEHAVIOR

When switching from the Ringing state to the Idle/Talk state via simple logic level input control, the Le75282 device is able to provide timing control when the ringing access contacts are released relative to the state of the line break contacts.

Make-before-break operation occurs when the line break switch contacts are closed (or made) before the ringing access switch contact is opened (or broken). Break-before-make operation occurs when the ringing access contact is opened (broken) before the line break switch contacts are closed (made).

Using the logic level input pins P1' and P2', either make-before-break or break-before-make operation of the Le75282 device is easily achieved. The logic sequences are presented in Tables 7 and 8. See Table 9, *Operating States: CFG = 0*, on page 17 for an explanation of the logic states.

When using an Le75282 device in the make-before-break mode during the ring-to-idle transition, for a period of up to one-half the ringing frequency, the B break switch and the pnpn-type ringing access switch can both be in the ON state. This is the maximum time after the logic signal at RD2 has transitioned, where the ringing access switch is waiting to open at the next zero current cross. During this interval, current that is limited to the DC break switch current-limit value will be sourced from the BD node of the SLIC device.

**Table 7. Make-Before-Break Operation**

| CFG=0, RD3=0 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **RD2** | **RD1** | **$\overline{OFFx}$** | **State** | **Timing** | **Break Switches 1x & 2x** | **Ringing Return Switch 3x** | **Ringing Access Switch 4x** | **Test Access Switches 5x & 6x** |
| 1 | 0 | 1 | Ringing | — | OFF | **ON** | **ON** | OFF |
| 0 | 0 | 1 | Make-before-break | SW4 waiting for next zero current crossing to turn off, maximum time—one-half of ringing. In this transition state, current that is limited to the dc break switch current-limit value will be sourced from the BD node of the SLIC. | **ON** | OFF | **ON** | OFF |
| 0 | 0 | 1 | Idle/Talk | Zero cross current has occurred. | **ON** | OFF | OFF | OFF |

**Table 8. Break-Before-Make Operation**

| CFG=0, RD3=0 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| RD2 | RD1 | $\overline{\text{OFFx}}$ | State | Timing | Break Switches 1x & 2x | Ringing Return Switch 3x | Ringing Access Switch 4x | Test Access Switches 5x & 6x |
| 1 | 0 | 1 | Ringing | — | OFF | **ON** | **ON** | OFF |
| X | X | 0 | All Off | Hold this state for 25 ms. SW4 waiting for zero current to turn off. | OFF | OFF | **ON** | OFF |
| X | X | 0 | All Off | Zero current has occurred and SW4 has opened. | OFF | OFF | OFF | OFF |
| 0 | 0 | 1 | Idle/Talk | Release break switches. | **ON** | OFF | OFF | OFF |

## POWER SUPPLIES

Both the VDD and battery supply are brought onto the Le75282 device. The Le75282 device requires only the VDD supply for switch operation; that is, state control is powered exclusively off of the VDD supply. Because of this, the Le75282 device offers extremely low power dissipation, both in the idle and active states.

## LOSS OF BATTERY VOLTAGE

As an additional protection feature, the Le75282 device monitors the battery voltage. Upon loss of battery voltage, both channels of the Le75282 device will automatically enter an All Off state and remain in that state until the battery voltage is restored. The Le75282 device is designed such that the device will enter the All Off state if the battery rises above –12 V (typ.) and will remain off until the battery drops below –14 V (typ.).

Monitoring the battery for the automatic shutdown feature will draw a small current from the battery, typically 4 μA. This will add slightly to the overall power dissipation of the device.

## IMPULSE NOISE

Using the Le75282 device will minimize and possibly eliminate the contribution to the overall system impulse noise that is associated with ringing access switches. Because of this characteristic of the Le75282 device, it may not be necessary to incorporate a zero cross switching scheme. This ultimately depends upon the characteristics of the individual system and is best evaluated at the board level.

## INTEGRATED SLIC DEVICE PROTECTION

### Diode Bridge

Le75282 device protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge, and a thermal shutdown mechanism.

During a positive lightning event, fault current is directed to ground via steering diodes in the diode bridge. Voltage is clamped to a diode drop above ground. Negative lightning is directed to battery via steering diodes in the diode bridge.

For power cross and power induction faults, the positive cycle of the fault is clamped a diode drop above ground and fault currents are steered to ground. The negative cycle of the power cross is steered to battery. Fault currents are limited by the current-limit circuit.

### Current Limiting

During a lightning event, the current that is passed through the Le75282 device is limited by the dynamic current-limit response of the break switches (assuming Idle/Talk state). When the voltage seen at the ALINEx/BLINEx nodes is properly clamped by an external secondary protector, upon application of a 1000 V 10 x 1000 pulse (LSSGR lightning), the current seen at the ASLICx/BSLICx nodes will typically be a pulse of magnitude 2.5 A and duration less than 0.5 μs.

During a power cross event, the current that is passed through the Le75282 is limited by the dc current-limit response of the break switches (assuming Idle/Talk state). The DC current limit is dependent on the switch differential voltage, as shown in Figure 2. on page 12.

Note that the current-limit circuitry has a negative temperature coefficient. Thus, if the device is subjected to an extended power cross, the value of current seen at ASLICx/BSLICx will decrease as the device heats due to the fault current. If sufficient heating occurs, the temperature shutdown mechanism will activate and the device will enter an All Off state.

## Temperature Shutdown Mechanism

When the device temperature reaches a minimum of 110 °C, the thermal shutdown mechanism will activate and force the device into an All Off state, regardless of the logic input pins. Pin TSDx will read low (0 V) when the device is in the thermal shutdown state and high ($V_{DD}$) during normal operation. When the device comes out of thermal shutdown and the TSDx output returns high, the Le75282 device returns to its previously programmed RD1-RD3 state.

During a lightning event, due to the relatively short duration, the thermal shutdown will not typically activate.

During an extended power cross, the device temperature will rise and cause the device to enter the thermal shutdown state. This forces an All Off state, and the current seen at ASLICx/BSLICx drops to zero. Once in the thermal shutdown state, the device will cool and exit the thermal shutdown state, thus re-entering the state it was in prior to thermal shutdown. Current, limited to the dc current-limit value, will again begin to flow and device heating will begin again. This cycle of entering and exiting thermal shutdown will last as long as the power-cross fault is present.

If the magnitude of power is great enough, the external secondary protector could trigger, thereby shunting all current to ground.

# EXTERNAL SECONDARY PROTECTION

An overvoltage secondary protection device on the loop side of the Le75282 device is required. The purpose of this device is to limit fault voltages seen by the Le75282 device so as not to exceed the breakdown voltage or input-output isolation rating of the device. To minimize stress on the Le75282 device, use of a foldback- or crowbar-type device is recommended. Basic design equations governing the choice of external secondary protector are given below:

- $|V_{BHmax}| + |V_{breakovermax}| < |V_{breakdownmin(break)}|$
- $|V_{ringingpeakmax}| + |V_{BHmax}| + |V_{breakovermax}| < |V_{breakdownmin(ring)}|$
- $|V_{ringingpeakmax}| + |V_{BHmax}| < |V_{breakovermin}|$

where:

$V_{BHmax}$—Maximum magnitude of battery voltage.

$V_{breakovermax}$—Maximum magnitude breakover voltage of external secondary protector.

$V_{breakovermin}$—Minimum magnitude breakover voltage of external secondary protector.

$V_{breakdownmin(break)}$—Minimum magnitude breakdown voltage of Le75282 break switch.

$V_{breakdownmin(ring)}$—Minimum magnitude breakdown voltage of Le75282 ringing access switch.

$V_{ringingpeakmax}$—Maximum magnitude peak voltage of ringing signal.

Series current-limiting fused resistors or PTC's should be chosen so as not to exceed the current rating of the external secondary protector. Refer to the manufacturer's data sheet for requirements.

## Test Access Switch Protection Considerations

The most robust design has proper capacitive termination of the test access switches. For a 24 or 32 channel test bus, when all the test leads are tied together, the overall capacitance of the test bus provides adequate termination for the test access switches. For a test bus with less than 24 channels, tie all the leads together and add a single test bus capacitor on ATESTx to ground and on BTESTx to ground with a value of 32 pF for each channel less than 24. For any termination scheme, capacitance to ground on the test nodes should be kept less than 10 nF.

Systems that do not use the test access switch functionality must also add capacitance to the test switch node or short the test switches. If the test access switches are not to be used, ATEST1 and ATEST2 can be tied together with a 1 nF, 100 V capacitor on this node to ground. Likewise, tie BTEST1 and BTEST2 together with a 1 nF, 100 V capacitor on this node to ground. Alternatively, the test access switches can be shorted out. ATESTx can be shorted to ALINEx and BTESTx shorted to BLINEx. Note, with the test switches shorted, test switch state becomes irrelevant.

In addition, using a low voltage secondary protector on A lead and an asymmetrical protector on B lead (with respect to positive and negative voltage) is recommended. Refer to the Le79232 ISLIC data sheet for protection values.

## TYPICAL PERFORMANCE CHARACTERISTICS

**Figure 1. Protection Circuit**

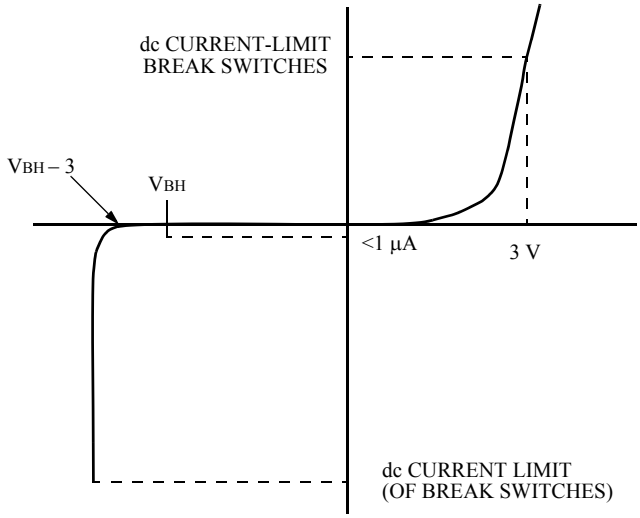



**Figure 2. Switches 1 – 3, Break Switches and Ringing Return Switch**

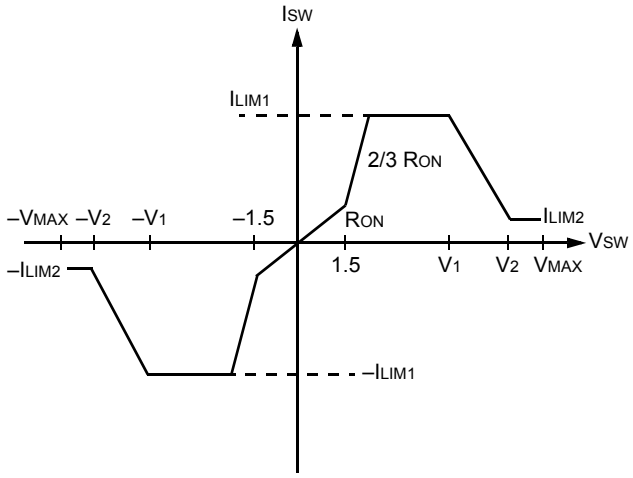



**Figure 3. Switch 4, Ringing Access Switch**

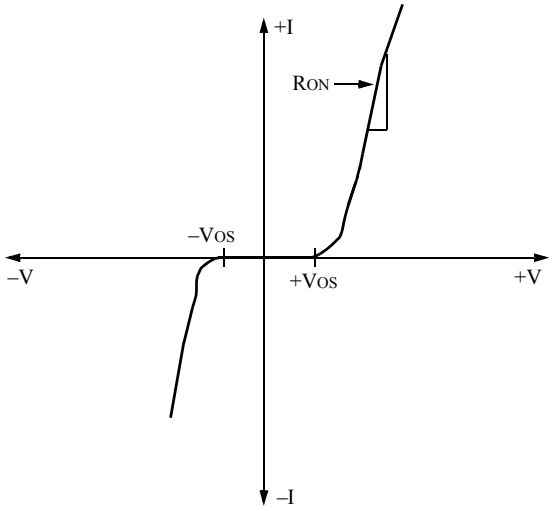
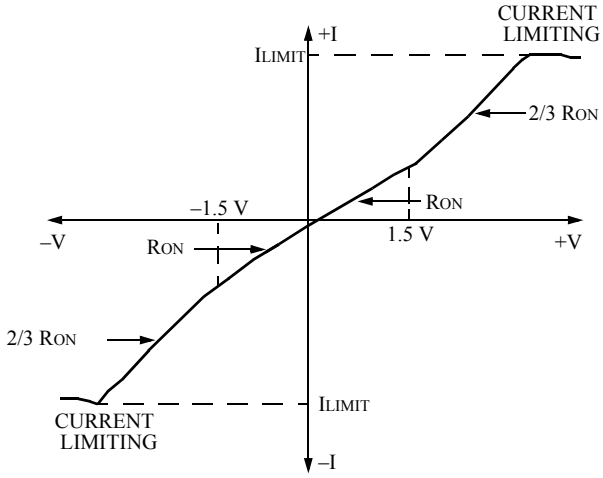


**Figure 4. Switches 5, 6, Test Access Switches**

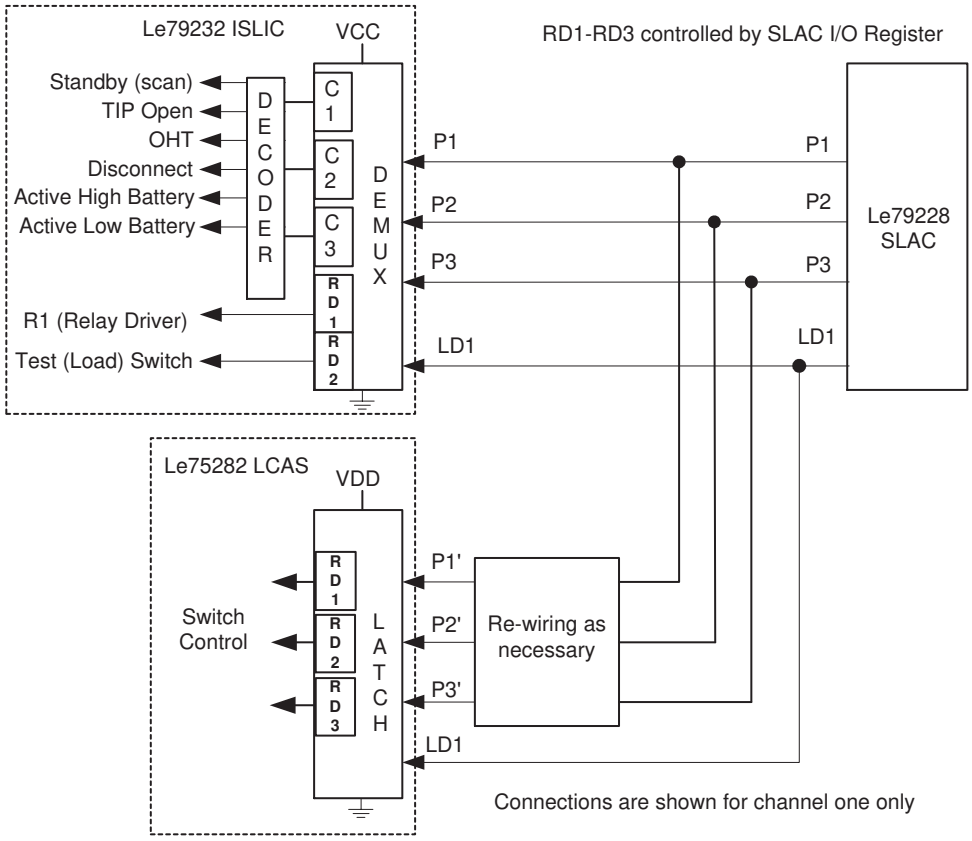


## APPLICATIONS

Figure 6, on page 16 illustrates the internal functionality of the Le75282 device.

There are numerous ways to control the Le75282 LCAS device using the P1'-P3'/LDx and $\overline{\text{OFFx}}$ inputs. A one-to-one wiring of SLAC P1 to LCAS P1', SLAC P2 to LCAS P2', and SLAC P3 to LCAS P3', is usually ***not*** the desired connection. When using the Le79Q224x/Le79228 SLAC as the controller, wiring of the control port varies dependent upon the desired operating states. P1, P2, and P3 control lines are used to control the ISLIC device and the LCAS device. When LDx is high, the P-bus controls the operating states of the ISLIC via C1, C2, and C3. When LDx is low, the P-bus controls the relay drivers and the test load in the ISLIC device as well as the operating states of the LCAS device via RD1, RD2, and RD3. So functionality between the ISLIC device and the LCAS device needs to be coordinated in order to provide the desired performance.

**Figure 5. ISLIC Device and LCAS Control**




Control and wiring scenarios for the ISLIC device and LCAS device follows.

The following LCAS operating state options are available through P-bus control:

1. Idle/Talk, Ringing, Test, Test/Monitor
2. Idle/Talk, Ringing, Test/Monitor, Test Ringing
3. Idle/Talk, Ringing, Test, All Off
4. Idle/Talk, Ringing, Test, Test/Monitor, Test Ringing
5. Idle/Talk, Ringing, Test, Test/Monitor, Test Ringing, All Off

Note, for all five states, the All Off operating state can be asserted by driving the $\overline{\text{OFFx}}$ pin Low.

For option 1, LCAS CFG = 0 and LCAS P3' = 0, wire SLAC P1 to LCAS P2', and wire SLAC P3 to LCAS P1', do not wire SLAC P2 to the LCAS. The test load (if enabled) can then be applied independent of the LCAS operating state. When SLAC P1 = 1, the Ringing and Test/Monitor state will be activated when the external ringing signal is at zero cross (assuming CCR4 RMODE is set for external ringing (1) and ZXR is set for enable zero cross ringing relay operation (0)). For the Ringing state this is the desired operation. For the Test/Monitor state, the delay in activation needs to be considered in the firmware.

For option 2, LCAS CFG = 0 or 1 and LCAS P3' = 1, wire SLAC P1 to LCAS P2', and wire SLAC P3 to LCAS P1', do not wire SLAC P2 to the LCAS. The test load (if enabled) can then be applied independent of the LCAS operating state. When SLAC P1 = 1, the Ringing and Test Ringing state will be activated when the external ringing signal is at zero cross (assuming CCR4 RMODE is set for external ringing (1) and ZXR is set for enable zero cross ringing relay operation (0)). This is desired operation.

For option 3, LCAS CFG = 1 and LCAS P3' = 0, wire SLAC P1 to LCAS P2', and wire SLAC P3 to LCAS P1', do not wire SLAC P2 to the LCAS device. The test load (if enabled) can then be applied independent of the LCAS operating state. When SLAC P1 = 1, the Ringing and All Off state will be activated when the external ringing signal is at zero cross (assuming CCR4 RMODE is set for external ringing (1) and ZXR is set for enable zero cross ringing relay operation (0)). For the Ringing state this is the desired operation. For the All Off state, the delay in activation needs to be considered in the firmware. An immediate All Off state can always be asserted by controlling $\overline{\text{OFFx}}$ or by writing the ZXR bit to disable zero cross ringing relay operation prior to writing the All Off state.

For option 4, LCAS CFG = 0, wire SLAC P1 to LCAS P2', wire SLAC P2 to LCAS P1', and wire SLAC P3 to LCAS P3'. The test load (if enabled) will be applied when the LCAS device is in the Test, Test/Monitor, and Test Ringing states. When SLAC P1 = 1, the Ringing, Test Ringing, and Test/Monitor state will be activated when the external ringing signal is at zero cross (assuming CCR4 RMODE is set for external ringing (1) and ZXR is set for enable zero cross ringing relay operation (0)). For the Ringing and Test Ringing state this is the desired operation. For the Test/Monitor state, the delay in activation needs to be considered in the firmware. An immediate Test/Monitor state can always be asserted by writing the ZXR bit to disable zero cross ringing relay operation prior to writing the Test/Monitor state.

For option 5, LCAS CFG = 1, wire SLAC P1 to LCAS P2', wire SLAC P2 to LCAS P1', and wire SLAC P3 to LCAS P3'. The test load (if enabled) will be applied when the LCAS device is in the Test, All Off, Test/Monitor, and Test Ringing states. When SLAC P1 = 1, the Ringing, Test Ringing, and All Off states will be activated when the external ringing signal is at zero cross (assuming CCR4 RMODE is set for external ringing (1) and ZXR is set for enable zero cross ringing relay operation (0)). For the Ringing and Test Ringing state this is the desired operation. For the All Off state, the delay in activation needs to be considered in the firmware. An immediate All Off state can always be asserted by controlling $\overline{\text{OFFx}}$ or by writing the ZXR bit to disable zero cross ringing relay operation prior to writing the All Off state.

A sixth option is to use the option 4 states but use the P1 relay driver in the ISLIC device to drive an electromechanical DPDT test-out relay. The relay would be wired between the protection and the ALINE/BLINE LCAS device pins. The relay, when actuated, would disconnect the LCAS device and apply an alternate test bus to the loop. For this option, LCAS CFG = 0, wire SLAC P1 to LCAS P3', wire SLAC P2 to LCAS P2', and wire SLAC P3 to LCAS P1'. The R1 relay driver drives the test-out electromechanical relay. When SLAC P1 = 0 the loop is connected, Idle/Talk, Test, Ringing, and Test/Monitor states are available. When SLAC P1 = 1 the loop is disconnected, and Idle/Talk, Test/Monitor, Ringing, and Test Ringing states are available. When SLAC P2 = 1, the Ringing, Test Ringing, and Test/Monitor states are activated when the external ringing signal is at zero crossing (assuming CCR4 RMODE is set for external ringing (1) and ZXR is set for enable zero cross ringing relay operation (0) and I/O Register RD2IO (Le792284 only) is set to automatically set and clear RD2 during external ringing). For the Ringing and Test Ringing state this is the desired operation. For the Test/Monitor state, the delay in activation needs to be considered in the firmware. An immediate Test/Monitor state can always be asserted by writing the ZXR bit to disable zero cross ringing relay operation prior to writing the Test/Monitor state. Since SLAC P1 is used to drive the electromechanical test-out relay, and SLAC P2 is used to activate the LCAS device ringing states at zero crossing, the per-channel test load is not used with this scenario.

### Reset

There are two possible ways to control reset of the Le75282 device.

If the $\overline{\text{OFFx}}$ pin is used, it can provide a power-up reset and an active device reset. When using a SLAC with the general purpose I/O pins, the I/O pins can be used to control $\overline{\text{OFFx}}$. At power-up the I/O pins default to high impedance inputs. The internal pull-down in the $\overline{\text{OFFx}}$ pin will clear the P1'-P3' inputs and set the Le75282 device into its All Off state at power-up. After the I/O pins are configured as outputs, they can be set high to allow programming of the Le75282 device. During operation, the RD1-RD3 control data can be cleared by bringing $\overline{\text{OFFx}}$ low.

If $\overline{\text{OFFx}}$ is not used, a power-up reset can be achieved by placing a 0.1 µf capacitor on each TSDx pin to ground. The Le75282 device will then power-up in the All Off state and remain in that state until an operating state is programmed.

**Figure 6. Le75282 Device Application, Idle/Talk State Shown**

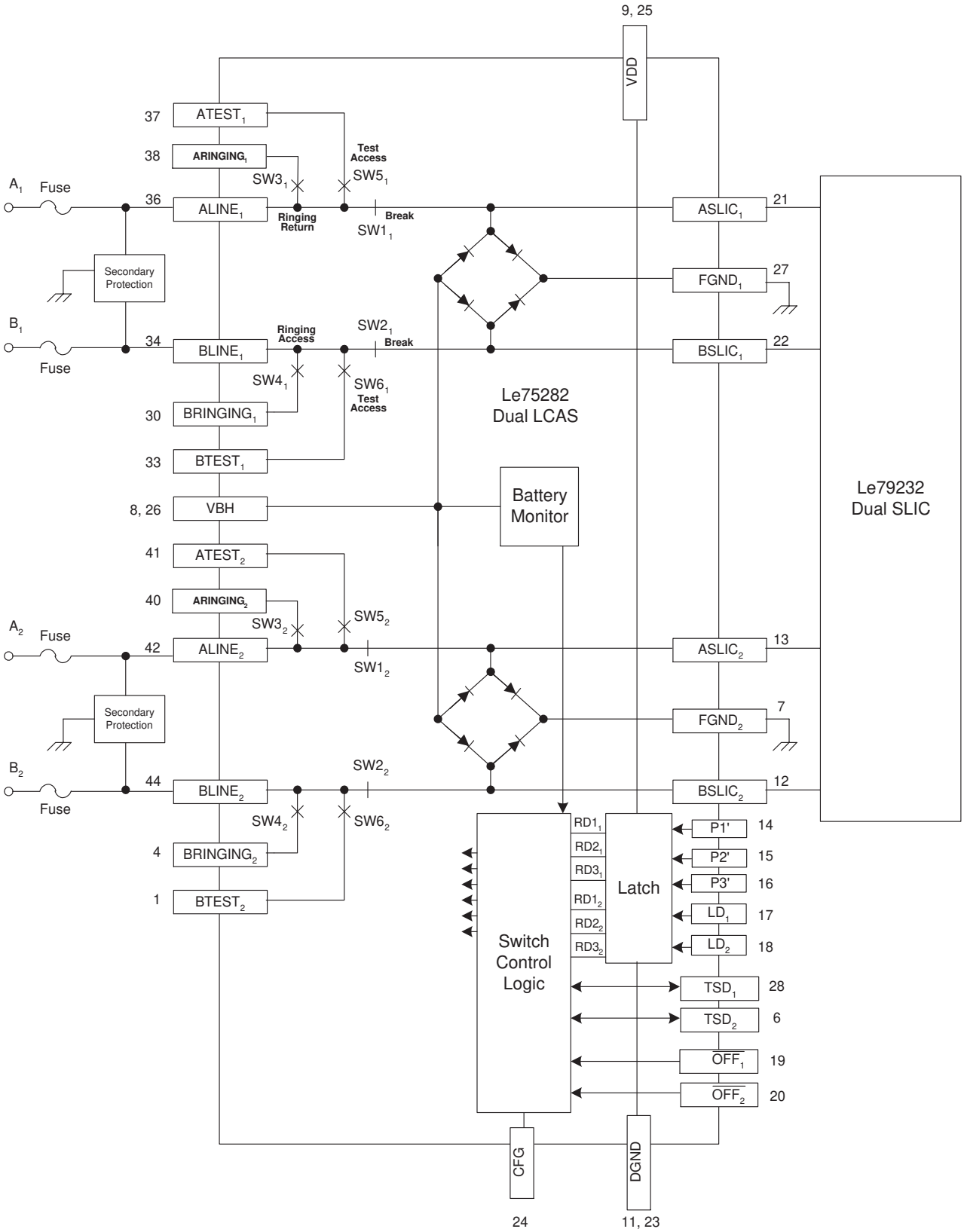


**Table 9. Operating States: CFG = 0**

| Operating State | Break Switches | Ringing Switches | Test Switches | RD3[1] | RD2[1] | RD1[1] | $\overline{OFFx}$[1] |
|---|---|---|---|---|---|---|---|
| Idle/Talk | **ON** | OFF | OFF | 0 | 0 | 0 | 1 |
| Test | OFF | OFF | **ON** | 0 | 0 | 1 | 1 |
| Ringing | OFF | **ON** | OFF | 0 | 1 | 0 | 1 |
| Test/Monitor | **ON** | OFF | **ON** | 0 | 1 | 1 | 1 |
| Idle/Talk | **ON** | OFF | OFF | 1 | 0 | 0 | 1 |
| Test/Monitor | **ON** | OFF | **ON** | 1 | 0 | 1 | 1 |
| Ringing | OFF | **ON** | OFF | 1 | 1 | 0 | 1 |
| Test Ringing | OFF | **ON** | **ON** | 1 | 1 | 1 | 1 |
| All Off | OFF | OFF | OFF | X | X | X | 0[2] |

***Notes:***

1. *RD1, RD2, and RD3 data input values are directed to a given channel when the respective LDx logic signal is set to 0. $\overline{OFFx}$ is a per-channel control.*
2. *A 0 on $\overline{OFFx}$ resets the Le75282 device, the device will remain in the All Off state until $\overline{OFFx}$ is returned to 1 and the next LDx signal is applied.*

**Table 10. Operating States: CFG = 1**

| Operating State | Break Switches | Ringing Switches | Test Switches | RD3[1] | RD2[1] | RD1[1] | $\overline{OFFx}$[1] |
|---|---|---|---|---|---|---|---|
| Idle/Talk | **ON** | OFF | OFF | 0 | 0 | 0 | 1 |
| Test | OFF | OFF | **ON** | 0 | 0 | 1 | 1 |
| Ringing | OFF | **ON** | OFF | 0 | 1 | 0 | 1 |
| All Off | OFF | OFF | OFF | 0 | 1 | 1 | 1 |
| Idle/Talk | **ON** | OFF | OFF | 1 | 0 | 0 | 1 |
| Test/Monitor | **ON** | OFF | **ON** | 1 | 0 | 1 | 1 |
| Ringing | OFF | **ON** | OFF | 1 | 1 | 0 | 1 |
| Test Ringing | OFF | **ON** | **ON** | 1 | 1 | 1 | 1 |
| All Off | OFF | OFF | OFF | X | X | X | 0[2] |

***Notes:***

1. *RD1, RD2, and RD3 data input values are directed to a given channel when the respective LDx logic signal is set to 0. $\overline{OFFx}$ and TSDx are per-channel controls.*
2. *A 0 on $\overline{OFFx}$ resets the Le75282 device, the device will remain in the All Off state until $\overline{OFFx}$ is returned to 1 and the next LDx signal is applied.*

A parallel-in/parallel-out data latch is integrated into the Le75282 device. Operation of the data latch is controlled by the LDx pins. The data inputs to the latch are the P1'-P3' logic level pins; the output of the data latch respectively is RD1-RD3 used for state control.

When the LDx control pin for a given channel is at logic 1 or VREF (of an Le79228 SLAC device), changes on the data inputs will be ignored.

When the LDx control pin for a given channel is at logic 0, the latch is transparent and changes on the data inputs is passed directly through as state control. Any changes in the data inputs will be reflected in the state of the switches. When the LDx control pin returns to logic 1 or VREF, the state of the switches becomes latched; that is, the state of the switches will remain until another logic 0 transition occurs.

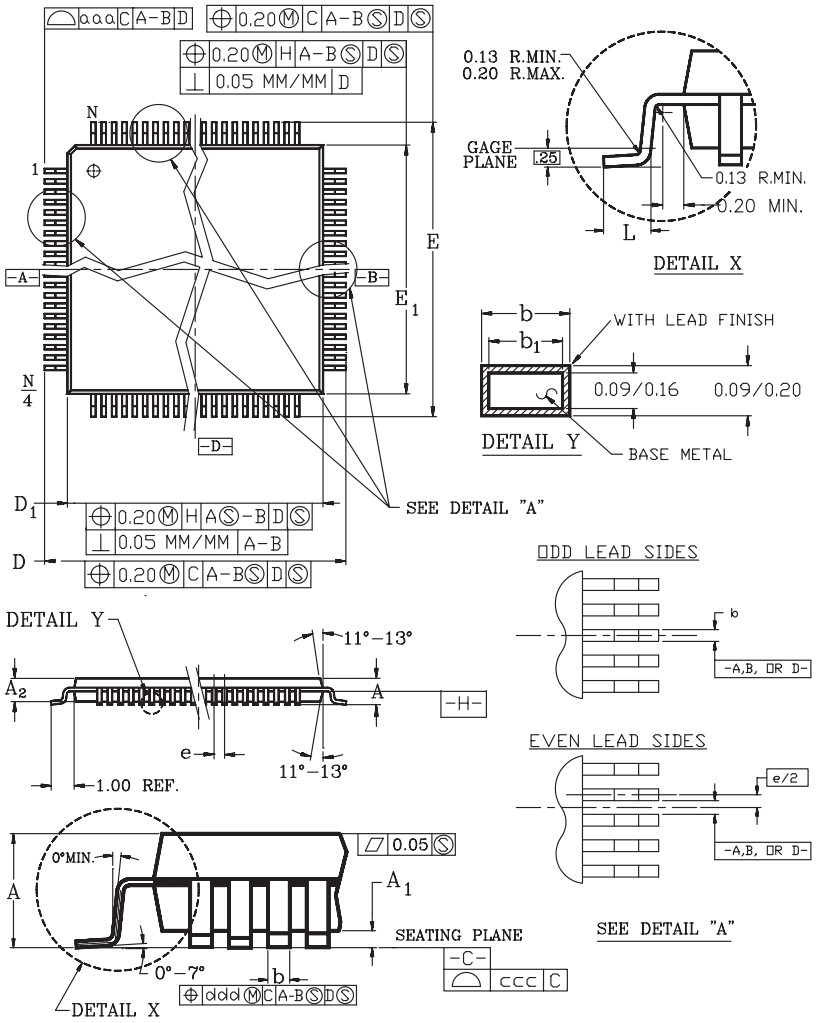
Note in Figure 6, on page 16 that the $\overline{OFFx}$ and TSDx are not tied to the data latch. $\overline{OFFx}$ and TSDx are not affected by the LD input. The $\overline{OFFx}$ and TSDx (in thermal shutdown state) will override the RD1-RD3 state control for that channel.

$\overline{OFFx}$ pins have internal pull-down resistors which set the Le75282 device into the All Off state at power-up.

CFG is intended to be fixed at VDD or DGND, if CFG switches states when VDD is applied, the change will be recognized by a given channel after an LD low transition is applied to that channel.

## PHYSICAL DIMENSIONS

### 44-Pin TQFP




| Symbol | Min | Nom | Max |
|---|---|---|---|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | 12 BSC | | |
| D1 | 10 BSC | | |
| E | 12 BSC | | |
| E1 | 10 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| N | 44 | | |
| e | 0.80 BSC | | |
| b | 0.30 | 0.37 | 0.45 |
| b1 | 0.30 | 0.35 | 0.40 |
| ccc | 0.10 | | |
| ddd | 0.20 | | |
| aaa | 0.20 | | |

JEDEC #: MS-026 (C) ACB

Notes:
1. All dimensions and toleerances conform to ANSI Y14.5-1982.
2. Datum plane -H- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.
3. Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.254mm per side. Dimensions "D1" and "E1" include mold mismatch and are determined at Datum plane -H- .
4. Dimension "B" does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar can not be located on the lower radius or the foot.
5. Controlling dimensions: Millimeter.
6. Dimensions "D" and "E" are measured from both innermost and outermost points.
7. Deviation from lead-tip true position shall be within ±0.076mm for pitch >0.5mm and within ±0.04 for pitch ≤0.5mm.
8. Lead coplanarity shall be within: (Refer to 06-500)
   1- 0.10mm for devices with lead pitch of 0.65-0.80mm.
   2- 0.076mm for devices with lead pitch of 0.50mm.
   Coplanarity is measured per specification 06-500.
9. Half span (center of package to lead tip) shall be 15.30 ± 0.165mm {.602"±.0065"}.
10. "N" is the total number of terminals.
11. The top of package is smaller than the bottom of the package by 0.15mm.
12. This outline conforms to Jedec publication 95 registration MS-026
13. The 160 lead is a compliant depopulation of the 176 lead MS-026 variation BGA.

**44-Pin TQFP**

***Note:***

*Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.*

# REVISION HISTORY

## Revision A1 to B1

- OFFx and TSDx designations changed.
- P1-P3 pins changed to P1'-P3'.
- Loss of Battery Detector Threshold specification added.
- Table 1, ON-state Voltage not tested in production note removed.
- Table 4, Test Access Switches, dc Current Limit Test Condition changed from 10 V to 20 V.
- Table 5, Additional Electrical Characteristics, Loss of Battery Detector Threshold, Loss of Battery limits changed from -16 V min and -8 V max to -19 V min and -5 V max, Resumption of Battery limits changed from -18 V min and -10 V max to -19 V min and -5 V max.
- Table 6 and 7 modified, P1 changed to RD2, P3 changed to RD1.
- Application section enhanced, figure 5 added.
- Table 9 and 10 modified, P3 changed to RD3, P2 changed to RD2, and P1 changed to RD1.

## Revision B1 to C1

- Added green package OPN to *Ordering Information*, on page 1
- In *Product Description*, on page 3, changed breakdown voltage rating from > 480 V to > 320 V.
- In Electrical Characteristics, changed all ON-resistance and current limit typical values to reflect actual values.
- Added *Package Assembly*, on page 5

## Revision C1 to D1

- Removed Le75282BVC package option in *Ordering Information*, on page 1.
- Added notes to table in *Ordering Information*, on page 1.
- Diode Bridge, Electrical Specifications table moved to page 8.
- Test Switch Protection Considerations section added to page 11.

## Revision D1 to E1

- Table 1, test condition wording for Dynamic Current Limit modified.
- Table 3, test conditions for Surge Current added.
- Test Switch Protection Considerations section modified.
- Minor text edits.

## Revision E1 to E2

- Enhanced format of package drawings in *Physical Dimensions*, on page 18
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

**For more information about all Zarlink products visit our Web Site at**

**www.zarlink.com**