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ZARLINK™ SEMICONDUCTOR

VoiceEdge

Le9502

Ringing Subscriber Line Interface Circuit
VE950 Series

APPLICATIONS

- **Short/Medium Loop: approximately 2000 ft. of 26 AWG, and 5 REN loads**
- **Voice over IP/DSL – Integrated Access Devices, Smart Residential Gateways, Home Gateway/Router**
- **Cable Telephony – NIU, Set-Top Box, Home Side Box, Cable Modem, Cable PC**
- **Fiber–Fiber In The Loop (FITL), Fiber to the Home (FTTH)**
- **Wireless Local Loop, Intelligent PBX, ISDN NT1/TA**

FEATURES

- **Integrated Dual-Channel Device**
  - Built-in boost switching power supply tracks line voltage minimizing power dissipation
  - Only +3.3 V and +12 V (nominal) required
  - Wide range of input voltages (+8 V to +40 V) supported
  - Minimal external discrete components
  - 44-pin eTQFP package
- **Ringing**
  - 70 Vpk into 5REN
  - 90 Vpk capable
  - Sinusoidal or trapezoidal capability
  - DC offset support
  - Common differential interface for both channels
- **World Wide programmability:**
  - Two-wire AC impedance
  - Dual Current Limit
  - Loop closure and ring trip thresholds
- **Five SLIC States, including:**
  - Low power Standby state
  - Reverse Polarity

RELATED LITERATURE

- **081189 Le9500 RSLIC Device Data Sheet**
- **081208 Le9501 RSLIC Device Data Sheet**
- **080696 Le77D11 VoSLIC™ Device Data Sheet**
- **080697 Le78D11 VoSLAC™ Device Sheet**
- **080716 Le77D11 /Le78D11 Chip Set User's Guide**
- **080780 Layout Considerations for the Le77D11 and Le9502 Devices Application Note**

ORDERING INFORMATION

Device	Package[1]	Packing[2]
Le9502BTC	44-pin eTQFP (Green Package)	Tray

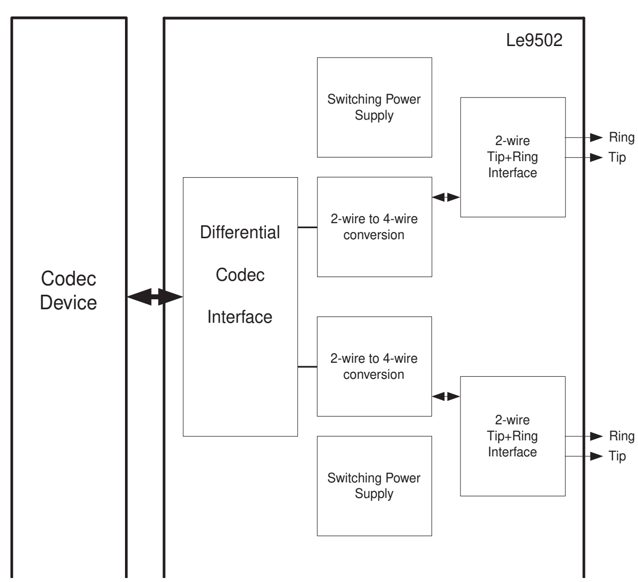
1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

The Zarlink Le9502 Ringing Subscriber Line Interface Circuit (RSLIC) device from the VE950 series has enhanced and optimized features to directly address the requirements of Voice over Broadband applications. Its goal is to reduce system level costs, space, and power through higher levels of integration, and to reduce the total cost of ownership by offering better quality of service. The Le9502 RSLIC device provides a totally configurable solution to the BORSCHT functions for two lines. The resulting system is less complex, smaller, and denser, yet cost effective with minimal external components.

The Le9502 RSLIC device requires only two power supplies: +3.3 VDC and nominally +12 VDC. The latter power supply can range from +8 VDC to +40 VDC, depending on the application. A single TTL-level clock source drives an external transistor which controls the ramp voltage that in turn feeds the switching regulators. Five programmable states are available: Active, Reverse Polarity, Ringing, Standby, and Disconnect. The DC feed, two-wire AC input impedance, hook-switch threshold, and ring trip threshold are programmable via external discrete components. Binary fault detection is provided upon application of fault conditions or thermal overload.

BLOCK DIAGRAM



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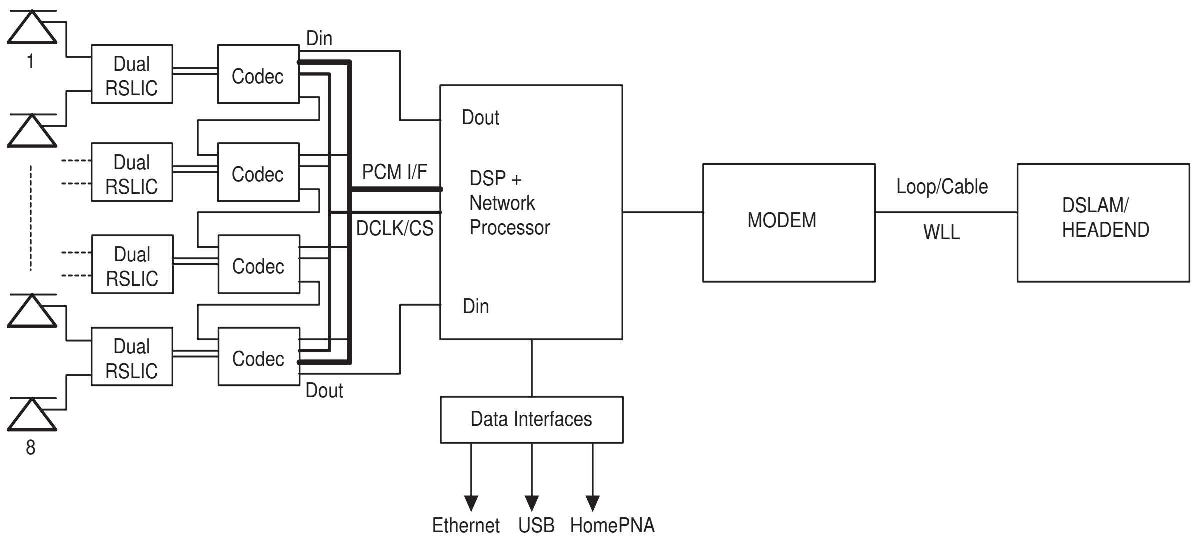
PRODUCT DESCRIPTION

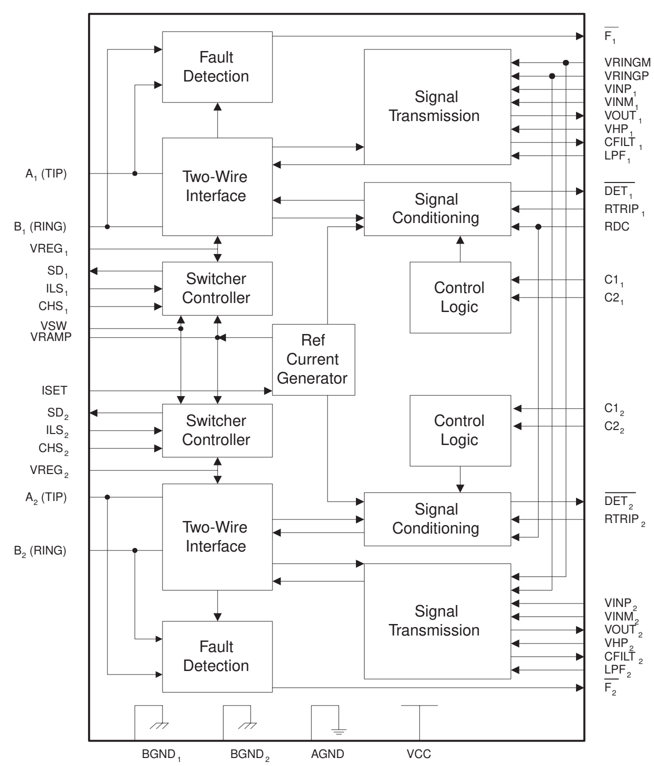
The VE950 series Le9502 RSLIC device uses reliable, dielectrically isolated, fully complementary bipolar technology to implement BORSCHT functions for short loop applications. Internal power dissipation is minimized by two independent line voltage tracking, buck-boost switching regulators. Two power supplies are required: 3.3 V and a positive supply (V_{SW}). A TTL-level clock is required to drive the switching regulator. Five programmable states control loop signaling, transmission, and ringing. The Le9502 RSLIC device DC current feed limit (I_{SC}) is resistor-programmable up to 45 mA.

Figure 1. Typical Le9502 RSLIC/Codec Application in an 8-Port Integrated Access Device in Customer Premises



BLOCK DESCRIPTIONS

Figure 2. Le9502 RSLIC Device Block Diagram



Two-Wire Interface

The two-wire interface block provides DC current and sends/receives voice signals to a telephone connected via the A_i(Tip) and B_i(Ring) pins. The A_i(Tip) and B_i(Ring) pins are also used to send the ringing signal to the telephone. The Le9502 RSLIC device can also be programmed in Disconnect state to place the A_i and B_i pins at high impedance with the Switching Regulator disabled.

DC Feed

DC feed is controlled in the Le9502 RSLIC device. Only the current limit threshold (I_{LTH}) can be set via the RDC pin. The current limit threshold can be set from 0 to 30 mA.

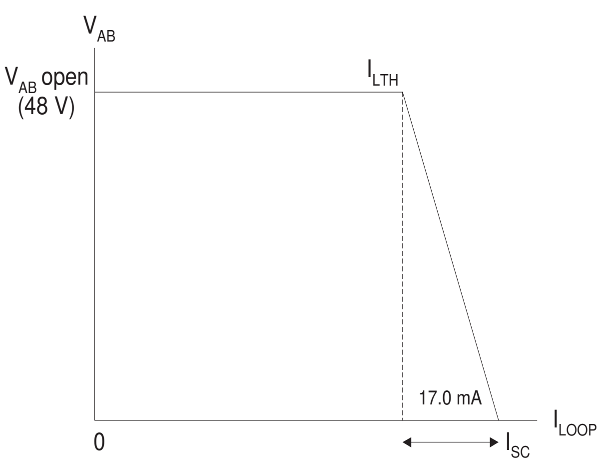
Referring to Figure 3, the DC feed curve consists of two distinct regions. The first region is a flat anti-sat region that supplies a constant Tip-Ring voltage (V_{AB} open). The second region is a constant current region that begins when the loop current reaches the programmed current limit threshold (I_{LTH}). This region looks like a constant current source with 3.2 kΩ shunt resistor. The short circuit current is nominally 17.0 mA greater than I_{LTH}.

A block diagram of the DC feed control circuit is shown in Figure 4. In the anti-sat region, current source CS1 creates a constant reference current, which is limited to sub-voice frequencies by C_{LPFi}. This filtered current is then steered by the Polarity Control, depending on whether the SLIC mode is Standby, Normal Active, or Reverse Polarity. The steered current then takes one of two paths to the Level Shift block, where it is used to set V_A (TIP) and V_B (RING). This voltage from the Level Shift block is buffered by the output amplifiers and appears at A_i (TIP) and B_i (RING).

When $I_{LOOP}/500$ becomes greater than $I_{LTH}/500$, the difference is subtracted from CS1, and again filtered by C_{LPFi}. This reduced current causes a reduced DC feed voltage. In Standby and Normal Active, A_i (TIP) is held constant, while B_i (RING) is changed to reduce the feed voltage. In Reverse Polarity, A_i (TIP) and B_i (RING) are swapped. When $(I_{LOOP}-I_{LTH})/500$ = CS1, all of the current from CS1 is subtracted, making the TIP-RING voltage = 0 V. This is the short circuit condition. At least 100 Ω loop and fuse resistance are required to ensure stability of the A_i (TIP) and B_i (RING) output amplifiers.

The capacitor C_{LPFi}, in conjunction with an internal 25 kΩ resistor (not shown), is used to create a low pass filter for the DC feed loop. This capacitor should nominally be 4.7 µF, setting a 1.4 Hz pole. The purpose of this capacitor is to stabilize the DC feed and filter any AC components.

Figure 3. DC Feed Curve



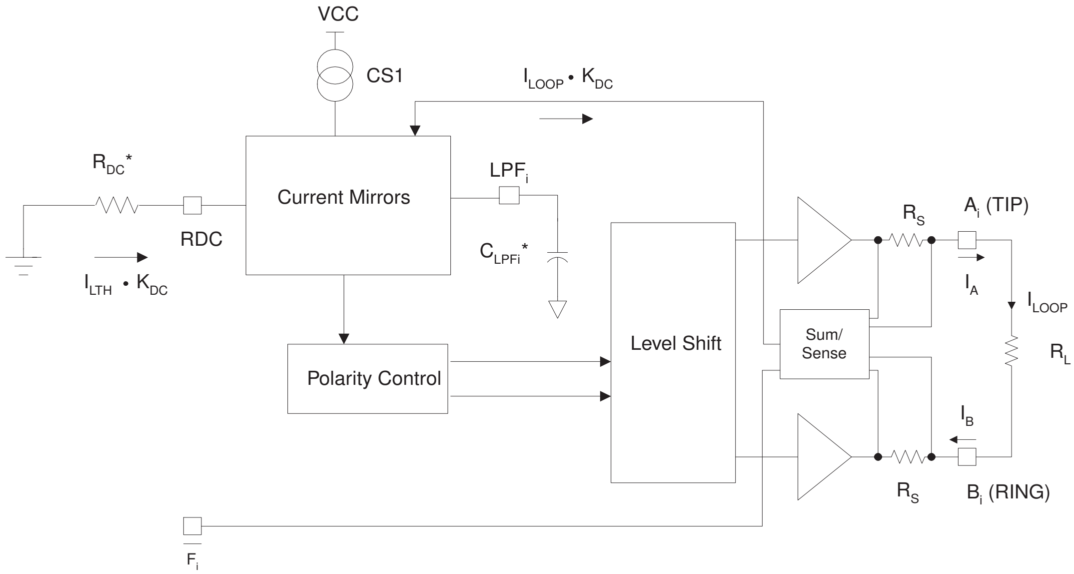
$$I_{SC} = I_{LTH} + 17.0\text{mA}$$

$$I_{LTH} = \frac{1.4\text{ V}}{R_{DC} K_{DC}}$$

Note:

1. *R_{DC} = external resistor from RDC to AGND*
2. *$V_{AB} = V_{Ai} – V_{Bi}$ Tip-Ring differential voltage*
3. *K_{DC} = Le9502 RSLIC device DC current gain, which is:* $K_{DC} = \frac{1}{500}$
4. *I_{SC} = Loop short circuit current limit.*
5. *I_{LTH} = Loop current limit threshold.*

Figure 4. DC Feed Block Diagram, Active and Standby Modes



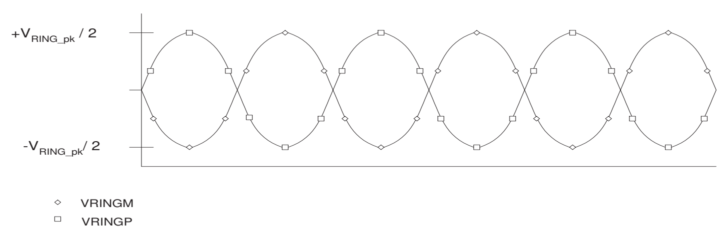
Note:

** denotes external components.*

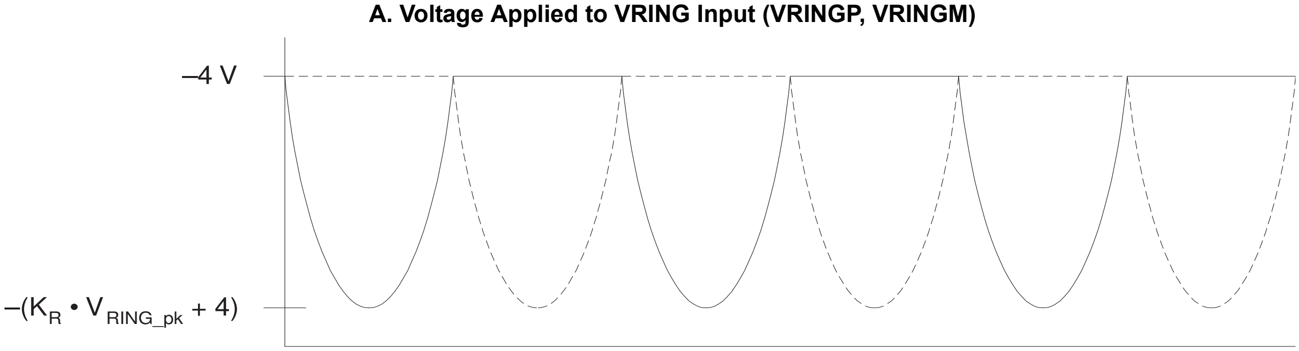
Ringing

The Le9502 RSLIC device only provides a method for creating internal ringing. Internal ringing is accomplished by applying a single or differential ringing waveform using the VRINGP and VRINGM pins, and placing the Le9502 RSLIC device into the ringing state via the device's control bits. When the Le9502 RSLIC device is in the Ringing state, the gain from the Le9502 RSLIC device's differential ringing input pin to the output, is K_R (the ringing voltage gain). The output waveform is a quasi-balanced waveform as shown below in Figure 5). On the positive half cycle of the input waveform, the A_i (TIP) lead of the Le9502 RSLIC device is near -4 V, and the B_i (RING) lead is brought negative. Likewise, on the negative half cycle of the input waveform, the B_i (RING) lead of the Le9502 RSLIC device is held near -4 V, while the A_i (TIP) lead is brought more negative. The low cost regulator solution, shown in the application circuit on page 20, incorporates the use of a higher power PNP bipolar switching transistor in the switching circuit that enables the Le9502 to provide a 90 Vpk ringing signal into a lower REN load. The waveform can be either sinusoidal or trapezoidal under the control of the codec device.

Figure 5. Ringing Waveforms



A. Voltage Applied to VRING Input (VRINGP, VRINGM)



B. Voltage Output at A (TIP) (dashed line) and B (RING) (solid line) Pins

For the reference schematic, Zetex part FZT955 in a SOT-223 package is used. Its V_{CEO} rating is 140 V. The switching efficiency and overhead voltage of the regulator allows a robust 70 Vpk ringing signal into a 5 REN load with V_{SW} = 12 V.

Switcher Controller

The switcher controller's main function is to provide a negative power supply (V_{REG}) that tracks Tip and Ring voltage for the 2-wire interface. As the Tip and Ring voltage decreases, the switcher will likewise lower V_{REG}. In doing so, the switcher saves power because the device is not forced to maintain static supply voltage in all states.

The switching power supply controller uses a discontinuous mode, buck-boost voltage converter topology. The frequency of operation is set by the ISET resistor and the VRAMP capacitor values. An external clock with approximately a 10% duty cycle drives the gate (base) of a small-signal FET which is used to reset the VRAMP capacitor voltage, creating the ramp voltage used internally by the switching power supply control circuitry. This clock signal controls the switching supply's operating frequency. The switcher circuit is nominally designed for 85 kHz operation based on the *Application Circuit* on page 20.

The duty cycle of the switching transistors is continuously variable up to 90% depending on the magnitude of the error voltage on the compensation (CHS) pin. The error signal on CHS is compared to the ramp signal. The ramp rate of the VRAMP signal is set by the ISET resistor (R_{SET}) and the VRAMP capacitor (C_{RAMP}). A 1% R_{SET} resistor should be chosen first (see *Signal Conditioning* on page 9) before using the following equation to calculate C_{RAMP}

$$C_{RAMP\_max} = I_{RAMP\_min} \bullet [(100\% - t_{CHCLK\_max}) / (f_{CHCLK} \bullet R_{SET\_max})]$$

where I_{RAMP_min} is the current going through C_{RAMP}, t_{CHCLK_max} is maximum duration of Chopper Clock High Duty Cycle provided in the specification section, f_{CHCLK} is the frequency of the chopper clock, and R_{SET_max} is R_{SET_nom} * 1.01. The calculated value for C_{RAMP} is the maximum value that can guarantee the switcher to operate. A NPO dielectric capacitor is recommended for C_{RAMP}.

When the external clock signal goes from a logic Low to a logic High, it will pull VRAMP voltage low which causes internal clock (from the square wave converter) to go Low, turning on the external power switch. When the external clock signal goes from High to Low, C_{RAMP} will charge up. When the VRAMP voltage exceeds internal voltage threshold, the rising edge of the internal clock from the square wave converter will reset the current limit latch getting it ready for the next cycle and turn off the external power switch. Also on a cycle-by-cycle basis, one of the following three events will shut off the power switch, depending on which event occurs first:

a) The VRAMP voltage exceeds the error voltage that is integrated on the CHS node (normal voltage feedback operation.)
b) The VRAMP voltage exceeds the internal voltage threshold.
c) The power switch current limit threshold is reached (set by R_{LIM}).

Cycle-by-cycle current limiting is provided by the current sense ILS_i pin which senses the external power switch current through the resistor R_{LIM}. If this pin exceeds VT_{ILS}, nominally –0.28 V with respect to V_{SW}, the switching supply will set the current limit latch and shut off the external switch drive until the next time the VRAMP pin is pulled Low to reset the latch. Thus the peak inductor current, and also peak switching converter power output can be controlled on a cycle-by-cycle basis and set by the equation $I_{LIM} = (VT_{ILS})/R_{LIM}$.

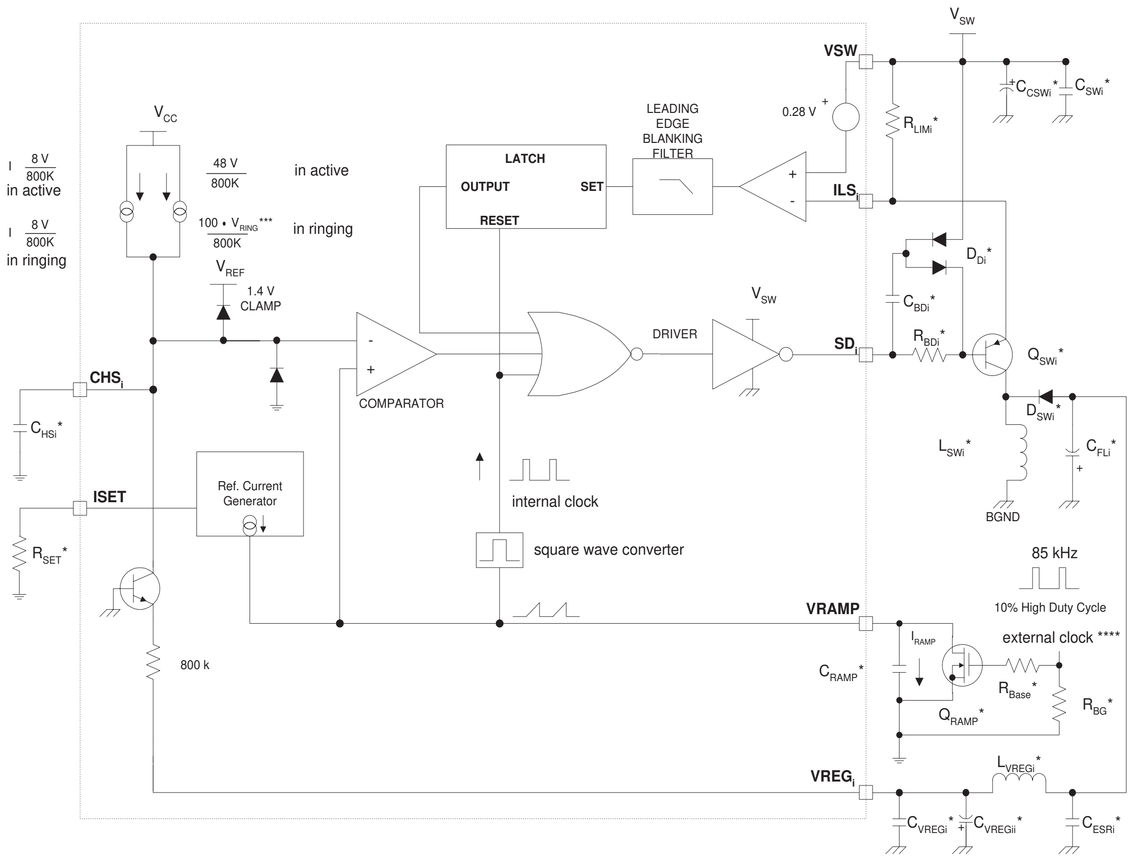
This sensing configuration has the added benefit that if the clock signal is removed for some reason, the power switch cannot be left on indefinitely. Leaving the ILS_i pin unconnected or shorting this pin to VSW will disable current limiting, but is not recommended.

A leading edge blanking filter is added at the output of the latch to ignore the first 150 ns of a current limit event. This feature is used to ignore a false current trip that may be caused by the power switch driving the reverse recovery charge (Q_{RR}) of the external power rectifier.

The on chip driver is designed to drive either an external PNP or a PMOS power device. Its output drive is clamped between 7-9 V below V_{SW}, and can source or sink approximately 100 mA. The driver has approximately 50 Ω of source resistance. The additional resistance should be added from the SD_i pin to the base of the external power device if a PNP is used to limit base drive for optimal efficiency.

When using a PMOS power switch, the SD_i pin will be able to drive approximately 100 mA of drive current to the gate of the PMOS device, and an internal clamp will limit the drive between 7-9 V. To keep system losses to a minimum, it is recommended that low gate charge be given higher consideration over low $r_{DS(on)}$ when selecting a power PMOS device for your application.

Figure 6. Switching Power Supply Block Diagram



Note:

** Denotes external components.*

*** Generated internally by band gap ≅ 1.4 V.*

**** $V_{RING} = V_{RINGP} - V_{RINGM}$*

***** Preferably, the external clock should be Low in startup. For a system (codec) which has a high impedance at the clock output in start up, the additional R_{Base} and R_{BG} resistors are recommended with values of 10 kΩ and 100 kΩ respectively.*

Signal Transmission

In Normal Active and Reverse Polarity states, the AC line current is sensed across the R_S resistors (see Figure 7), summed and attenuated, and converted to voltage at the $CFILT_i$ pin. The voltage then goes through a high pass filter implemented using the external C_{HPi} capacitor, is amplified, and sent to the codec device at the $VOUT_i$ pin. This output is proportional to the AC metallic component of the line voltage. Additionally, the signal transmission block receives the analog signal from the codec device. The analog signal is amplified and sent to the line. Finally, a proportion of the signal at V_{OUT} is fed back to the line.

There are three parameters which define the AC characteristics of the Le9502 RSLIC device. First is the input impedance presented to the line or 2-wire (V_{AB}) side (Z_{2WIN}), second is the gain from the 4-wire (V_{IN}) to the 2-wire (V_{AB}) side (G_{42}), and third is the gain from the 2-wire (V_{AB}) side to the 4-wire (V_{OUT}) side (G_{24}).

Input Impedance (Z_{2WIN})

Z_{2WIN} is the impedance presented to the line at the 2-wire side and is defined by:

$$Z_{2WIN} = 2R_F + K_V K_{OUT} R_{IMT}$$

where $2 \cdot R_F$ is the total resistance of the external fuse resistors in the circuit, R_{IMT} is the impedance setting resistor for return loss purpose, K_{OUT} is the gain from V_{OUT} to V_{AB}, and K_V is the voice current gain defined in the Transmission Specifications Table. Note that the equation reveals that Z_{2WIN} is a function of the selectable resistors, R_{IMT} and R_F. For example, if $R_F = 0\ \Omega$ and R_{IMT} is 100 k, the terminating impedance is 600 Ω. This is the configuration used in this data sheet for defining the device specifications. However, in a real application, $R_F = 50\ \Omega$ is recommended, and RIMT is set to 80.6 KΩ to provide an approximate 600 Ω input impedance.

2-Wire to 4-Wire Gain (G_{24})

The 2-wire to 4-wire gain is the gain from the phone line to the VOUT output of the Le9502 RSLIC device. To solve for G_{24}, set $V_{IN} = V_{INP} - V_{INM} = 0$ V (see Figure 7).

$$\frac{V_{OUT}}{V_{AB}} = G_{24} = \frac{1}{\frac{2R_F}{K_V R_{IMT}} + K_{OUT}}$$

or

$$G_{24} = -20\log\left(K_{OUT} + \frac{2R_F}{K_V R_{IMT}}\right) \text{ in dB}$$

4-Wire to 2-Wire Gain (G_{42})

G_{42} is the gain from the VIN input to the line. This gain is defined as V_{AB}/V_{IN}. For the analysis of G_{42}, substitute the load resistor R_L in place of the test voltage source V_T (see Figure 7).

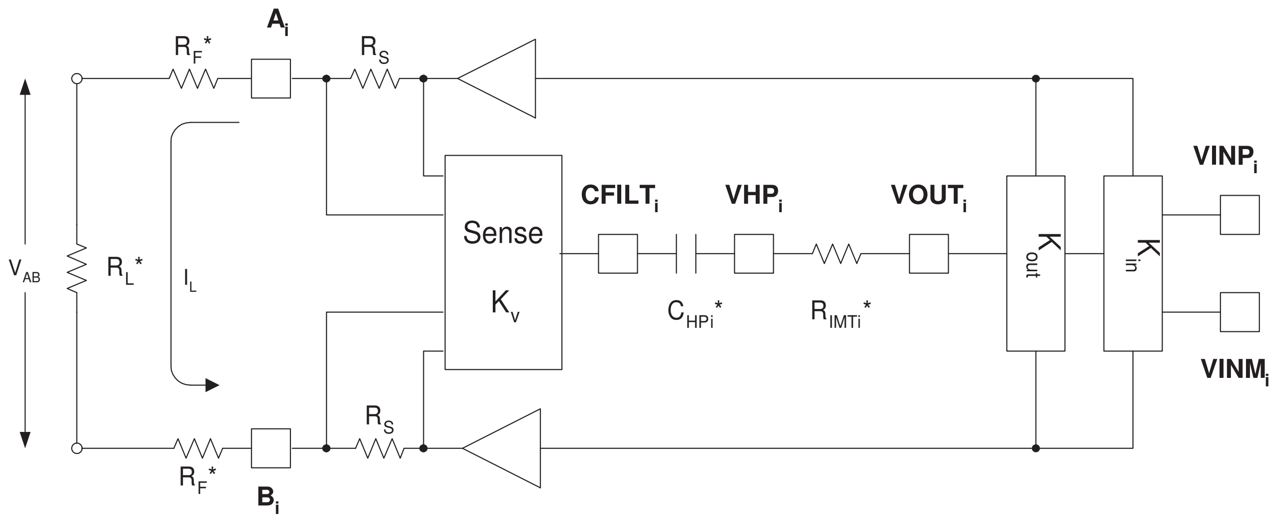
$$\frac{V_{AB}}{V_{IN}} = G_{42} = \frac{K_{IN}\left(\frac{R_L}{R_L + 2R_F}\right)}{\left(1 + \frac{K_{OUT} R_{IMT} K_V}{R_L + 2R_F}\right)}$$

or

$$G_{42} = -20\log\left(\frac{K_{IN}\left(\frac{R_L}{R_L + 2R_F}\right)}{\left(1 + \frac{K_{OUT} R_{IMT} K_V}{R_L + 2R_F}\right)}\right) \text{ in dB}$$

where K_{IN} is the gain from VIN to V_{AB}.

Figure 7. Transmission Block Diagram



Note:
** denotes external components.*

Fault Detection

Each channel of the Le9502 RSLIC device has a fault detection pin, $\overline{F}_1$ or $\overline{F}_2$. These pins are driven low when a longitudinal current fault or foreign voltage fault occurs. When not in Disconnect state, there are three conditions that will cause the $\overline{F}_i$ pin to indicate a fault condition:

- $|I_A - I_B| > I_{LONG}$
- In Normal Active and Standby state, a foreign voltage fault occurs in which V_A is above ground or V_B is close to V_{REG}.
- In Reverse Polarity state, a foreign voltage fault occurs in which V_B is above ground or V_A is close to V_{REG}.

In the Disconnect state, fault detection is not supported.

Signal Conditioning

The $\overline{DET}_i$ outputs are used for both off-hook and ring trip detection. The threshold for each of these functions is set by external components.

If the Le9502 RSLIC device is in Low Power Standby or Normal Active modes, the $\overline{DET}_i$ output is used to indicate an off-hook condition. The following equation will set the off-hook threshold:

$$R_{SET} = \frac{500 \bullet V_{REF}}{I_{offhook\_threshold}}$$

where $I_{offhook\_threshold}$ is a user-chosen off-hook current threshold. R_{SET} is 68.1 kΩ as specified in the *Application Circuit* on page 20. This value produces a nominal off-hook threshold of 10.3 mA.

If the SLIC device is in the Ringing state, the $\overline{DET}_i$ output will indicate the ring trip condition. The threshold for ring trip detection is set with an external resistor, R_{TRIP}, from the $RTRIP_i$ to $VREG_i$ pins. The ring trip threshold is set on a per-channel basis. To select the value of R_{TRIP}, the following equation is used:

$$R_{TRIP} = \frac{500 \bullet (V_{RING\ PK} + 10\ V)}{I_{trip\_threshold}}$$

where $V_{RING\ PK} + 10\ V \text{(overhead voltage)} \approx V_{REG}$,

For Zarlink's application, the ring trip current threshold is 74.6 mA which results in a R_{TRIP} value of 536 kΩ. C_{TRIP} is used as a transient filter to debounce the output ring trip signal at the $\overline{DET}_i$ pin. The value for C_{TRIP} is nominally 47 nF as in the *Application Circuit* on page 20.

The RDC_i pin is used to set the DC feed current limit, as described in *DC Feed* on page 4.

Thermal Overload

When the die temperature around the power amplifier of a Le9502 RSLIC device channel reaches approximately 160° C, the $\overline{F}_i$ pins are pulled Low and V_{REG} will collapse. At the same time, all the blocks controlling that channel of the device are shut off, except for the logic interface block. The SLIC channel goes into a state similar to Disconnect, making the line current zero. When the temperature drops below 145° C, the SLIC channel returns to its previous state. It is important to recognize that even while a channel experiences thermal overload, the state of the device can be modified.

Reference Current Generator

To set the hook switch threshold for both channels, an external resistor (R_{SET}) from ISET to AGND pins is used. For R_{SET} value, please refer to *Line Card Parts List* on page 21.

Moreover, internally this block generates I_{RAMP} which is used to help set the frequency of operation desired for the switcher.

Control Logic

Each channel of the Le9502 RSLIC device has three input pins from a codec device (CHS, C2, and C1). The inputs set the operational state of each channel. There are five operational SLIC device states (See Table 1): Low Power Standby, Disconnect, Normal Active, Reverse Polarity, and Ringing

.

Table 1. SLIC Device Operating States

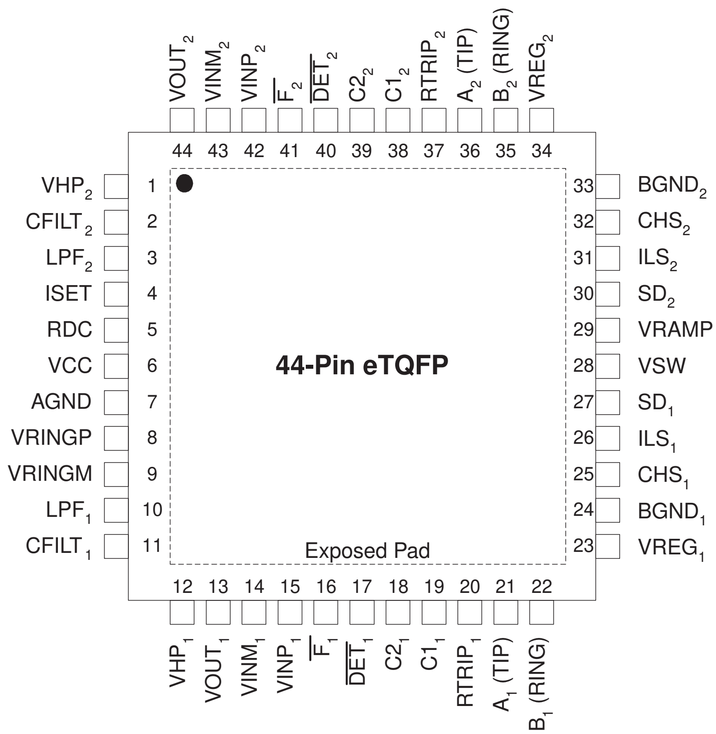
CHS	C2	C1	Operating State	Description
Float	0	0	Low Power Standby	Voice Transmission Disabled. Loop current capability is reduced.
Float	0	1	Reverse Polarity	Similar to normal active, but DC polarity is reversed so that the Ring lead is more positive than the Tip. Supports on hook transmission.
Float	1	0	Normal Active	SLIC device fully operational. Supports on hook transmission.
Float	1	1	Ringing	Ringing state with V_{AB} set to $K_R \bullet (V_{RINGP} – V_{RINGM})$. The switching supply maintains minimum headroom for the sourcing and sinking amplifiers in order to maximize power efficiency.
Pull Low *	0	0	Disconnect**	SLIC device is shut down. Mainly used if a line fault is detected or to shut down a line.

Note:

** See CHS Specifications on page 17.*

*** Standby state with switcher turned off.*

CONNECTION DIAGRAM



Note:

1. *Pin 1 is marked for orientation.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND	Ground	Analog and digital ground return for VCC circuitry (common to both channels).
$A_{1,2}$ (TIP)	Output	A (TIP lead) power amplifier output for channels 1 and 2.
$BGND_{1,2}$	Ground	Battery ground return for power amplifiers on channel 1 and 2.
$B_{1,2}$ (RING)	Output	B (RING lead) power amplifier output for channels 1 and 2.
$C1_1$, $C2_1$	Input	Logic control inputs to control channel 1 state.
$C1_2$, $C2_2$	Input	Logic control inputs to control channel 2 state.
$CFILT_{1,2}$	Output	AC coupling pin for 4-wire amplifier
$CHS_{1,2}$	Input	Compensation node for switching power supply channels 1 and 2.
$\overline{DET}_{1,2}$	Output	Loop detector or ring trip detector output, depending on state of control bits. If the SLIC device is in Ringing state then ring trip indication is given, if the SLIC device is in Low Power Standby, Normal Active or Reverse Polarity then hook switch indication is given.
$\overline{F}_{1,2}$	Output	Fault detect pin for channels 1 and 2. A low indicates a fault for the respective channel, which can be triggered by large longitudinal current, ground key, or thermal overload.
$ILS_{1,2}$	Input	Voltage sense pin to limit peak current in external switching power supply transistor (channels 1 and 2).
ISET	Input	Dual purpose pin: 1. sets the hook switch detection threshold (for both channels); 2. sets the current source for triangle wave generation for the switching power supply.
$LPF_{1,2}$	Output	A capacitor tied to from this pin to AGND stabilizes the DC feed loop, and lowers Idle Channel Noise.
RDC	Input	Resistor connection to GND. Sets DC feed current limit, I_{LTH} (common to both channels).
$RTRIP_{1,2}$	Input	Network tied from RTRIP to VREG. Sets the ring trip threshold detection level.
$SD_{1,2}$	Output	Base (gate) drive for switching power supply transistor (channels 1 and 2).
VCC	Supply	Positive supply for internal VCC circuitry (common to both channels).
$VHP_{1,2}$	Output	High pass invert summing node of the VOUT amplifier driven by the AC current coming from $CFILT_1$ and $CFILT_2$.
$VOUT_{1,2}$	Output	Analog (4-wire side) VOUT amplifier transmit output
$VINM_{1,2}$ $VINP_{1,2}$	Input	Differential (P-M) analog (4-wire side) voice signal input.
VRAMP	Input	Switching power supply ramp voltage that sets the frequency of the switcher and the maximum duty cycle (common to both channels).
$VREG_{1,2}$	Supply	Negative power supply generated by SLIC device Switching Regulator. (channels 1 and 2)
VRINGP, VRINGM	Input	Differential ringing input (common to both channels).
VSW	Supply	Positive supply used by the SLIC device to generate the negative regulated supplies of $VREG_1$, $VREG_2$ (common to both channels).
Exposed Pad	Isolated	Exposed pad on underside of device must be connected to a heat spreading area. The AGND plane is recommended.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage temperature	–55 to +150°C
Ambient temperature, under bias	–40° to +85°C
V_{CC} with respect to AGND	–0.4 to +6.5 V
V_{REG} with respect to BGND	+0.4 to –115 V
BGND with respect to AGND	–100 to 100 mV
A (TIP) or B (RING) to BGND:	
Continuous	V_{REG} –1 to BGND +1
10 ms (F = 0.1 Hz)	V_{REG} –5 to BGND +5
1 µs (F = 0.1 Hz)	V_{REG} –10 to BGND +10
250 ns (F = 0.1 Hz)	V_{REG} –15 to BGND +15
Current from A (TIP) or B (RING)	±150 mA
C1 and C2 with respect to AGND	–0.4 to VCC + 0.4 V
CHCLK	AGND to VCC
V_{SW}	BGND to +44 V
Maximum power dissipation, T_A = 85° C (See notes)	1.8 W
Thermal Data: In 44-pin eTQFP package	θ_{JA} 32° C/W
Thermal Data: In 44-pin eTQFP package	θ_{JC} 9.2° C/W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Note:

Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 160ºC. Continuous operation above 145ºC junction temperature may degrade device reliability.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through 16 0.3 mm diameter vias on a 1.27 mm pitch to a large (> 500 mm^2) internal copper plane. (Refer to Zarlink application note Layout Considerations for the Le77D112 and Le9502 RSLIC devices, document ID# 081013).

Package Assembly

Green package devices are assembled with enhanced environmental, compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Zarlink guarantees the performance of this device over commercial (0° to 70°C) and industrial (–40° to 85°C) temperature ranges by conducting electrical characterization over each range, and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40° to +85° C

Electrical Ranges

V_{CC}	3.3 V ± 5%
V_{SW}	8 to 40 V
V_{REG}	–7 to –110 (0 V in Disconnect state).

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, test conditions are: V_{CC} = 3.3 V, V_{SW} = 12.0 V, AGND = BGND, no fuse resistors, R_L = 600 Ω, 85 kHz CHCLK, I_{LTH}=20 mA (R_{DC} = 34.8 kΩ). Ringing configuration is V_{RING} = V_{RINGP} - V_{RINGM} = 0.7 Vpk. 20 Hz sinusoidal. Please refer to *Test Circuit* on page 19 for all other component values.

Supply Currents and Power Dissipation

Operation States	Condition	3.3 V VCC Supply Current (mA)			VREG Supply Current (mA) (Note 4)			VREG Supply Power (mW)			SLIC Device Power (mW) (Note 5)			VSW Pin Current (mA)	Note
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Typ	
Standby	R_L = open V_{IN} =0 V	3.0	5.5	8.0	0.25	1.0	3.5	15.0	50.0	130.0	20.0	75.0	130.0	2.0	1
Disconnect	R_L = open V_{IN} = 0 V	2.0	5.0	7.5	—	0.1	—	0.0	0.5	3.0	5.0	15.0	25.0	0.1	1
Active	R_L = open V_{IN} = 0 V	4.0	7.0	10.0	1.0	3.0	5.0	50.0	200.0	360.0	100.0	215.0	320.0	2.5	1
	R_L = 300 Ω V_{IN} = 0 V	4.0	7.5	10.0	28.0	38.0	48.0	500.0	850.0	1150.0	250.0	475.0	650.0	4.1	1
	R_L = 900 Ω V_{IN} = 0 V	—	7.0	—	—	26.0	—	—	820.0	—	—	360.0	—	4.6	1,2
Pol Rev	R_L = open V_{IN} = 0 V	4.0	7.0	10.0	1.0	3.0	5.0	50.0	200.0	360.0	100.0	215.0	320.0	2.5	1,2
	R_L = 300 Ω V_{IN} = 0 V	4.0	7.5	10.0	28.0	38.0	48.0	500.0	850.0	1150.0	250.0	525.0	650.0	4.1	1
	R_L = 900 Ω V_{IN} = 0 V	—	7.0	—	—	26.0	—	—	833.0	—	—	360.0	—	4.6	1,2
Ringing	R_L = open V_{RING} = 0.7 Vac	—	7.0	—	—	3.0	—	—	152.0	—	—	180.0	—	2.1	1,2
	R_L = 1400 Ω V_{RING} = 0.7 Vac	4.0	7.5	10.0	33.0	38.0	42.0	2000.0	2500.0	2900.0	500.0	800.0	1010.0	5.7	1, 3

Notes:

1. *Values shown are for one channel only but are tested with both channels in the same state.*
2. *Not tested in production. Parameter is guaranteed by characterization or correlation to other tests.*
3. *Production test forces Vin=0.5Vdc which is equivalent to V_{RING}=0.7Vac.*
4. $I_{VSW} = \frac{V_{REG} \bullet I_{VREG}}{\eta \bullet V_{SW}}$ *, where* η *= efficiency. For our recommended circuit, an efficiency of 0.6 can be assumed under heavy loads.*
5. *SLIC device power is defined as the power delivered through the VCC and VREG pins minus the power delivered to the load. It does not include any power associated with the VSW pin and the external switcher.*

SPECIFICATIONS

Device Specifications

Specification	Condition	Min	Typ	Max	Unit	Note
Line Characteristics						
V_A, Active V_B, Reverse Polarity	R_L = open		–4		V	
V_A	Standby, R_L = open		–1			
V_{AB}	Active or Reverse Polarity, R_L = open	45	48	53		1.
	Standby, R_L = open	45	48	54.5		
V_{REG}	Active or Reverse Polarity, R_L = open	–50	–63	–69		4.
	Standby, R_L = open	–48	–58	–64		
Current limit threshold, I_{LTH} accuracy	Active or Reverse Polarity and Standby	17.5	20	22.5	mA	4.
I_{SC}	R_L = 100 Ω, Active or Reverse Polarity; I_{LTH}=20mA.	I_{LTH}+10	I_{LTH}+17	I_{LTH}+29		
	R_L = 100 Ω, Standby; I_{LTH}=20mA.	I_{LTH}+10	I_{LTH}+17	I_{LTH}+25		
Loop Current I_L accuracy	R_L = 600 Ω, Active or Reverse Polarity; I_{LTH}=20mA.	I_{LTH}+7	I_{LTH}+11	I_{LTH}+20		
	R_L = 600 Ω, Standby; I_{LTH}=20mA.	I_{LTH}+7	I_{LTH}+11	I_{LTH}+20		
LPF_i	Output impedance		25		kΩ	3.
	Bias voltage with respect to GND		2.2		V	
	Leakage current for capacitor value of 4.7 μF ± 20%			0.1	μA	
RDC	Input impedance		10		Ω	
	Input voltage tolerance	1.33	1.4	1.47	V	
Hook Switch detection threshold programming range		5		15	mA	4.
Loop detect threshold tolerance ($I_{offhook\_threshold}$)	Standby, Active and Reverse Polarity	8.8	11.5	14.5		
Ring trip current accuracy ($I_{trip\_threshold}$)	V_{REG}i = -85V	59.7	80	89.5		
Ringing						
V_A, V_B	V_{RING} = 0 V, R_L = 1400 Ω		–4		V	3.
V_{AB} offset	V_{RING} = 0 V, R_L = 1400 Ω	–2		+2		
Ringing voltage gain (K_R)	Ringing, $K_R = \frac{V_{AB}}{V_{RING}}$, Vin = 0.7Vpk, R_L = 1400Ω	95	100	105	V/V	1.
VRINGP, VRINGM Input Range		–0.3		2.4	V	4.
(VRINGP - VRINGM) Differential Input Impedance		200			kΩ	3.
Ringing Current Limit, I_{RSC}	Ringing, R_L = 100 Ω	90	135	180	mApk	4.
Ringing distortion	Vin = 0.7Vpk, R_L = 1400Ω		0.5	3.5	%	
Switching Power Supply						
f_{CHCLK}		80	85	90	kHz	3.
Chopper Clock High Duty Cycle (t_{CHCLK})		7.5	10	12.5	%	

Specification	Condition	Min	Typ	Max	Unit	Note
VT_{ILS} (current limit sense threshold)		0.25	0.28	0.31	V	3.
ILS_i	Input impedance		7000		Ω	
	Bias current	–1		+1	µA	
SD_i	Output impedance		50		Ω	
	Slew Rate negative	3			V/µsec	
	Slew Rate positive	25				
	V_{OH} where $V_{SW} \geq 12$ V, R_{BD} = 330 Ω	V_{SW} - 0.4	V_{SW} - 0.3	V_{SW}	V	
	V_{OL} where $V_{SW} \geq 12$ V, R_{BD} = 330 Ω		V_{SW} - 8.0			
CHS_i	Input impedance		1		MΩ	
	Ringing			180	µA	
	Standby and Active			75		
	Disconnect			1		
I_{RAMP}	C_{RAMP} current	72.0	82.2	92.9		
ISET	Input impedance		10		Ω	3.
	Input voltage tolerance	1.33	1.4	1.47	V	
Power Supply Rejection Ratio at the 2-wire Interface						
V_{CC}	200 to 4000 Hz, 50 mVrms	25	45		dB	
	4k to 50 kHz	20	40			4.
V_{REG} to V_{AB}	200 to 4000 Hz, 100 mVrms	25	45			
	4k to 50 kHz	20	40			4.
	50k to 100k	15	30			4.
Longitudinal Capability						
Longitudinal balance	R_L = 600 Ω, 300 to 3400 Hz, 0 dBm, Active and Reverse Polarity	46	63		dB	
T-L balance	1 kHz, 0 dBm	40	50			
Longitudinal current per pin	A(TIP) or B(RING)	30			mA	4.
Longitudinal impedance	A(TIP) or B(RING), 0 to 100 Hz		1	5	Ω/pin	4.
Longitudinal current detect, I_{LONG}	$\overline{F}_i$ low	18	26	35	mA	
Transmission Performance						
2WRL	300 to 3400 Hz, for 600 Ω	26			dB	4.
V_{IN} to V_{AB} (K_{IN})	R_L = open, 0dBm, 2-wire	9.34	9.54	9.74		
V_{OUT} to V_{AB} (K_{OUT})		9.34	9.54	9.74		4.
Gain Accuracy, 2-Wire to 4-Wire	0dBm, 1 kHz	–9.74	–9.54	–9.34		
Gain Accuracy, 4-Wire to 2-Wire	0dBm, 1 kHz	3.32	3.52	3.72		
Gain Accuracy, 4-Wire to 4-Wire	0dBm, 1 kHz	–6.42	–6.02	–5.62		
K_V, Voice Current gain	Line Test:, Standby, I_L < |20 mA| Active or Rev. Pol.L, I_L < |80 mA| Ringing, I_L < |100 mA|	$\frac{1}{520}$	$\frac{1}{500}$	$\frac{1}{480}$	A/A	3.

Specification	Condition	Min	Typ	Max	Unit	Note
Gain Accuracy over frequency	Relative to gain at 1 kHz 300 to 3400 Hz	–0.1		+0.1	dB	
Gain tracking at 1 kHz, relative to 0 dBm	–30 dBm to +3 dBm, 2-Wire	–0.1		+0.1		
	–55 dBm to –30 dBm, 2-Wire	–0.1		+0.1		4.
Gain tracking, On Hook, relative to 0 dBm	0 to –30 dBm, 2-wire	–0.15		+0.15		4.,5.
	+3 to 0 dBm, 2-wire	–0.35		+0.35		
THD (Total Harmonic Distortion)	0 dBm, 2-wire, 1 kHz		–64	–50		
	+7 dBm, 2-wire, 1 kHz		–55	–40		
THD, On hook	0 dBm, 2-wire, 1 kHz			–36		5.
Overload Level, 2-Wire	Active or Polarity Reversal	2.5			V	2.
ICN	C-message		12	15	dBrnC	4.
ICN	Psophmetric		–78	–75	dBmP	
$CFILT_i$	Output impedance		8000		Ω	3., 6.
	Drive capability, Active State	–150		+150	µA	
VHP_i	Input impedance		5		Ω	
	Offset voltage with respect to V_{REF}	–20		+20	mV	3.,7.
$VOUT_i$	Offset voltage with respect to V_{REF}	–40		+40	mV	
	Capacitive load on VOUT to AGND			100	pF	3.
	Resistive load on VOUT to AGND	20			kΩ	
	Drive capability, R_L = 20 kΩ	$\frac{V_{REF}-1}{20\text{ k}}$		$\frac{V_{REF}+1}{20\text{ k}}$	µA	3.,7.
	VOUT Output Range	0.4		2.4	V	3.
	VOUT Common Mode		1.4			
VINP – VINM	Offset voltage voice	–20		+20	mV	
	Differential Input Impedance	200			kΩ	
	Differential Mode Input	–1		1	V	
	VINP, VINM Input Range	–0.3		2.4		
Metering gain	R_L = 300 Ω, 12.0 kHz, Active	0	0.25	0.5	dB	4.
	R_L = 300 Ω, 16.0 kHz, Active					
Metering distortion, R_L = 300 Ω, V_{AB} = 1.5 Vpk	Frequency = 12 kHz, Active		–45	–40	dB	4.
	Frequency = 16 kHz, Active					
Crosstalk Between Channels						
Crosstalk coupling loss	F = 200 Hz to 3.4 kHz			–75	dB	
Logic Interface						
Inputs (C1, C2)						
V_{IL}				0.8	V	
V_{IH}		2.0				
I_{IL}	V_{IN} = 0.4 V	–100	0	100	µA	
I_{IH}	V_{IN} = 2.4 V	–100	30	100		
CHS_{IL}	V_{IN} = 50 mV		90		µA	4.
$CHS_{Float\_Leakage}$		–1		+1		4.

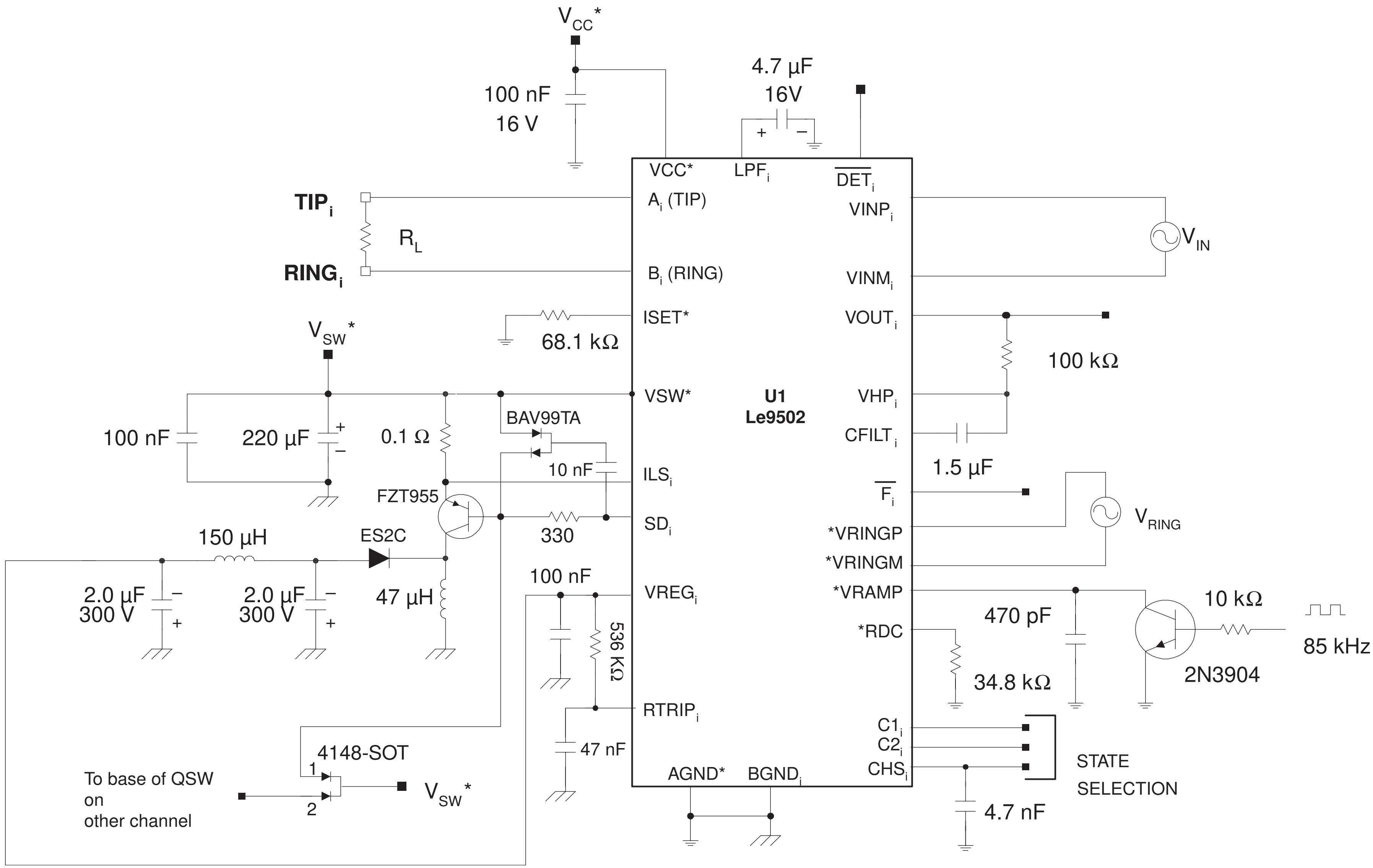
Specification	Condition	Min	Typ	Max	Unit	Note
Outputs ($\overline{F}_1$, $\overline{F}_2$)						
V_{OH}	I_{OUT} = –25 µA	2.4	2.8		V	
V_{OL}	I_{OUT} = 25 µA		0.2	0.4		
$\overline{DET}$ Pin Characteristics						
V_{OH}	I_{OUT} = –165µA	2.4	2.8		V	
V_{OL}	I_{OUT} = 165 µA		0.2	0.4		

Note:

1. *V_{AB} = Voltage between the A_i (TIP) and B_i (RING) pins.*
2. *Overload level is defined when THD = 1%.*
3. *Guaranteed by design.*
4. *Not tested in production. Parameter is guaranteed by characterization or correlation to other tests.*
5. *When On hook, R_{LDC} is open circuit, R_{LAC} = 600 Ω.*
6. *Layout should have less than 10 pF from pin to ground.*
7. V_{REF} *is an internal value of typically* V_{REF} *= 1.4V.*

TEST CIRCUIT

Per Channel

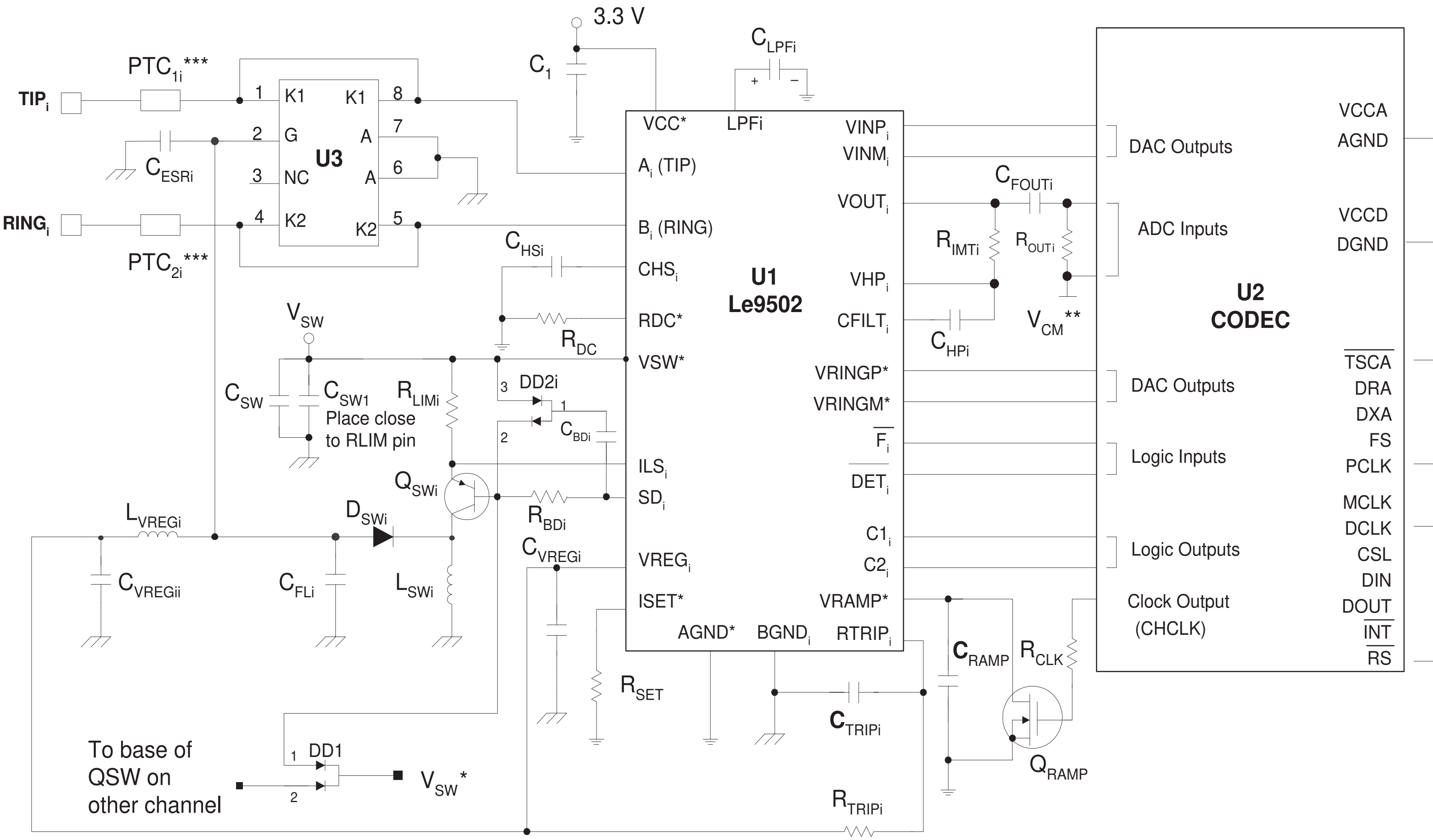


Note:

** Denotes pins that are common to both channels.*

i = per channel component/pin

APPLICATION CIRCUIT



Note:

** Denotes pins that are common to both channels.*

*** V_{CM} is the bias voltage, which is ≥ (maximum ADC input voltage / 2)*

**** Total fuse resistance = 100Ω guarantees a minimum DC load.*

LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1, 2). The protection circuit is included.

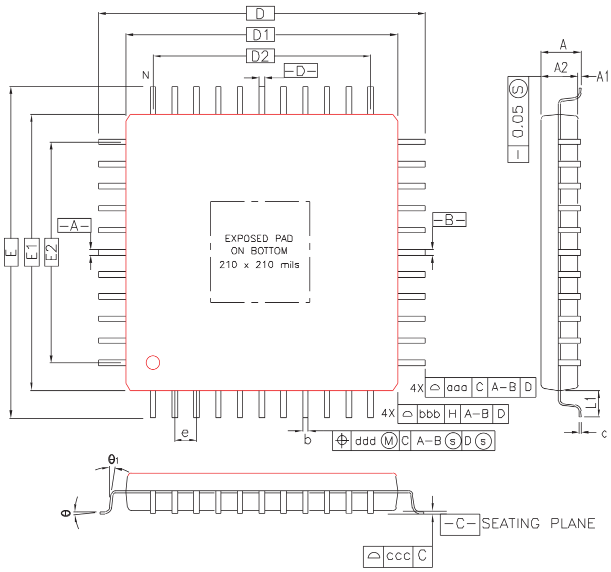
Item	Quantity (see note 1)	Type	Value	Tol.	Rating	Comments	Note
C_1	1	Capacitor	100 nF	10%	16 V	Panasonic / ECJ-1VB1C104K, 0603	
C_{BDi}	2	Capacitor	27 nF	10%	16 V	Panasonic / ECJ-1VB1C273K, 0603	
C_{ESRi}, C_{VREGi}	4	Capacitor	0.1uF	10%	200 V	CalChip / GMB31X7R104K200NT, 1206	
C_{FOUTi}	2	Capacitor	1 µF	10%	50 V	Panasonic / ECJ-1VC1H100D, 0603	
C_{HSi}	2	Capacitor	1 nF	10%	50 V	Panasonic / ECJ-1VC1H102J, 0603	
C_{HPi}	2	Capacitor	1.5 µF	10%	6.3 V	Panasonic / ECJ-2YB0J155K, 0805	
C_{LPFi}	2	Capacitor	4.7 µF Tantalum	10%	6.3 V	Panasonic / ECS-T0JY475R, 1206	
C_{RAMP}	1	Capacitor	470 pF	5%	50 V	Panasonic / ECJ-1VC1H471J, 0603	
C_{TRIPi}	2	Capacitor	47 nF	10%	50 V	Panasonic / ECJ-1VB1C473K, 0603	
C_{SW}	1	Capacitor	220 µF Alum. Elect.	20%	25 V	Panasonic / ECE-V1EA221UP, 8mmCan	
C_{SW1}	1	Capacitor	100 nF	10%	50 V	Panasonic / ECJ-2YB1H104K, 0805	
C_{FLi},	2	Capacitor	2.2 µF	20%	200 V	United Chemi / THCR70E2D225MT, 3025	
C_{VREGii}	2	Capacitor	1.0 µF	10%	300 V	Tecate / CMC-300/105KX1825T060	
D_{SWi}	2	Diode	ES2C		2 A	General Semi. / ES2C, DO-214AA	
DD1	1	Diode	4148CC		200 mA	Fairchild / MMBD4148CC, SOT-23	
DD2i	2	Diode	BAV99		200 mA	Fairchild / BAV99, SOT-23	
L_{SWi}	2	Inductor	47 µH		2.95 A	Cooper Coiltronics / DR127-470	
L_{VREGi}	2	Inductor	150 µH		205 mA	Coilcraft 1812LS154X_B	
PTC_{1i}, PTC_{2i}	4	PTC	50 Ω			AsiaCom / MZ2L-50R	
Q_{RAMP}	1	N-channel MOSFET	FDV301N			Fairchild / FDV301N, SOT-23	
Q_{SWi}	2	PNP Transistor	FZT955		-140 V	Zetex / FZT955TA, SOT-223	
R_{BDi}	2	Resistor	180 Ω	1%	1/8 W	Yageo / 9C08052A1800FKHFT, 0805	
R_{CLK}	1	Resistor	1 k	1%	1/16 W	Panasonic / ERJ-3EKF1002V, 0603	
R_{DC}	1	Resistor	34.8 k	1%	1/16 W	Panasonic / ERJ-3EKF3482V, 0603	
R_{IMTi}	2	Resistor	84.5 k	1%	1/16 W	Panasonic / ERJ-3EKF84R5V, 0603	
R_{LIMi}	2	Resistor	0.1 Ω	1%	1/4 W	Panasonic / ERJ-L14KF10CU, 1210	
R_{OUTi}	2	Resistor	51 k	5%	1/16 W	Panasonic / ERJ-3GEYJ513V, 0603	
R_{SET}	1	Resistor	68.1 k	1%	1/16 W	Panasonic / ERJ-3EKF6812V, 0603	
R_{TRIPi}	2	Resistor	536 k	1%	1/16 W	Panasonic / ERJ-3EKF5363V, 0603	
U1	1	SLIC	Le9502	-	-	Zarlink / Le79502, 44-pin eTQFP	
U2	1	CODEC	-	-	-	-	
U3	1	Protection	TISP61089	-170V	30A	Bourns / TISP61089BDR, DOO8	

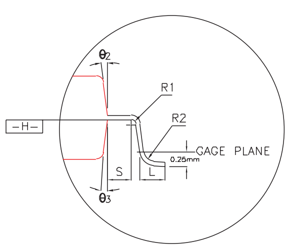
Note:

1. *Quantities required for a complete two-channel solution.*

PHYSICAL DIMENSIONS

44-Pin eTQFP





SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	12.00 BSC.		
D1	10.00 BSC.		
E	12.00 BSC.		
E1	10.00 BSC.		
R2	0.08	—	0.20
R1	0.08	—	—
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	—	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	—	—
b	0.17	0.20	0.27
e	0.80 BSC		
D2	8.00		
E2	8.00		
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
N	44		

NOTES:

1. CONTROLLING DIMENSION IN MILLIMETER UNLESS OTHERWISE SPECIFIED.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" DIMENSION BY MORE TAHN 0.08 mm.
4. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 mm AND 0.5 mm PITCH PACKAGES.
5. SQUARE DOTTED LINE IS E-PAD OUTLINE.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A1 to B1

- In *Absolute Maximum Ratings*, the following changes were made:
  - Changed T_A from 22.7° to 32°C/W
  - Added another note describing eTQFP package
- In *Supply Currents and Power Dissipation*, Ringing operation state, removed condition V_{IN} = 0.7 V_{DC}
- In *Device Specifications*, Metering gain, changed min, typ, and max values from 4.24, 4.44, and 4.64, respectively, to –0.2, 0, and 0.2, respectively
- In *Device Specifications*, Logic Interface, I_{IH}, changed min and max values from ±40 to ±50.
- Updated Switching Power Supply block diagram
- Updated Application Circuit and Parts List
- Updated Physical Dimensions drawing

Revision B1 to C1

- In *Features*, the following changes were made:
  - Removed (5V Tolerant) statement.
  - Changed "5REN" statement to "70 Vpk @ 5REN"
  - Changed "Up to 90 Vpk, Balanced" statement to "90 Vpk capable".
- In *Related Literature*, added references to Le9500 and Le9501 data sheets.
- In *Two-Wire Interface*, updated the paragraph under the "Ringing" section.
- In *Electrical Characteristics*, the following changes were made:
  - Removed "0° C < T_A < 70° C" statement.
  - Updated the entire table entry.
  - Changed "V_{IN}" to "V_{RING}" for Ringing State and in Note 3.
- In *Device Specifications*, the following changes were made:
  - Increased VREG typical and maximum specifications.
  - Removed "R_L=34.8 kΩ " from I_{LTH} accuracy and added note 4.
  - Increased I_{SC} typical and maximum specifications, and added R_L=600 Ω case.
  - Updated DC feed graphic and I_{SC} nominal value to reflect typical value of (I_{LTH} + 17.0mA).
  - Added I_L accuracy @ R_L=600Ω case.
  - Increased $I_{offhook\_threshold}$ typical and maximum specifications and merged "mA" column units.
  - Changed "Vin = 0.9 Vpk" references to "Vin = 0.7 Vpk".
  - Increased I_{RSC} typical and maximum specifications and added note 4.
  - Added note 4. to "VRINGP, VRINGM Input Range".
  - Added note 7. to K_R and Ringing distortion.
  - Adjusted SD_i, V_{OH} and V_{OL} : minimum, typical and maximum values and merged "uA" column units.
  - Adjusted I_{LONG} minimum and maximum specifications.
  - Added note 4. to "Negative foregin voltage threshold at V_A or V_B".
  - Removed "TBD" references and filled with data accordingly.
  - Updated "Metering gain" minimum, typical, and maximum specifications.
  - Adjusted I_{IL}, I_{IH}, CHS_{IL}, and $CHS_{Float\_Leakage}$ minimum, typical, and maximum specifications.
  - Added note 4. to CHS_{IL} and $CHS_{Float\_Leakage}$.
  - Add Note. 7 definition.
- Updated Test Circuit, Application Circuit and Parts List.
- Added "***" definition for PTCi fuse in Application Circuit.

Revision C1 to D1

- Added green package OPN to *Ordering Information* on page 1
- Added *Package Assembly* on page 13
- In Device Specifications, *Metering Gain*, changed min/typ/max values from -0.5, .2, .05 to 0, .25, and .5, respectively.

Revision D1 to E1

- In *Electrical Characteristics*, the following changes were made:
  - Updated the entire table entry.
- In *Device Specifications*, the following changes were made:
  - Increased V_{AB} maximum specifications for Standby.
  - Lowered V_{REG} minimum specifications.
  - Added "I_{LTH} = 20mA" for I_{SC}, and I_L. This required increase in 'Condition' table size and squeezing the 'Note' column.
  - Increased I_{SC} maximum specifications
  - Increased $I_{trip\_threshold}$ typical specifications and added "V_{REG}i = -85V" in the 'Condition' column.
  - Removed note 7 definition and references to it from K_R and Ringing distortion. Changed note 8 references to note 7 (as note 8 definition now defaults to note 7).
  - Increased I_{LONG} typical specifications.
  - Added note 4. to "Gain tracking, On Hook, relative to 0 dBm".
  - Updated "Metering gain" minimum, typical, and maximum specifications.
  - Added "Active" for the 12kHz "Metering gain" and "Metering distortion".
- Updated Test Circuit, the following changes were made:
  - Changed CSW, CFL, CVREG, CHS, and LVREG values.

Revision E1 to F1

- In *Electrical Characteristics*, the following changes were made:
  - Updated the 'Supply Currents and Power Dissipation' table entries for VREG and SLIC Power.
  - Updated the 'Device Specifications' table entries for V_{REG}.
  - Added note 3. to ISET and RDC - Input voltage tolerance.

Revision F1 to G1

- In *Electrical Characteristics* on page 14 the following changes were made:
  - Updated SLIC Device Power typical specifications for Pol.Rev.: R_L=300Ω.
- In *Device Specifications* on page 15, the following changes were made:
  - Increased V_{AB} maximum specifications for Active or Reverse Polarity.

Revision G1 to G2

- Made minor edits to *Features* on page 1.
- Added note to *Physical Dimensions* on page 22.

Revision G2 to G3

- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007.

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