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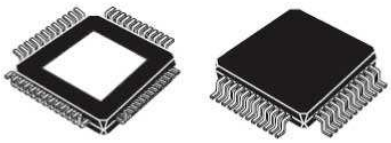
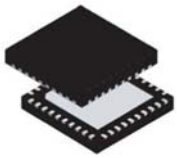
LED2472G

24-channels LED driver with error detection and gain control

Datasheet - production data



TQFP48-EP



MLPQ40-EP 5x5

Features

- 24 constant current output channels
- Output current: from 4 mA to 72 mA
- 8 x 3 independently controlled channels (RGB)
- Current programmable through external resistor
- 7-bit global current gain adjustment in two ranges
- Error detection mode (both open and shorted LED)
- Programmable shorted LED detection thresholds
- Auto power-saving / auto wakeup
- Gradual output delay (selectable)
- Supply voltage: 3 V to 5.5 V
- Thermal shutdown and thermal flag
- Up to 30 MHz CLK 4 wires interface
- 20 V current generators rated voltage

Applications

- Full color large displays
- LED signage
- LED screens for indoor and outdoor billboards

Description

The LED2472G is a monolithic, low voltage, low current power 24-bit shift register designed for LED panel displays with particular features oriented to indoor and outdoor LED screen billboards. The LED2472G guarantees 20 V of output driving capability, allowing several LEDs to be connected in series. The device is configured in 3 groups (red, green and blue) of 8 independently-controlled channels. The LED current can be separately regulated for each color within the range from 4 mA to 72 mA. This range is divided into two sub-ranges and the current can be adjusted within each range in 64 steps of resolution (6 bits per color). A single external resistor is required. All the controls and the shift register data are accessible via serial interface. A single 24-bit configuration register is used to choose features and settings to fit the application. The LED failure detection circuit checks 3 different conditions that can occur at the output line: short to GND, short to LED power supply rail or open channel. The auto power shutdown and auto power-on feature (selectable) allows the device to save power without any external intervention. Thermal management includes overtemperature flag and the output thermal shutdown (170 °C). The high clock frequency of up to 30 MHz makes the device suitable for high data rate transmission. A selectable gradual output delay reduces the inrush current. The supply voltage ranges from 3 V and 5.5 V.

Table 1. Device summary

Order code	Package	Packaging
LED2472GBTR	TQFP48-EP	Tape and reel
LED2472GQTR	MLPQ40-EP 5x5	

Contents

List of tables

List of figures

1 Pin description

Figure 1. Pinout for TQFP48EP (top view)

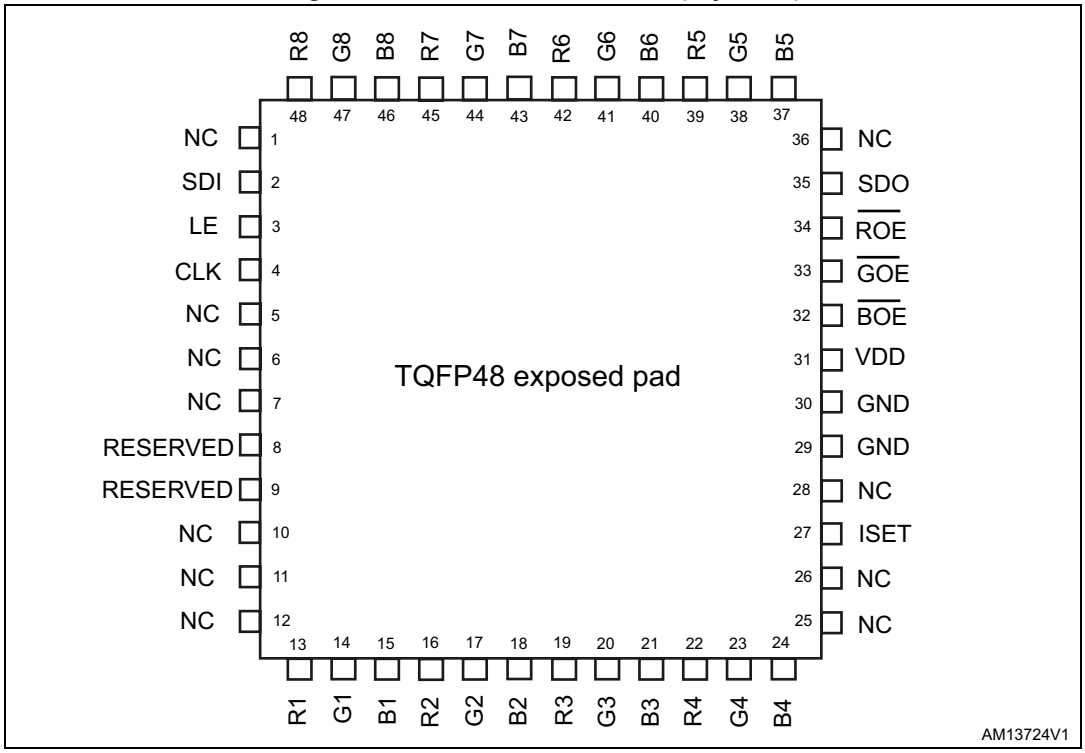


Figure 2. Pinout for MLPQ40 (top view)

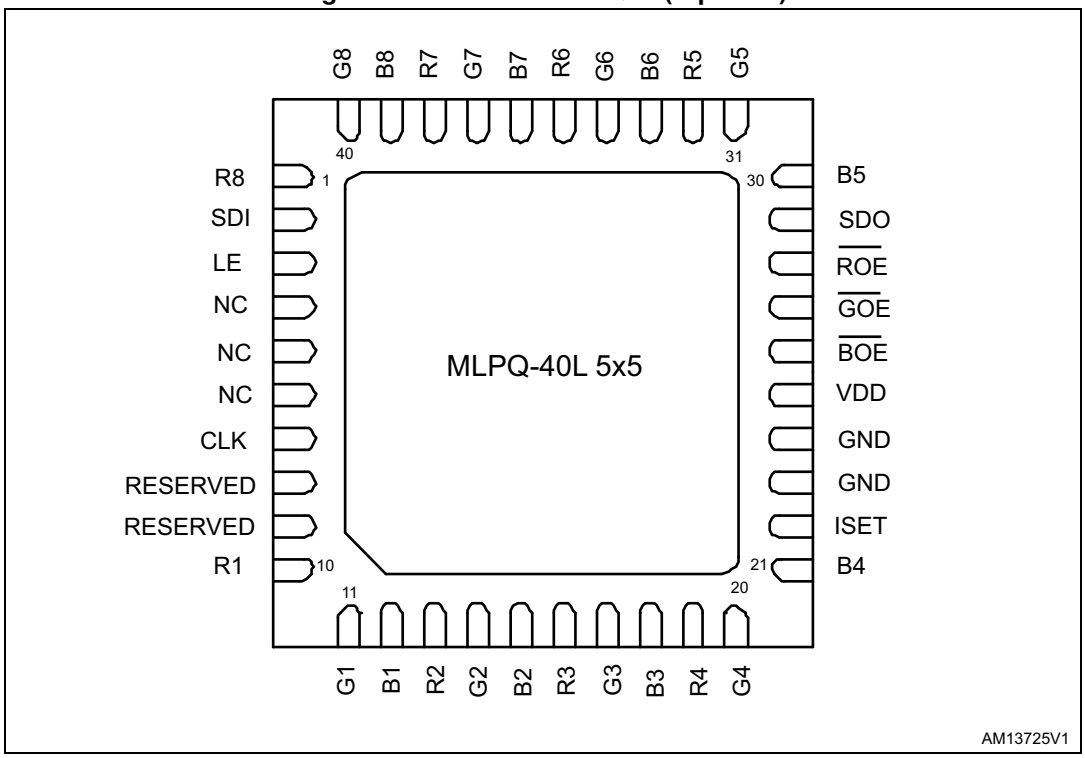


Table 2. Pin description

Pin		Symbol	Name and function
TQFP48	MLPQ40		
29, 30	23, 24	GND	Ground
2	2	SDI	serial data input
3	3	LE	Latch enable
8,9	8, 9	Reserved	Not used in applications
4	7	CLK	Clock
1, 5, 6, 7, 10, 11, 12, 25, 26, 28, 36	4, 5, 6	NC	Not connected
31	25	VDD	Power supply voltage
13	10	R1	Red output 1
14	11	G1	Green output 1
15	12	B1	Blue output 1
16	13	R2	Red output 2
17	14	G2	Green output 2
18	15	B2	Blue output 2
19	16	R3	Red output 3
20	17	G3	Green output 3
21	18	B3	Blue output 3
22	19	R4	Red output 4
23	20	G4	Green output 4
24	21	B4	Blue output 4
27	22	ISET	Current setup
32	26	BOE	Blue output enable
33	27	GOE	Green output enable
34	28	ROE	Red output enable
35	29	SDO	Serial data output
37	30	B5	Red output 5
38	31	G5	Green output 5
39	32	R5	Blue output 5
40	33	B6	Red output 6
41	34	G6	Green output 6
42	35	R6	Blue output 6
43	36	B7	Red output 7
44	37	G7	Green output 7
45	38	R7	Blue output 7
46	39	B8	Red output 8

Table 2. Pin description (continued)

Pin		Symbol	Name and function
TQFP48	MLPQ40		
47	40	G8	Green output 8
48	1	R8	Blue output 8

2 Absolute maximum ratings

Stressing the device above the ratings listed in the *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.4 to 7	V
V_I	Digital inputs voltage	-0.4 to Vdd+0.4	V
OUT	Driver outputs voltage (R<1:8>, G<1:8>, B<1:8>)	20	V
Io	Output current	80	mA
IGND	GND terminal current	1.9	A
ESD	Electrostatic discharge protection HBM human body model	±2	KV
	Electrostatic discharge protection MM machine model	±200	V

3 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Value	Unit
Ta	Operative free-air temperature range(1)	-40 to +85	°C
TJ-OPR	Operative thermal junction temperature range	-40 to +125	
Tstg	Storage temperature range	-55 to +150	
Rth_{ja}	Junction-ambient thermal resistance; QFN40-EP(2)	25.3	°C/W
	Junction-ambient thermal resistance; TSSOP48-EP(1)	33	°C/W

1. This data must be considered in adequate power dissipation conditions. The junction temperature must be maintained below 150 °C.
2. In accordance with JEDEC standard 51-7B. The exposed pad should be soldered directly to the PCB to obtain the thermal benefits.

4 Electrical characteristics

Vdd = 3.3 V, Tj = 25 °C, GRG = “1” (gain reg), R_{ext} = 13 kΩ, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Vdd	Supply voltage		3		5.5	V
V_{OUT}	Output voltage	For all outputs	-	-	19	
V_{IH}	Input voltage		0.7•Vdd	-	Vdd	
V_{IL}			GND	-	0.3•Vdd	
V_{OL}	Serial data output voltage (SDO)	V_{DD} = 3 to 5.5 V I = +/- 1 mA	-	-	0.4	
V_{OH}			V_{DD}-0.4	-	-	
I_{Oleak}	Output leakage current	Vo = 19 V, all outputs OFF	-	-	0.5	uA
V_{uvlo1}	UVLO threshold voltage (rising)			2.7	2.9	V
V_{uvlo1}	UVLO threshold voltage (falling)		2.2	2.3		V
Hy_{uvlo}	UVLO hysteresis			400		mV
ΔI_{OL1}	Output current precision channel-to-channel per each color group (all outputs ON)(1)(2)	V_o = 0.3 V; (Io=5 mA) CFG-0 = CFG-1 = CFG-2 = “0” GRG = “0”	-	-	±4	%
ΔI_{OL3}		V_o = 0.6 V; (Io = 21 mA) CFG-0 = CFG-1 = CFG-2 = “0”	-	-	±3	
ΔI_{OL2}		V_o = 0.5 V; (Io=15 mA) CFG-0 = CFG-1 = CFG-2 = “1” GRG = “0”	-	-	±3	
ΔI_{OL4}		Vo = 1.2 V; (Io=61 mA) CFG-0 = CFG-1 = CFG-2 = “1”	-	-	±3	
ΔI_{OL1a}	Output current error device-to-device per each color group (all outputs ON)(1)	V_o = 0.3 V; (Io = 5 mA) CFG-0 = CFG-1 = CFG-2 = “0” GRG = “0”	-	-	±6	
ΔI_{OL3a}		V_o = 0.6 V; (Io=21 mA) CFG-0 = CFG-1 = CFG-2 = “0”	-	-	±6	
ΔI_{OL2a}		V_o = 0.5 V; (Io = 15 mA) CFG-0 = CFG-1 = CFG-2 = “1” GRG = “0”	-	-	±6	
ΔI_{OL4a}		Vo = 1.2 V; (Io = 61 mA) CFG-0 = CFG-1 = CFG-2 = “1”	-	-	±6	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
%/ΔV_{OUT}	Output current vs. output voltage regulation(3)	V_o from 1.2 V to 3 V; (Io = 61 mA) CFG-0 = CFG-1 = CFG-2 = “1”	-	±0.2	-	%/V
%/ΔV_{DD}	Output current vs. supply voltage regulation(4)	Vdd from 3 V to 5.5 V V_o = 1.2 V; (Io = 61 mA) CFG-0 = CFG-1 = CFG-2 = “1”	-	±1	-	
Rup	Pull-up resistor for OE pin		400	500	650	kΩ
Rdw	Pull-down resistor for LE pin					
R_{ext}	External current setup resistance				100	
I_{DD1}	Supply current (OFF)	No data transfers, all outputs OFF, CFG-0 = CFG-1 = CFG-2 = “0” GRG = “0”; CFG-6 = “0”			8	mA
I_{DD2}		No data transfers, all outputs OFF, CFG-0 = CFG-1 = CFG-2 = “1” CFG-6 = “0”			16	
I_{DD1}	Supply current (ON)	No data transfers, all outputs ON, CFG-0 = CFG-1 = CFG-2 = “0” GRG = “0”	-		8	mA
I_{DD2}		No data transfers, all outputs ON, CFG-0 = CFG-1 = CFG-2 = “1”	-		15	
IDD (AutoOFF)	Supply current (autoOFF)	All output OFF CFG-6 = “1”	-	200	500	µA
SDE_1	LED short detection voltage	CFG-3 = CFG-4 = CFG-5 = “0”		2.0		V
SDE_2		CFG-3 = CFG-4 = CFG-5 = “1”		3.0		
ODC	LED open detection current			0.5 I_{OL}		

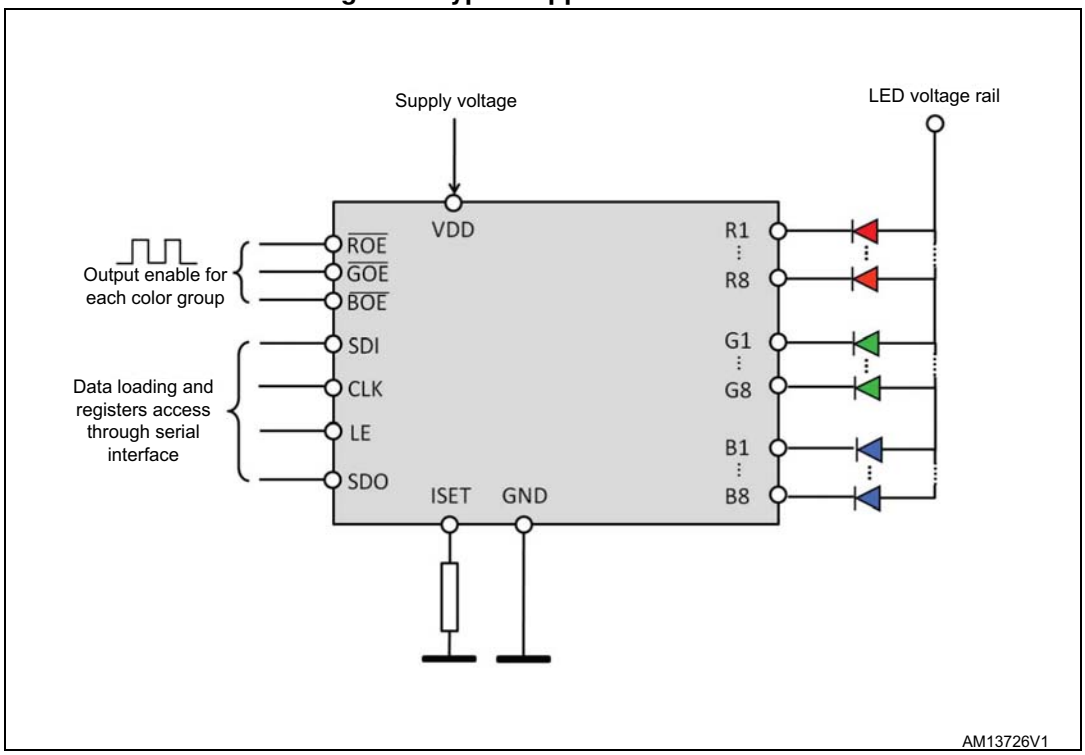
Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Tflg	Thermal flag			150		°C
Tsd	Thermal shutdown(5)			170		
Tsd-hy	Thermal shutdown hysteresis(5)			15	20	

1. Tested with just one output loaded
2. $((Iout_n - Iout_{avg1\text{-}15})/ Iout_{avg1\text{-}15}) \times 100$
3. $$\Delta(\%/V) = \frac{(Ioutn @ Voutn = 3.0V) - (Ioutn @ Voutn = 1.0V)}{(Ioutn @ Voutn = 1.0V)} \times \frac{100}{3-1}$$
4. $$\Delta(\%/V) = \frac{(Ioutn @ Vdd = 5.5V) - (Ioutn @ Vdd = 3.0V)}{(Ioutn @ Vdd = 3.0V)} \times \frac{100}{5.5-3}$$
5. Not tested, guaranteed by design.

4.1 Typical application circuit

Figure 3. Typical application circuit



5 Switching characteristics

Vdd = 3.3 V, Tj = 25 °C, GRG = “1” (gain reg), R_{ext} = 13 kΩ, unless otherwise specified.

Table 6. Switching characteristics(1)(2)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency		Cascade operation	-	-	30	MHz
$tr_{(SDO)}$	SDO rise time		R_{ext} = 13 kΩ; Iout = 21 mA Vout = 0.6 V VIH = VDD; VIL = GND RL = 56 Ω; CL = 10 pF CFG-0 = CFG-1 = CFG-2 = “0”	-	5	-	ns
$tf_{(SDO)}$	SDO fall time			-	5	-	
tPLH2	LE-OUTn(3)	Propagation delay time (“L” to “H”)		-	70	-	
tPLH3	$\overline{OE}$-OUTn(3)			-	100	-	
tPLH	CLK-SDO CFG-7 = ‘0’			8	15	25	
tPHL2	LE-OUTn(3)	Propagation delay time (“H” to “L”)		-	70	-	
tPHL3	$\overline{OE}$-OUTn(3)			-	100	-	
tPHL	CLK-SDO CFG-7= ‘0’			8	15	25	
tw(CLK)	CLK	Pulse width		20	-	-	
$t_W(\overline{OE})$	$\overline{OE}$			150(4)	-	-	
tw(L)	LE			20	-	-	
t_{gr-d}	Gradual delay Ch to Ch				10		
$t_{su(L)}$	Setup time for LE			5	-	-	
$t_{h(L)}$	Hold time for LE			5	-	-	
$t_{su(D)}$	Setup time for SDI			5	-	-	
$t_{h(D)}$	Hold time for SDI			10	-	-	
tor(5)	Maximum CLK rise time			-	-	5	µs
tof(5)	Maximum CLK fall time			-	-	5	
I_{out-ov}	Output current turn-on overshoot		Vout = 0.3 to 3 V CL = 10 pF; Iout = 5 to 61 mA	-	-	10	%
t_{n-err}	Normal error detection minimum output ON time			-	-	1	µs

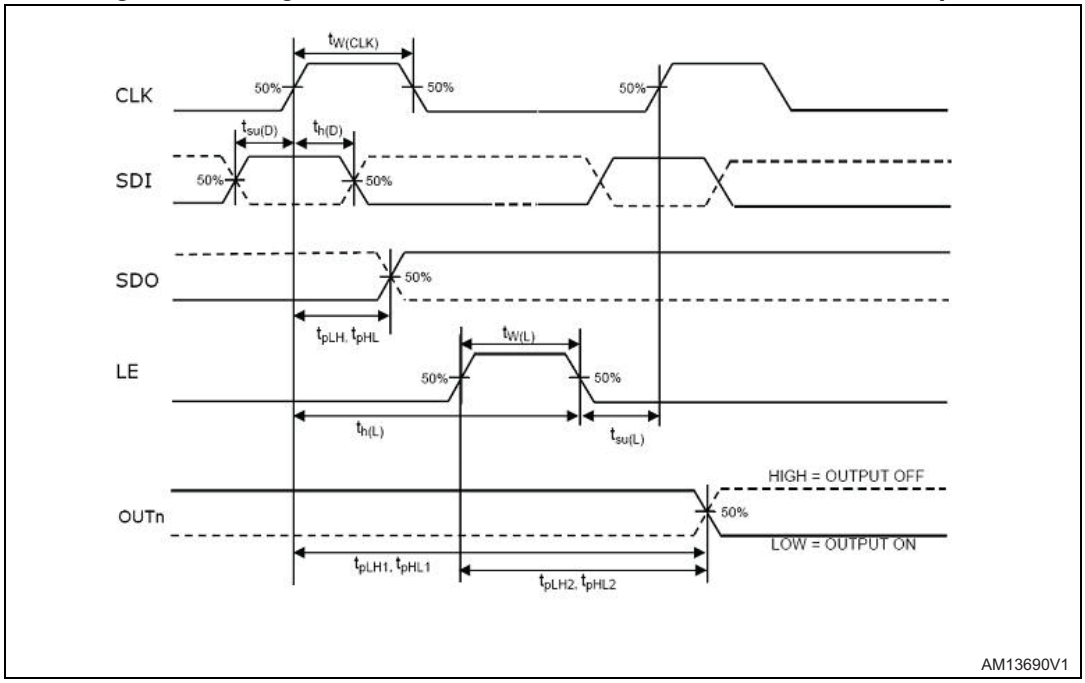
Table 6. Switching characteristics(1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{shut\text{-}down}$	Auto power shutdown time (autoOFF)	From LE falling edge to R_{ext} voltage reference at -10%	-	75	-	ns
$t_{wake\text{-}up}$	Auto power wakeup time	From LE falling edge to R_{ext} voltage reference at 90%	-	1	-	µs

1. All table limits are guaranteed by design.
2. Not tested in production.
3. CFG-8 = “1” (no output gradual delay)
4. In normal error detection mode must be longer than 1µs
5. If devices are connected in cascade and t_{or} or t_{of} is large, it may be critical to achieve the timing required for data transfer between two cascaded devices

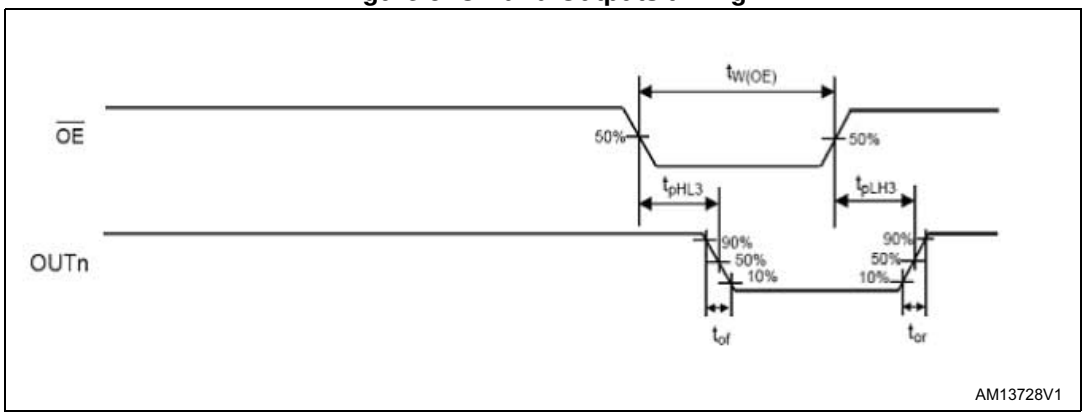
6 Timing

Figure 4. Timing for clock, serial-in, serial-out, latch enable and outputs



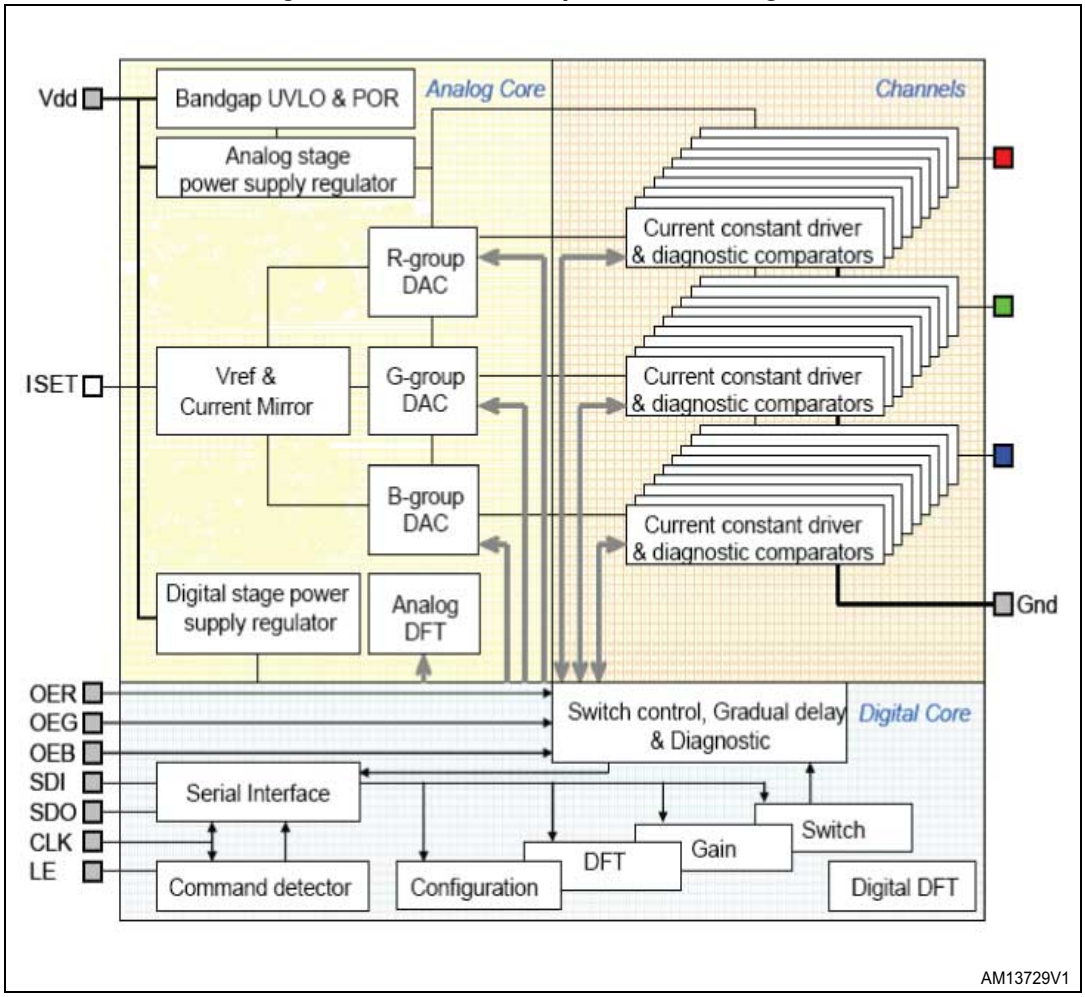
Correct sampling of the data depends on the stability of the data at SDI on the rising edge of the clock signal and it is assured by a proper data setup and hold time ($t_{SU(D)}$ and $t_{h(D)}$), as shown in *Figure 4*. The same figure shows the propagation delay from CLK to SDO (t_{PLH}/t_{PHL}). *Figure 4* describes also the minimum duration of CLK and LE pulses ($t_{W(CLK)}$ and $t_{W(L)}$, respectively) and the propagation delay from LE to OUT_n (t_{PLH1}/t_{PHL1} and t_{PLH2}/t_{PHL2}, respectively). Finally, *Figure 5* also defines the turn-on and turn-off time (t_{of} and t_{or}) of the output voltage.

Figure 5. OE and Outputs timing



7 Simplified Internal block diagram

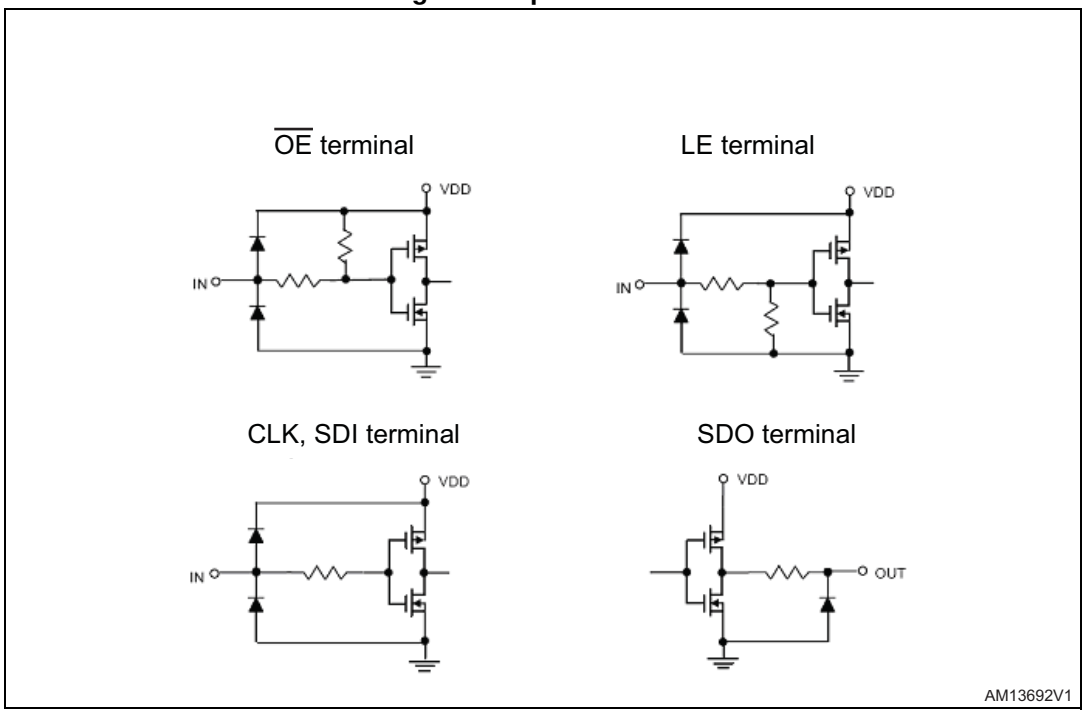
Figure 6. LED2472G simplified block diagram



7.1 Equivalent circuits of inputs and outputs

Input terminals LE and /OE have pull-down and pull-up connections, respectively. CLK and SDI must be connected to external circuits to fix the logic level.

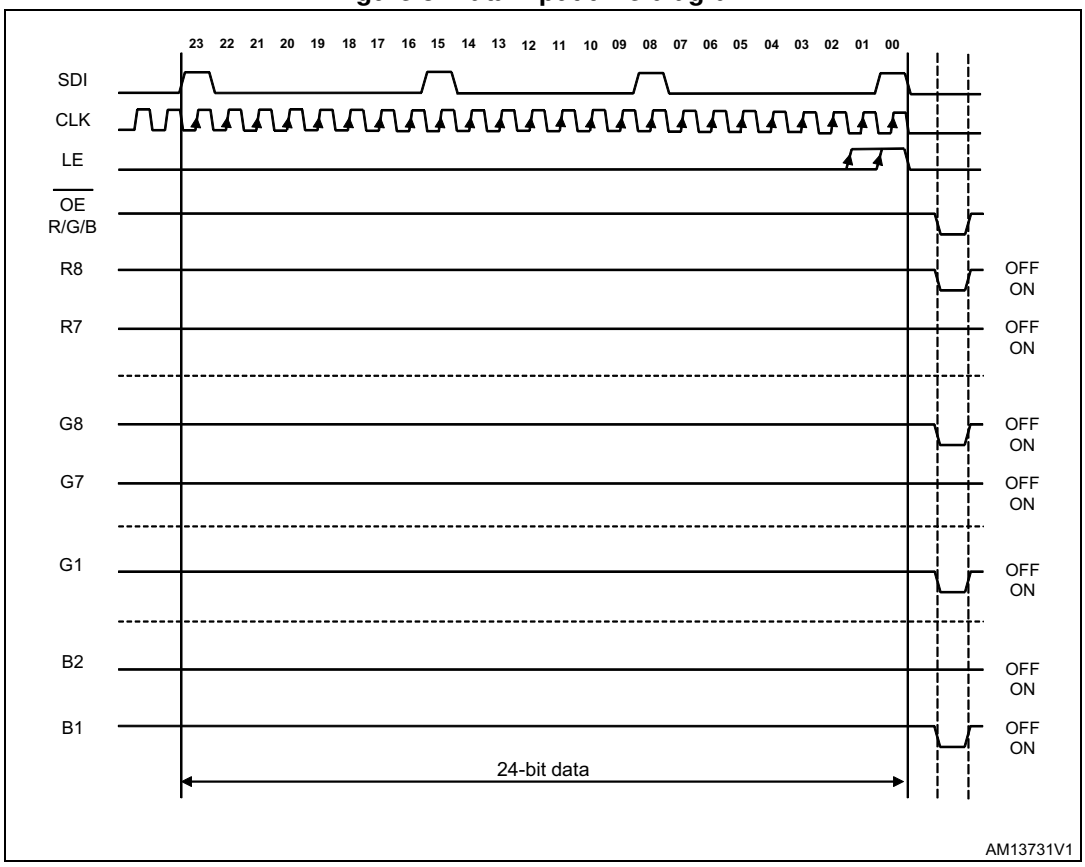
Figure 7. Input terminals



8 Digital blocks

The data inputs come in through the serial interface at each CLK rising edge and after 24 CLK cycles all data are loaded into the shift register. The LE signal is used to latch the loaded data and also to generate digital keys for CFG management, scrolling, thermal check and LED error detection. When one of the output enable signal (OER, OEB or OEG) is low, the corresponding data are transferred to the relative output drivers. The data flow is “first in, first out”. To latch the data, the LE signal must be high during the last data loading CLK rising edge (*Table 7*). When one of the output enable signals (OER, OEB or OEG) is at low level, output terminals (R1-R8,G1-G8, B1-B8) respond to the data either ON or OFF. When one of the output enable signals (OER, OEB or OEG) goes to “1”, all outputs switch off all the data on the output terminal. LE and /OE signals are asynchronous with respect to the CLK signal. The time diagram below refers to RGB flow setting.

Figure 8. Data input time diagram



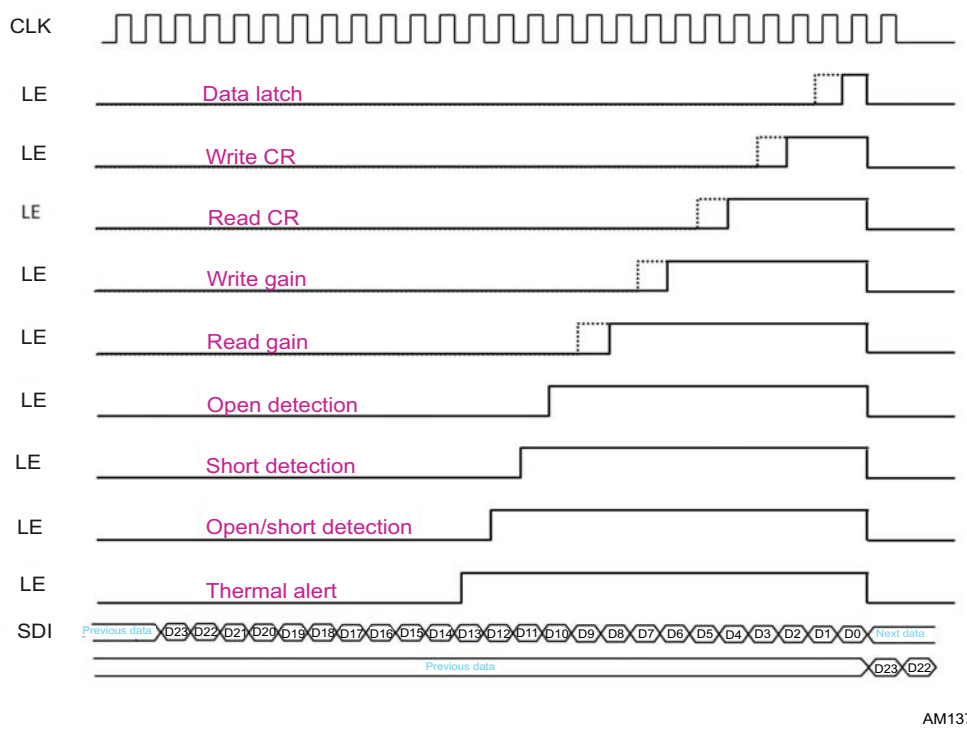
8.1 Register access

Access to the different registers of the device (configuration register, gain register, etc.) is achieved by using different digital keys, defined as a number of CLK pulses during which the LE signal is asserted. The available digital keys are summarized in *Table 7*.

Table 7. Digital keys summary

#CLK rising edges with the LE asserted	Description
1-2	Data latch
3-4	Write configuration register
5-6	Read configuration register
7-8	Write gain
9-10	Read gain
11	Open detection
12	Short detection
13	Open/short detection
14	Thermal alert reading
15	Reserved
16	Reserved

Figure 9. Digital key timing diagram



8.2 Configuration register

The configuration register is used to enable or disable some device features, to program some parameters and to change other settings. Access to this register (read or write) is

managed as described in *Table 8* where a description is provided for each bit. The default value of the configuration register (when the device is switched ON or after a reset) is all bits set to “0”. To change anything in the configuration register, a 24-bit digital word must be sent (CFG-0 represents the LSB, CFG-23 the MSB).

Figure 10. Configuration register

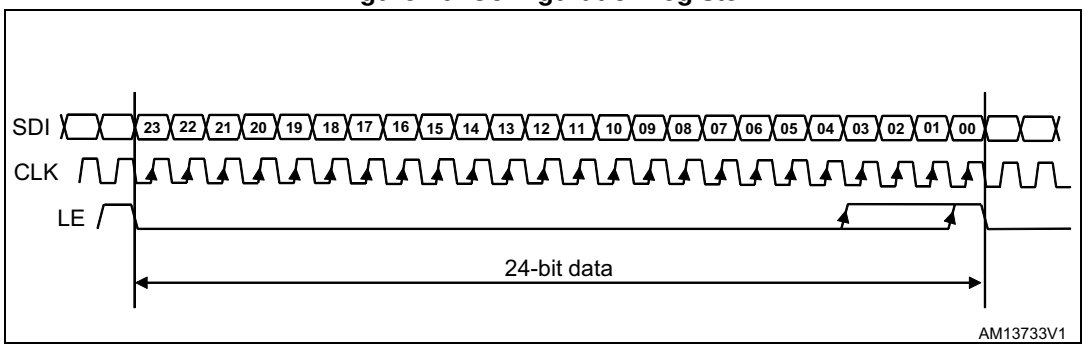


Table 8. Configuration register

BIT	Definition	Attribute read/write	Configuration register function description	Default
CFG-0	RED current range	R/W	”0” low current range “1” high current range	0
CFG-1	GREEN current range	R/W	”0” low current range “1” high current range	0
CFG-2	BLUE current range	R/W	”0” low current range “1” high current range	0
CFG-3	RED voltage det. thr.	R/W	“0” LED short-circuit detection threshold 2 V “1” LED short-circuit detection threshold 3 V	0
CFG-4	GREEN voltage det. thr.	R/W	“0” LED short-circuit detection threshold 2 V “1”LE D short-circuit detection threshold 3 V	0
CFG-5	BLUE voltage det. thr.	R/W	“0” LED short-circuit detection threshold 2 V “1” LED short-circuit detection threshold 3 V	0
CFG-6	Auto OFF	R/W	“0” device always ON ”1” auto power shutdown active (Auto OFF)	0
CFG-7	SDO delay	R/W	“0” SDO half clock delay disabled “1” SDO half clock delay enabled	0
CFG-8	Gradual output delay	R/W	“0” gradual outputs delay is applied ”1” all channels switch ON and OFF simultaneously	0

Table 8. Configuration register (continued)

BIT	Definition	Attribute read/write	Configuration register function description					Default
CFG-9	Data flow	R/W	Color data flow management	CFG9	CFG10	CFG11		0
				0	0	0	RGB	
				0	0	1	GBR	
CFG-10				0	1	0	GRB	0
				0	1	1	BGR	
CFG-11				1	0	0	BRG	0
				1	0	1	RBG	
CFG 12 ÷ 23	Don't care							

8.3 Current ranges (CFG 0-CFG 2)

The output LED currents can be programmed using an external resistor connected to GND from the ISET pin and can be adjusted using 6 bits in a dedicated gain register with two possible current ranges selectable in the configuration register. Each range can be separately selected for each color by the bits CFG-0, CFG-1 and CFG-2, respectively, for the RED, GREEN and BLUE channels.

8.4 Error detection conditions (CFG 3-CFG 5)

During error detection phases for each channel, the following are checked:

- output current for open circuit detection
- output voltage for short-circuit detection

The thresholds for the error diagnostics are summarized in the *Table 9*:

Table 9. Diagnostic thresholds

Error detection	Checked malfunction	CFG-x(1)	Thresholds
Open detection combined mode	Open line or output short to GND	Don't care	Io < 0.5 x Io_programmed
Short detection	Short on LED or short to VLED	0	Vo > 2 V
		1	Vo > 3 V

1. x=3 for RED, x=4 for GREEN, x=5 for BLUE

8.5 Auto power shutdown / wakeup (CFG 6)

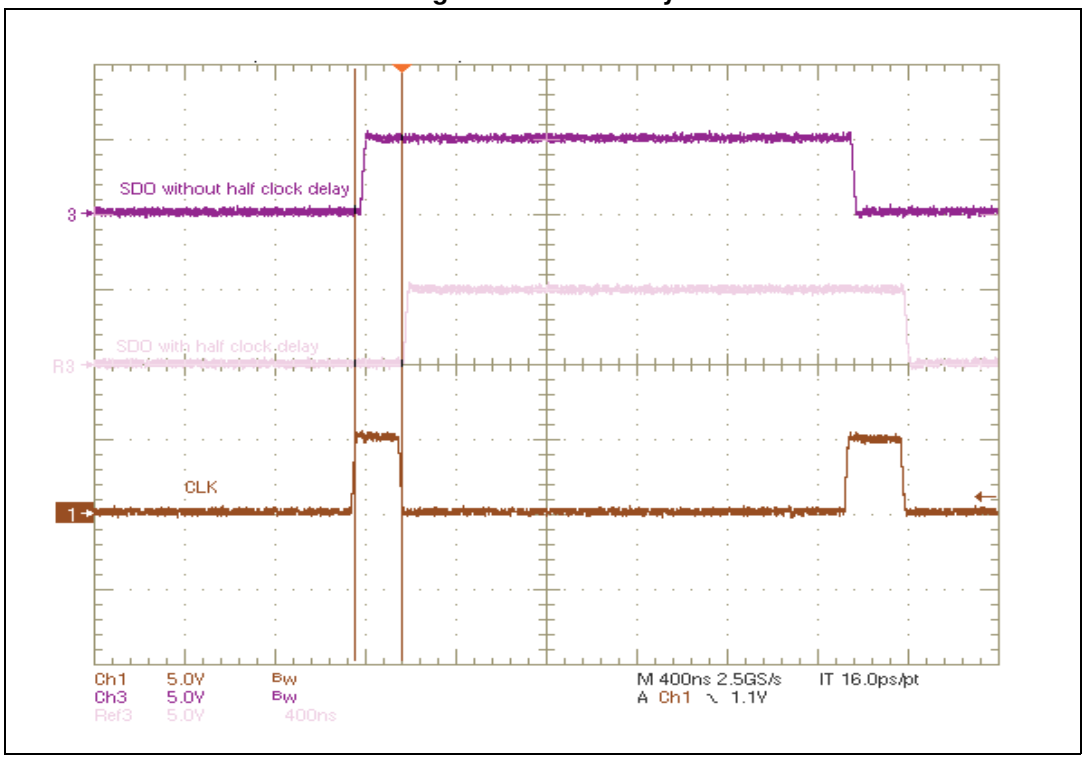
This feature reduces the power consumption when all outputs are OFF. It is active when the bit CFG-6 of the configuration register is at "1". The auto power shutdown (auto OFF) starts when the data latched is "0" for all channels, and the device will be active again (wakeup) at the first latched data string including at least one bit equal to "1" (at least one channel ON).

Timings for shutdown and wakeup are present in the dynamic features table. While the auto power shutdown is active, the device ignores any other command except channel power-on.

8.6 SDO delay (CFG 7)

Normally, on SDO terminals data is shifted out at the rising edge of the CLK signal with a propagation delay of about 15 ns [signal (1) in *Figure 11*]. The device provides the possibility to shift data out also at the falling edge of the CLK signal with a propagation delay of few ns [signal (2) in *Figure 11*]. This feature can be activated by setting to “1” the bit CFG-7 of the configuration register. The default setting for this bit is “0”, hence the SDO delay is not activated by default. This feature is particularly useful when multiple devices are connected in daisy chain configuration with non-matched delays between the CLK and SDO data paths (board routing).

Figure 11. SDO Delay



8.7 Gradual output delay (CFG 8)

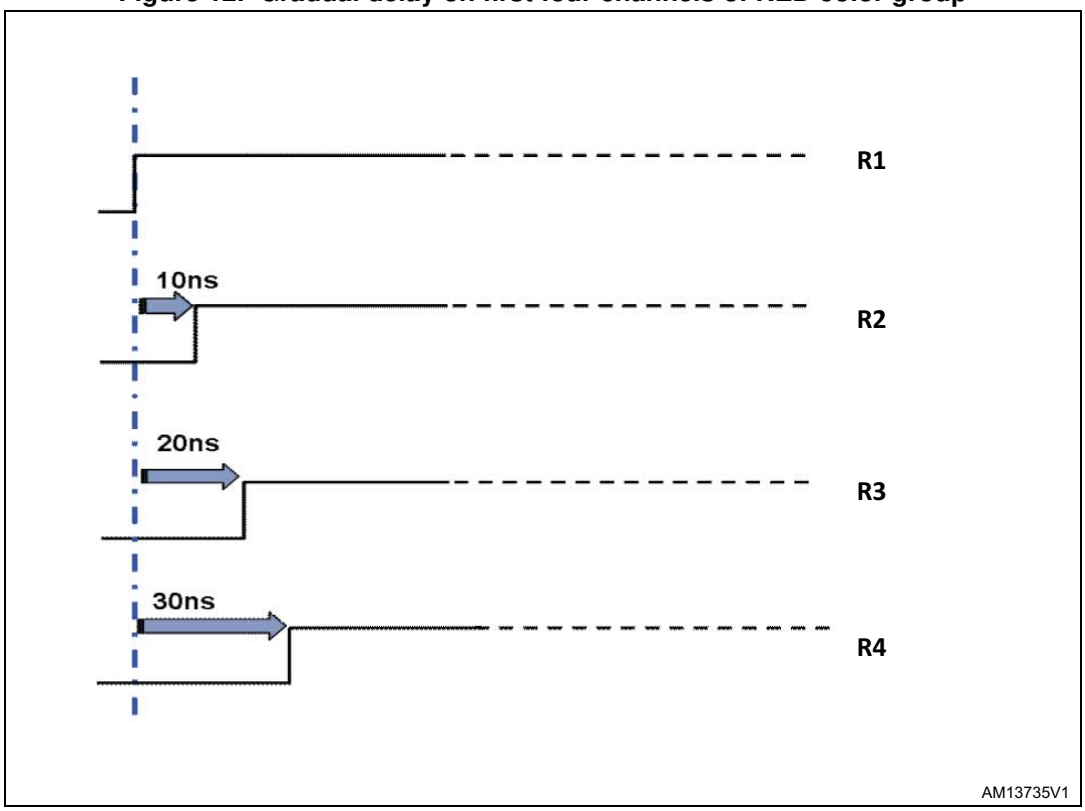
The gradual output delay consists in turning on gradually the current generators, avoiding turning on all channels at the same time. This feature prevents large inrush current and reduces the bypass capacitor values. The fixed delay time can be activated by bit CFG-8 of the configuration register, and the typical delay is 10 ns for each group of 8 outputs R, G, B (e.g. R1, G1, B1 has no delay, R2, G2, B2 has 10 ns of delay and R3, G3, B3, has 20 ns delay, and so on), as described in *Table 10*.

Table 10. Gradual output delay values

Delay time (ns) from the falling edge of $\overline{xOE}$	R1 G1 B1	R2 G2 B2	R3 G3 B3	R4 G4 B4	R5 G5 B5	R6 G6 B6	R7 G7 B7	R8 G8 B8
CFG-8 = “0”	0	10	20	30	40	50	60	70
CFG-8 = “1”	0	0	0	0	0	0	0	0

Figure 12 shows an example of the effect of the output gradual delay on the RED color group outputs.

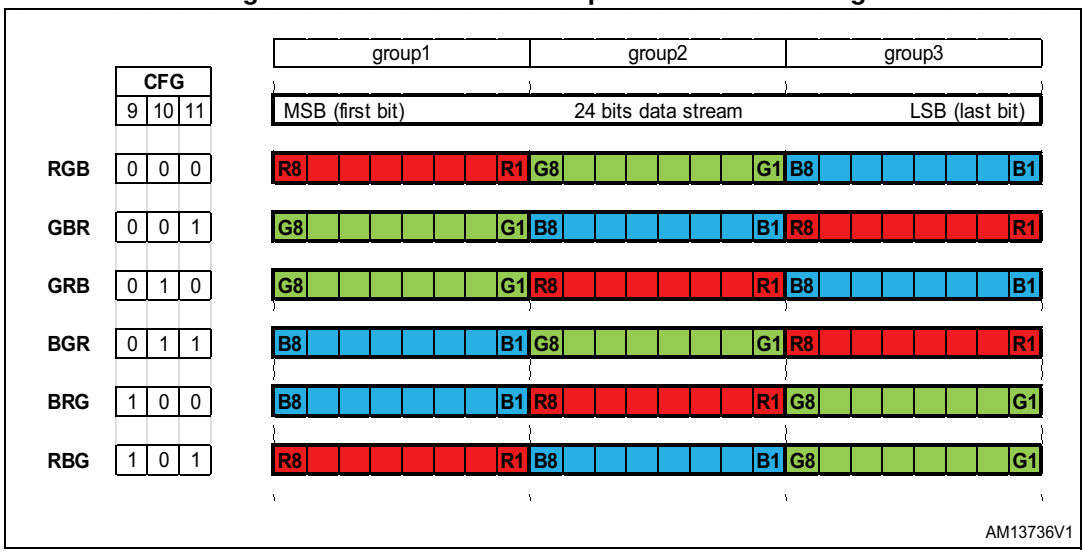
Figure 12. Gradual delay on first four channels of RED color group



8.8 Data flow management (CFG 9-CFG 11)

The 8x3 shift registers have a default RGB sequence serial data flow according to the table shown into the configuration register (bit CFG-9, CFG-10 and CFG-11). *Figure 13* shows how serial data are loaded in accordance with the data flow sequence selected through the configuration register. The default sequence is RGB (first bit will be R8, last bit B1 then: R8-R1, G8-G1, B8-B1).

Figure 13. Different color sequence in data loading



8.9 Gain register

The LED current can be programmed using an external resistor connected to GND from R-EXT pin and can be adjusted using the dedicated bits of the gain register (G-0 to G-17 defines the gain and CFG-0/1/2 the current range within the gain can be adjusted). The device can regulate the current up to 72 mA and down to 4 mA. To change anything in the gain register, a 24-bit digital word must be sent (CFG-0 represents the LSB, CFG-23 the MSB). The accuracy of the LED current depends on the selected range and it is assured only in the ranges indicated in the static electrical characteristics (see *Table 5*).

Table 11. Gain register

BIT	Definition	Attribute read/write	Register function description	Default
G-0	RED current gain adjustment	R/W	6-bit DAC allows adjustment of the device output current in 64 steps for each range (defined by CFG-0). default: gain = 1	1
G-1				1
G-2				1
G-3				1
G-4				1
G-5				1
G-6	GREEN current gain adjustment	R/W	6-bit DAC allows adjustment of the device output current in 64 steps for each range (defined by CFG-1). default: gain = 1	1
G-7				1
G-8				1
G-9				1
G-10				1
G-11				1

Table 11. Gain register (continued)

BIT	Definition	Attribute read/write	Register function description	Default
G-12	BLUE current gain adjustment	R/W	6-bit DAC allows adjustment of the device output current in 64 steps for each range (defined by CFG-2). default: gain = 1	1
G-13				1
G-14				1
G-15				1
G-16				1
G-17				1
G-18 to G-23	Don't care			

Figure 14. I_{out} vs. gain