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LED6000

3 A, 61 V monolithic current source with dimming capability

Datasheet - production data

HTSSOP16 (R_{TH} = 40 °C)

Features

- Up to 3 A DC output current
- 4.5 V to 61 V operating input voltage
- $R_{DS,ON}$ = 250 mΩ typ.
- Adjustable f_{SW} (250 kHz - 1.5 MHz)
- Dimming function with dedicated pin
- Low I_Q shutdown (10 µA typ. from VIN)
- Low I_Q operating (2.4 mA typ.)
- ± 3% output current accuracy
- Synchronization
- Enable with dedicated pin
- Adjustable soft-start time
- Adjustable current limitation
- Low dropout operation (12 µs max.)
- VBIAS improves efficiency at light-load
- Output voltage sequencing
- Auto recovery thermal shutdown
- MLCC output capacitor

Applications

- HB LED driving applications
- Halogen bulb replacement

Description

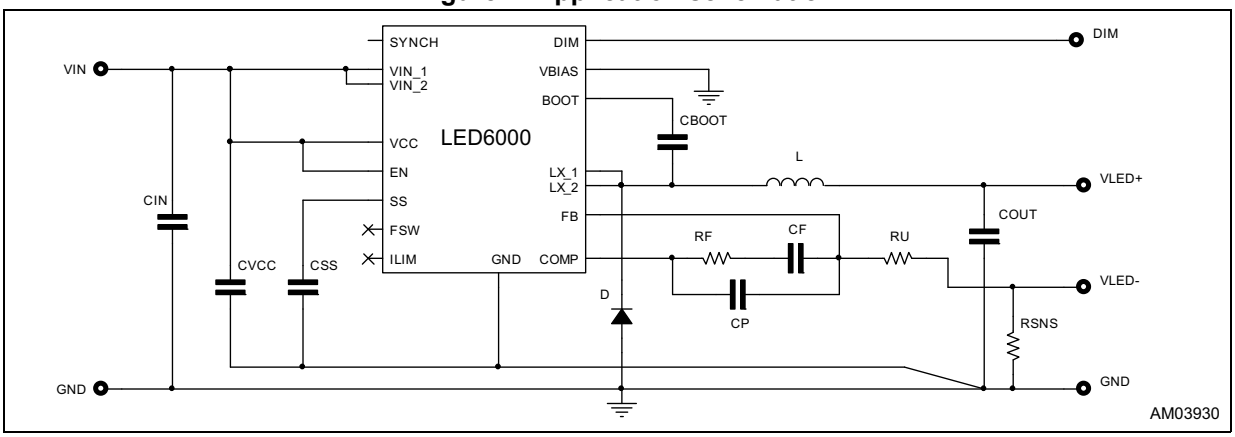
The LED6000 is a step-down monolithic switching regulator designed to source up to 3 A DC current for high power LED driving. The 250 mV typical RSENSE voltage drop enhances the efficiency. Digital dimming is implemented by driving the dedicated DIM pin.

The adjustable current limitation, designed to select the inductor RMS in accordance with the nominal output LED current, and the adjustability of the switching frequency allow the size of the application to be compact. The embedded switchover feature on the VBIAS pin maximizes efficiency. Multiple devices can be synchronized by sharing the SYNCH pin to prevent beating noise in low-noise applications, and to reduce the input current RMS value.

The device is fully protected against overheating, overcurrent and output short-circuit.

The LED6000 is available in an HTSSOP16 exposed pad package.

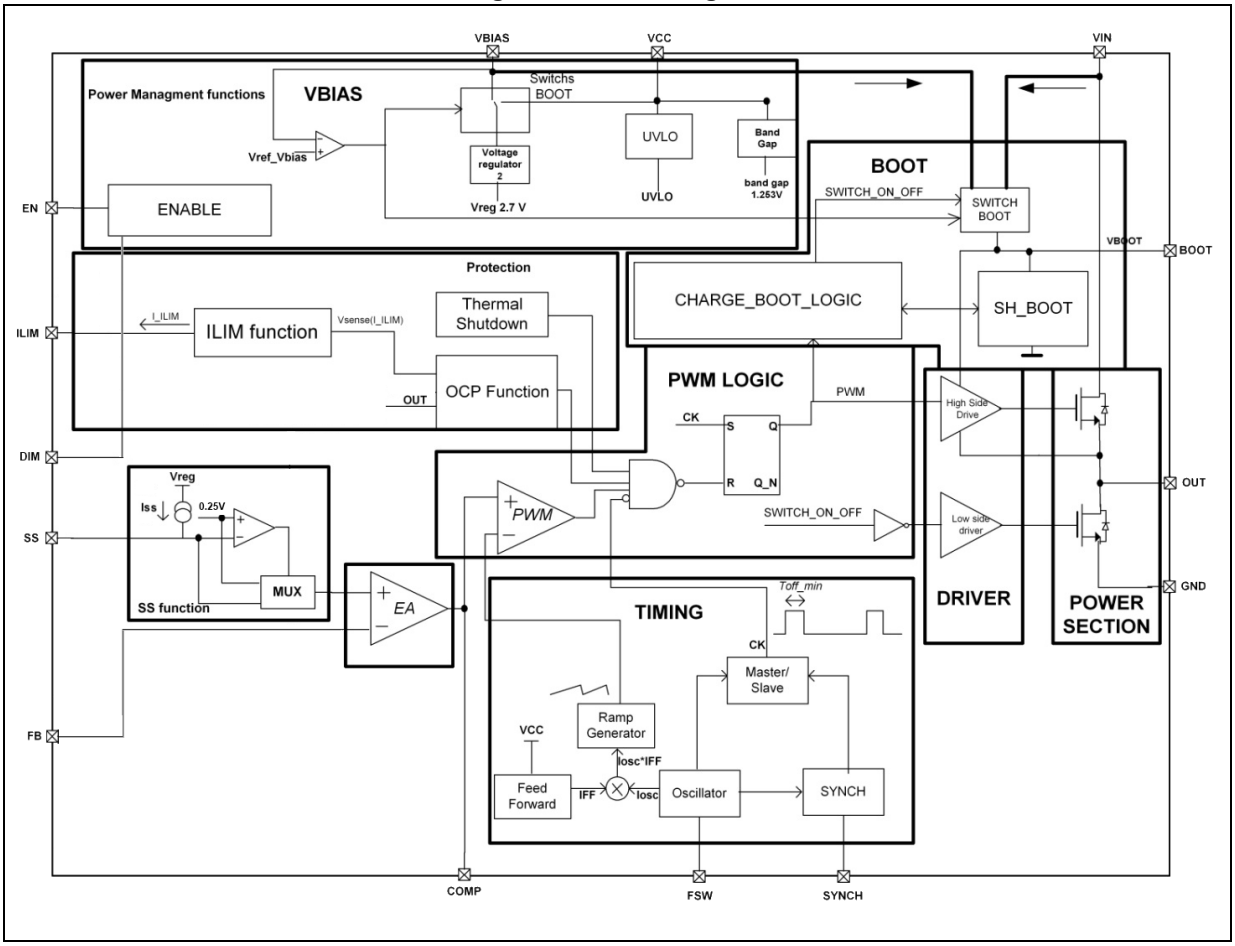
Figure 1. Application schematic



Contents

1 Block diagram

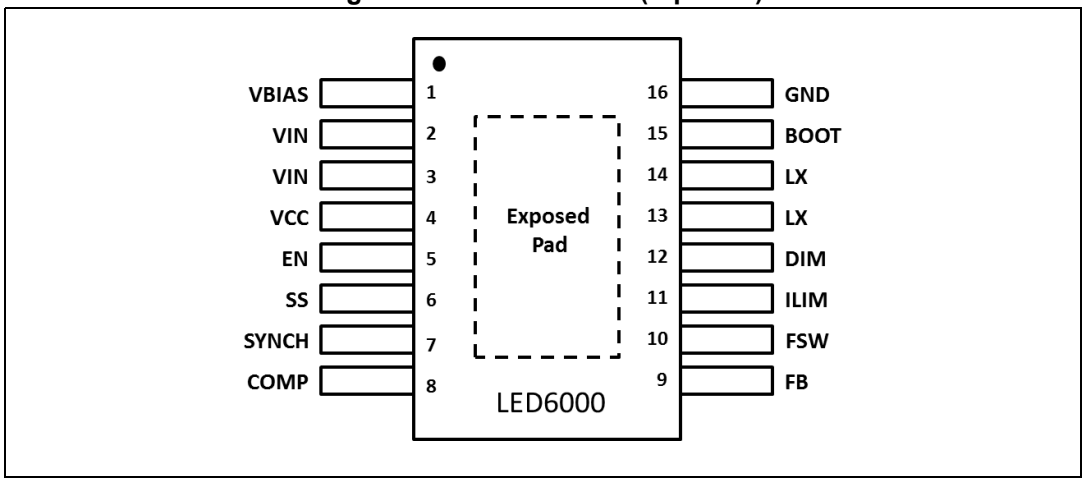
Figure 2. Block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	VBIAS	Auxiliary input that can be used to supply a part of the analog circuitry to increase the efficiency at the light-load. Connect to GND if not used or bypass with a 1 µF ceramic capacitor if supplied by an auxiliary rail.
2	VIN	DC input voltage
3	VIN	DC input voltage
4	VCC	Filtered DC input voltage to the internal circuitry. Bypass to the signal GND by a 1 µF ceramic capacitor.
5	EN	Active high enable pin. Connect to the VCC pin if not used.
6	SS	An internal current generator (5 µA typ.) charges the external capacitor to implement the soft-start.
7	SYNCH	Master / slave synchronization
8	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
9	FB	Inverting input of the error amplifier
10	FSW	A pull-down resistor to GND selects the switching frequency.
11	ILIM	A pull-down resistor to GND selects the peak current limitation.
12	DIM	A PWM signal in this input pin implements the LED PWM current dimming. It's pulled-down by an internal 2 µA current.
13	LX	Switching node
14	LX	Switching node
15	BOOT	Connect an external capacitor (100 nF typ.) between BOOT and LX pins. The gate charge required to drive the internal n-DMOS is recovered by an internal regulator during the off-time.
16	GND	Signal GND
--	E. P.	The exposed pad must be connected to the signal GND.

2.3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VIN		-0.3	61	V
VCC		-0.3	61	V
BOOT	V_{BOOT} - GND	-0.3	65	V
	V_{BOOT} - V_{LX}	-0.3	4	V
VBIAS		-0.3	VCC	V
EN		-0.3	VCC	V
DIM		-0.3	VCC	V
LX		-0.3	VIN + 0.3	V
SYNCH		-0.3	5.5	V
SS		-0.3	3.6	V
FSW		-0.3	3.6	V
COMP		-0.3	3.6	V
ILIM		-0.3	3.6	V
FB		-0.3	3.6	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C
I_{HS}	High-side RMS current		3	A

2.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board)	40	°C/W

2.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	CDM	500	V

3 Electrical characteristics

All the population tested at T_J = 25 °C, V_{IN} = V_{CC} = 24 V, VBIAS = GND, V_{DIM} = V_{EN} = 3 V and R_{ILIM} = N. M. unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		(1)	4.5		61	V
$R_{DSON\ HS}$	High-side RDSON	I_{LX} = 0.5 A			0.25	0.32	Ω
		I_{LX} = 0.5 A	(1)		0.25	0.42	Ω
f_{SW}	Switching frequency	FSW pin floating;		233	250	267	kHz
		FSW pin floating	(1)	225	250	275	kHz
	Selected switching frequency	R_{FSW} = 10 kΩ		1350	1500	1650	kHz
I_{PK}	Peak current limit	ILIM pin floating; V_{FB} = 0.2 V	(2)	3.5	4.1	4.7	A
	Selected peak current limit	R_{ILIM} = 100 kΩ; V_{FB} = 0.2 V	(2)	0.68	0.85	1.01	A
I_{SKIP}	Pulse skipping peak current	ILIM pin floating	(2)		0.40		A
		R_{ILIM} = 100 kΩ	(2)		0.15		A
T_{ONMIN}	Minimum on-time				120	150	ns
T_{ONMAX}	Maximum on-time	Refer to *Section 4: Functional description* for T_{ONMAX} details.			12		µs
T_{OFFMIN}	Minimum off-time		(3)		360		ns
VCC / VBIAS							
V_{CCH}	VCC UVLO rising threshold		(1)	3.85	4.10	4.30	V
V_{CCHYST}	VCC UVLO hysteresis		(1)	160	250	340	mV
SWO	VBIAS threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{BIAS} ramping up from 0 V.	(1)	2.82	2.90	2.98	V
		Hysteresis	(3)		80		mV
	VCC -VBIAS threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{IN} = V_{CC} = 24 V, V_{BIAS} falling from 24 V to GND.	(1)	3.35	4.05	4.90	V
		Hysteresis	(3)		750		mV
Power consumption							
I_{SHTDWN}	Shutdown current from VIN	V_{EN} = GND			10	15	µA
I_{QUIESC}	Quiescent current from VIN and VCC	LX floating, V_{FB} = 1 V, VBIAS = GND, FSW floating.			2.4	3.4	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
I_{QOPVIN}	Quiescent current from VIN and VCC	LX floating, V_{FB} = 1 V, VBIAS = 3.3 V, FSW floating			0.9	1.4	mA
$I_{QOPVBIAS}$	Quiescent current from VBIAS				1.5	2.4	mA
Enable							
V_{ENL}	Device OFF level			0.06		0.30	V
V_{ENH}	Device ON level			0.35		0.90	V
Soft-start							
$T_{SSSETUP}$	Soft-start setup time	Delay from UVLO rising to switching activity	(3)		640		µs
I_{SSCH}	C_{SS} charging current	V_{SS} = GND		4.3	5.0	5.7	µA
Error amplifier							
V_{FB}	Voltage feedback			0.242	0.250	0.258	V
			(1)	0.240	0.250	0.260	V
V_{COMPH}		V_{FB} = GND; V_{SS} = 3.2 V		3.20	3.35	3.50	V
V_{COMPL}		V_{FB} = 3.2 V; V_{SS} = 3.2 V				0.1	V
I_{FB}	FB biasing current	V_{FB} = 3.6 V			5	50	nA
$I_{OSOURCE}$		V_{FB} = GND; SS pin floating; V_{COMP} = 2 V	(3)		3.1		mA
I_{OSINK}	Output stage sinking capability	Unity gain buffer configuration (FB connected to COMP). No load on COMP pin.	(3)		5		mA
A_{V0}	Error amplifier gain		(3)		100		dB
GBWP		Unity gain buffer configuration (FB connected to COMP). No load on COMP pin.	(3)		23		MHz
Synchronization (fan out: 5 slave devices max.)							
$f_{SYN\ MIN}$	Synchronization frequency	Pin FSW floating		280			kHz
V_{SYNOUT}	Master output amplitude	I_{LOAD} = 4 mA		2.45			V
		I_{LOAD} = 0 A; pin SYNCH floating				3.8	
V_{SYNOW}	Output pulse width	I_{LOAD} = 0 A; pin SYNCH floating		150	215	280	ns
V_{SYNIH}	SYNCH slave high level input threshold			2.0			V
V_{SYNIL}	SYNCH slave low level input threshold					1.0	
I_{SYN}	Slave SYNCH pull-down current	V_{SYNCH} = 5 V		450	700	950	µA
V_{SYNIW}	Input pulse width			150			ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Dimming							
V_{DIMH}	DIM rising threshold				1.23	1.7	V
V_{DIML}	DIM falling threshold			0.75	1.00		V
V_{DIMPD}	DIM pull-down current	V_{DIM} = 2 V		0.5	1.5	2.5	µA
T_{DIMTO}	Dimming timeout		(3)		42		ms
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(3)		170		°C
T_{HYS}	Thermal shutdown hysteresis		(3)		15		°C

1. Specifications referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
3. Not tested in production.

4 Functional description

The LED6000 device is based on a voltage mode, constant frequency control loop. The LEDs current, monitored through the voltage drop on the external current sensing resistor, RSNS, is compared to an internal reference (0.25 V) providing an error signal on the COMP pin. The COMP voltage level is then compared to a fixed frequency sawtooth ramp, which finally controls the on- and off-time of the power switch.

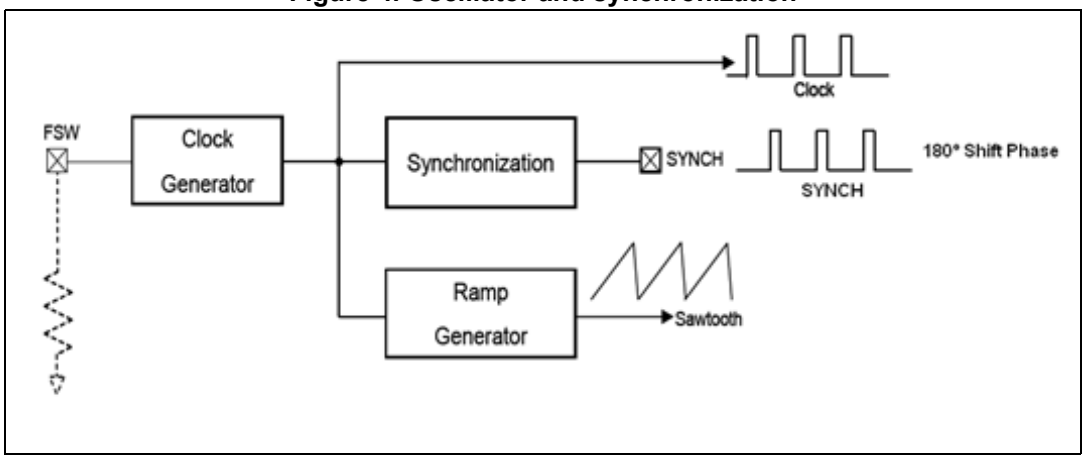
The main internal blocks are shown in *Figure 2: Block diagram on page 4* and can be summarized as follow.

- The fully integrated oscillator that provides the sawtooth ramp to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The input voltage feedforward is implemented.
- The soft-start circuitry to limit the inrush current during the startup phase.
- The voltage mode error amplifier.
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch.
- The high-side driver for the embedded N-channel power MOSFET switch and bootstrap circuitry. A dedicated high resistance low-side MOSFET, for anti-boot discharge management purposes, is also present.
- The peak current limit sensing block, with a programmable threshold, to handle the overload including a thermal shutdown block, to prevent the thermal runaway.
- The bias circuitry, which includes a voltage regulator and an internal reference, to supply the internal circuitry and provide a fixed internal reference and manages the current dimming feature. The switchover function from VCC to VBIAS can be implemented for higher efficiency. This block also implements voltage monitor circuitry (UVLO) that checks the input and internal voltages.

4.1 Oscillator and synchronization

Figure 4 shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock, whose frequency depends on the resistor externally connected between the FSW pin and ground.

Figure 4. Oscillator and synchronization

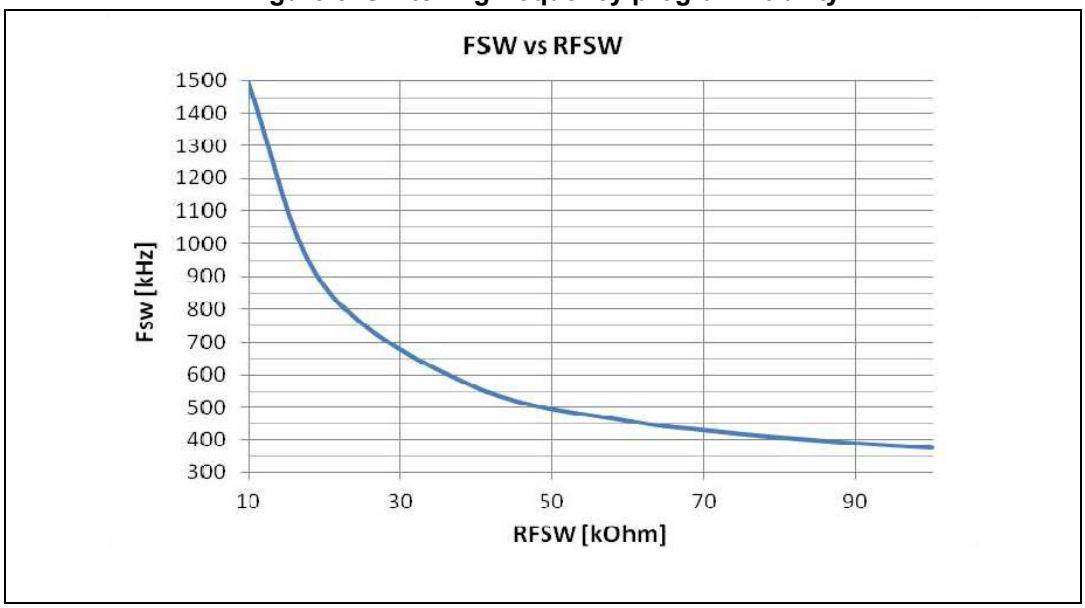


If the FSW pin is left floating, the programmed frequency is 250 kHz (typ.); if the FSW pin is connected to an external resistor, the programmed switching frequency can be increased up to 1.5 MHz, as shown in *Figure 5*. The required R_{FSW} value (expressed in kΩ) is estimated by *Equation 1*:

Equation 1

$$F_{SW} = 250kHz + \frac{12500}{R_{FSW}}$$

Figure 5. Switching frequency programmability



To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the input voltage feedforward is implemented by changing the slope of the sawtooth ramp, according to the input voltage change (*Figure 6* a).

The slope of the sawtooth also changes if the oscillator frequency is programmed by the external resistor. In this way a frequency feedforward is implemented (*Figure 6* b) in order to keep the PWM modulator gain constant versus the switching frequency.

On the SYNCH pin the synchronization signal is generated. This signal has a phase shift of 180° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pins together. When SYNCH pins are connected, the device with a higher oscillator frequency works as a master, so the slave device switches at the frequency of the master but with a delay of half a period. This helps reducing the RMS current flowing through the input capacitor. Up to five LED6000s can be connected to the same SYNCH pin; however, the clock phase shift from master switching frequency to the slave input clock is 180°.

The LED6000 device can be synchronized to work at a higher frequency, in the range of 250 kHz - 1500 kHz, providing an external clock signal on the SYNCH pin. The synchronization changes the sawtooth amplitude, also affecting the PWM gain (*Figure 6* c). This change must be taken into account when the loop stability is studied. In order to

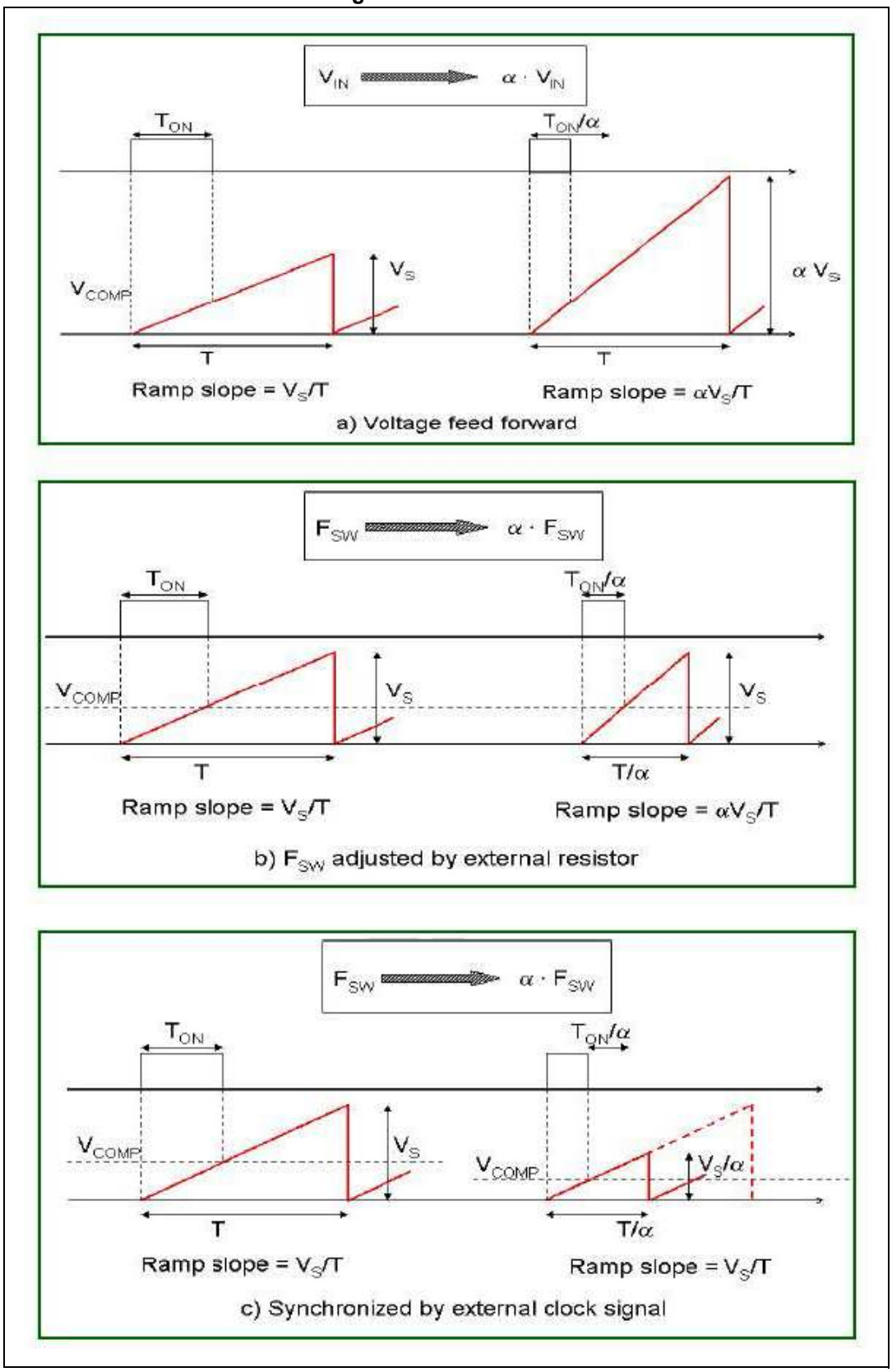
minimize the change of the PWM gain, the free-running frequency should be set (with a resistor on the FSW pin) only slightly lower than the external clock frequency.

This pre-adjusting of the slave IC switching frequency keeps the truncation of the ramp sawtooth negligible.

In case two or more (up to five) LED6000 SYNCH pins are tied together, the LED6000 IC with higher programmed switching frequency is typically the master device; however, the SYNCH circuit is also able to synchronize with a slightly lower external frequency, so the frequency pre-adjustment with the same resistor on the FSW pin, as suggested above, is required for a proper operation.

The SYNCH signal is provided as soon as EN is asserted high; however, if DIM is kept low for more than T_{DIMTO} timeout, the SYNCH signal is no more available until DIM re-assertion high.

Figure 6. Feedforward

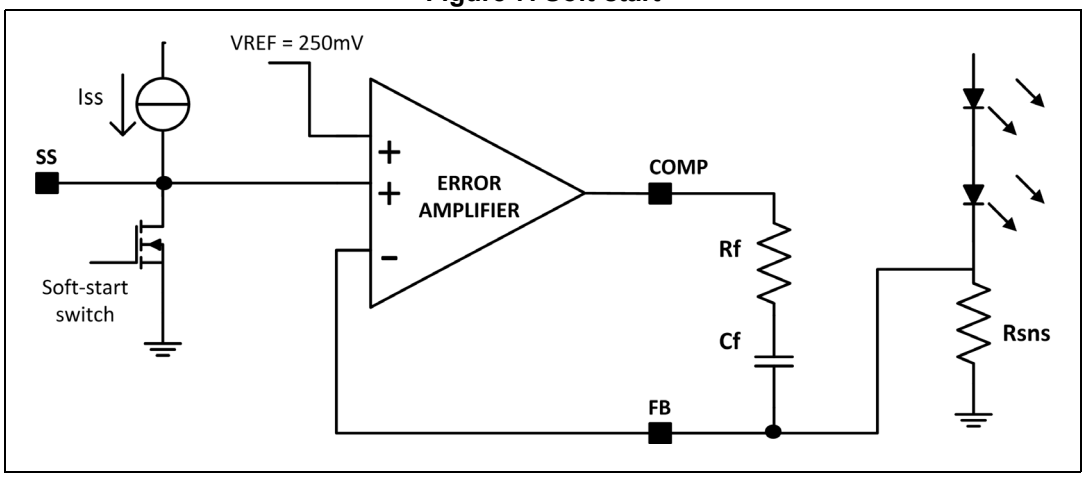


4.2 Soft-start

The soft-start is essential to assure a correct and safe startup of the step-down converter. It avoids an inrush current surge and makes the output voltage to increase monotonically.

The soft-start is performed as soon as the EN and DIM pin are asserted high; when this occurs, an external capacitor, connected between the SS pin and ground, is charged by a constant current (5 µA typ.). The SS voltage is used as reference of the switching regulator and the output voltage of the converter tracks the ramp of the SS voltage. When the SS pin voltage reaches the 0.25 V level, the error amplifier switches to the internal 0.25 V reference to regulate the output voltage.

Figure 7. Soft-start



During the soft-start period the current limit is set to the nominal value.

The dV_{SS}/dt slope is programmed in agreement with *Equation 2*:

Equation 2

$$C_{SS} = \frac{I_{SS} \cdot T_{SS}}{V_{REF}} = \frac{5\mu A \cdot T_{SS}}{0.25V}$$

Before starting the C_{SS} capacitor charge, the soft-start circuitry turns-on the discharge switch shown in *Figure 7* for $T_{SSDISCH}$ minimum time, in order to completely discharge the C_{SS} capacitor.

As a consequence, the maximum value for the soft-start capacitor, which assures an almost complete discharge in case of the EN signal toggle, is provided by:

Equation 3

$$C_{SS\_MAX} \leq \frac{T_{SSDISCH}}{5 \cdot R_{SSDISCH}} \cong 270nF$$

given $T_{SSDISCH}$ = 530 µs and $R_{SSDISCH}$ = 380 Ω typical values.

The enable feature allows to put the device into the standby mode. With the EN pin lower than V_{ENL} the device is disabled and the power consumption is reduced to 10 µA (typ.). If the EN pin is higher than V_{ENH}, the device is enabled. If the EN pin is left floating, an internal pull-down current ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also VCC compatible.

4.3 Digital dimming

The switching activity is inhibited as long as the DIM pin is kept below the V_{DIML} threshold.

When the DIM is asserted low, the HS MOS is turned-off as soon as the minimum on-time is expired and the COMP pin is parked close to the maximum ramp peak value, in order to limit the input inrush current when the IC restarts the switching activity. The internal oscillator and, consequently, the IC quiescent current are reduced only if the DIM is kept low for more than T_{DIMTO} timeout.

The inductor current dynamic performance, when dimming input goes high, depends on the designed system response. The best dimming performance is obtained by maximizing the bandwidth and phase margin, when possible.

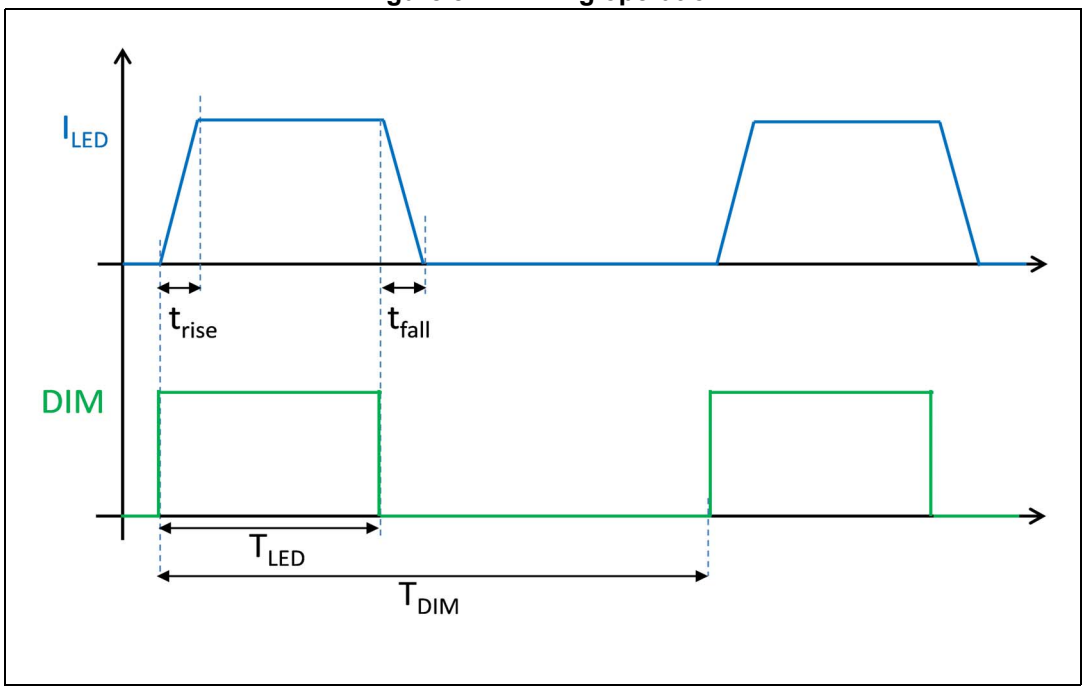
As a general rule, the output capacitor minimization improves dimming performance in terms of the shorter LEDs current rising time and reduced inductor peak current.

An oversized output capacitor value requires an extra current for the fast charge so generating an inductor current overshoot and oscillations.

Refer also to *Section 5.2 on page 25* for output capacitor design hints.

The dimming performance depends on the current pulse shape specification of the final application.

Figure 8. Dimming operation



The ideal current pulse has rectangular shape; however, in any case it degenerates into a trapezoid or, at worst, into a triangle, depending on the ratio (t_{RISE} + t_{FALL})/ T_{LED}.

Figure 9. Dimming operation (rising edge) - VIN = 44 V, 12 LED

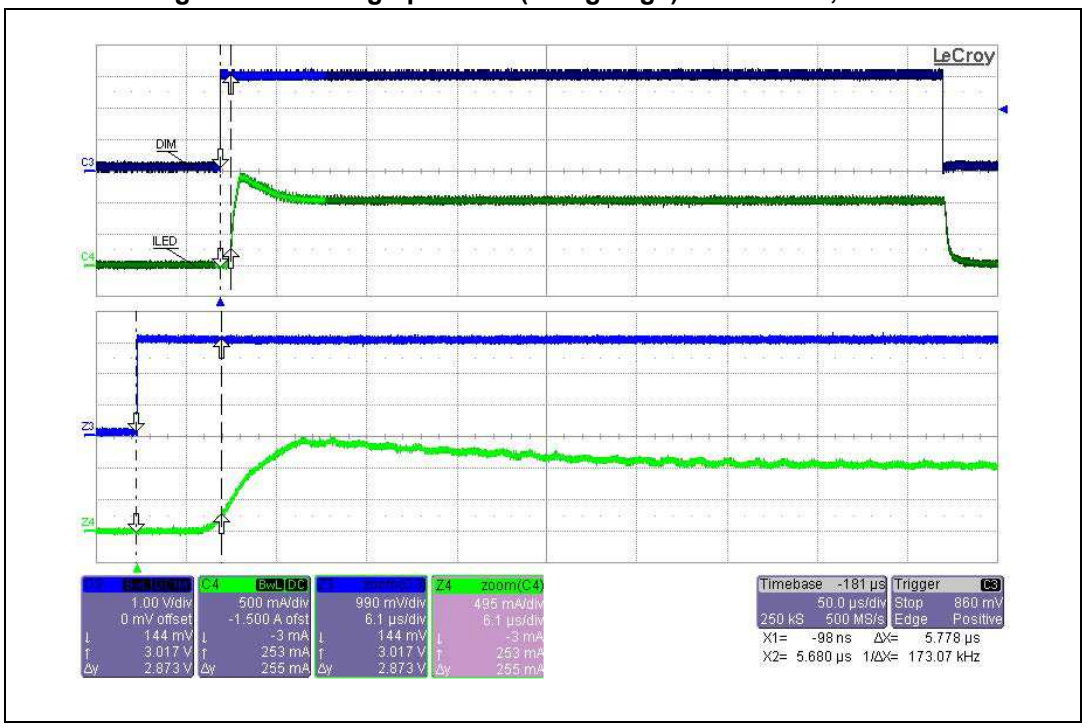
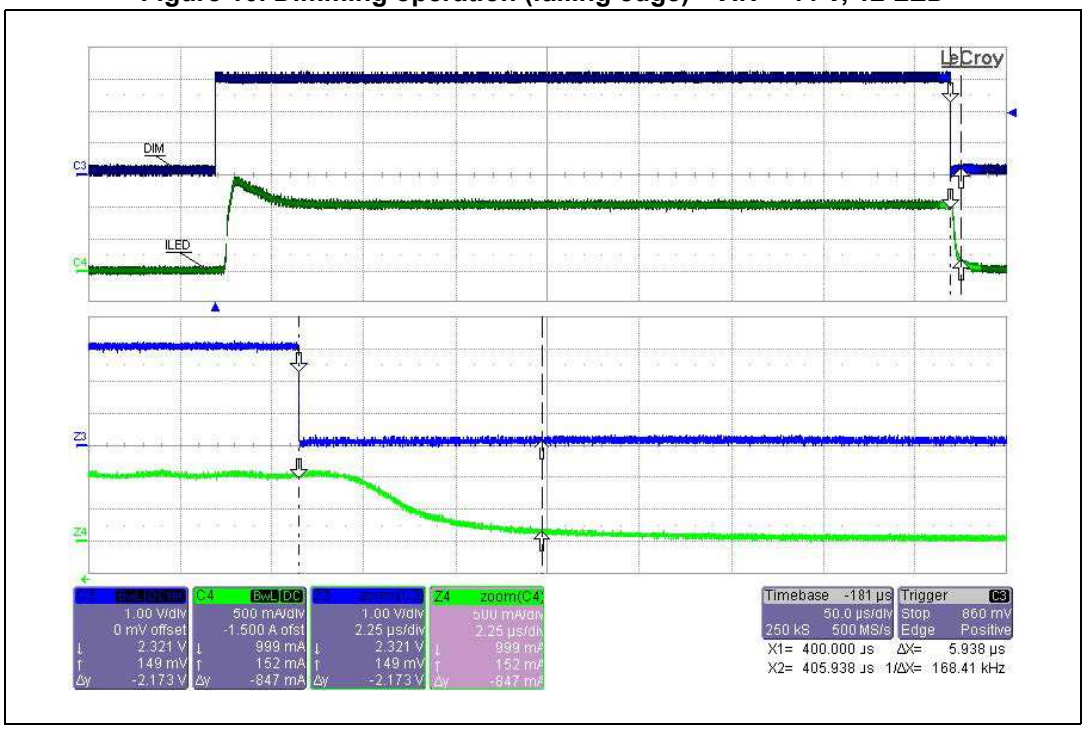
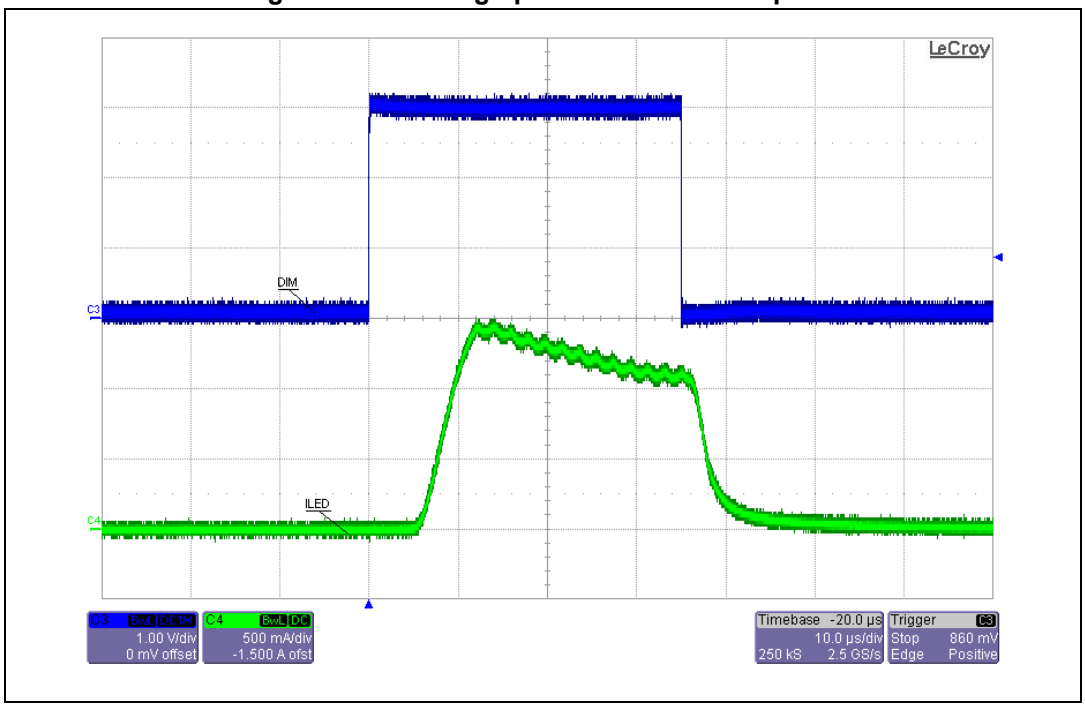


Figure 10. Dimming operation (falling edge) - VIN = 44 V, 12 LED



In *Figure 11* a very short DIM pulse is shown, measured in the standard demonstration board, V_{IN} = 44 V, 12 LEDs. The programmed LED current, 1 A, is reached at the end of the DIM pulse (35 µs).

Figure 11. Dimming operation - short DIM pulse



The above consideration is crucial when short DIM pulses are expected in the final application. Once the external power components and the compensation network are selected, a direct measurement to determine t_{RISE} and t_{FALL} is necessary to certify the achieved dimming performance.

When the DIM is forced above the V_{DIMH} threshold after T_{DIMTO} has elapsed, a new soft-start sequence is performed.

4.4 Error amplifier and light-load management

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non-inverting input is internally connected to a 0.25 V voltage reference and its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier, therefore, with the high DC gain and low output impedance.

The uncompensated error amplifier characteristics are summarized in *Table 6*.

Table 6. Error amplifier characteristics

Parameters	Value
Low frequency gain (A_0)	100 dB
GBWP	23 MHz
Output voltage swing	0 to 3.5 V
Source/sink current capability	3.1 mA / 5 mA

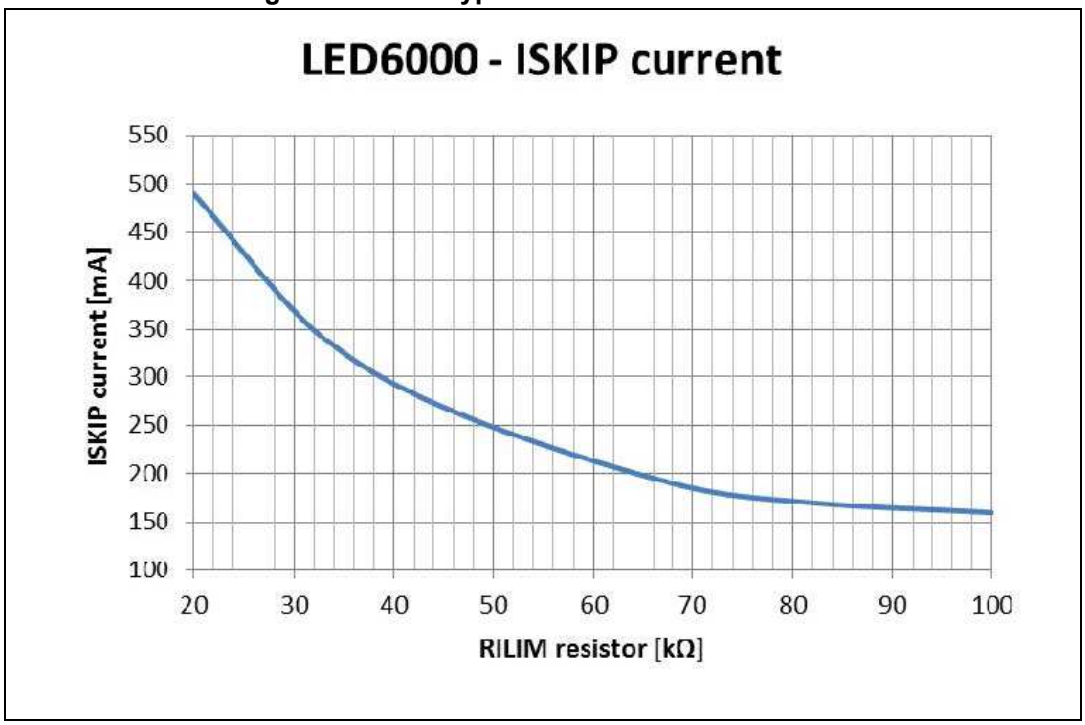
In the continuous conduction working mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor.

If the zero introduced by the output capacitor helps to compensate the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see *Section 5.3 on page 27* for details on the compensation network design).

In case of the light-load (i.e.: if the output current is lower than the half of the inductor current ripple) the LED6000 enters the pulse-skipping working mode. The HS MOS is kept off if the COMP level is below 200 mV (typ.); when this bottom level is reached the integrated switch is turned on until the inductor current reaches I_{SKIP} value. So, in the discontinuous conduction working mode (DCM), the HS MOS on-time is only related to the time necessary to charge the inductor up to the I_{SKIP} level.

The I_{SKIP} threshold is reduced with increasing the RILIM resistor value, as shown also in *Table 5 on page 8* and plotted in *Figure 12*, so allowing the LED6000 device work in the continuous conduction mode also in case lower current LEDs are selected.

Figure 12. ISKIP typical current and RILIM value



However, due to the current sensing comparator delay, the actual inductor charge current is slightly impacted by the V_{IN} and selected inductor value.

In order to let the bootstrap capacitor recharge, in case of an extremely light-load the LED6000 is able to pull-down the LX net through an integrated small LS MOS. In this way the bootstrap recharge current can flow from the V_{IN} through the C_{BOOT}, LX and LS MOS.

This mechanism is activated if the HS MOS has been kept turned-off for more than 3 ms (typ.).

4.5 Low VIN operation

In normal operation (i.e.: VOUT programmed lower than input voltage) when the HS MOS is turned off, a minimum off time (T_{OFFMIN}) interval is performed.

In case the input voltage falls close or below the programmed output voltage (low dropout, LDO) the LED6000 control loop is able to increase the duty cycle up to 100%. However, in order to keep the boot capacitor properly recharged, a maximum HS MOS on-time is limited (T_{ONMAX}). When this limit is reached the HS MOS is turned-off and an integrated switch working as a pull-down resistor between the LX and GND is turned on, until one of the following conditions is met:

- A negative current limit (300 mA typ.) is reached
- A timeout (1 µs typ.) is reached.

So doing the LED6000 device is able to work in the low dropout operation, due to the advanced boot capacitor management, and the effective maximum duty cycle is about 12 µs / 13 µs = 92%.

4.6 Overcurrent protection

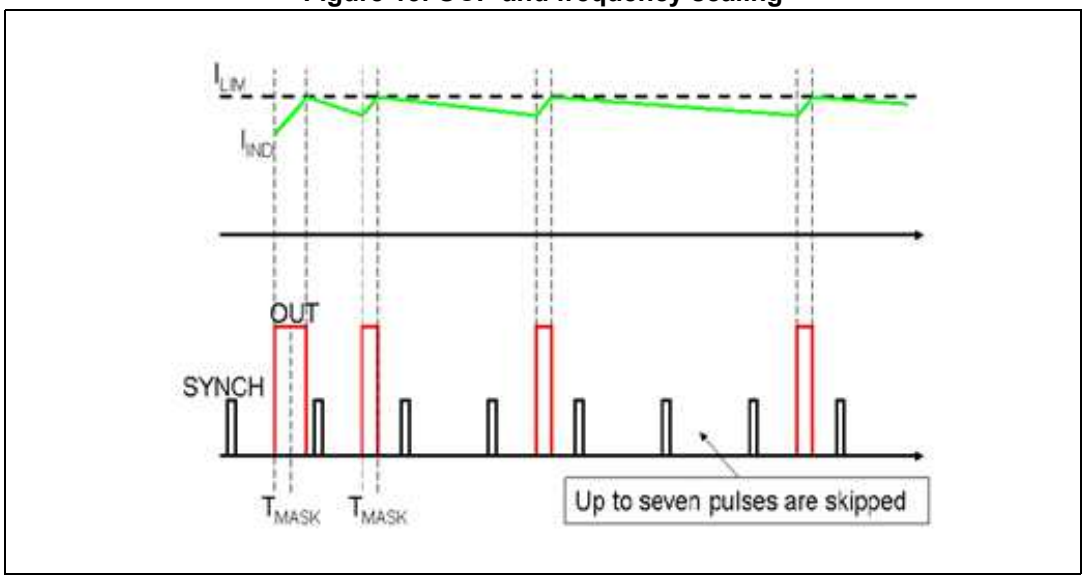
The LED6000 implements overcurrent protection by sensing the current flowing through the power MOSFET. Due to the noise created by the switching activity of the power MOSFET, the current sensing circuitry is disabled during the initial phase of the conduction time. This avoids erroneous detection of fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is about 120 ns.

If the overcurrent limit is reached, the power MOSFET is turned off implementing pulse by pulse overcurrent protection. In the overcurrent condition, the device can skip turn-on pulses in order to keep the output current constant and equal to the current limit. If, at the end of the “masking time”, the current is higher than the overcurrent threshold, the power MOSFET is turned off and one pulse is skipped. If, at the following switching on, when the “masking time” ends, the current is still higher than the overcurrent threshold, the device skips two pulses. This mechanism is repeated and the device can skip up to seven pulses (refer to *Figure 13*).

If at the end of the “masking time” the current is lower than the overcurrent threshold, the number of skipped cycles is decreased by one unit.

As a consequence, the overcurrent protection acts by turning off the power MOSFET and reducing the switching frequency down to one eighth of the default switching frequency, in order to keep constant the output current close to the current limit.

Figure 13. OCP and frequency scaling



This kind of overcurrent protection is effective if the inductor can be completely discharged during HS MOS turn-off time, in order to avoid the inductor current to run away. In case of the output short-circuit the maximum switching frequency can be computed by the following equation:

Equation 4

$$F_{SW,MAX} \leq \frac{8 \cdot \left(V_F + R_{DCR} \cdot I_{LIM}\right)}{V_{IN} - \left(R_{ON} + R_{DCR}\right) \cdot I_{LIM}} \cdot \frac{1}{T_{ON,MIN}}$$

Assuming V_F = 0.6 V the free-wheeling diode direct voltage, R_{DCR} = 30 mΩ inductor parasitic resistance, $I_{LIM} = I_{PK}$ = 4 A the peak current limit, R_{ON} = 0.25 Ω HS MOS resistance and $T_{ON,MIN}$ = 120 ns minimum HS MOS on duration, the maximum F_{SW} frequency which avoids the inductor current runaway in case of the output short-circuit and VIN = 61 V is 801 kHz.

If the programmed switching frequency is higher than the above computed limit, an estimation of the inductor current in case of the output short-circuit fault is provided by *Equation 5*:

Equation 5

$$I_{LIM} = \frac{F_{SW} \cdot T_{ON} \cdot V_{IN} - 8 \cdot V_F}{8 \cdot R_{DCR} + F_{SW} \cdot T_{ON,MIN}\left(R_{ON} + R_{DCR}\right)}$$

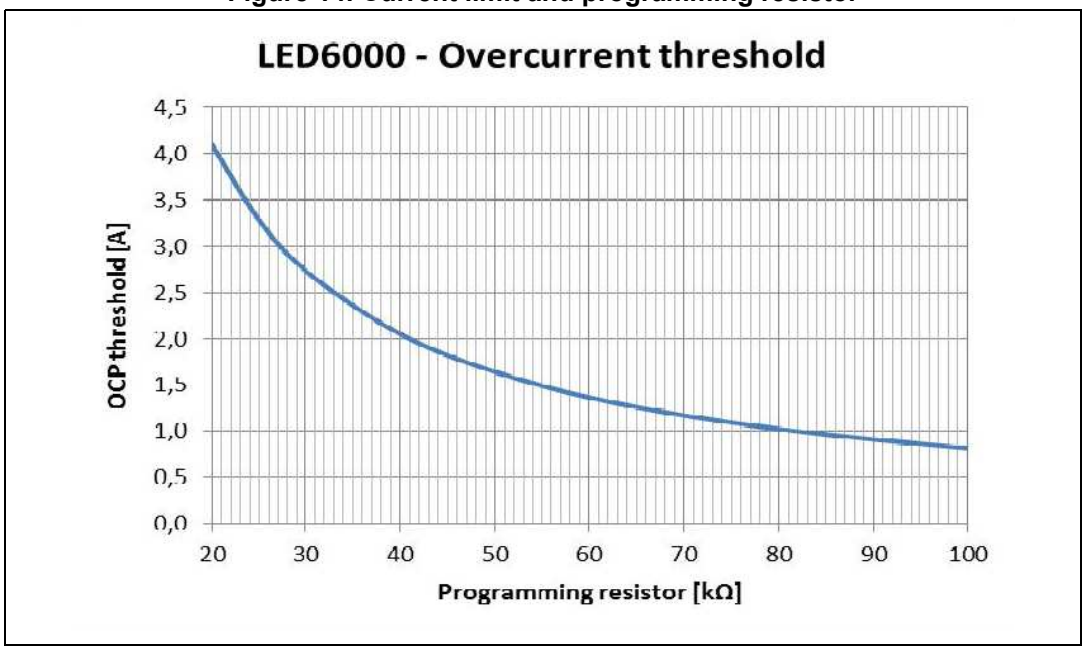
The peak current limit threshold (I_{LIM}) can be programmed in the range 0.85 A - 4.0 A by selecting the proper R_{ILIM} resistor, as suggested in *Equation 6*.

Equation 6

$$R_{ILIM} = 20k\Omega \cdot \frac{I_{PK}}{I_{LIM}}$$

I_{PK} is the default LED6000 current limit in case of R_{ILIM} not mounted, as shown in *Table 5 on page 8*.

Figure 14. Current limit and programming resistor



4.7 Overtemperature protection

It is recommended that the device never exceeds the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated by the integrated power MOSFET.

To avoid any damage to the device when reaching high temperature, the LED6000 implements a thermal shutdown feature: when the junction temperature reaches 170 °C (typ.) the device turns off the power MOSFET and shuts-down.

When the junction temperature drops to 155 °C (typ.), the device restarts with a new soft-start sequence.

5 Application notes - step-down conversion

5.1 Input capacitor selection

The input capacitor must be rated for the maximum input operating voltage and the maximum RMS input current.

Since the step-down converters input current is a sequence of pulses from 0A to I_{OUT}, the input capacitor must absorb the equivalent RMS current which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The RMS input current (flowing through the input capacitor) in step-down conversion is roughly estimated by:

Equation 7

$$I_{CIN,RMS} \cong I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The actual DC/DC conversion duty cycle, $D = V_{OUT}/V_{IN}$, is influenced by a few parameters:

Equation 8

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{IN,MIN} - V_{SW,MAX}}$$

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{IN,MAX} - V_{SW,MIN}}$$

where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal high-side MOSFET. Considering the range D_{MIN} to D_{MAX} it is possible to determine the maximum $I_{CIN,RMS}$ flowing through the input capacitor.

The input capacitor value must be dimensioned to safely handle the input RMS current and to limit the VIN and VCC ramp-up slew rate to 0.5 V/µs maximum, in order to avoid the device active ESD protections turn-on.

Different capacitors can be considered:

- **Electrolytic capacitors**

These are the most commonly used due to their low cost and wide range of operative voltage. The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

- **Ceramic capacitors**

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is their high cost.

- **Tantalum capacitor**

Small, good quality tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to a very high current, for example when they are connected to the power supply.

The amount of the input voltage ripple can be roughly overestimated by *Equation 9*.

Equation 9

$$V_{IN,PP} = \frac{D \cdot (1 - D) \cdot I_{OUT}}{C_{IN} \cdot F_{SW}} + R_{ES,IN} \cdot I_{OUT}$$

In case of MLCC ceramic input capacitors, the equivalent series resistance ($R_{ES,IN}$) is negligible.

In addition to the above considerations, a ceramic capacitor with an appropriate voltage rating and with a value 1 µF or higher should always be placed across VIN and power ground and across VCC and the IC GND pins, as close as possible to the LED6000 device. This solution is necessary for spike filtering purposes.

5.2 Output capacitor and inductor selection

The output capacitor is very important in order to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required.

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The allowed LED current ripple ($\Delta I_{LED,PP}$) is typically from 2% to 5% of the LED DC current.