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LED7706

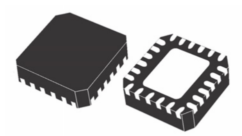
6-rows 30 mA LEDs driver with boost regulator for LCD panels backlight

Features

- Boost section
  - 4.5 V to 36 V input voltage range
  - Internal power MOSFET
  - Internal +5 V LDO for device supply
  - Up to 36 V output voltage
  - Constant frequency peak current-mode control
  - 250 kHz to 1 MHz adjustable switching frequency
  - External synchronization for multi-device application
  - Pulse-skip power saving mode at light load
  - Programmable soft-start
  - Programmable OVP protection
  - Stable with ceramic output capacitors
  - Thermal shutdown
- Backlight driver section
  - Six rows with 30 mA maximum current capability (adjustable)
  - Rows disable option
  - Less than 500 ns minimum dimming on-time (1 % minimum dimming duty-cycle at 20 kHz)
  - ±2 % current matching between rows
  - LED failure (open and short-circuit) detection

Applications

- LCD monitors and TV panels
- PDAs panel backlight
- GPS panel backlight



VFQFPN-24 4x4

Description

The LED7706 consists of a high efficiency monolithic boost converter and six controlled current generators (rows) specifically designed to supply LEDs arrays used in the backlighting of LCD panels. The device can manage an output voltage up to 36 V (i.e. 10 white LEDs per row).

The generators can be externally programmed to sink up to 30 mA and can be dimmed via a PWM signal (1 % dimming duty-cycle at 20 kHz can be managed). The device allows to detect and manage the open and shorted LED faults and to let unused rows floating. Basic protections (output over-voltage, internal MOSFET over-current and thermal shutdown) are provided.

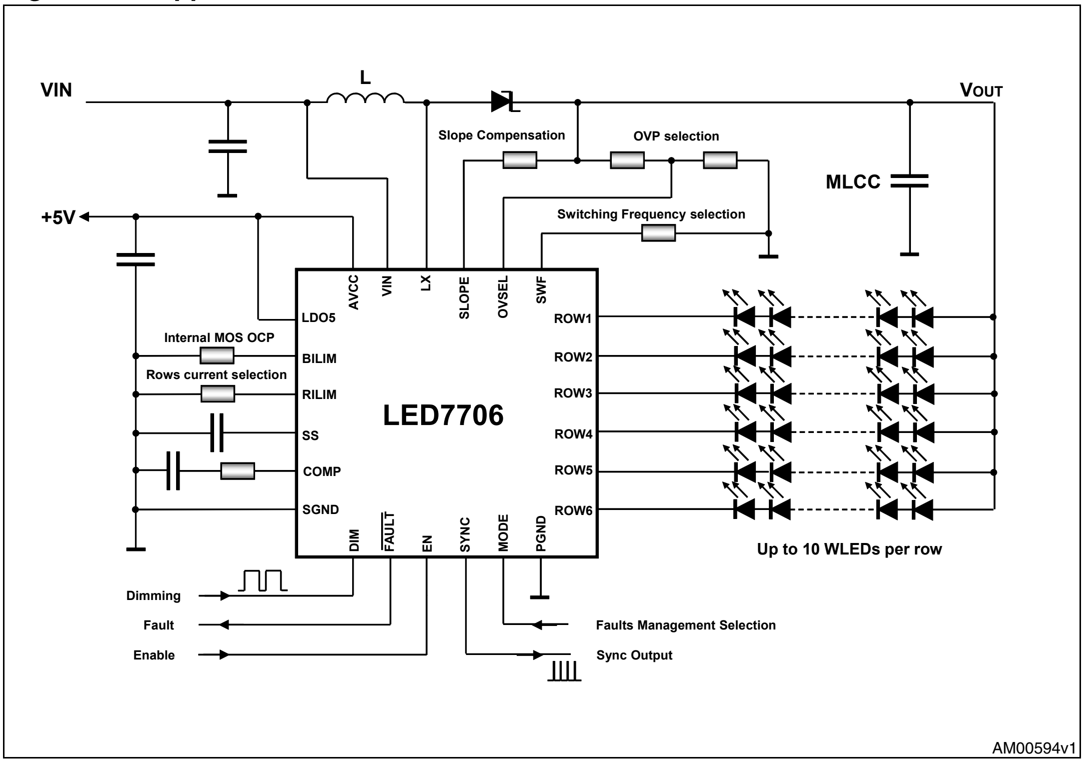
Table 1. Device summary

Order codes	Package	Packaging
LED7706	VFQFPN-24 4x4 (exposed pad)	Tube
LED7706TR		Tape and reel

Contents

1 Typical application circuit

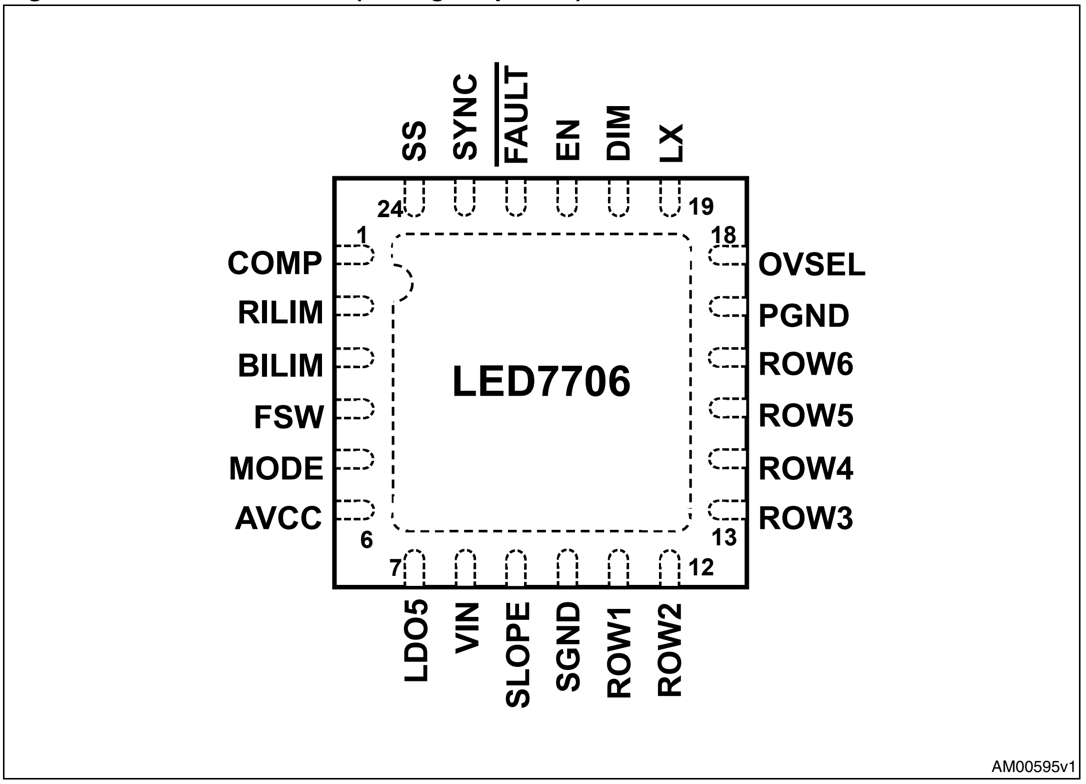
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	COMP	Error amplifier output. A simple RC series between this pin and ground is needed to compensate the loop of the boost regulator.
2	RILIM	Output generators current limit setting. The output current of the rows can be programmed connecting a resistor to SGND.
3	BILIM	Boost converter current limit setting. The internal MOSFET current limit can be programmed connecting a resistor to SGND.
4	FSW	Switching frequency selection and external sync input. A resistor to SGND is used to set the desired switching frequency. The pin can also be used as external synchronization input. See *Section 5.1.5 on page 15* for details.
5	MODE	Current generators fault management selector. It allows to detect and manage LEDs failures. See *Section 5.3.2 on page 21* for details.
6	AVCC	+ 5 V analog supply. Connect to LDO5 through a simple RC filter.
7	LDO5	+ 5 V LDO output and power section supply. Bypass to SGND with a 1 µF ceramic capacitor.
8	VIN	Input voltage. Connect to the main supply rail.
9	SLOPE	Slope compensation setting. A resistor between the output of the boost converter and this pin is needed to avoid sub-harmonic instability. Refer to *Section 6.1 on page 24* for details.
10	SGND	Signal ground. Supply return for the analog circuitry and the current generators.
11	ROW1	Row driver output #1.
12	ROW2	Row driver output #2.
13	ROW3	Row driver output #3.
14	ROW4	Row driver output #4.
15	ROW5	Row driver output #5.
16	ROW6	Row driver output #6.
17	PGND	Power ground. Source of the internal Power MOSFET.
18	OVSEL	Over-voltage selection. Used to set the desired OV threshold by an external divider. See *Section 5.1.4 on page 14* for details.
19	LX	Switching node. Drain of the internal Power MOSFET.
20	DIM	Dimming input. Used to externally set the brightness by using a PWM signal.
21	EN	Enable input. When low, the device is turned off. If tied high or left open, the device is turned on and a soft-start sequence takes place.
22	$\overline{\text{FAULT}}$	Fault signal output. Open drain output. The pin goes low when a fault condition is detected (see *Section 5.3.1 on page 21* for details).
23	SYNC	Synchronization output. Used as external synchronization output.
24	SS	Soft-start. Connect a capacitor to SGND to set the desired soft-start duration.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{LDO5}	LDO5 to SGND	-0.3 to 6	
	PGND to SGND	-0.3 to 0.3	
V_{IN}	VIN to PGND	-0.3 to 40	
V_{LX}	LX to SGND	-0.3 to 40	
	LX to PGND	-0.3 to 40	
	RILIM, BILIM, SYNC, OVSEL, SS to SGND	-0.3 to V_{AVCC} + 0.3	
	EN, DIM, SW, MODE, FAULT to SGND	-0.3 to 6	
	ROWx to PGND/ SGND	-0.3 to 40	
	SLOPE to VIN	V_{IN} - 0.3 to V_{IN} + 6	
	SLOPE to SGND	-0.3 to 40	
	Internal switch maximum RMS current (flowing through LX node)	2.0	A
P_{TOT}	Power dissipation @ T_A = 25 °C	2.3 (2)	W
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”	±1000	V

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. Power dissipation referred to the device mounted on the demonstration board described in section 5.5

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Junction operating temperature range	-40 to 150	°C

4 Electrical characteristics

V_{IN} = 12 V; T_J = 25 °C and LDO5 connected to AVCC if not otherwise specified [(a)]

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply section						
V_{IN}	Input voltage range		4.5		36	V
V_{BST}	Boost section output voltage				36	
V_{LDO5} V_{AVCC}	LDO output and IC supply voltage	EN High I_{LDO5} = 0 mA	4.4	5	5.5	V
$I_{IN,Q}$	Operating quiescent current	R_{RILIM} = 51 kΩ, R_{BILIM} = 220 kΩ, R_{SLOPE} = 680 kΩ DIM tied to SGND.		1		mA
$I_{IN,SHDN}$	Operating current in shutdown	EN low		20	30	µA
$V_{UVLO,ON}$	LDO5 under voltage lock out upper threshold			3.8	4.0	V
$V_{UVLO,OFF}$	LDO5 under voltage lock out lower threshold		3.3	3.6		V
LDO linear regulator						
	Line regulation	6 V ≤ V_{IN} ≤ 36 V, I_{LDO5} = 30 mA			30	mV
	LDO dropout voltage	V_{IN} = 4.3 V, I_{LDO5} = 10 mA		80	120	mV
	LDO maximum output current	V_{LDO5} > $V_{UVLO,ON}$	25	40	60	mA
		V_{LDO5} < $V_{UVLO,OFF}$		20	30	mA
Boost section						
$t_{ON,min}$	Minimum switching on-time				200	ns
f_{SW}	Default switching frequency	FSW connected to AVCC	570	660	750	kHz
	Minimum FSW sync frequency			210		kHz
	FSW sync input threshold		240			mV
	FSW sync low level				350	mV
	FSW sync input hysteresis			20		mV
	FSW sync min. ON time				270	ns
	SYNC output Duty-Cycle	FSW connected to AVCC (Internal oscillator selected)		34	40	%
	SYNC output high level	I_{SYNC} = 10 µA	V_{AVCC} -20V			mV
	SYNC output low level	I_{SYNC} = -10 µA			20	mV

a. Specification referred to T_J from 0 °C to +85 °C. Specification over the 0 to +85 °C T_J range are assured by design, characterization and statistical correlation.

Table 5. Electrical characteristics (continued)

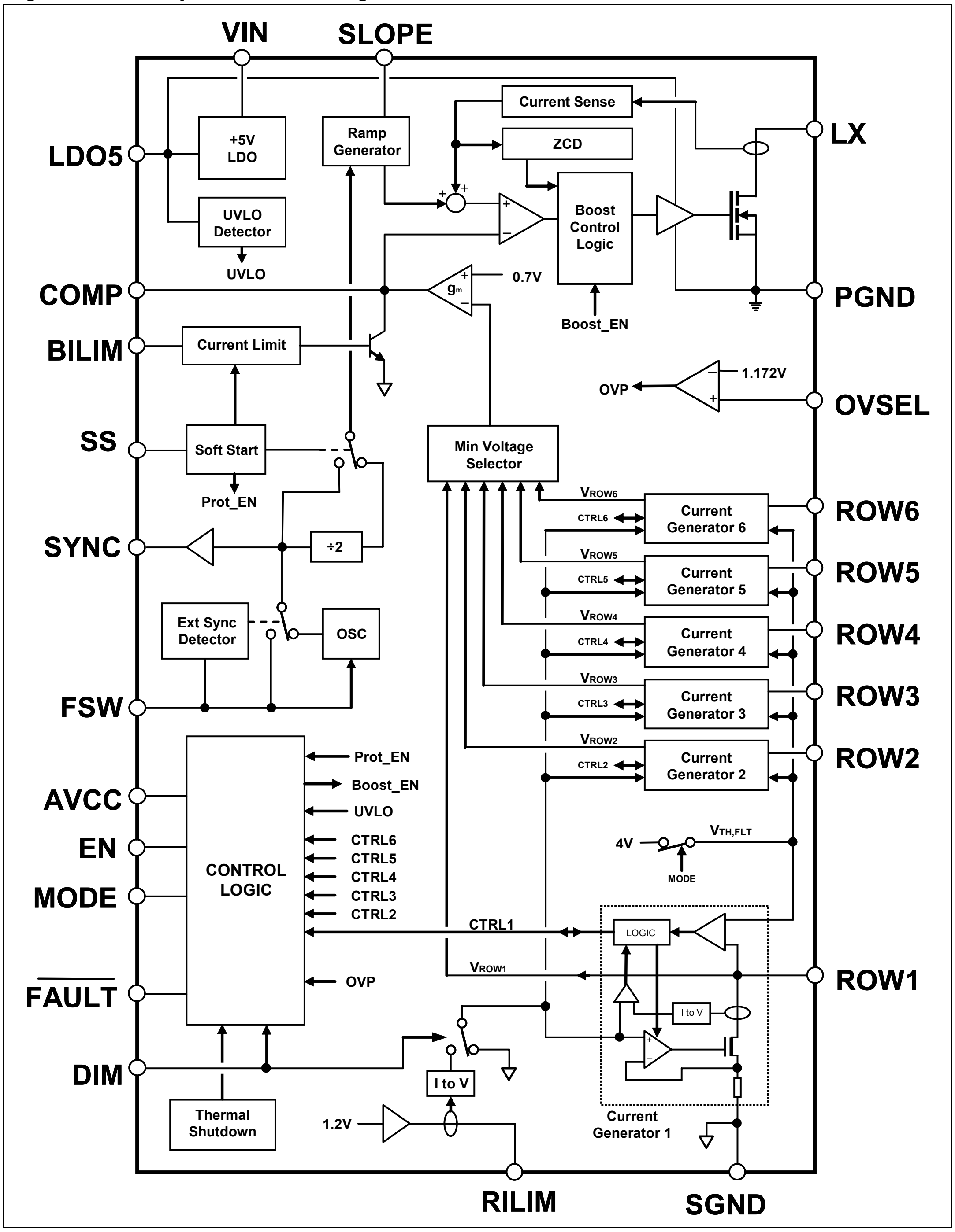
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power switch						
K_B	LX current coefficient	R_{BILIM} = 600 kΩ	$5 \cdot 10^5$	$6 \cdot 10^5$	$7 \cdot 10^5$	V
R_{DSon}	Internal MOSFET on-resistance			280	500	mΩ
OC and OV protections						
$V_{TH,OVP}$	Over voltage protection reference threshold (OVSEL)		1.190	1.234	1.280	V
$V_{TH,FRD}$	Floating channel detection threshold		1.100	1.145	1.190	V
$\Delta V_{OVP,FRD}$	Voltage gap between OVP and FRD thresholds			90		mV
Soft-start and power management						
	EN, Turn-on threshold				1.6	V
	EN, Turn-off threshold		0.8			V
	DIM, high level threshold		1.3			V
	DIM, low level threshold				0.8	V
	EN, pull-up current			2.5		µA
	SS, charge current		4	5	6	µA
	SS, end-of-startup threshold		2.0	2.4	2.8	V
	SS, reduced switching frequency release threshold			0.8		V
Current generators section						
$T_{DIM-ON,min}$	Minimum dimming on-time			500		ns
K_R	Current generators gain			987		V
ΔK_R (1)	Current generators gain accuracy				±2.0	%
V_{IFB}	Feedback regulation voltage			400		mV
$V_{rowx,FAULT}$	Shorted LED fault detection threshold	MODE tied to SGND		3.4		V
		MODE connected to AVCC		6.0		V
$V_{FAULT,LOW}$	FAULT pin low-level voltage	$I_{FAULT,SINK}$ = 4 mA		200	350	mV
Thermal shutdown						
T_{SHDN}	Thermal shutdown turn-off temperature			150		°C
	Thermal shutdown hysteresis			30		°C

1. $I_{ROW} = K_R / R_{RILIM}$, $\Delta I_{ROW}/I_{ROW} \approx \Delta K_R/K_R + \Delta R_{RILIM}/R_{RILIM}$

5 Operation description

The device can be divided into two sections: the boost section and the backlight driver section. These sections are described in the next paragraphs. *Figure 3* provides an overview of the internal blocks of the device.

Figure 3. Simplified block diagram



5.1 Boost section

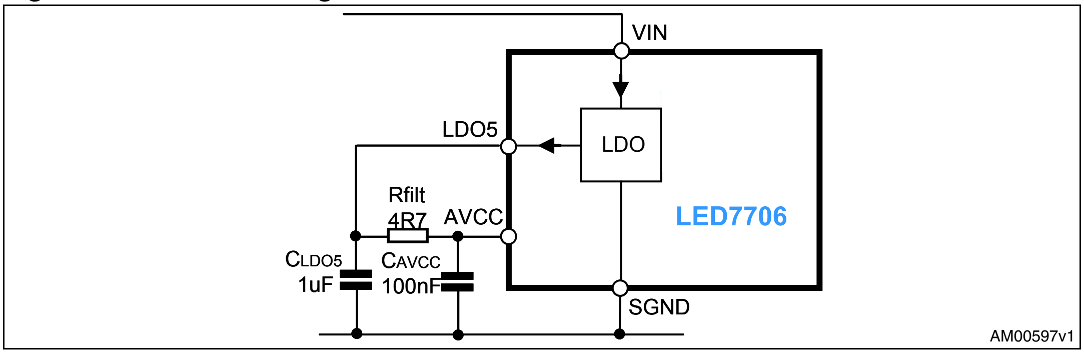
5.1.1 Functional description

The LED7706 is a monolithic LEDs driver for the backlight of LCD panels and it consists of a boost converter and six PWM-dimmable current generators.

The boost section is based on a constant switching frequency, peak current-mode architecture. The boost output voltage is controlled such that the lowest row's voltage, referred to SGND, is equal to an internal reference voltage (400 mV typ. see *Figure 5*). The input voltage range is from 4.5 V up to 36 V. In addition, the LED7706 has an internal LDO that supplies the internal circuitry of the device and is capable to deliver up to 40 mA. The input of the LDO is the VIN pin.

The LDO5 pin is the LDO output and the supply for the power MOSFET driver at the same time. The AVCC pin is the supply for the analog circuitry and should be connected to the LDO output through a simple RC filter in order to improve the noise rejection.

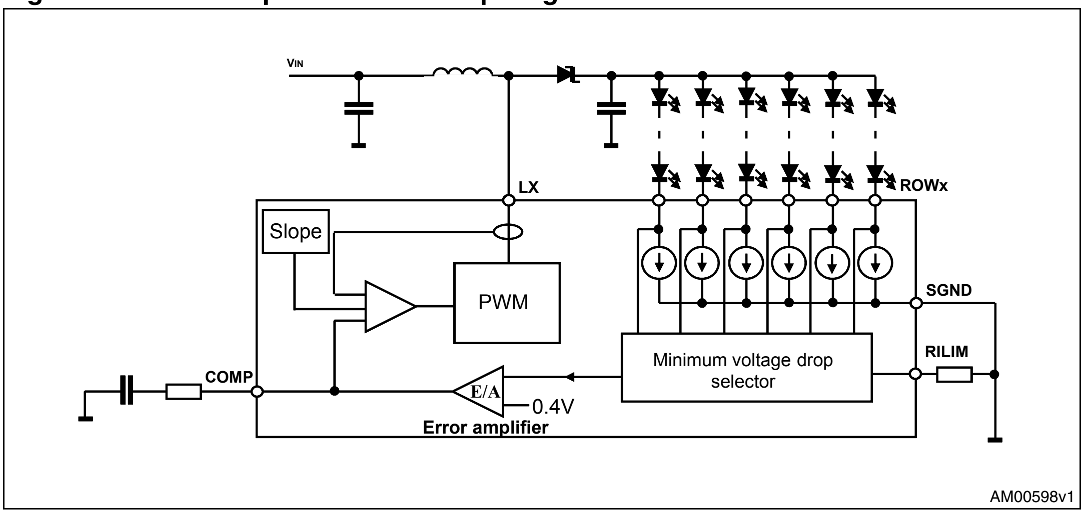
Figure 4. AVCC filtering



Two loops are involved in regulating the current sunk by the generators.

The main loop is related to the boost regulator and uses a constant frequency peak current-mode architecture to regulate the power rail that supplies the LEDs (*Figure 5*), while an internal current loop regulates the same current (flowing through the LEDs) at each row according to the set value (RILIM pin).

Figure 5. Main loop and current loop diagram



A dedicated circuit automatically selects the lowest voltage drop among all the rows and provides this voltage to the main loop that, in turn, regulates the output voltage. In fact, once the reference generator has been detected, the error amplifier compares its voltage drop to the internal reference voltage and varies the COMP output. The voltage at the COMP pin determines the inductor peak current at each switching cycle. The output voltage of the boost regulator is thus determined by the total forward voltage of the LEDs strings (see *Figure 6*):

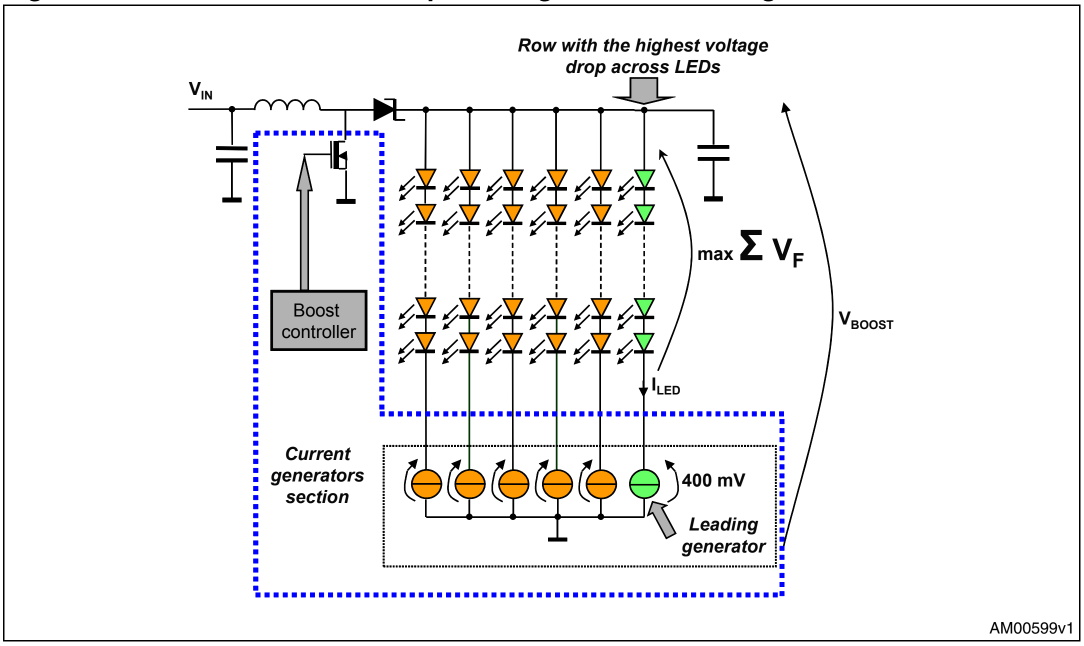
Equation 1

$$V_{OUT} = \max_{i=1}^{N_{ROWS}}\left(\sum_{j=1}^{m_{LEDS}} V_{F,j}\right) + 400mV$$

where the first term represents the highest total forward voltage drop over N active rows and the second is the voltage drop across the leading generator (400 mV typ.).

The device continues to monitor the voltage drop across all the rows and automatically switches to the current generator having the lowest voltage drop.

Figure 6. Calculation of the output voltage of the boost regulator

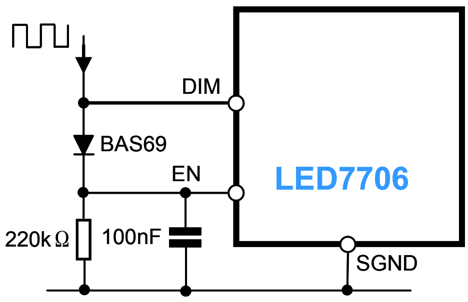


5.1.2 Enable function

The LED7706 is enabled by the EN pin. This pin is active high and, when forced to SGND, the device is turned off. This pin is connected to a permanently active 2.5 µA current source; when sudden device turn-on at power-up is required, this pin must be left floating or connected to a delay capacitor. When turned off, the LED7706 quickly discharges the soft-start capacitor and turns off the power MOSFET, the current generators and the LDO. The power consumption is thus reduced to 20 µA only.

In applications where the dimming signal is used to turn on and off the device, the EN pin can be connected to the DIM pin as shown in *Figure 7*.

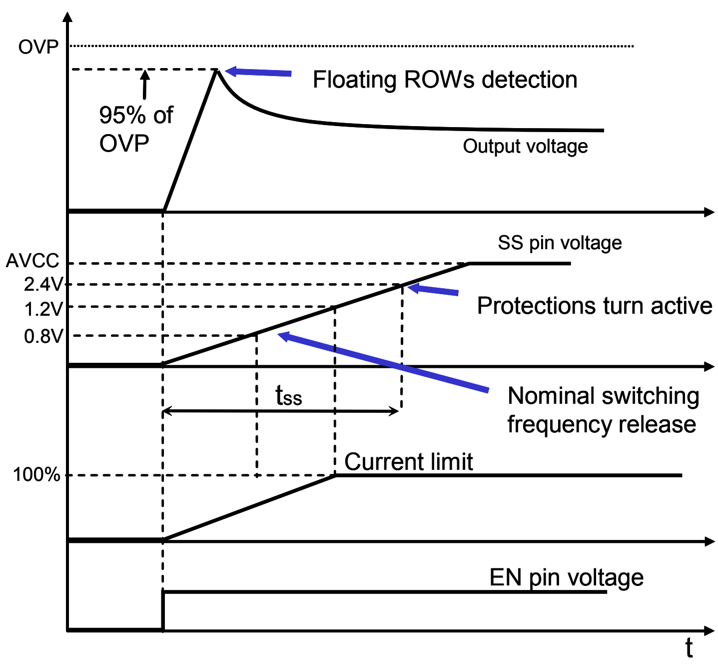
Figure 7. Enable pin driven by dimming signal



5.1.3 Soft-start

The soft-start function is required to perform a correct start-up of the system, controlling the inrush current required to charge the output capacitor and to avoid output voltage overshoot. The soft-start duration is set connecting an external capacitor between the SS pin and ground. This capacitor is charged with a 5 µA (typ.) constant current, forcing the voltage on the SS pin to ramp up. When this voltage increases from zero to nearly 1.2 V, the current limit of the power MOSFET is proportionally released from zero to its final value. However, because of the limited minimum on-time of the switching section, the inductor might saturate due to current runaway. To solve this problem the switching frequency is reduced to one half of the nominal value at the beginning of the soft-start phase. The nominal switching frequency is restored after the SS pin voltage has crossed 0.8 V.

Figure 8. Soft-start sequence waveforms in case of floating rows



During the soft-start phase the floating rows detection is also performed. In presence of one or more floating rows, the voltage across the involved current generator drops to zero. This voltage becomes the inverting input of the error amplifier through the minimum voltage drop selector (see *Figure 5*). As a consequence the error amplifier is unbalanced and the loop reacts by increasing the output voltage. When it reaches the floating row detection (FRD) threshold (95% of the OVP threshold), the floating rows are managed according to *Table 6* (see *Section 5.3 on page 21*). After the SS voltage reaches a 2.4 V threshold, the start-up finishes and all the protections turn active. The soft-start capacitor C_{SS} can be calculated according to equation 2.

Equation 2

$$C_{SS} \cong \frac{I_{SS} \cdot t_{SS}}{2.4}$$

Where I_{SS} = 5 µA and t_{SS} is the desired soft-start duration.

5.1.4 Overvoltage protection

An adjustable over-voltage protection is available. It can be set feeding the OVSEL pin with a partition of the output voltage. The voltage of the central tap of the divider is thus compared to a fixed 1.234 V threshold. When the voltage on the OVSEL pin exceeds the OV threshold, the FAULT pin is tied low and the device is turned off; this condition is latched and the LED7706 is restarted by toggling the EN pin or by performing a Power-On Reset (the POR occurs when the LDO output falls below the lower UVLO threshold and subsequently crosses the upper UVLO threshold during the rising phase of the input voltage). Normally, the value of the high-side resistors of the divider must be chosen as high as possible (but lower than 1 MΩ) to reduce the output capacitor discharge when the boost converter is off (during the off phase of the dimming cycle). The R2/R1 ratio is calculated to trigger the OVP circuitry as soon as the output voltage is 2 V higher than the maximum value for a given LED string (see equation 3). Two additional filtering capacitors, C_{10} and C_{13}, may be required to improve noise rejection at the OVSEL pin, as shown in *Figure 9*. The typical value for C_{10} is in the 100 pF-330 pF range, while the C_{13} value is given by equation 4.

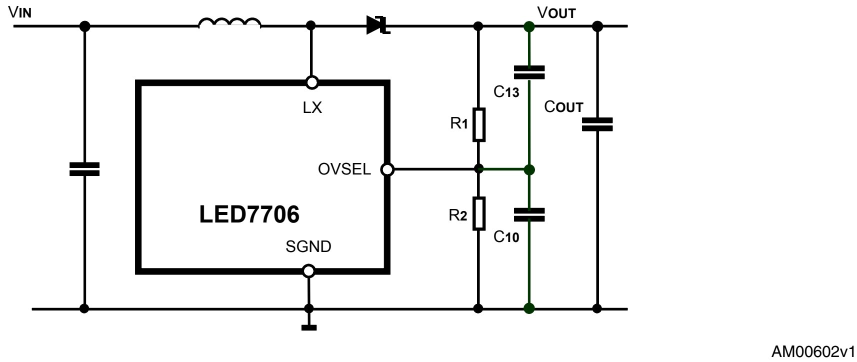
Equation 3

$$R_2 = R_1 \cdot \frac{1.234V}{(V_{OUT,OVP} + 2V - 1.234V)}$$

Equation 4

$$C_{13} = 2 \cdot C_{10} \frac{R_2}{R_1}$$

Figure 9. OVP threshold setting



5.1.5 Switching frequency selection and synchronization

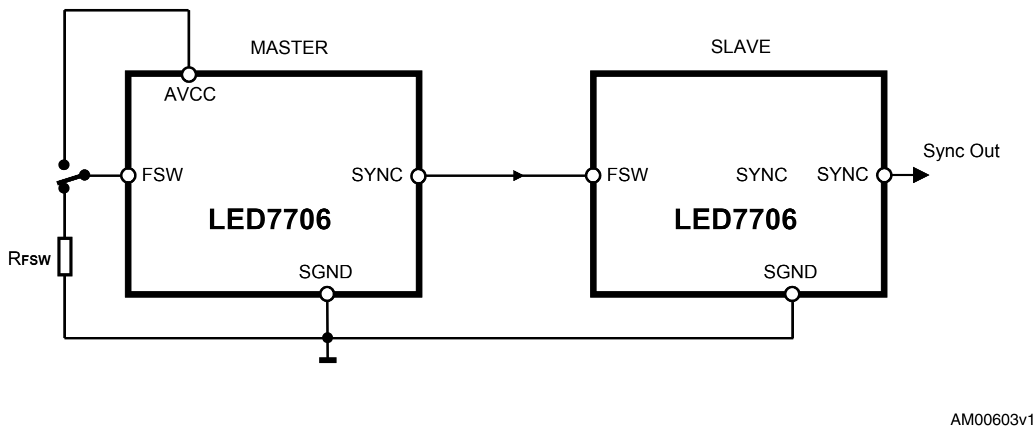
The switching frequency of the boost converter can be set in the 250 kHz-1 MHz range by connecting the FSW pin to ground through a resistor. Calculation of the setting resistor is made using equation 5 and should not exceed the 100 kΩ-400 kΩ range.

Equation 5

$$R_{FSW} = \frac{F_{SW}}{2.5}$$

In addition, when the FSW pin is tied to AVCC, the LED7706 uses a default 660 kHz fixed switching frequency, allowing to save a resistor in minimum component-count applications.

Figure 10. Multiple device synchronization

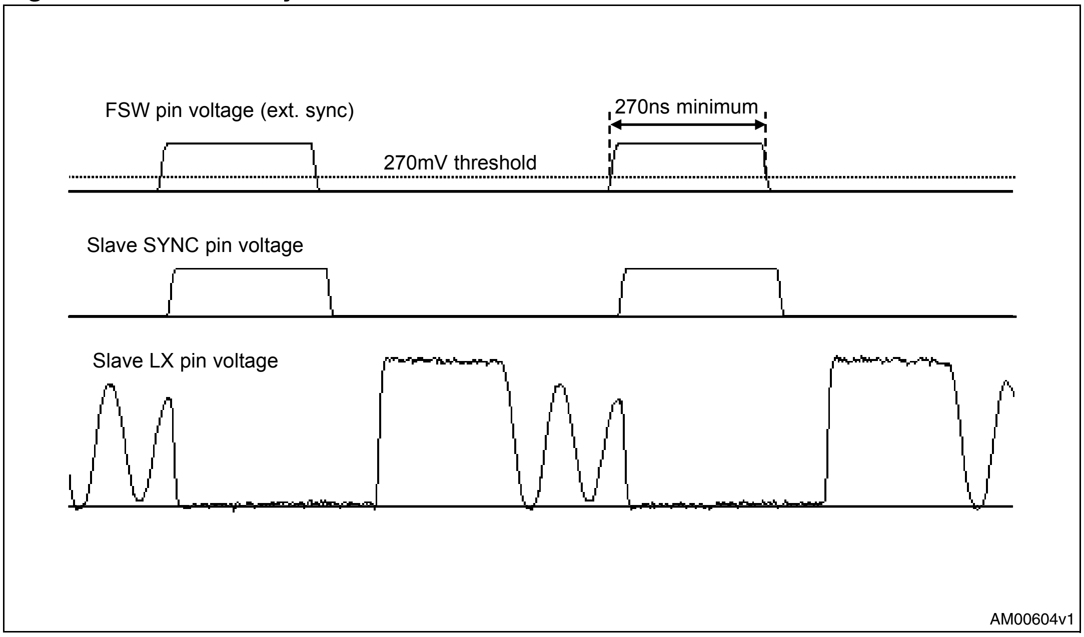


The FSW pin can also be used as synchronization input, allowing the LED7706 to operate both as master or slave device. If a clock signal with a 210 kHz minimum frequency is applied to this pin, the device locks synchronized. The signal provided to the FSW pin must cross the 270 mV threshold in order to be recognized. The minimum pulse width which allows the synchronizing pulses to be detected is 270 ns. An Internal time-out allows synchronization as long as the external clock frequency is greater than 210 kHz.

Keeping the FSW pin voltage lower than 270 mV for more than 4.8 µs results in a stop of the device switching activity. Normal operation is resumed as soon as FSW rises above the mentioned threshold and the soft-start sequence is repeated.

The SYNC pin is a synchronization output and provides a 35 % (typ.) duty-cycle clock when the LED7706 is used as master or a replica of the FSW pin when used as slave. It is used to connect multiple devices in a daisy-chain configuration or to synchronize other switching converters running in the system with the LED7706 (master operation). When an external synchronization clock is applied to the FSW pin, the internal oscillator is over-driven: each switching cycle begins at the rising edge of the clock, while the slope compensation (*Figure 11*) ramp starts at the falling edge of the same signal. Thus, to prevent sub-harmonic instability (see *Section 5.1.6*), the external synchronization clock is required to have a 40 % maximum duty-cycle when the boost converter is working in continuous-conduction mode (CCM) in order to assure that the slope compensation is effective (starts with duty-cycle lower than 40%)

Figure 11. External sync waveforms



5.1.6 Slope compensation

The constant frequency, peak current-mode topology has the advantage of very easy loop compensation with output ceramic caps (reduced cost and size of the application) and fast transient response. In addition, the intrinsic peak-current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor.

On the other side, this topology has a drawback: there is an inherent open loop instability when operating with a duty-ratio greater than 0.5. This phenomenon is known as “Sub-Harmonic Instability” and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called “slope compensation”. In *Figure 12*, where the switching duty-cycle is higher than 0.5, the small perturbation ΔI_L dies away in subsequent cycles thanks to the slope compensation and the system reverts to a stable situation.

The SLOPE pin allows to properly set the amount of slope compensation connecting a simple resistor R_{SLOPE} between the SLOPE pin and the output. The compensation ramp starts at 35% (typ.) of each switching period and its slope is given by the following equation:

Equation 6

$$S_E = K_S \left(\frac{V_{OUT} - V_{IN} - V_{BE}}{R_{SLOPE}} \right)$$

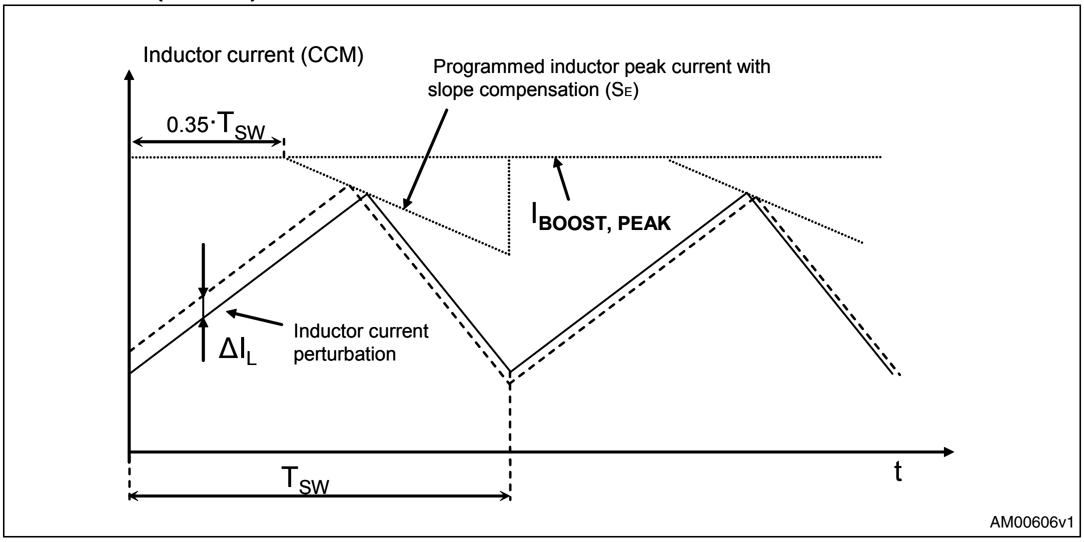
Where KS = 5.8 $\cdot 10^{10}$ s^{-1}, V_{BE} = 2 V (typ.) and S_E is the slope ramp in [A/s].

To avoid sub-harmonic instability, the compensating slope should be at least half the slope of the inductor current during the off-phase when the duty-cycle is greater than 50%. The value of R_{SLOPE} can be calculated according to equation 7.

Equation 7

$$R_{SLOPE} \leq \frac{2 \cdot K_S \cdot L \cdot (V_{OUT} - V_{IN} - V_{BE})}{(V_{OUT} - V_{IN})}$$

Figure 12. Effect of slope compensation on small inductor current perturbation (D > 0.5)



5.1.7 Boost current limit

The design of the external components, especially the inductor and the flywheel diode, must be optimized in terms of size relying on the programmable peak current limit. The LED7706 improves the reliability of the final application giving the way to limit the maximum current flowing into the critical components. A simple resistor connected between the BILIM pin and ground sets the desired value. The voltage at the BILIM pin is internally fixed to 1.23 V and the current limit is proportional to the current flowing through the setting resistor, according to the following equation:

Equation 8

$$I_{BOOST,PEAK} = \frac{K_B}{R_{BILIM}}$$

where

$$K_B = 6 \cdot 10^5 V$$

The maximum allowed current limit is 5 A, resulting in a minimum setting resistor R_{BILIM} > 120 kΩ. The maximum guaranteed RMS current in the power switch is 2 A.

In a boost converter the RMS current through the internal MOSFET depends on both the input and output voltages, according to equations 9a (DCM) and 9b (CCM).

The current limitation works by clamping the COMP pin voltage proportionally to R_{BILIM}. Peak inductor current is limited to the above threshold decreased by the slope compensation contribution.

Equation 9 a

$$I_{MOS,rms} = \frac{V_{IN} \cdot D}{F_{SW} \cdot L}\sqrt{\frac{D}{3}}$$

Equation 9 b

$$I_{MOS,rms} = I_{OUT}\sqrt{\left(\frac{D}{(1-D)^2} + \frac{1}{12}\left(\frac{V_{OUT}}{I_{OUT} \cdot f_{SW} \cdot L}\right)^2 (D(1-D))^3\right)}$$

5.1.8 Thermal protection

In order to avoid damage due to high junction temperature, a thermal shutdown protection is implemented. When the junction temperature rises above 150 °C (typ.), the device turns off both the control logic and the boost converter and holds the FAULT pin low. The LDO is kept alive and normal operation is automatically resumed after the junction temperature has been reduced by 30 °C.

5.2 Backlight driver section

5.2.1 Current generators

The LED7706 is a LEDs driver with six channels (rows); each row is able to drive multiple LEDs in series (max. 36 V) and to sink up to 30 mA maximum current, allowing to manage different kinds of LEDs.

The LEDs current can be set by connecting an external resistor (R_{RILIM}) between the RILIM pin and ground. The voltage across the RILIM pin is internally set to 1.23 V and the rows current is proportional to the RILIM current according to the following equation:

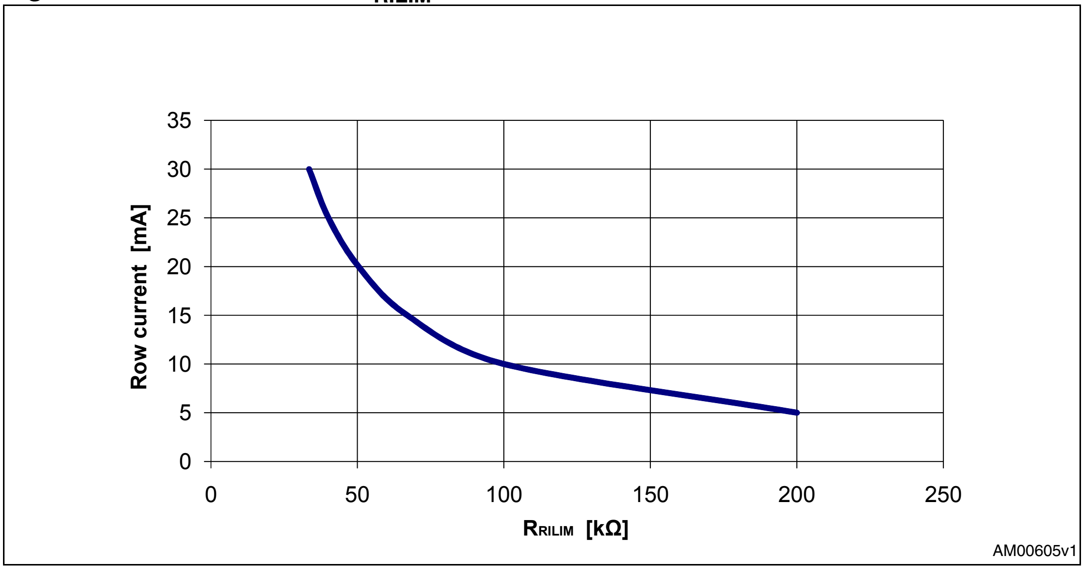
Equation 10

$$I_{ROWx} = \frac{K_R}{R_{RILIM}}$$

Where K_R = 987 V.

The graph in *Figure 13* better shows the relationship between I_{ROW} and R_{RILIM} and helps to choose the correct value of the resistor to set the desired row current.

Figure 13. Row current vs R_{RILIM}



The maximum current mismatch between the rows is ± 2 % @ I_{rowx} = 20 mA.

5.2.2 PWM dimming

The brightness control of the LEDs is performed by a pulse-width modulation of the rows current. When a PWM signal is applied to the DIM pin, the current generators are turned on and off mirroring the DIM pin behavior. Actually, the minimum dimming duty-cycle depends on the dimming frequency.

The real limit to the PWM dimming is the minimum on-time that can be managed for the current generators; this minimum on-time is approximately 500 ns.

Thus, the minimum dimming duty-cycle depends on the dimming frequency according to the following formula:

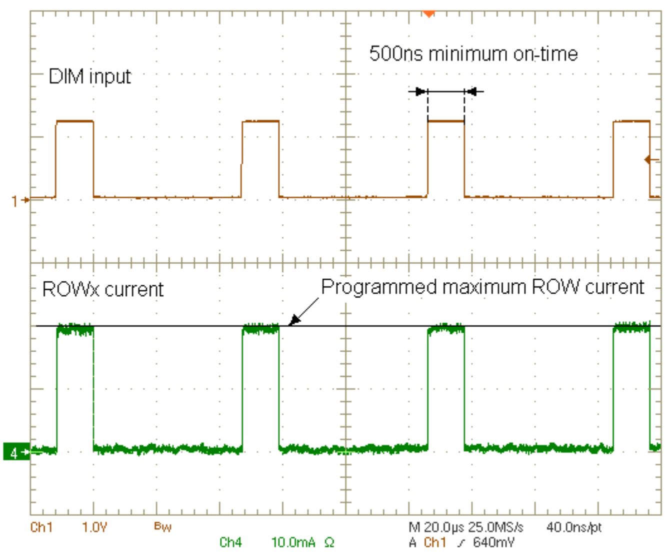
Equation 11

$$D_{DIM,min} = 500ns \cdot f_{DIM}$$

For example, at a dimming frequency of 20 kHz, 1% of dimming duty-cycle can be managed.

During the off-phase of the PWM signal the boost converter is paused and the current generators are turned off. The output voltage can be considered almost constant because of the relatively slow discharge of the output capacitor. During the start-up sequence (see *Section 5.1.3 on page 13*) the dimming duty-cycle is forced to 100% to detect floating rows regardless of the applied dimming signal.

Figure 14. PWM dimming waveforms



5.3 Fault management

The main loop keeps the row having the lowest voltage drop regulated to about 400 mV. This value slightly depends on the voltage across the remaining active rows. After the soft-start sequence, all protections turn active and the voltage across the active current generators is monitored to detect shorted LEDs.

5.3.1 FAULT pin

The FAULT pin is an open-collector output, (with 4 mA current capability) active low, which gives information regarding faulty conditions eventually detected. This pin can be used either to drive a status LED or to warn the host system.

The FAULT pin status is strictly related to the MODE pin setting (see *Table 6* for details).

5.3.2 MODE pin

The MODE pin is a digital input and can be connected to AVCC or SGND in order to choose the desired fault detection and management. The LED7706 can manage a faulty condition in two different ways, according to the application needs. *Table 6* summarizes how the device detects and handles the internal protections related to the boost section (over-current, over-temperature and over-voltage) and to the current generators section (open and shorted LEDs).

Table 6. Faults management summary

FAULT	MODE to GND	MODE to VCC
Internal MOSFET over current	FAULT pin HIGH Power MOS turned OFF	
Output over voltage	FAULT pin LOW Device turned OFF, latched condition	
Thermal shutdown	FAULT pin LOW. Device turned OFF. Automatic restart after 30 C temperature drop.	
LED short shorted led	FAULT pin LOW Device turned OFF, latched condition (Vth = 3.4 V)	FAULT pin LOW Faulty row(s) disconnected Device keeps on working with the remaining row(s) (Vth = 6 V)
Open row(s)	FAULT pin LOW Device turned OFF at first occurrence, latched condition	FAULT pin HIGH Faulty row(s) disconnected. Device keeps on working with the remaining row(s)

5.3.3 Open LED fault

In case a row is not connected or a LED fails open, the device has two different behaviors according to the MODE pin status.

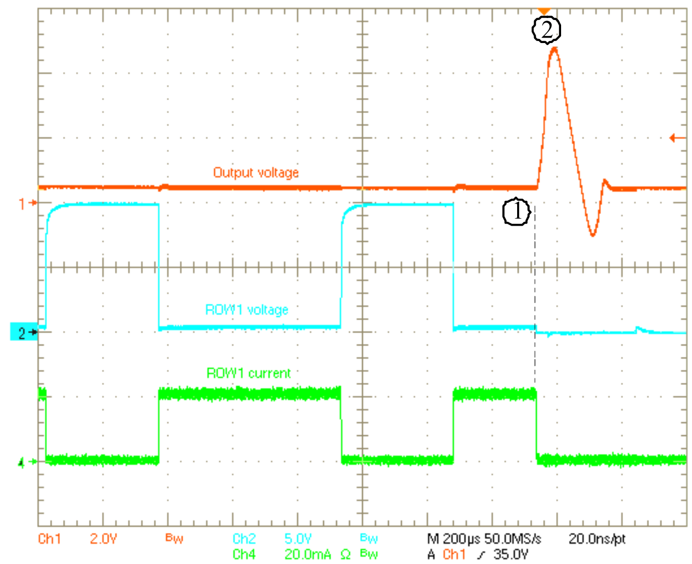
Connecting the MODE pin to SGND, as soon as an open row is detected the FAULT pin is tied low and the device is turned off. The internal logic latches this status: to restore the normal operation, the device must be restarted by toggling the EN pin or performing a Power-On Reset (POR occurs when the voltage at the LDO5 pin falls below the lower UVLO threshold and subsequently rises above the upper one).

If the MODE pin is high (i.e. connected to AVCC), the LED7706 behaves in a different manner: the open row is excluded from the control loop and the device continues to work properly with the remaining rows. The FAULT pin is not affected. Thus, if less than six rows are used in the application, the MODE pin must be set high.

Figure 15 shows an example of open channel detection in case of MODE connected to AVCC.

At the point marked as “1” in *Figure 15*, the row opens (row current drops to zero). From this point on the output voltage is increased as long as the output voltage reaches the floating row detection threshold (see *Section 5.1.3 on page 13*). Then (point marked as “2”) the faulty row is disconnected and the device keeps on working only with the remaining rows.

Figure 15. Open channel detection (MODE to AVCC)



5.3.4 Shorted LED fault

When a LED is shorted, the voltage across the related current generator increases of an amount equal to the missing voltage drop of the faulty LED. Since the feedback voltage on each active generator is constantly compared with a fault threshold $V_{TH,FAULT}$, the device detects the faulty condition and acts according to the MODE pin status.

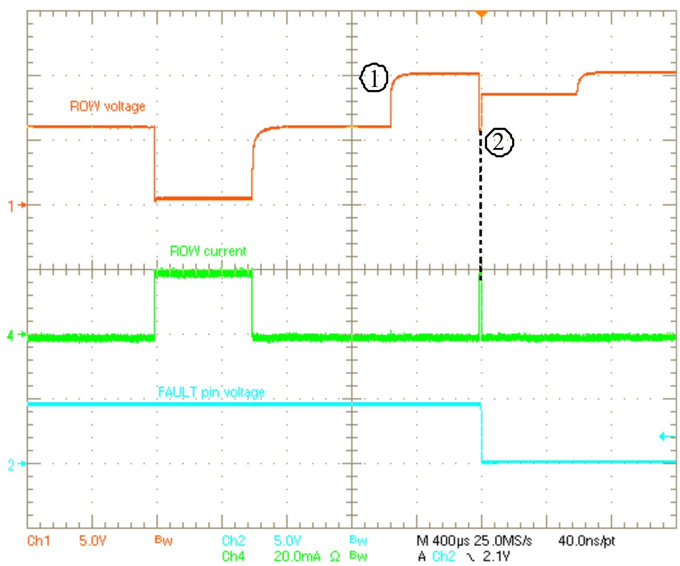
If the MODE pin is low, the fault threshold is $V_{TH,FAULT}$ = 3.4 V. When the voltage across a row is higher than this threshold, the FAULT pin is set low and the device is turned off. The internal logic latches this status until the EN pin is toggled or a POR is performed.

In case the MODE pin is connected to AVCC, the fault threshold is set to 6 V. The LED7706 simply disconnects the rows whose voltage is higher than the threshold and the FAULT pin is forced low. This option is also useful to avoid undesired triggering of the shorted-LED protection simply due to the high voltage drop spread across the LEDs.

Figure 16 shows an example of shorted LED detection in case MODE is connected to GND.

At the point marked as “1” in *Figure 16* one LED fails becoming a short-circuit. The voltage across the current generator of the channel where the failed LED is connected increases by an amount equal to the forward voltage of the faulty LED. Since the voltage across the current generator is above the threshold (3.4 V in this case), the device is turned off and the fault pin is set low (point “2”).

Figure 16. Shorted LED detection (MODE to GND)



6 Application information

6.1 System stability

The boost section of the LED7706 is a fixed frequency, current-mode converter. During normal operation, a minimum voltage selection circuit compares all the voltage drops across the active current generators and provides the minimum one to the error amplifier. The output voltage of the error amplifier determines the inductor peak current in order to keep its inverting input equal to the reference voltage (400 mV typ). The compensation network consists of a simple RC series (R_{COMP} - C_{COMP}) between the COMP pin and ground.

The calculation of R_{COMP} and C_{COMP} is fundamental to achieve optimal loop stability and dynamic performance of the boost converter and is strictly related to the operating conditions.

6.1.1 Loop compensation

The compensation network can be quickly calculated using equations 12 to 16. Once both R_{COMP} and C_{COMP} have been determined, a fine-tuning phase may be required in order to get the optimal dynamic performance from the application.

The first parameter to be fixed is the switching frequency. Normally, a high switching frequency allows reducing the size of the inductor and positively affects the dynamic response of the converter (wider bandwidth) but increases the switching losses. For most of applications, the fixed value (660 kHz) represents a good trade-off between power dissipation and dynamic response, allowing to save an external resistor at the same time. In low-profile applications, the inductor value is often kept low to reduce the number of turns; an inductor value in the 4.7 µH-15 µH range is a good starting choice.

In order to avoid instability due to interaction between the DC-DC converter's loop and the current generators' loop, the bandwidth of the boost should not exceed the bandwidth of the current generators. A unity-gain frequency (f_U) in the order of 30-40 kHz is acceptable. Also, take care not to exceed the CCM-mode right half-plane zero (RHPZ).

Equation 12

$$f_U \leq 0.2 \cdot F_{SW}$$

Equation 13

$$f_U \leq 0.2 \cdot \frac{M^2 R}{2\pi \cdot L} = 0.2 \cdot \frac{\left(\frac{V_{IN,min}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT}}{I_{OUT}}\right)}{2\pi \cdot L}$$

Equation 14 a

$$M = \frac{V_{IN,min}}{V_{OUT}}$$

Equation 14b

$$R = \frac{V_{OUT}}{I_{OUT}}$$

Where $V_{IN,min}$ is the minimum input voltage and I_{OUT} is the overall output current.

Note that, the lower the inductor value (and the higher the switching frequency), the higher the bandwidth can be achieved. The output capacitor is directly involved in the loop of the boost converter and must be large enough to avoid excessive output voltage drop in case of a sudden line transition from the maximum to the minimum input voltages.

However a more significant requirement concerns the output voltage ripple.

The output capacitor should be chosen in accordance with the following expression:

Equation 15

$$C_{OUT} > \frac{(I_{L,peak} - I_{OUT}) \cdot T_{OFF}}{2 \cdot \Delta V_{OUT,max}}$$

where $\Delta V_{OUT, max}$ is the maximum acceptable output voltage ripple, $I_{L, peak}$ is the peak inductor current, T_{OFF} is the off-time of the switching cycle (for an extensive explanation see *Section 6.4.4 on page 31*).

Once the output capacitor has been chosen, the R_{COMP} can be calculated as:

Equation 16

$$R_{COMP} = \frac{2\pi \cdot f_U \cdot C}{G_M \cdot g_{EA} \cdot M}$$

Where G_M = 2.7 S and g_{EA} = 375 µS

Equation 16 places the loop bandwidth at f_U. Then, the C_{COMP} capacitor is determined to place the frequency of the compensation zero 5 times lower than the loop bandwidth:

Equation 17

$$C_{COMP} = \frac{1}{2\pi \cdot f_Z \cdot R_{COMP}}$$

Where $f_Z = f_U/5$.

In most of the applications an experimental approach is also very valid to compensate the circuit. A simple technique to optimize different applications is to choose C_{COMP} = 4.7 nF and to replace R_{COMP} with a 10 kΩ trimmer adjusting its value to properly damp the output transient response. Insufficient damping will result in excessive ringing at the output and poor phase margin.

Figure 17 (a and b) give an example of compensation adjustment for a typical application.