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LED7708

16 channels x 85 mA LED driver with boost controller and 4-wire serial interface

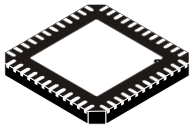
Datasheet —production data

Features

- Boost controller section
  - 3.6 V to 36 V input voltage range (LDO)
  - Adaptive output voltage for high efficiency
  - Internal +5 V LDO for gate driver supply
  - Internal +3.3 V LDO for device supply
  - High performance external MOSFET driver
  - 250 kHz to 1 MHz switching frequency
  - Programmable OV and OC protection
  - Fixed frequency peak current-mode control
  - External synchronization for multi-device application
  - Overtemperature alert and thermal shutdown
- LED array driver section
  - 16 channels with 85 mA/ch current capability
  - ±2% channel current accuracy
  - ±2% channel-to-channel current matching
  - LED short-circuit and open channel fault detection and management
  - 4-wire, 30 MHz serial interface
  - 16 x16-bit, 1x256-bit or 1x192-bit serial data formats
  - Grouped or independent channel PWM control
  - Selectable 12/16-bit grayscale brightness control for local dimming
  - Programmable internal dimming oscillator
  - Programmable grayscale latency
  - Master/slave chain configuration supported

Applications

- TV and monitor backlight units for LCD panels
- Medium and large size LCD panel backlights
- RGB/RGGB backlight solutions



VFQFPN 7x7x1.0 48L
(pitch 0.50)

Description

The LED7708 has been specifically designed to supply several LEDs starting from a single low-voltage rail. It integrates a boost controller, sixteen current generators and a 4-wire serial interface. The boost controller regulates the output voltage in an adaptive way, according to the LED requirements, resulting in an improved overall efficiency. All the current generators are 40 V-rated, allowing the LED7708 to drive several LEDs in series on each channel. The channels can be put in parallel for higher output current.

The brightness of the LEDs is controlled by using the serial interface. A selectable 12-bit or 16-bit grayscale brightness control allows independent PWM on each channel. A programmable on-chip dimming oscillator is provided for external circuitry simplification. The device has dedicated pins to lock to an external synchronization with other devices (master or slave) for noise reduction in multi-device applications. The LED7708 implements basic protection (OVP, OCP and thermal shutdown) as well as LED array protection. It can detect and manage open-LED and shorted-LED faults and different fault-management options are available in order to cover most application needs.

Table 1. Device summary

Order codes	Package	Packing
LED7708	VFQFPN-48 7x7 (exposed pad)	Tube
LED7708TR		Tape and reel

Contents

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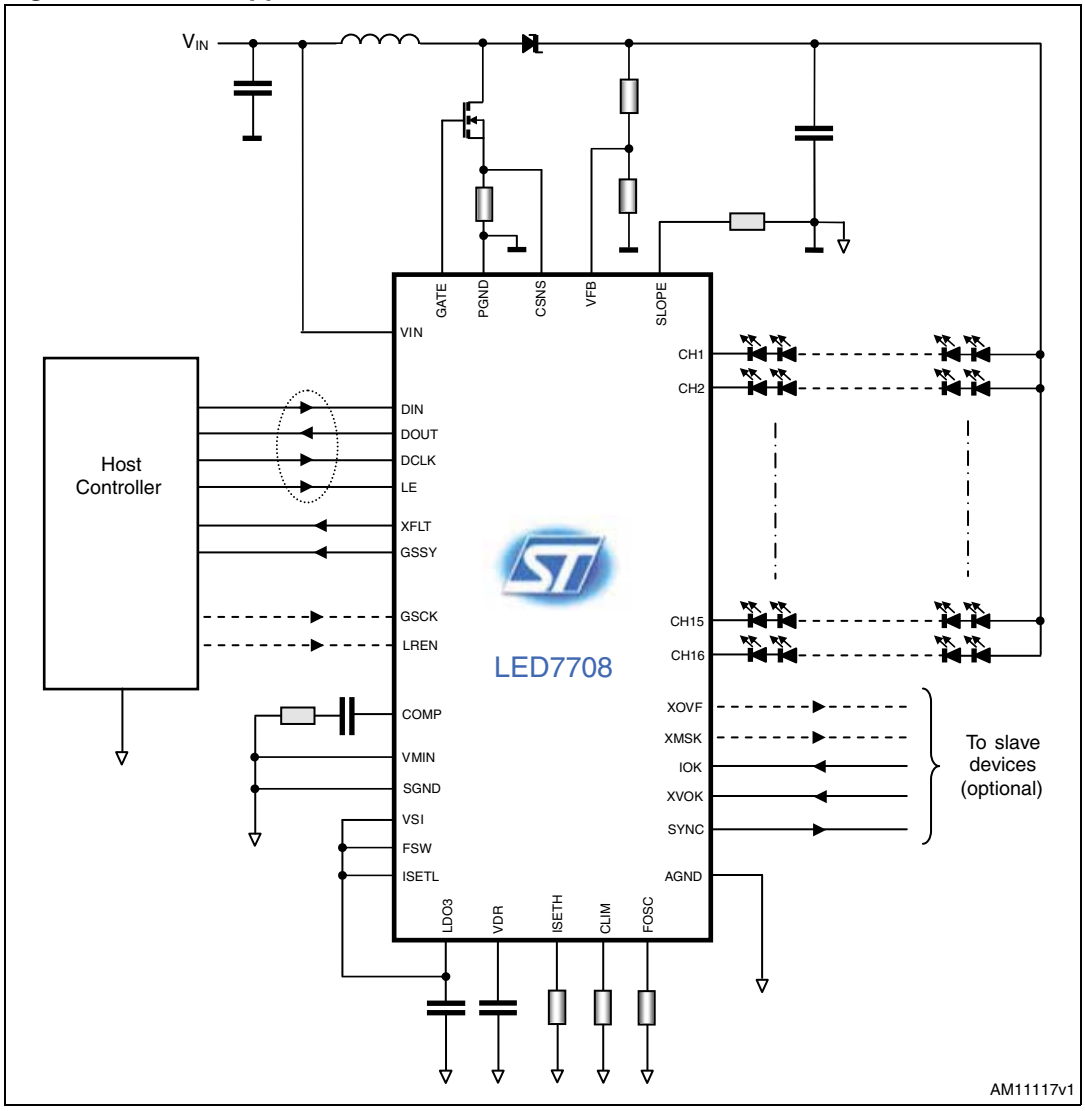
1 Typical application circuit

Figure 1. Basic application circuit schematic



2 Pin function

Figure 2. Pin connection (through top view)

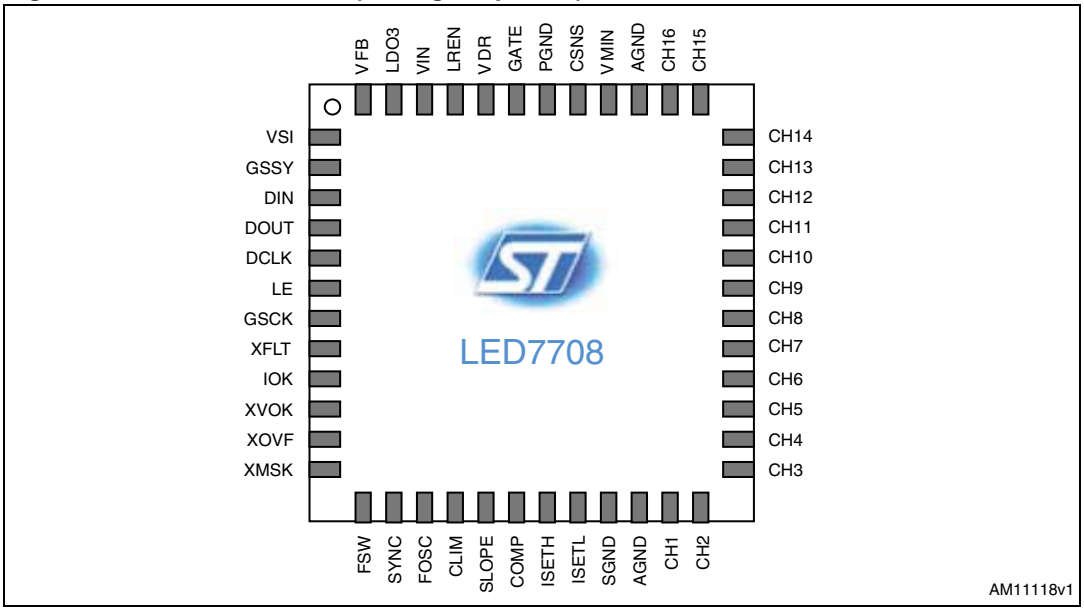


Table 2. Pin description

Pin		Function
1	VSI	Serial interface (SI) core and digital I/O buffer supply input. Connect to LDO3 or to an external supply (3 V-5 V). Insert a 100 nF bypass ceramic capacitor between this pin and SGND. Connect to the host controller's supply when possible.
2	GSSY	Grayscale synchronization output or VSYNC input. When the internal dimming generation is set, a pulse at the end of each dimming cycle is provided for data stream synchronization. Also used as dimming synchronization input to lock the dimming cycles on the vertical sync pulses.
3	DIN	Serial interface data input.
4	DOUT	Serial interface data out.
5	DCLK	Serial interface data clock.
6	LE	Serial interface latch enable.
7	GSCK	Grayscale clock I/O. When the internal dimming oscillator is used, the grayscale clock is provided at this pin. The pin becomes the grayscale clock input if the internal dimming oscillator is disabled (see FOSC pin).
8	XFLT	Fault signal, open drain output. The pin goes low when a faulty condition occurs.
9	IOK	Channel current OK handshake I/O. Used for extended output voltage regulation in multi-device applications. Used by slave devices to request a higher output voltage to the master. A 100 k pull-up resistor to LD03 is required.
10	XVOK	Channel voltage OK I/O (inverted). Used for extended output voltage regulation in multi-device applications. Used by slave devices to request an output voltage reduction to the master. A 100 k pull-up resistor to LD03 is required.

Table 2. Pin description (continued)

Pin		Function
11	XOVF	Internal DAC overflow I/O. Used for extended output voltage regulation and fault management in multi-device applications. It is used to inform slave devices that the maximum output voltage has been reached. A 100 k pull-up resistor to LD03 is required.
12	XMSK	Fault detection masking I/O. This signal is used for extended output voltage regulation & fault management in multi-device applications. It is used to avoid incorrect fault detection by forcing slave devices to ignore LED-short detection during output voltage steering. A 100 k pull-up resistor to LD03 is required.
13	FSW	Switching frequency selection / synchronization input. Used to set the desired switching frequency of the boost controller. Also used as synchronization input.
14	SYNC	Boost converter synchronization output. The buffered switching clock signal is provided at this pin to eventually synchronize other SMPS in the host system.
15	FOSC	Dimming oscillator frequency. A resistor to ground sets the frequency of the internal grayscale clock dimming oscillator. If set high, the internal dimming oscillator is disabled and the GSCK pin becomes the clock input (see GSCK pin).
16	CLIM	Boost section current limit setting. A resistor between this pin and SGND sets the boost converter current limit.
17	SLOPE	Slope compensation setting. A resistor between this pin and SGND is required to set the proper amount of slope compensation to avoid sub-harmonic instability.
18	COMP	Transconductance amplifier output. Connect a simple RC series between this pin and SGND to properly compensate the loop-gain of the boost converter.
19	ISETH	Output current setting (on). Connect a resistor between this pin and SGND to set the current sunk by each channel during the on-phase of the dimming.
20	ISETL	Output current setting (off). Connect a resistor between this pin and SGND to set the current sunk by each channel during the off-phase of the dimming (LED biasing). Connect to LDO3 to disable the bias current.
21	SGND	Signal ground. Common return for signals and settings.
22	AGND	Analog Ground. Common return for the current generators (channels).
23	CH1	Driver output (channel) #1.
24	CH2	Driver output (channel) #2.
25	CH3	Driver output (channel) #3.
26	CH4	Driver output (channel) #4.
27	CH5	Driver output (channel) #5.
28	CH6	Driver output (channel) #6.
29	CH7	Driver output (channel) #7.
30	CH8	Driver output (channel) #8.
31	CH9	Driver output (channel) #9.
32	CH10	Driver output (channel) #10.
33	CH11	Driver output (channel) #11.
34	CH12	Driver output (channel) #12.
35	CH13	Driver output (channel) #13.

Table 2. Pin description (continued)

Pin		Function
36	CH14	Driver output (channel) #14.
37	CH15	Driver output (channel) #15.
38	CH16	Driver output (channel) #16.
39	AGND	Analog ground. Common return for the current generators (channels).
40	VMIN	Minimum output voltage setting. Multi-level input (high, low, floating or resistor to SGND). Used in conjunction with the VFB pin to set the best output voltage range swing for a given LED array. See related section for further details.
41	CSNS	External MOSFET current sense input. Connect to the sensing resistor in series with the power switch (source of the power MOSFET node).
42	PGND	Power ground. Reference for the external MOSFET current sensing circuit and return for the gate driver.
43	GATE	External MOSFET gate driver output. Connected to the gate of the power MOSFET.
44	VDR	Gate driver supply. Internally connected to the 5 V LDO regulator. Bypass with a 1 µF ceramic capacitor to PGND as close as possible to the chip.
45	LREN	3.3 V linear regulator enable. When high or floating, the internal 3.3 V linear regulator is used to supply the device. Also used to turn off the device for power consumption reduction. To be left floating the internal 3.3 V LDO is overdriven by an external 3.3 V supply rail.
46	VIN	Input of the LDO linear regulators. Bypass with a 1µF ceramic capacitor to ground as close as possible to the chip.
47	LDO3	3.3 V device supply and internal 3.3 V linear regulator output. Bypass with a 1 µF ceramic capacitor to ground as close as possible to the chip.
48	VFB	Output voltage feedback for the boost controller. Connect to the central tap of the output resistor divider. See the related section for details.

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Pin	Min.	Max.	Unit
	Maximum pin voltage	VIN, CH1 to CH16	-	40	V
		LDO3	-	VIN+0.3 3.6	
		COMP, SYNC, ISETH, ISETL, SLOPE, CLIM, FOSC, VFB, XOVF, VMIN	-	LDO3+0.3 3.6	
		VSI	-	6	
		DCLK, LE, DIN, GSCK, DCLK, DOUT, GSSY	-	VSI+0.3 6	
		IOK, XMASK, XVOK, XFLT, FSW, LREN,	-	6	
		VDR	-	6 VIN+0.3	
		GATE	-	VDR+0.3 6	
		CSNS	-	LDO3+0.3 3.6	
	Continuous channel current	CH1 to CH16	-	90	mA
	Maximum current generator power dissipation	CH1 to CH16	-	0.5	W
ESD	ESD Rating	Human body model JEDEC JESD22-A114	-	2	kV

Table 4. Thermal data

Symbol	Parameter	Conditions	Min.	Max.	Unit
P_D	Power dissipation(1)	T_A = 25 °C			W
		T_A = 50 °C			
		T_A = 85 °C			
$T_{J,OP}$	Operating junction temperature		-40	150	°C

Table 4. Thermal data (continued)

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{STG}	Storage temperature range		-50	150	
$R_{th,JA}$	Junction-ambient thermal resistance			30	°C/W

1. Device soldered to the STEVAL-ILL035V1 demonstration board.

4 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC Characteristics					
V_{VIN}	VIN pin input voltage range		3.6	36	V
V_{LDO3}	LDO pin input voltage range	VIN, LDO3 and VDR shorted together	3.0	3.6	
V_{VDR}	VDR pin input voltage range	VDR and VIN shorted together	3.0	5.5	
V_{CHx}	Channel voltage range			36	
V_{VSI}	Serial interface supply voltage		3.0	5.5	
I_{CHx}	Channel continuous current		20	85	mA
	Channel current when OFF (adjustable)		2	200	µA
AC Characteristics (V_{SI} = 3.3 V)					
f_{GSC}	Grayscale clock frequency			25	MHz
f_{DCLK}	Serial clock frequency			30	
f_{SW}	Boost converter switching frequency		200	1000	kHz
$T_{w,DCLK}$	DCLK pulse width		20		ns
$T_{w,GSC}$	GSC pulse width		20		
$T_{w,LE}$	LE pulse width		15		
$T_{su,DIN}$	DIN setup time		5		
$T_{h,DIN}$	DIN hold time		5		
$T_{su,LE}$	LE setup time		5		
$T_{h,LE}$	LE hold time		5		

5 Electrical characteristics

(V_{IN} = 12 V; T_{AMB} = 25 °C and VSI connected to LDO3 if not otherwise specified.)

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply section						
	LREN turn-on threshold				1.4	V
	LREN turn-off threshold		1			µA
	LREN pull-up current			3		
$V_{UVLO,ON}$	LDO3 undervoltage lockout upper threshold			2.9	3.0	V
$V_{UVLO,OFF}$	LDO3 undervoltage lockout lower threshold		2.6	2.7		
$V_{VSI,ON}$	VSI turn-on threshold			3.0	3.1	
$V_{VSI,OFF}$	VSI turn-off threshold		2.6	2.7		
V_{LDO3}	3.3 V LDO output voltage	3.6 V ≤V_{VIN} ≤28 V I_{LDO3}=0 mA, DEN=0	3.2	3.3	3.4	mV
	3.3 V LDO load regulation	V_{VIN}=3.6 V, DEN=0 0 mA ≤I_{LDO3} ≤40 mA		30	100	
	3.3 V LDO drop-out voltage	I_{LDO3}=40 mA, V_{LDO3}=3.2 V	180	270		
V_{VDR}	5 V LDO output voltage	6 V ≤V_{VIN} ≤28 V I_{VDR}=0 mA, DEN=1	4.5	5.0	5.5	V
	5 V LDO load regulation	V_{VIN}=6 V, DEN=1 0 mA ≤I_{VDR}≤40 mA		60	200	mV
	5 V LDO drop-out voltage	I_{VDR} =40 mA, V_{VDR}=4.5 V	150	200		mV
Boost controller						
$t_{ON,min}$	Minimum switching on-time			100	170	ns
f_{SW}	Default switching frequency	FSW to LDO3	550	610	670	kHz
	Synchronization input frequency		180		1020	
K_{FSW}	Switching frequency constant	R_{FSW} = 100 kΩ	4.4 x10^{10}	5.0 x10^{10}	5.6 x10^{10}	Hz • Ω
$I_{GATE,Pk}$	Gate driver current capability	C_L=3.3 nF, sourcing		1.9		A
		C_L=3.3 nF, sinking		2.1		
$t_{r,GATE}$	Gate driver rise time (10 to 90%)	C_L=3.3 nF		9		ns
$t_{f,GATE}$	Gate driver fall time (90 to10%)			10		

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	FSW synchronization input low level				0.5	V
	FSW synchronization input high level		2.2			
	SYNC output duty cycle	FSW connected to LDO3	25	30	35	%
	SYNC output high level	I_{SYNC}=1 mA	V_{LDO3} -0.3 V			V
	SYNC output low level	I_{SYNC}=-1 mA			0.4	
	Adjustable power MOSFET current sensing voltage	R_{CLIM}=100 kΩ		100		mV
		R_{CLIM}=300 kΩ		300		
Power consumption						
I_{VIN1}	Shutdown current (SI off, LED drivers off, SMPS off, LDOs off)	LREN low, VSI low			30	µA
I_{VIN2}	Shutdown current (SI active, LED drivers off, SMPS off, LDOs on)	LREN floating VSI to LDO3 DEN=0		300	450	
I_{VIN3}	Quiescent current (LED drivers off, boost section not switching)	LREN floating; VSI, FOSC and ISETL to LDO3; DIN, DCLK, LE, GSCK and GSSY to GND; V_{CHx}=2 V; R_{ISETH}=60 kΩ		4		mA
I_{VIN4}	Operating current (serial interface active, boost not switching)	LREN floating VSI and FOSC to LDO3, DIN and DCLK toggling at 15 MHz, DOUT, GSSY and GSCK floating, LE to GND. V_{CHx}=2 V, R_{ISETH}=60 kΩ		7		
I_{VSI1}	Standby current (DIN, DCLK and LE to SGND, LED drivers off, SMPS off, LREN floating)	VSI = 3.3 V		7		µA
		VSI = 5.0 V		9		
OV protection, output regulation						
$V_{FB,OVP}$	Overvoltage protection reference threshold	V_{MIN} tied to GND	1.275	1.30	1.325	V
		V_{MIN} to LDO3	1.105	1.13	1.155	
		R_{VMIN}=220 kΩ	0.985	1.01	1.035	
		V_{MIN} floating	0.765	0.8	0.815	
$V_{FB,OVP}$	OVP hysteresis			6		mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DAC,FB}$	Maximum internal reference voltage for output regulation	VMIN to GND	1.136	1.161	1.186	V
		VMIN to LDO3	0.967	0.992	1.017	
		R_{VMIN}=220 kΩ	0.847	0.872	0.897	
		VMIN floating	0.630	0.655	0.680	
	Minimum internal reference voltage for output regulation	VMIN to GND	0.836	0.861	0.886	
		VMIN to LDO3	0.667	0.692	0.717	
		R_{VMIN}=220 kΩ	0.547	0.572	0.597	
		VMIN floating	0.330	0.355	0.380	
Current generators						
ΔI_{CHxn}	Maximum output current accuracy with respect to nominal value(1)	V_{CHx}=0.6 V, 20 mA ≤ I_{CHx} ≤85 mA		±2%	±3%	
ΔI_{CHxy}	Maximum channel-to-channel output current mismatch(1) (all channels active)	V_{CHx}=0.6 V, R_{ISETH}=60 kΩ (I_{CHx}=20 mA)		±2%		
V_{CHx}	Minimum master channel feedback voltage	R_{ISETH}=60 kΩ, CRS=0		500	600	mV
		R_{ISETH}=15 kΩ, CRS=1		700	800	
V_{RW}	Regulation window amplitude	R_{ISETH}=60 kΩ, RWAS=0	190	250	310	
		R_{ISETH}=60 kΩ, RWAS=1	400	500	600	
$I_{CHx,OFF1}$	Off-state channels current	V_{CHx}=10 V, R_{ISETL}=50 kΩ	70	80	90	µA
$I_{CHx,OFF2}$		V_{CHx}=10 V, ISETL to LDO3		1	2	
$V_{TH,ISETL}$	ISETL input threshold $I_{CHx, OFF2}$		V_{LDO3-1}			V
K_{ISETH}	Output current high-state constant	20 mA ≤ I_{CHx} ≤85 mA	1164	1200	1236	
K_{ISETL}	Output current low-state constant		3.5	4.0	4.5	
Serial interface						
	DIN, DCLK, LE, GSCK, GSSY low level input threshold	VSI=LDO3=3.3 V			1.32	V
	DIN, DCLK, LE, GSCK, GSSY high level input threshold		1.6			
	DOUT and GSSY output low level	VSI=LDO3=3.3 V I_{LOAD}=-200 µA			1.22	
	DOUT and GSSY output high level	VSI=LDO3=3.3 V I_{LOAD}=200 µA	1.75			

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Fault management						
$V_{CHx,FLT1}$	LED short-circuit detection threshold	DTS0=1& DTS1=0	3.0	3.2	3.4	V
$V_{CHx,FLT2}$		DTS0=0& DTS1=1	6.2	6.4	6.6	
$V_{CHx,FLT3}$		DTS0=1& DTS1=1	7.7	8.0	8.3	
	XFLT output low level	$I_{XFLT, SINK}$=4 mA		200	220	mV
Dimming oscillator						
K_{OSC}	Internal dimming oscillator constant	R_{FOSC}=33.2 kΩ	3.86 x10^{11}	4 x10^{11}	4.14 x10^{11}	Hz•Ω
$F_{GSCK,OSC}$	Internal dimming oscillator frequency	R_{FOSC}=100 kΩ		4		MHz
		R_{FOSC}=16 kΩ		25		
Thermal flag and protection						
T_{OTA}	Overtemperature alert threshold			125		°C
	Overtemperature alert hysteresis			20		
T_{OTP}	Overtemperature protection threshold			155		

1. Channel current accuracy is calculated as:

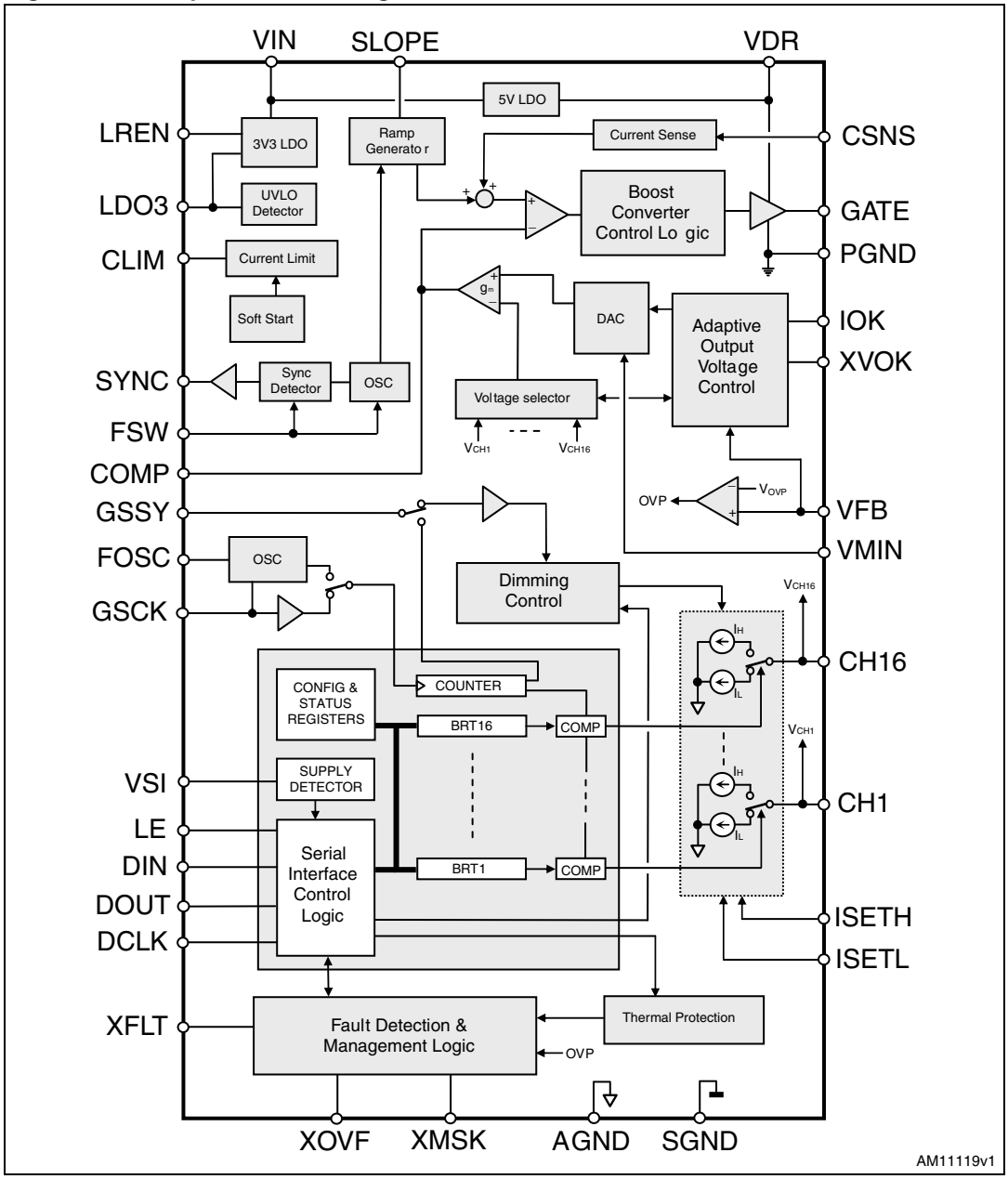
$$\Delta I_{CHX} = \max\frac{(|I_{CHX} - I_{TARGET}|)}{I_{TARGET}} \bullet 100$$

$$\Delta I_{CHY} = \max\frac{(|I_{CHX} - I_{CHY}|)}{I_{TARGET}} \bullet 100$$

where X, Y=1..16, X≠Y.

6 Block diagram

Figure 3. Simplified block diagram



7 Device description

The LED7708 is an LED driver that integrates a boost controller, sixteen current generators and a 4-wire serial interface. It has been specifically designed for driving the LED backlight in medium to large LCD panels.

The device is controlled by a 4-wire serial interface and can operate both as standalone driver and as master driver in conjunction with other slave devices.

Basic and advanced dimming functions are supported in order to meet different application requirements. Regardless of the dimming control technique, the LED7708 can optimize the power dissipation by controlling the output voltage of the boost converter. Two internal linear regulators derive the device supply (3.3 V) and the gate driver supply (5 V) from a single power rail.

7.1 Device supply

The LED7708 integrates two low drop-out linear regulators to derive the +3.3 V (typ.) main supply and the +5 V supply for the gate driver. The VIN pin is the input terminal for both linear regulators. The output of the 3.3 V LDO is the LDO3 pin, the output of the 5 V LDO is the VDR pin. The 3.3 V LDO (LDO3 pin) is active if the LREN (linear regulator enable) pin is left floating or externally set high (see *Section 5: Electrical characteristics* for the thresholds involved).

The serial interface I/O stage is supplied through the VSI pin. This pin is used to enable the serial interface and it allows the setting of the logic level of the serial interface signals (3.3 V or 5 V) at the same time. The serial interface can be powered by the internal 3.3 V LDO (by simply connecting the LDO3 pin to the VSI pin) or by an external source, usually the same supply rail as the host controller.

When an external +3.3 V source is available, it is possible to bypass the 3.3 V LDO by connecting VIN, VDR and LDO3 together to the +3.3 V rail; in this case the gate driver is supplied at 3.3 V too and a super-logic level MOSFET is required as the power switch.

The 3.3 V regulator is self-protected against overcurrent and thermal damage thanks to a foldback mechanism. The continuous current capability of the 3.3 V LDO is calculated to not exceed the junction temperature limit in worst power dissipation conditions.

A 1 µF MLCC on the LDO3 pin is required for ripple filtering and LDO output stability.

The LDO3 pin is internally connected to the undervoltage lockout (UVLO) protection; the upper and lower UVLO thresholds are reported in *Section 5: Electrical characteristics*. When the voltage at the LDO3 pin falls below the lower UVLO threshold, the device is turned off (non-latched condition). The device turns on when the voltage at the LDO3 pin crosses the upper UVLO threshold. Crossing the lower and upper thresholds in sequence performs the so called “power-on reset” (POR). The POR sequence is used, as well as toggling the internal DEN bit (see internal registers), when the device is asked to restore normal operation after a latched fault condition. The 5 V linear regulator, whose output is connected to the VDR pin, is turned off when the device is disabled, while the 3.3 V linear regulator is controlled by the LREN pin only.

8 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC Characteristics					
V_{VIN}	VIN pin input voltage range		3.6	36	V
V_{LDO3}	LDO pin input voltage range	VIN, LDO3 and VDR shorted together	3.0	3.6	
V_{VDR}	VDR pin input voltage range	VDR and VIN shorted together	3.0	5.5	
V_{CHx}	Channel voltage range			36	
V_{VSI}	Serial interface supply voltage		3.0	5.5	
I_{CHx}	Channel continuous current		20	85	mA
	Channel current when OFF (adjustable)		2	200	µA
AC Characteristics (V_{SI} = 3.3 V)					
f_{GSC}	Grayscale clock frequency			25	MHz
f_{DCLK}	Serial clock frequency			30	
f_{SW}	Boost converter switching frequency		200	1000	kHz
$T_{w,DCLK}$	DCLK pulse width		20		ns
$T_{w,GSC}$	GSC pulse width		20		
$T_{w,LE}$	LE pulse width		15		
$T_{su,DIN}$	DIN setup time		5		
$T_{h,DIN}$	DIN hold time		5		
$T_{su,LE}$	LE setup time		5		
$T_{h,LE}$	LE hold time		5		

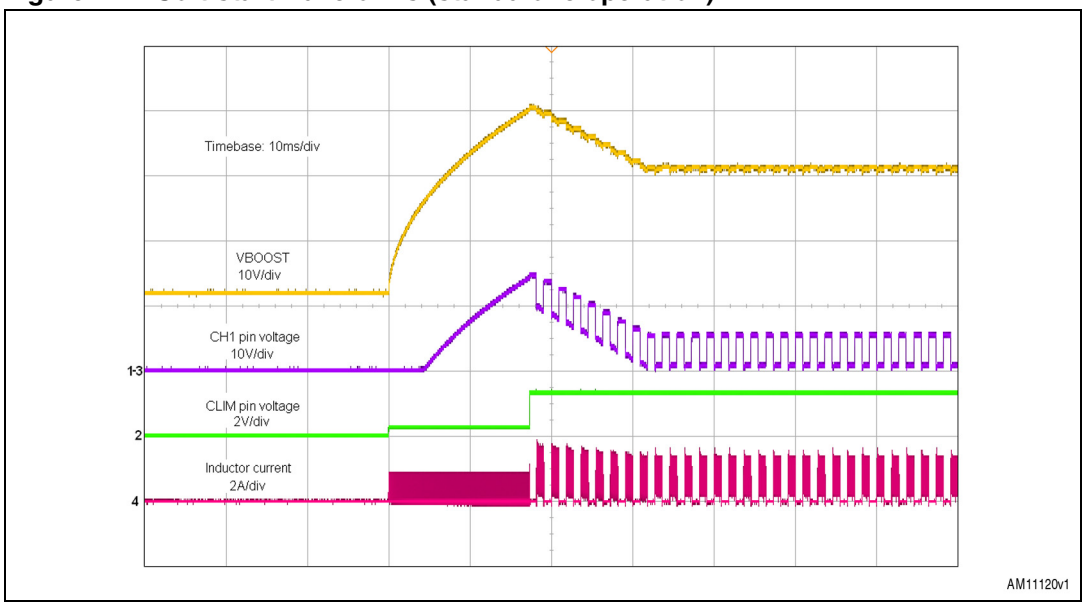
8.1 Device power-up and soft-start

The VSI pin (supply input for the serial interface) has a high level threshold lower than the upper UVLO threshold at the LDO3 pin, ensuring that the serial interface is enabled prior to the device being turned on. Anyway, after the POR, the DEN (device enable) bit of the internal DEVCFG0 control register is low (default value) and the device is off. The soft-start sequence takes place as soon as this bit is asserted.

If the LED7708 is set to operate in standalone, the soft-start procedure takes place in two steps (*Figure 4*):

1. The switching frequency is reduced to one fourth of the nominal value and the boost current limit is set to 20%. This phase finishes approximately 1 ms after the output voltage reaches the maximum value (not the OVP level). During this phase the channels are disabled.
2. Both the switching frequency and the boost current limit are released to their respective nominal values and then the channels are enabled.

Figure 4. Soft-start waveforms (standalone operation)



A slightly different soft-start procedure takes place if the LED7708 is set to operate as master in conjunction with other slave devices:

1. The switching frequency is reduced to one eighth of the nominal value and the boost current limit is set to 20%. This phase finishes approximately 1 ms after the output voltage reaches the maximum value (not the OVP level). During this phase the channels are active.
2. The switching frequency is increased to half the nominal value. This phase is held for approximately 2 ms.
3. The switching frequency is further increased to the nominal value while the current limit changes to 40% (~5 ms duration).
4. The current limit is released to its nominal values.

8.2 Device shutdown

The device is turned off by clearing the DEN bit of the DEVCFG0 register. The content of most of the internal registers is not cleared acting on the DEN bit.

The LREN pin can be also used to turn the device on and off whenever the internal 3.3 V LDO is used to supply the LED7708 (POR). In this case the content of the internal registers is lost.

8.3 Boost controller section and output voltage control

The boost section of the LED7708 consists of:

- Fixed-frequency current-mode step-up controller
- Output voltage optimization loop
- External MOSFET gate driver
- Related protection circuitry.

8.3.1 Output voltage optimization

The output voltage of the boost section is the supply rail for the LED strings and is regulated in an adaptive way to improve the overall efficiency. A dedicated digital-to-analog converter (DAC) is used to change the reference voltage of the loop and the output voltage is adjusted in order to keep the power dissipation of the LED driving section to the minimum level.

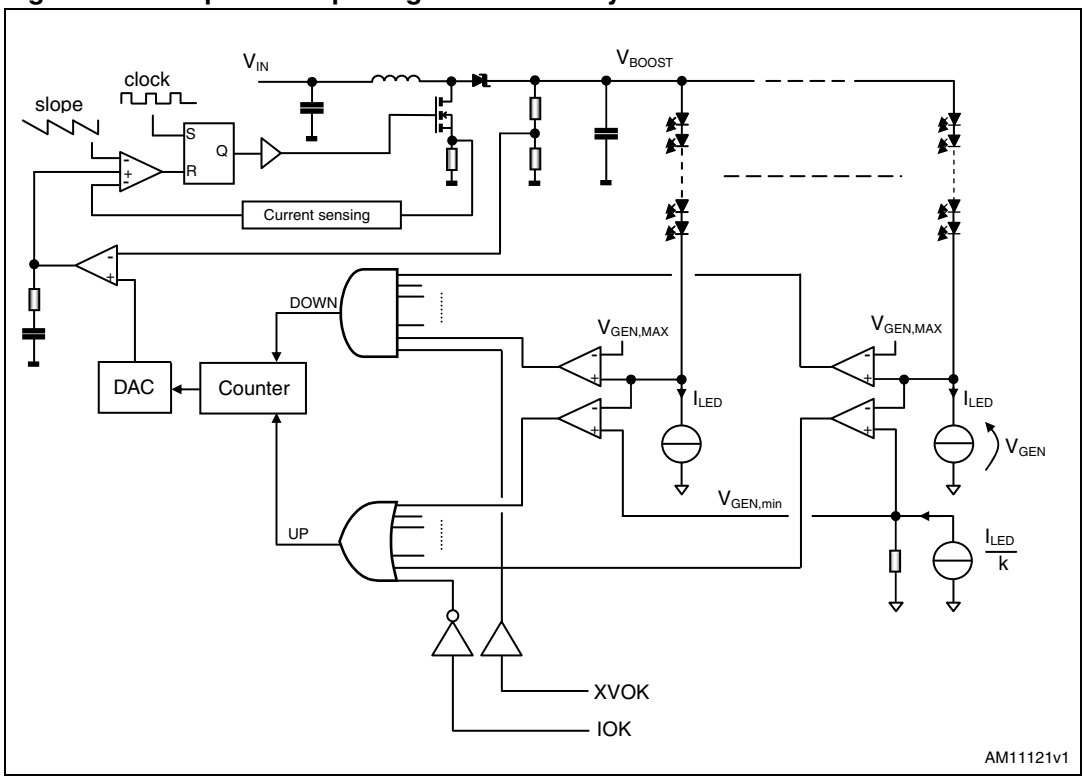
The optimization is achieved by keeping the voltage drop across the channels inside a fixed window (regulation window) and its amplitude can be selected between two values (300 mV and 600 mV) by acting on the internal registers. The lower threshold of the regulation window (V_{RWL}) is a function of the set LED current (*Equation 1*) and the upper threshold (V_{RWH}) is therefore determined.

Equation 1

$$V_{RWL} = K_W \cdot R_{ISETH}$$

Figure 5 shows the simplified regulation circuit.

Figure 5. Simplified output regulation circuitry



During normal operation, the regulation algorithm is the following:

- if at least one active channel has a voltage drop below the lower threshold, the internal DAC counts up and the output voltage is increased
- if all the active channels have a voltage drop higher than the upper threshold, the internal DAC counts down and the output voltage is reduced.

Therefore, the possible operating configurations are shown in *Table 8*.

Table 8. Output voltage states during regulation

Output voltage	Condition
Excessive	All the channels have their voltage above the upper threshold of the regulation window.
Optimal	All the channels have their voltage inside the regulation window.
Regulated	Most of the channels have their voltage inside the regulation window; the remaining channels have a voltage drop above the upper threshold.
Insufficient	At least one channel has its voltage drop below the lower threshold of the regulation window.

The algorithm can also manage faulty conditions that may occur on the LED array (open channels and LED short-circuit) in order to prevent excessive power dissipation.

The LED7708 has been designed to interface with other slave devices and can provide them with the correct LED supply voltage by extending the above mentioned output voltage optimization. For this purpose, some handshake signals have been reserved:

Table 9. Handshake signals summary

Pin	Function
IOK	Used by the slaves to increase the output voltage (algorithm is overdriven)
XVOK	Used by the slaves to ask for an output voltage reduction
XOVF	Used by the master to inform that the maximum output voltage has been reached (each slave uses this information to tag as “faulty” its open channels)
XMSK	Used by the master to inform the slaves that the output voltage is out of regulation and the LED fault detection must be masked to prevent false detection

The two signals IOK and XVOK are connected (wired-or) to all the slave devices sharing the same output voltage rail: if a channel has a low-voltage drop (below V_{RWL}), the device that owns that channel forces low the IOK signal. In a similar way, the XVOK is released if the voltage across all the channels of a slave is higher than required (above V_{RWH}). The wire-or connection of this signal ensures that the output voltage reduction takes place only if all the slaves (and the master itself) need this operation. Refer to the special functions section for a detailed explanation of the daisy chain connection between the master and slave devices.

The boost converter is always active regardless of how many channels are active (i.e. even if all channels are off) in order to improve the load transient dynamic response.

The output voltage regulation can be enabled/disabled (the OVRE bit of the DEVCFG0 register), allowing the user to perform the optimization continuously or on demand.

In real applications, the spread of the forward voltage of the LEDs may cause the channels to have different voltage drops. In any case, the leading channel (i.e. the channel requiring the highest voltage to drive its LED string) is kept inside the regulation window.

The reference voltage, provided by the internal DAC, spans between the minimum and maximum values, programmable through the VMIN pin (see *Section 5: Electrical characteristics*).

As a consequence, the output voltage can be varied by the device in the following range:

Equation 2

$$V_{BOOST,min} = \left(\frac{R_1 + R_2}{R_1}\right) \cdot V_{VFB,min}$$

Equation 3

$$V_{BOOST,MAX} = \left(\frac{R_1 + R_2}{R_1}\right) \cdot V_{VFB,MAX}$$

where R1 and R2 are the resistors of the divider connected to the output rail and V_{VFB} is the reference voltage at the VFB pin.

The LED7708 regulates the output voltage in order to optimize the overall efficiency and, to do this, it needs to read the voltage drop across the active current generators. Unfortunately, in some cases (e.g. during the soft-start phase or when all the channels are set to 0% brightness), the current generators are off and there is no useful information coming from them. Therefore the output voltage is regulated to the minimum value (*Equation 2:*). It must be ensured that the minimum output voltage is below the minimum expected output voltage

in order to guarantee enough steering room for the optimization. Because of the significant dependence of the LED forward voltage with temperature, this must be taken into account when calculating the minimum expected output voltage.

The best way to proceed when designing the external components is the following:

1. Determine the output voltage range required by the LED strings, considering V_F spread and temperature variation:

$$V_{LED} = \max_{i=1}^{N_{ROWS}} \left(\sum_{j=1}^{m_{LEDS}} V_{F,j} \right)$$

2. Calculate the middle-point of the output voltage range $V_{BOOST,middle}$.
3. Calculate the output divider through *Equation 4* and *5*.
4. Calculate the resulting four output voltage ranges (VMIN setting options).
5. Select the output voltage range closest to the one calculated at point 1.

Equation 4

$$R_2 = \frac{(V_{BOOST,middle} - V_{VFB})}{V_{VFB}} \cdot R_1$$

Equation 5

$$\frac{V_{BOOST,MAX}}{R_1 + R_2} \leq 100\mu A$$

8.3.2 Boost converter loop

The voltage drop of each current generator is sent to the minimum voltage selector: the lowest one is used as feedback and sent to the window comparator, whose outputs are used to increase or decrease the loop-counter. The digital outputs of the counter are connected to the DAC and the target reference is generated. As previously mentioned, this reference voltage is compared to a partition of the output voltage: the difference is translated into an error current at the output of the trans-conductance amplifier (see *Figure 4*, COMP pin).

At this point the compensation network, externally connected to the COMP pin, provides the programmed trip level for the inductor current. An additional slope compensation ramp is mixed, as usual, to avoid possible sub-harmonic instability when the boost converter operates in continuous conduction mode (CCM). The SLOPE pin allows the proper setting of the amount of slope compensation connecting a simple resistor RSLOPE between the SLOPE pin and ground. The compensation ramp of a master device starts at 35% (typ.) of each switching period.

The boost converter switching frequency can be set in the 200 kHz-1 MHz range by connecting the FSW pin to ground through a resistor, calculated according to *Equation 6*:

Equation 6

$$R_{FSW} = \frac{K_F}{f_{SW}}$$

In addition, when the FSW pin is tied to LDO3, the LED7708 uses a default 610 kHz fixed switching frequency, allowing the saving of a resistor in minimum component-count applications.

The FSW pin can also be used as synchronization input, allowing the LED7708 to operate both as master or slave device. If a clock signal having a frequency within the capture range is applied to this pin, the device locks synchronized. The minimum pulse width which allows the synchronizing pulses to be detected is 270 ns (typ.). The SYNC pin is a synchronization output and provides a 35% (typ.) duty cycle clock when the LED7708 is set as master or a replica of the FSW pin when it is set as slave. It is used to connect multiple devices in a daisy chain configuration or to synchronize other switching converters running in the system with the LED7708. When an external synchronization clock is applied to the FSW pin, the internal oscillator is overdriven and the external power MOSFET is ignited on the rising edge of the synchronization signal while the slope compensation ramp starts on the falling edge of the same signal. For this reason, the duty cycle of the external synchronization clock should be 30% to 40% to prevent sub-harmonic instability when the boost converter is working in continuous-conduction mode (CCM).

8.3.3 Slope compensation

The constant frequency, peak current-mode topology has the advantage of very easy loop compensation with output ceramic caps (reduced cost and size of the application) and fast transient response. In addition, the intrinsic peak current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor. On the other side, this topology has a drawback: there is inherent open loop instability when operating with a duty cycle greater than 0.5. This phenomenon is known as “sub-harmonic instability” and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called “slope compensation”. As seen in *Figure 6*, when the switching duty cycle is higher than 0.5, the small perturbation ΔIL dies away in subsequent cycles thanks to the slope compensation and the system reverts to a stable situation.