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ispXPGA™ Evaluation Board

User's Guide

October 2004
ebug02_02

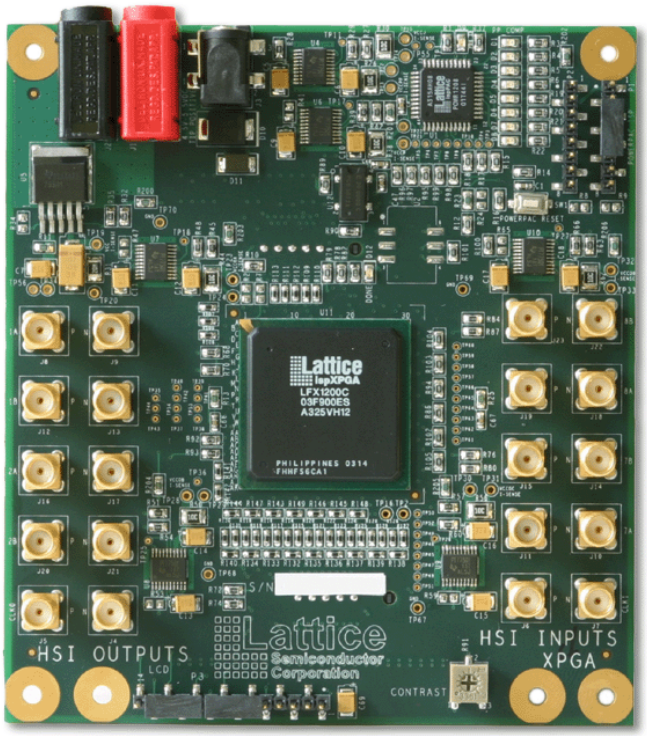
Introduction

The ispXPGA Evaluation Board is a versatile platform that enables the user to program, evaluate, and de-bug a design for the Lattice ispXPGA architecture. The board features a 900-ball fpBGA ispXPGA device with SMA connectors for access to the device's High Speed Interface (sysHSI™) and other I/Os. Connectors are also available to access general-purpose I/Os. Termination is provided for selected I/Os for LVDS operation.

Features

- Power management provided via ispPAC® Power Manager device
- On-board 20MHz oscillator
- Multiple integrated Low Drop-Out (LDO) regulators provide power from single 5V supply
- ispVM® programming support
- Jumperless implementation
- ispDOWNLOAD® Cable (pDS4102-DL2A) included
- 900-ball fpBGA ispXPGA device (ispXPGA 1200 or ispXPGA 500)

Figure 1. ispXPGA Evaluation Board



Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 4.5 inches by 5 inches. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: < 95% without condensation

- 5VDC input, accessible via banana jacks or the included 5V, 4A AC adapter

Holes are included at the corners of the PCB to provide attachment of vertical stand-offs. The pads at these holes are electrically floating.

Resources relating to the ispXPGA Evaluation Board, including a simple demonstration design, can be found on the Lattice web site at www.latticesemi.com.

Table 1. Embedded Functions

Description	Source	ispXPGA Pin	Notes
20MHz clock	On-board oscillator	GCLK0 (R3)	3.3V TTL output
Reset	ispPAC device	Global RST (AK28) AND I/O pin AF21	Active low by default, programmable via ispPAC

ispXPGA Device

The board features an ispXPGA device in a 900-ball fpBGA package. Benefiting from a compatible layout, it is also possible to use an ispXPGA device in the smaller 516-ball fpBGA package. This provides a future option to evaluate devices with a smaller density.

ispPAC-POWR1208 Power Manager Device

The Power Manager device controls the sequencing and monitoring of the various independent power supplies available on the ispXPLD board. Each supply can be activated in stages, with programmable delay increments. As the Power Manager device enables each LDO, a corresponding LED deactivates for visual confirmation.

The Power Manager design and JEDEC files can be downloaded from the Lattice web site. The device is shipped preprogrammed with this default configuration.

For a complete description of the operation of the ispPAC-POWR1208 device and the default design used on this board, refer to the ispPAC-POWR1208 data sheet and PAC-Designer® documentation (PAC-Designer is the design software for the ispPAC-POWR1208). These are available on the Lattice web site at www.latticesemi.com.

V_{CCO} Configurations

The ispXPGA device supports multiple I/O standards and individual I/O bank supply pins for simultaneous support of different interfaces. The ispXPGA evaluation board is set by default to supply 2.5V to all I/O banks. This is adjustable via the addition of resistors. For alternate supply levels, specific resistor values can be installed as described in Figure 2.

Figure 2. I/O Voltage Adjustments

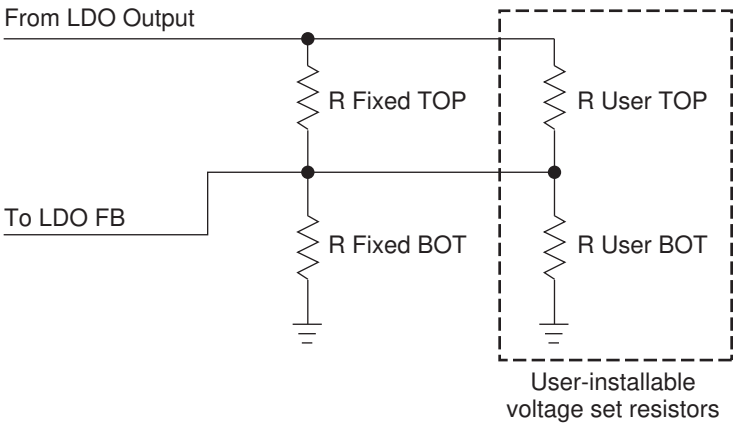


Table 2. VCCOX LDO Adjustments

VCCOX	R Fixed TOP	R Fixed BOT	R User TOP	R User BOT
2.5V	127.0K	110.0K	DNP	DNP
3.3V	127.0K	110.0K	DNP	200.0K
1.8V	127.0K	110.0K	110.0K	DNP
1.5V	127.0K	110.0K	402K	DNP

Resistor numbers and physical location can be found in the schematic and bottom silk screen drawing, at the end of this document.

Switches

One push-button reset switch (SW1) is provided to force a reset of the ispPAC-POWR1208 device. When this switch is activated, the power-up cycle of the ispPAC-POWR1208 device is re-started. This, in turn, cycles power to the rest of the board. The ispXPGA device contains power-on reset circuitry, for predicable initialization.

Programming Headers

Separate 1x8 headers are provided to allow independent configuration the ispXPGA and ispPAC devices. Pin 1 of both headers is V_{CC} (red wire from download cable). Table 3 shows the programming header locations.

Table 3. Programming Connectors

Connector	Target Device
JTAG Connector P1	ispPAC-POWR1208
JTAG Connector P2	ispXPGA

I/O Connectors

Connectivity for general-purpose I/O pins is provided by both 2mm DIP headers and Mictor connectors on the underside of the board. Tables 2 and 3 provide locations for the ispXPGA I/Os. Table 4 lists the High-Speed SMA connector locations.

Table 4. I/O Banks 2, 3

P4 (2mm)	J26 (Mictor)	Description	ispXPGA Pin	Notes
1	1	GCLK2	T4	
2	2	GND	—	
3	3	GCLK3	T5	
4	4	GND	—	
5	5	BK3_IO12_LP180_LVDT	AH18	LVDS Transmit Resistor Network
6	6	BK3_IO14_LP182_LVDT	AJ18	LVDS Transmit Resistor Network
7	7	BK3_IO13_LP180_LVDT	AG18	LVDS Transmit Resistor Network
8	8	BK3_IO15_LP182_LVDT	AK18	LVDS Transmit Resistor Network
9	9	BK3_IO10_LP179_LVDT	AF17	LVDS Transmit Resistor Network
10	10	BK3_IO8_LP178_LVDT	AH17	LVDS Transmit Resistor Network
11	11	BK3_IO11_LP179_LVDT	AE17	LVDS Transmit Resistor Network
12	12	BK3_IO9_LP178_LVDT	AG17	LVDS Transmit Resistor Network
13	13	BK3_IO6_LP175_LVDT	AK17	LVDS Transmit Resistor Network
14	14	BK3_IO0_LP172_LVDT	AK16	LVDS Transmit Resistor Network
15	15	BK3_IO7_LP175_LVDT	AJ17	LVDS Transmit Resistor Network
16	16	BK3_IO1_LP172_LVDT	AJ16	LVDS Transmit Resistor Network

Table 4. I/O Banks 2, 3 (Continued)

P4 (2mm)	J26 (Mictor)	Description	ispXPGA Pin	Notes
17	17	BK3_IO2_LP173_LVDT	AH16	LVDS Transmit Resistor Network
18	18	BK3_IO4_LP174_LVDT	AF16	LVDS Transmit Resistor Network
19	19	BK3_IO3_LP173_LVDT	AG16	LVDS Transmit Resistor Network
20	20	BK3_IO5_LP174_LVDT	AE16	LVDS Transmit Resistor Network
21	21	BK3_IO16_LP187_LVDT	AE18	LVDS Transmit Resistor Network
22	22	BK2_IO16_LP134_LVDR	AG8	100Ω LVDS Receive Termination
23	23	BK3_IO17_LP187_LVDT	AD18	LVDS Transmit Resistor Network
24	24	BK2_IO17_LP134_LVDR	AH8	100Ω LVDS Receive Termination
25	—	GND	—	
26	—	GND	—	
27	25	BK2_IO0_LP116_LVDR	AG5	100Ω LVDS Receive Termination
28	26	BK2_IO10_LP123_LVDR	AG7	100Ω LVDS Receive Termination
29	27	BK2_IO1_LP116_LVDR	AH5	100Ω LVDS Receive Termination
30	28	BK2_IO11_LP123_LVDR	AH7	100Ω LVDS Receive Termination
31	29	BK2_IO18_LP135_LVDR	AJ7	100Ω LVDS Receive Termination
32	30	BK2_IO4_LP118_LVDR	AG6	100Ω LVDS Receive Termination
33	31	BK2_IO19_LP135_LVDR	AK7	100Ω LVDS Receive Termination
34	32	BK2_IO5_LP118_LVDR	AH6	100Ω LVDS Receive Termination
35	33	BK2_IO14_LP129_LVDR	AJ6	100Ω LVDS Receive Termination
36	34	BK2_IO6_LP121_LVDR	AJ5	100Ω LVDS Receive Termination
37	35	BK2_IO15_LP129_LVDR	AK6	100Ω LVDS Receive Termination
38	36	BK2_IO7_LP121_LVDR	AK5	100Ω LVDS Receive Termination
39	37	BK2_IO2_LP117_LVDR	AJ4	100Ω LVDS Receive Termination
40	38	BK2_IO8_LP122_LVDR	AE7	100Ω LVDS Receive Termination
41	—	BK3_IO2_LP117_LVDR	AH16	100Ω LVDS Receive Termination
42	—	BK2_IO9_LP122_LVDR	AF7	100Ω LVDS Receive Termination
43	—	GND	—	
44	—	GND	—	
45	—	BK3_IO20_LP189	AH19[1]	
46	—	BK3_IO21_LP189	AG19[1]	
47	—	BK3_IO22_LP190	AK20[1]	
48	—	BK3_IO23_LP190	AJ20[1]	
49	—	GND	—	
50	—	GND	—	

1. Available on the ispXPGA 1200 only.

Table 5. I/O Banks 6, 7

P6 (2mm)	J28 (Mictor)	Description	ispXPGA Pin	Notes
1	1	GCLK6	R27	100Ω LVDS Receive Termination
2	2	GCLK7	R26	100Ω LVDS Receive Termination
3	—	GND	—	
4	—	GND	—	
5	3	BK6_IO0_INITB	D26	
6	4	BK6_IO1_CCLK	C26	
7	5	BK6_IO4_CSB	D25	
8	6	BK6_IO5_READ	C25	
9	7	BK6_IO8_LP350	F24	
10	8	BK6_IO9_LP350	E24	
11	9	BK6_IO10_LP351	A25	
12	10	BK6_IO11_LP351	B25	
13	11	BK6_IO32_DATA7	F20	
14	12	BK6_IO33_DATA6	E20	
15	13	BK6_IO36_DATA5	F19	
16	14	BK6_IO37_DATA4	E19	
17	15	BK6_IO50_DATA3	F17	
18	16	BK6_IO51_DATA2	E17	
19	17	BK6_IO54_DATA1	B17	
20	18	BK6_IO55_DATA0	A17	
21	19	PGMF	A28	10KΩ Resistor to V_{CCJ}
22	20	DONE	B28	Drives LED, See Figure 8.
23	21	CFG0	C27	10KΩ Resistor to V_{CCJ}
24	22	BK7_IO33_LP429	E10[1]	
25	-	GND	—	
26	-	GND	—	
27	23	BK7_IO34_LP430	A9[1]	49.9Ω to V_{CCOD}
28	24	BK7_IO35_LP430	B9[1]	49.9Ω to V_{CCOD}
29	25	BK7_IO36_LP432	F10[1]	49.9Ω to V_{CCOD}
30	26	BK7_IO37_LP432	G10[1]	49.9Ω to V_{CCOD}
31	27	BK7_IO38_LP433	A8[1]	24.9Ω in Series
32	28	BK7_IO39_LP433	B8[1]	24.9Ω in Series
33	29	BK7_IO40_LP434	D9	24.9Ω in Series
34	30	BK7_IO41_LP434	E9	24.9Ω in Series
35	31	BK7_IO42_LP435	A7	
36	32	BK7_IO43_LP435	B7	
37	33	BK7_IO44_LP439	C8	
38	34	BK7_IO45_LP439	D8	
39	35	BK7_IO48_LP448	E8	
40	36	BK7_IO49_LP446	F8	
41	37	BK7_IO50_LP447	C7	

Table 5. I/O Banks 6, 7 (Continued)

P6 (2mm)	J28 (Mictor)	Description	ispXPGA Pin	Notes
42	38	BK7_IO51_LP447	D7	
43	—	BK7_IO52_LP448	E7	
44	—	BK7_IO53_LP448	F7	
45	—	BK7_IO54_LP449	A5	
46	—	BK7_IO55_LP449	B5	
47	—	BK7_IO56_LP453	C6	
48	—	BK7_IO57_LP453	D6	
49	—	GND	—	
50	—	GND	—	

1. Available on the ispXPGA 1200 only

Table 6. HSI SMA Connectors

SMA	Description	ispXPGA Pin	Notes
J6	SS_CLK_IN_1P	V29	100Ω LVDS Receive Termination
J7	SS_CLK_IN_1N	V30	100Ω LVDS Receive Termination
J11	HSI7A_SINP	N29	100Ω LVDS Receive Termination
J10	HSI7A_SINN	N30	100Ω LVDS Receive Termination
J15	HSI7B_SINP	L30	100Ω LVDS Receive Termination
J14	HSI7B_SINN	L29	100Ω LVDS Receive Termination
J19	HSI8A_SINP	L26	100Ω LVDS Receive Termination
J18	HSI8A_SINN	L25	100Ω LVDS Receive Termination
J23	HSI8B_SINP	H30[1]	100Ω LVDS Receive Termination
J22	HSI8B_SINN	H29[1]	100Ω LVDS Receive Termination
J8	HSI1A_SOUTP	H1[1]	
J9	HSI1A_SOUTN	H2[1]	
J12	HSI1B_SOUTP	K1	
J13	HSI1B_SOUTN	K2	
J16	HSI2A_SOUTP	M1	
J17	HSI2A_SOUTN	M2	
J20	HSI2B_SOUTP	N1	
J21	HSI2B_SOUTN	N2	
J5	SS_CLK_OUT_0P	U2	
J4	SS_CLK_OUT_0N	U1	

1. Available on the ispXPGA 1200 only.

The topside of the board also contains a 14-pin header, which is suitable for connection to an LCD display. 5V Power and GND are provided in addition to 11 I/Os from the ispXPGA device. A contrast control is also available via a 20K-ohm potentiometer mounted near the header. A compatible display is the Optrex DMC16207 (or equivalent) 16x2 character LCD module. Table 7 lists the pin locations for this feature.

Table 7. LCD Header

P3	Description	ispXPGA Pin
1	GND	—
2	+5V	—
3	Contrast	—
4	BK7_IO13_LCD1	D13
5	BK7_IO14_LCD2	B13
6	BK7_IO15_LCD3	A13
7	BK7_IO16_LCD4	F13
8	BK7_IO17_LCD5	G13
9	BK7_IO18_LCD6	A12
10	BK7_IO19_LCD7	B12
11	BK7_IO20_LCD8	C12[1]
12	BK7_IO21_LCD9	D12[1]
13	BK7_IO22_LCDA	A11[1]
14	BK7_IO23_LCDB	B11[1]

1. Available on the ispXPGA 1200 only.

Running the Sample Program

The following example is shown with the ispXPGA 1200 device targeted. To target the ispXPGA 500 device, use the sample program for the ispXPGA 500 and follow the same procedure (selecting LFX500C as appropriate). Both sample programs are available for download from the Lattice web site at www.latticesemi.com/boards.

Requirements

- PC with Lattice ispVM System version 13.1 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). Note: An option to install these drivers is included as part of the ispVM System setup.
- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A or HW-USB-1A)

This sample program consists of a 10-bit counter running from the on-board 20MHz oscillator. The sysCLOCK™ PLL adjusts the internal clock frequency to 70MHz. The 10-bit counter value is routed to output pins as well as a sysHSI™ block, where it is 10b12b encoded and serialized. The outputs for observation are listed in Table .

Table 8. Sample Program Signal Locations

Output	Board Location	Function
Counter[9]	P3, pin 14[1]	Counter MSB output
Counter[8]	P3, pin 13[1]	
Counter[7]	P3, pin 12[1]	
Counter[6]	P3, pin 11[1]	
Counter[5]	P3, pin 10	
Counter[4]	P3, pin 9	
Counter[3]	P3, pin 8	
Counter[2]	P3, pin 7	
Counter[1]	P3, pin 6	
Counter[0]	P3, pin 5	Counter LSB output
cslock	P3, pin 4	CSPLL Lock Indicator from sysHSI Block

Table 8. Sample Program Signal Locations (Continued)

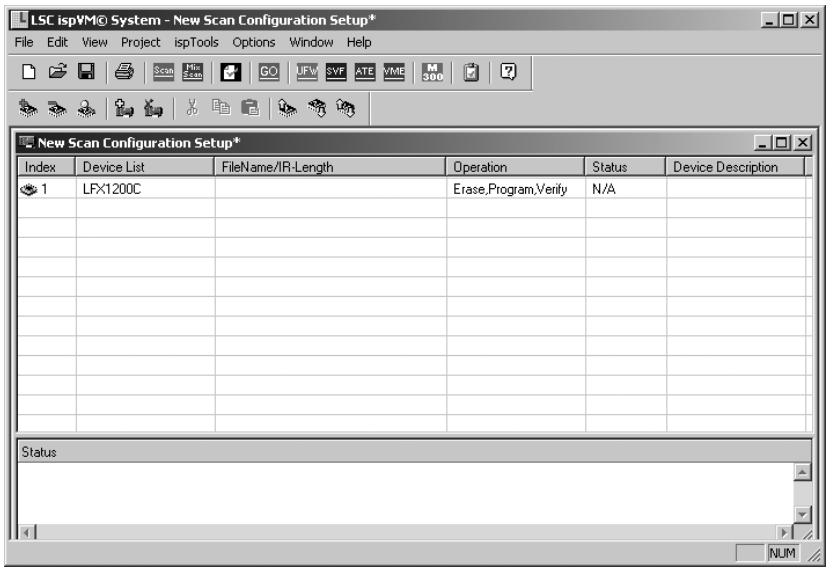
Output	Board Location	Function
sout_p	SMA J8[1]	High-speed Serial Output, Positive Polarity (LVDS).
sout_n	SMA J9[1]	High-speed Serial Output, Negative Polarity (LVDS).
sout_p	SMA J12[2]	High-speed Serial Output, Positive Polarity (LVDS).
sout_n	SMA J13[2]	High-speed Serial Output, Negative Polarity (LVDS).

1. ispXPGA 1200 only
2. ispXPGA 500 only

Download Procedures

1. Connect the ispXPGA Evaluation Board to the AC adaptor or an external 5V supply.
2. Connect the ispDOWNLOAD cable to connector P2 to access the ispXPGA device. Pin 1 corresponds to V_{CC} (red wire on cable).
3. Start the ispVM System software.
4. Click the 'SCAN' button located in the toolbar. The ispXPGA should be automatically detected. The resulting screen should be similar to Figure 3.

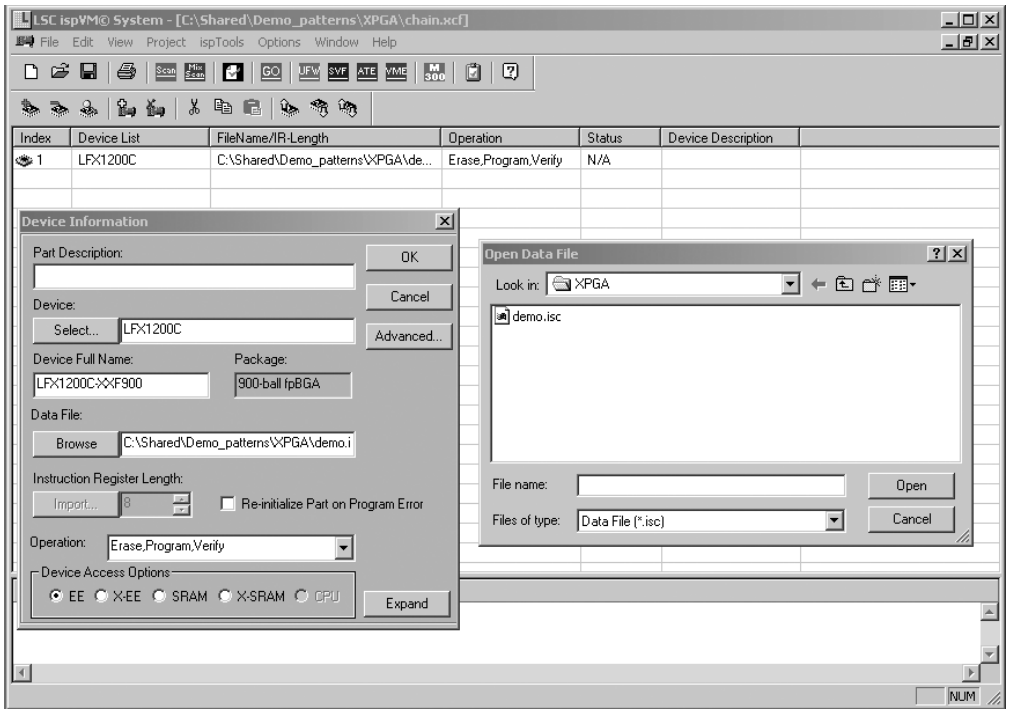
Figure 3. ispVM System Interface



5. Double-click the device to open the properties dialog, as shown in Figure 4.

In the device properties dialog, click the Browse button located under 'Data File'. Locate the 'demo.isc' file. Click OK to both dialog boxes.

Figure 4. Selecting the Data File



6. Click the green 'GO' button. This will begin the download process into the device.

Once the download is complete, the counter outputs, CSLOCK signal, and high speed data should be viewable in the corresponding locations.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-408-826-6002 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Appendix A. Schematics

Figure 5. Lattice ispXPGA Evaluation Board Schematic

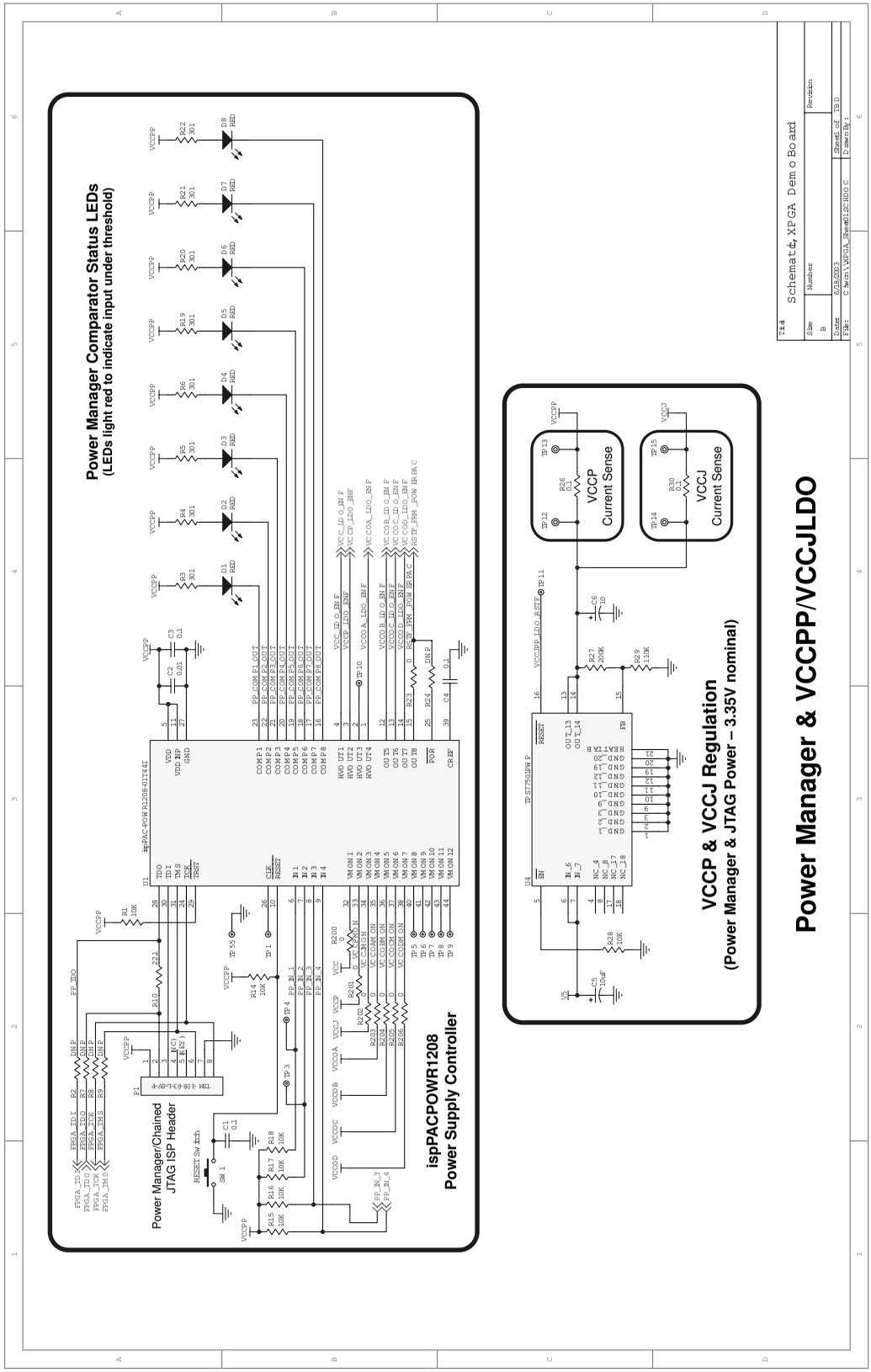


Figure 6. Lattice ispXPGA Evaluation Board Schematic

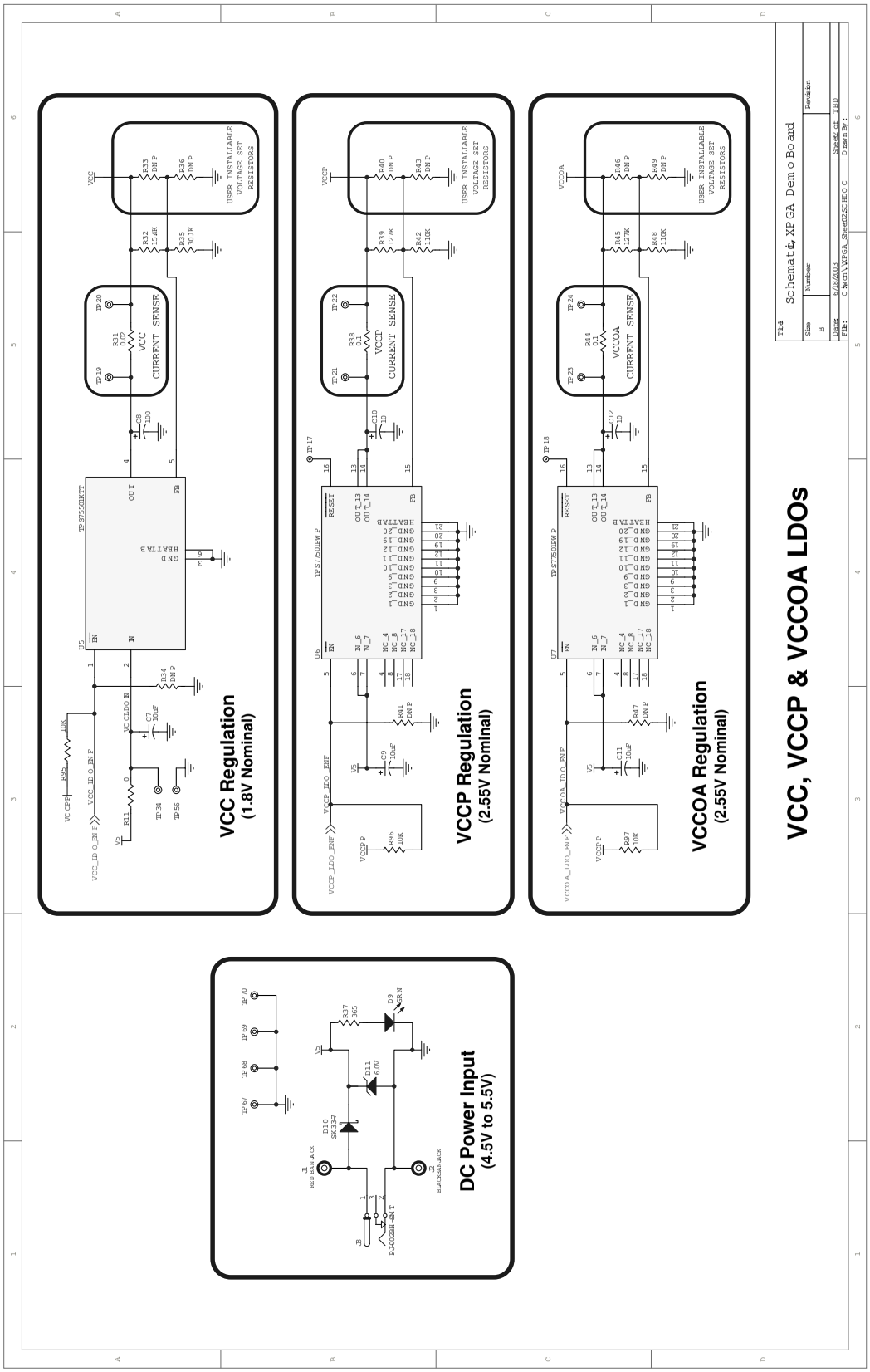
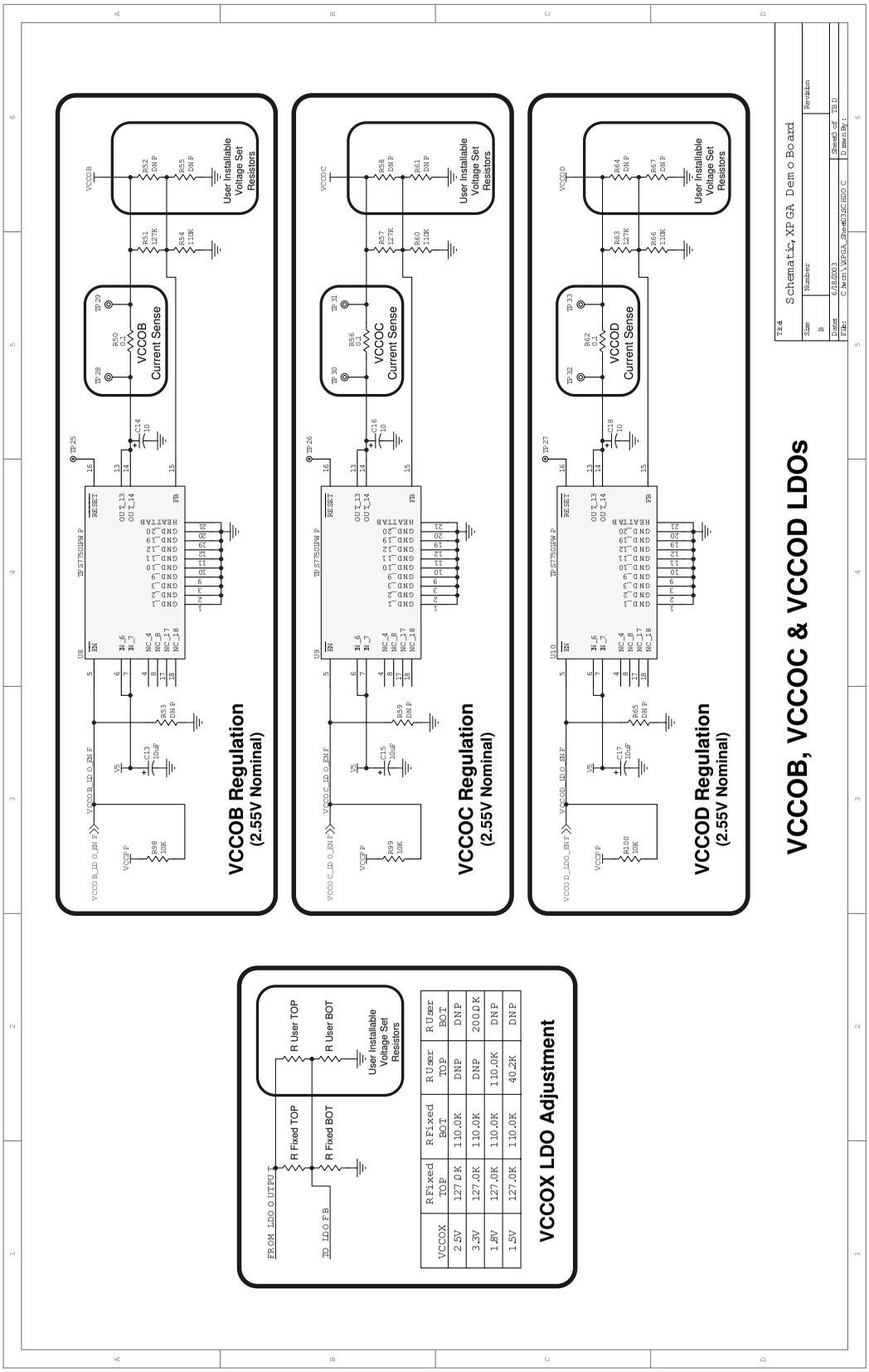


Figure 7. Lattice ispXPGA Evaluation Board Schematic



VCCOX	RFixed TOP	RFixed BOT	RUser TOP	RUser BOT
2.5V	127.0K	110.0K	DNP	DNP
3.3V	127.0K	110.0K	DNP	200.0K
1.8V	127.0K	110.0K	110.0K	DNP
1.5V	127.0K	110.0K	40.2K	DNP

Figure 8. Lattice ispXPGA Evaluation Board Schematic

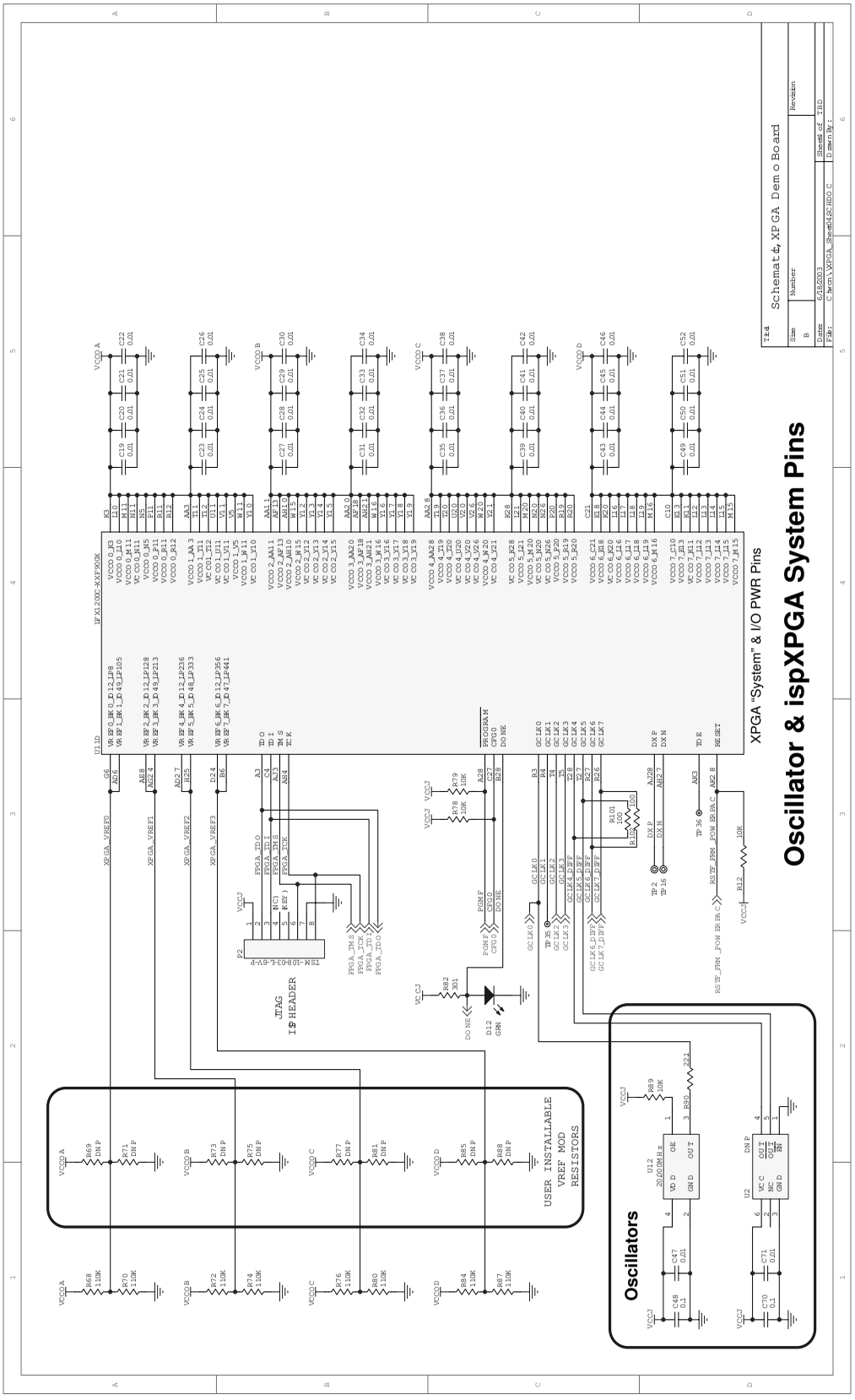


Figure 9. Lattice ispXPGA Evaluation Board Schematic

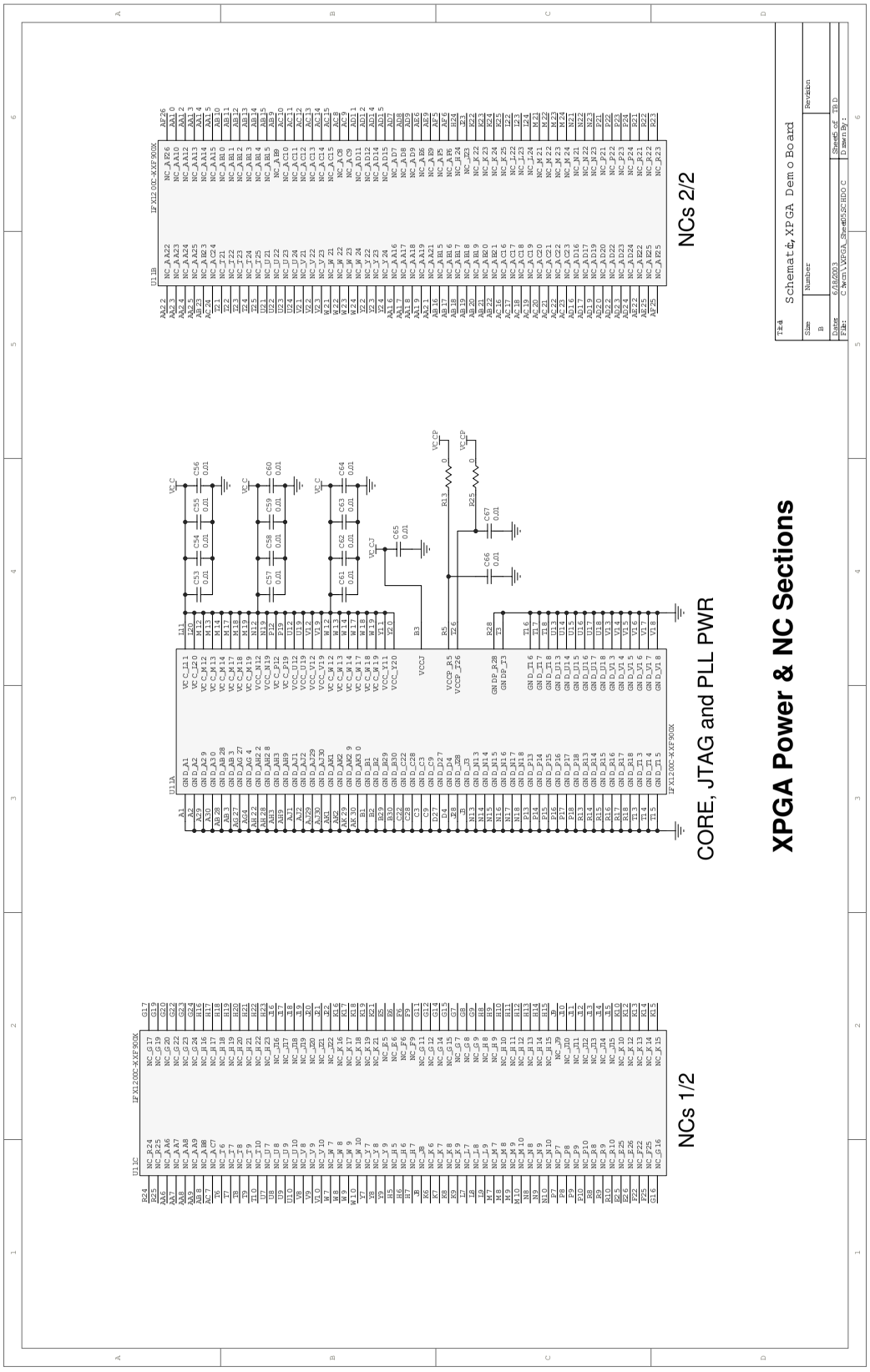


Figure 10. Lattice ispXPGA Evaluation Board Schematic

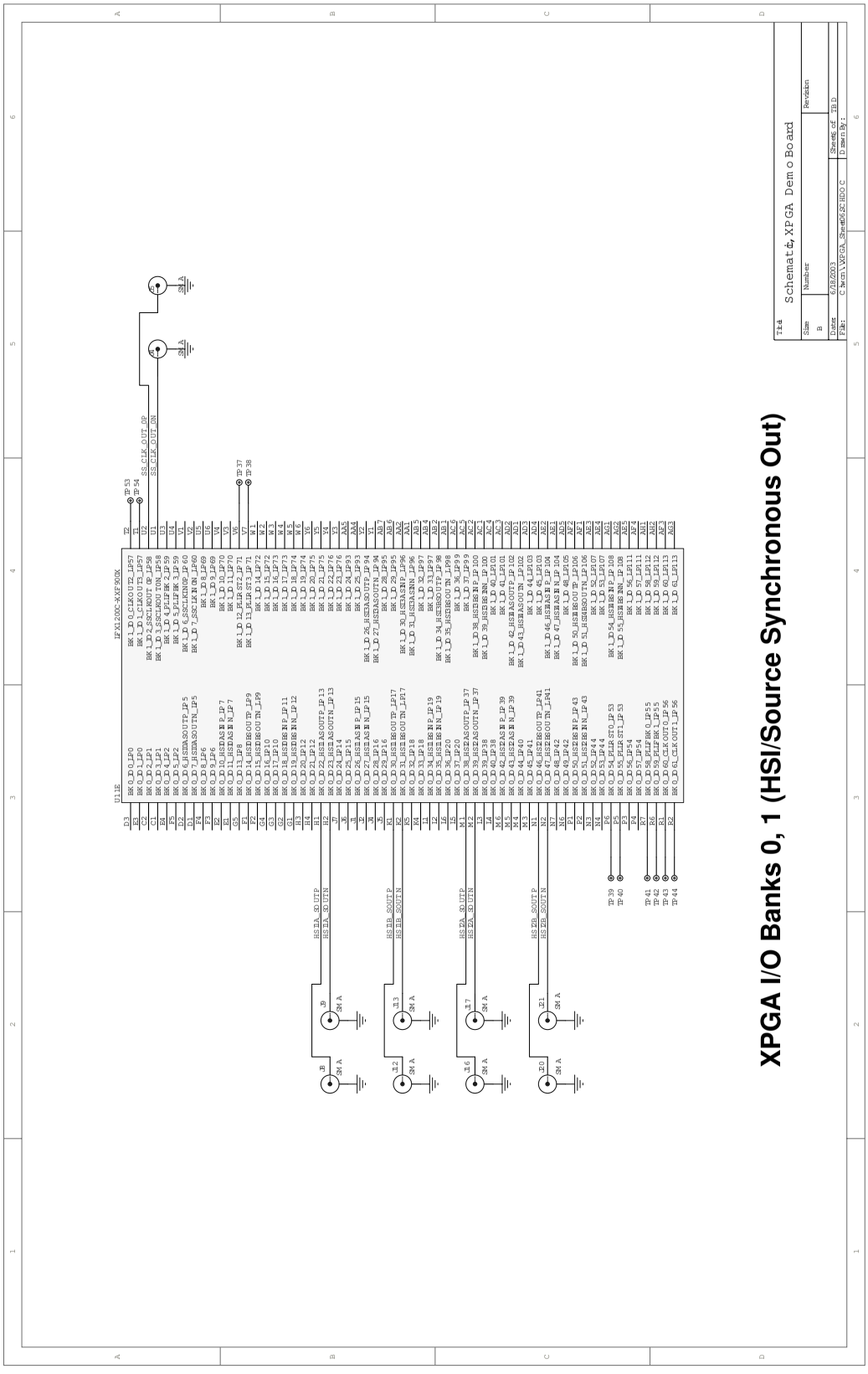


Figure 11. Lattice ispXPGA Evaluation Board Schematic

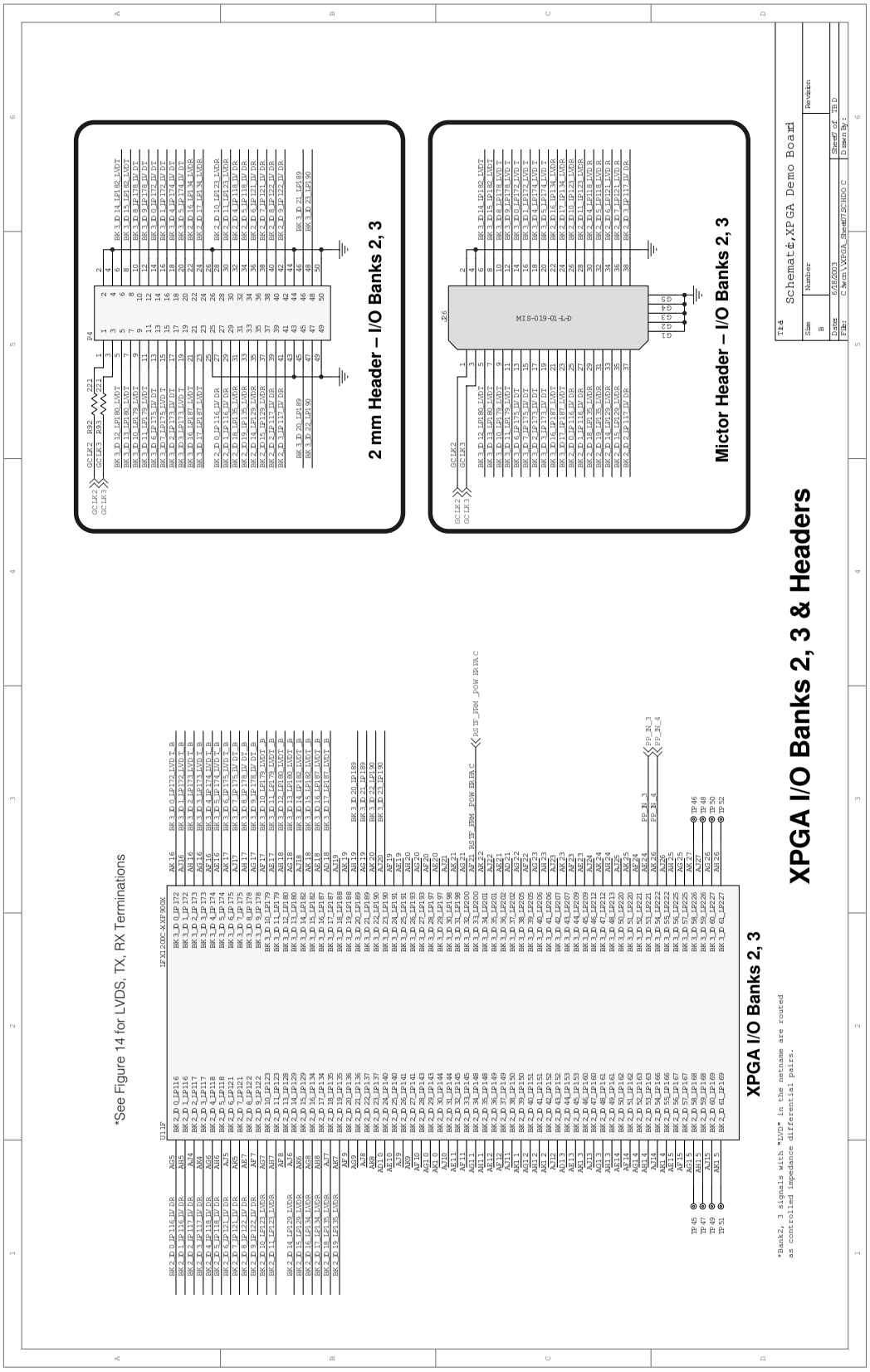


Figure 12. Lattice ispXPGA Evaluation Board Schematic

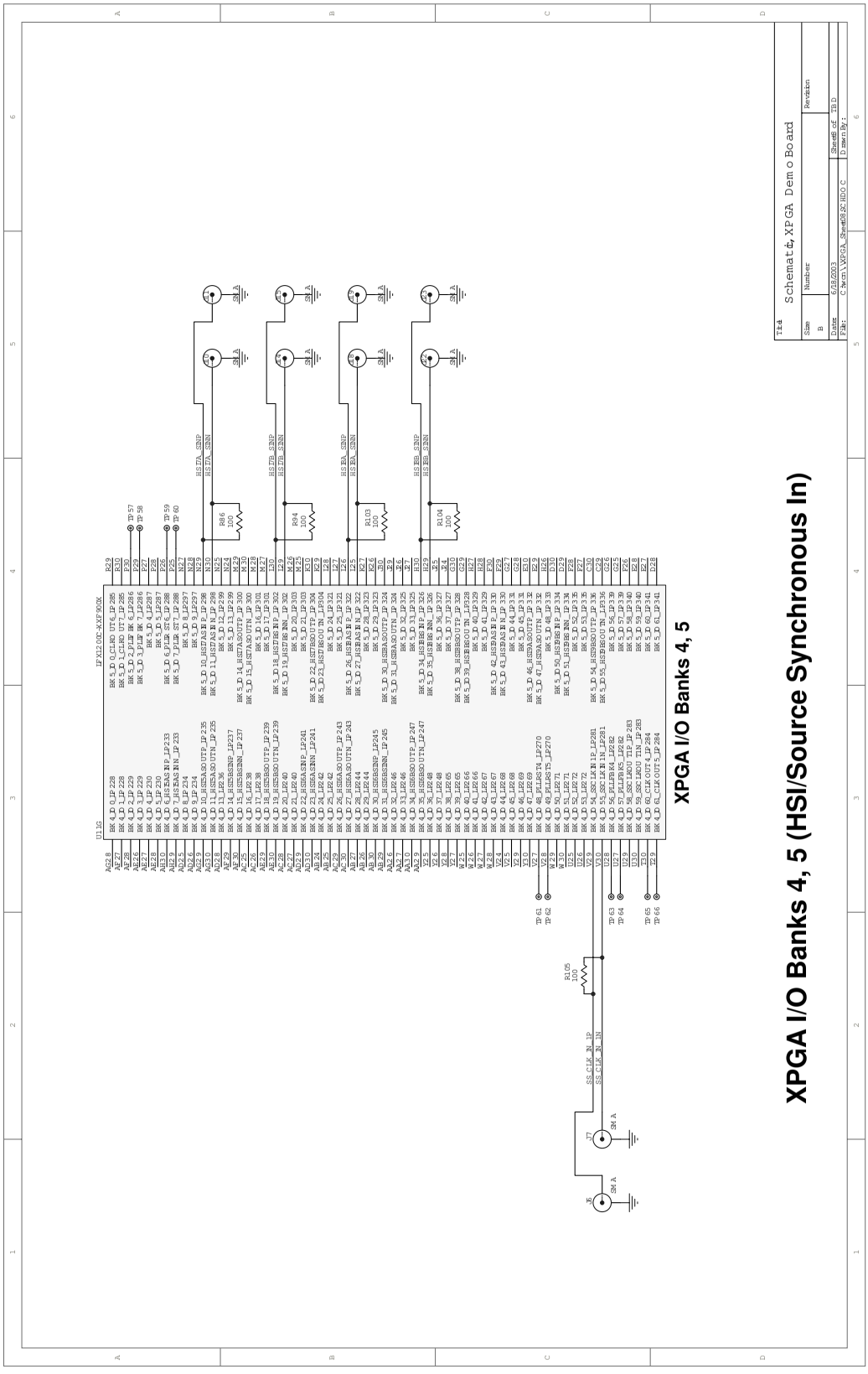


Figure 13. Lattice ispXPGA Evaluation Board Schematic

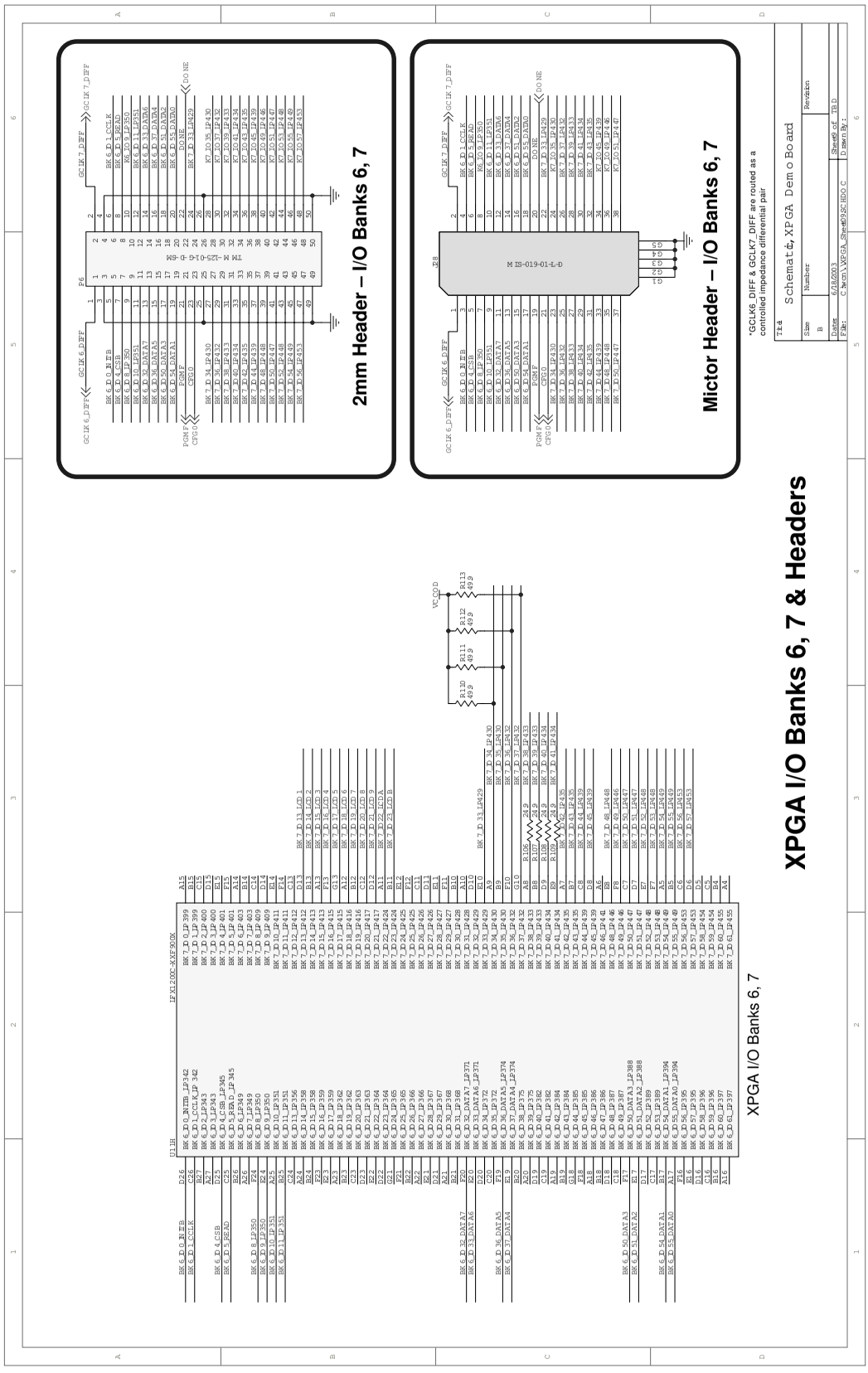
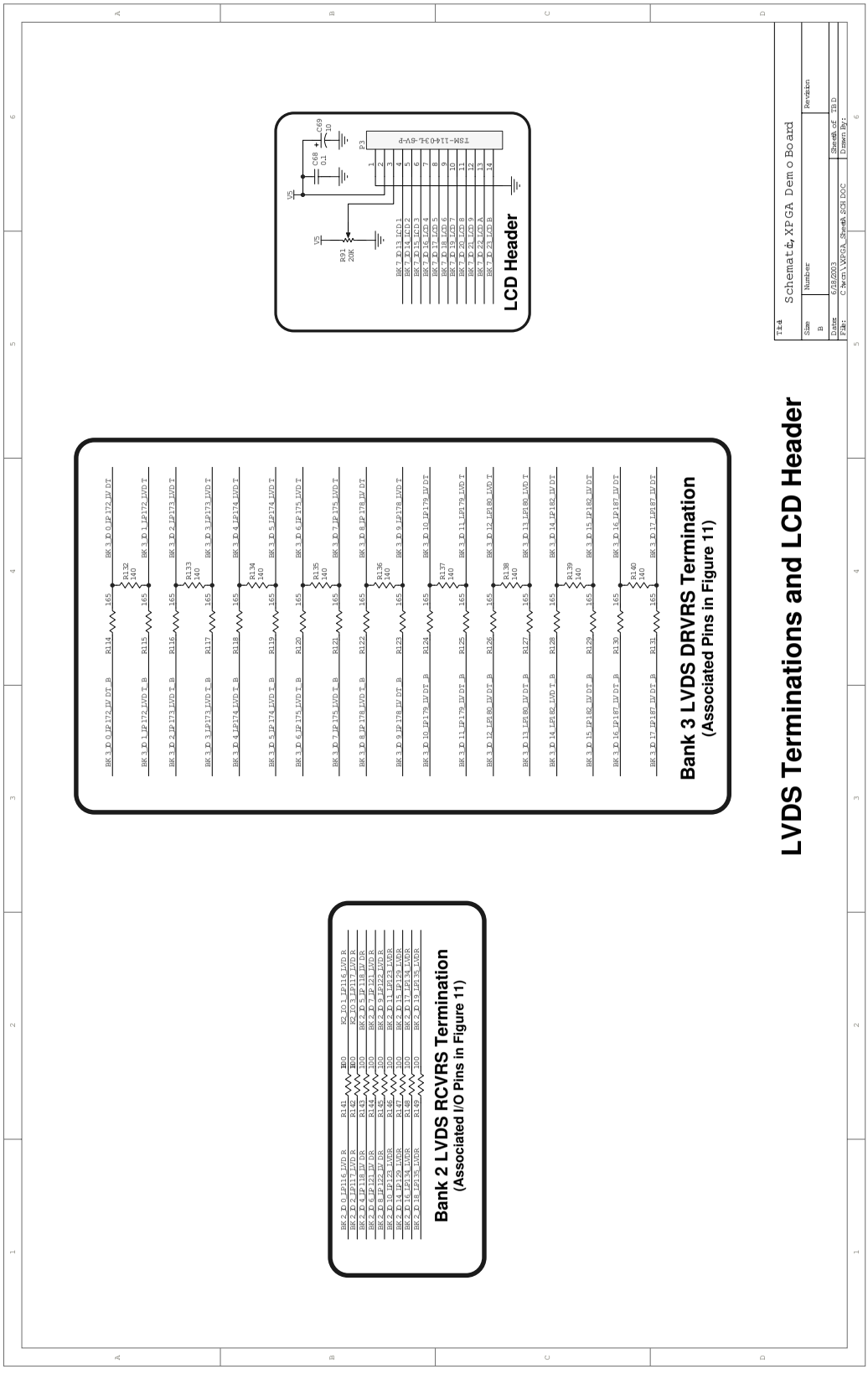


Figure 14. Lattice ispXPGA Evaluation Board Schematic



Appendix B. Bottom Silkscreen Drawing