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LatticeECP3™ I/O Protocol Board – Revision C

User's Guide

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Introduction

The LatticeECP3™ I/O Protocol Board provides a convenient platform to evaluate, test and debug user designs and IP cores targeted for the LatticeECP3-150 FPGA. The board features a LatticeECP3-150 FPGA in the 1156 fpBGA package. The LatticeECP3 I/Os are connected to a rich variety of both generic and application-specific interfaces described later in this document.

Important: *This document (including the schematics in the appendix) describes LatticeECP3 I/O Protocol Boards marked as* ***Rev C****. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo.*

The LatticeECP3 is a third-generation device utilizing reconfigurable SRAM logic technology optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. The LatticeECP3 devices also provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), and advanced configuration support, including encryption, multi-boot capabilities and TransFR™ field upgrade features. The LatticeECP3 SERDES dedicated PCS functions, high jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII), SATA I/II, OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

For a full description of the LatticeECP3 FPGA, see the Lattice website at www.latticesemi.com for the LatticeECP3 Family Data Sheet, technical notes and more.

Some common uses for the LatticeECP3 I/O Protocol Board include:

- Applications requiring large DDR3 memory width and depth
- High-speed parallel ADC/DAC Interface
- SERDES data transfer with external devices
- 1000base-T PHY/RJ45 networking
- A single-board computer system
- A platform for evaluating the Input/Output (I/O) characteristics of the FPGA
- A platform for evaluation and development with Lattice IP cores

Features

Key features of the LatticeECP3 I/O Protocol Board include:

- SPI Serial Flash device included for low-cost, non-volatile LatticeECP3 configuration storage
- Two 64-bit DDR3 DIMM module sockets
- Tri-speed (10/100/1000 Mbit) Ethernet PHY with RJ-45 (includes 12 core magnetics)
- USB 2.0 transceiver
- Built-in USB 2.0 download for LatticeECP3 and ispPAC® bitstreams.
- Also includes ispDOWNLOAD™ JTAG headers for LatticeECP3, ispPAC, and MachXO™ bitstreams
- High-speed HMZD connector with 80 differential pair connections and selectable VTT voltage
- 8-pin DIP switch and three user-definable debounced pushbuttons
- Discrete LEDs and 7-segment LED
- LCD module connector

- Prototyping areas with 125 spare test point I/O pins
- 1 selectable user I/O bank voltage with access to 2 VREF test points
- Logic analyzer probe connection
- 5 pairs of high-speed differential I/O using SMA connectors
- 5 crystal oscillators
- 2 selectable high-speed differential external clock sources with PLL feed back inputs
- 4 channels (1 quad) of differential SERDES (TX and RX) using SMA connectors
- 1 high-current high-speed I/O connection using an SMA connector
- 3.3V, 2.5V, 1.5V, 1.2V and DDR3 voltages are generated from a single 12V power source
- 3 fixed or adjustable DDR3 reference voltages
- 1 Mbit serial EEPROM for general data storage over I^2C bus
- Power Manager II ispPAC-POWR1220AT8 chip for monitoring input power and regulator outputs to be within nominal tolerance with programmable trims
- ispVM™ System programming support
- Multi-board JTAG programming capability and sysCONFIG™ connector

General Description

The heart of the board is the LatticeECP3 FPGA. The board also provides several different interconnections and support devices that permit it to be used for a variety of purposes. The DDR3 sockets, and Tri-speed Ethernet PHY are useful for applications using Lattice IP cores.

A number of connectors are useful for general purpose LatticeECP3 I/O capability. These include the SMA, USB, Ethernet PHY, LCD connector, and the various generic prototype access points.

Other features on the board help in evaluating the capabilities and performance of the LatticeECP3. The 4 channels of SERDES PCS allow straight forward, flexible, high data rate connections to external devices. The various SMA connectors permit the evaluation of high-speed differential signals, and protocols. The HMZD connector provides a wide parallel data path for up to 80 high-speed differential signal connections with easy bench top board to board plug in expansion with low signal skew. The SPI memory showcases the fail-safe capabilities of the LatticeECP3.

The board also acts as a showcase for the ispPAC-POWR1220 Power Manager. The ispPAC-POWR1220 is a programmable device useful for safely managing the power supply system on the board. It can be programmed to sequence, monitor, and adjust the voltages on the LatticeECP3 I/O Protocol Board.

Additional resources for the LatticeECP3 I/O Protocol Board, such as updates to this document, sample programs and links to demos can be found on the Lattice web site. Go to www.latticesemi.com/boards, and navigate to the appropriate page for this board.

Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: *The devices on the board can be damaged by improper handling.*

The devices on the evaluation board contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static sensitive to conditions that exceed their

designed-in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation board when it is removed from the static shielding bag. If you will not be using the board for a while, it's best to put it back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the board when it is not in use.

When reaching for the board, it is recommended that you first touch the outside threaded portion of one of the gold SMA connectors. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: *To minimize the possibility of ESD damage, the first and last electrical connection to the board, should be always be from test equipment chassis ground to GND on the board (left side post of TB1 labeled GND on the board).*

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the GND on the board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged, should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board when it is not in a static shielding bag, please keep one finger on the threaded portion of one of the gold SMA connectors. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back inside.

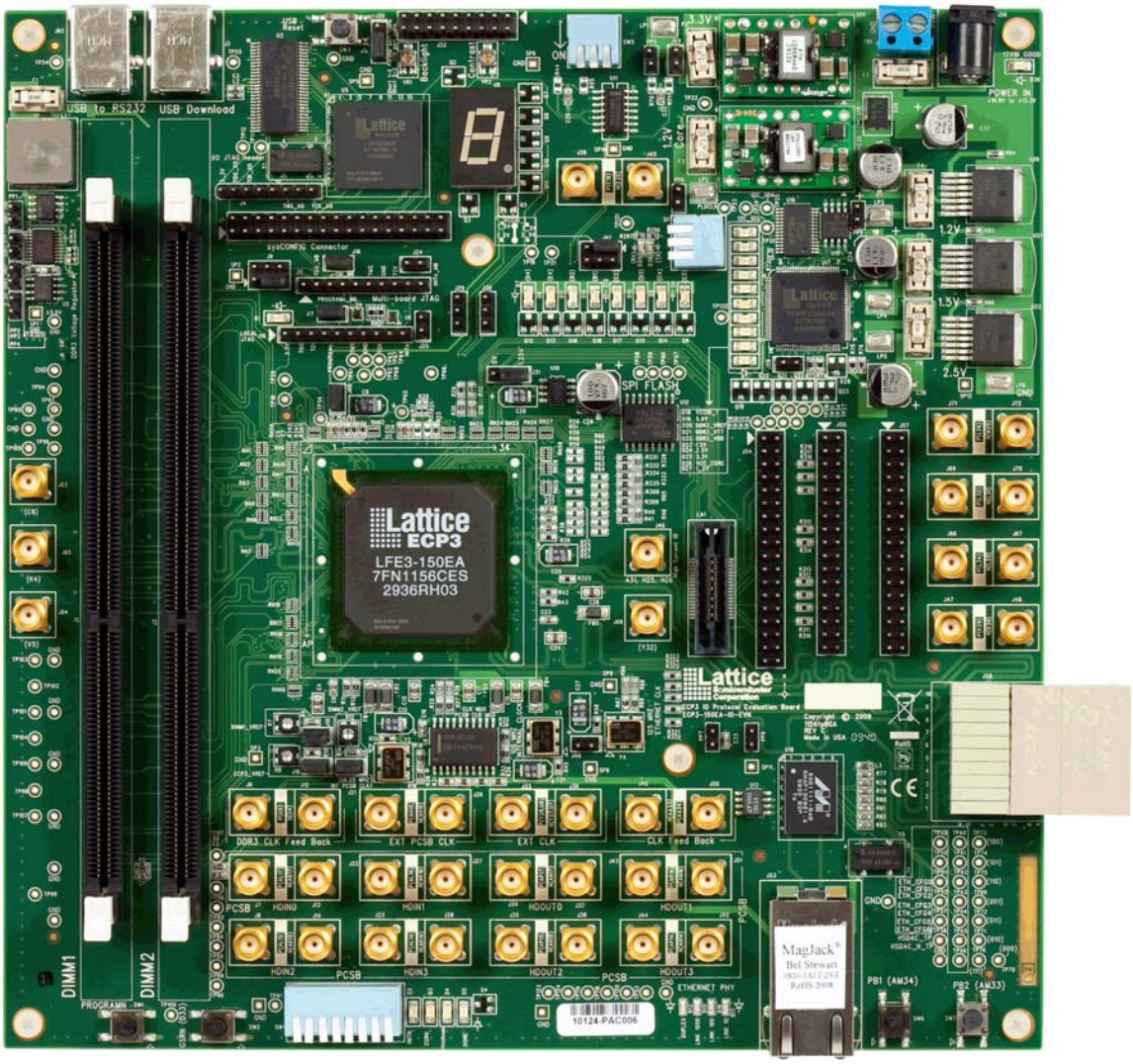
Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 8 inches by 8 inches. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: <95% without condensation
- 12V +/-10% DC (20 watts max.)

Functional Description

Figure 1. LatticeECP3 I/O Protocol Board



LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V DC core in a 1156-ball fpBGA package. The default device is the LatticeECP3-150. The LatticeECP3-95 device density in this package can be accommodated but will incur some loss of board level signal I/O functionality. A complete description of these devices can be found in the LatticeECP3 Family Data Sheet.

Power Setup

The board is supplied by a single 12V +/-10% DC power supply while on-board regulators will provide the necessary supply voltages: 3.3V, 2.5V, 1.5V, 1.2V, and 0.75V. The DC power may be applied through the power jack at J56 using an AC adapter with 12V +/-10% DC output range. The requirements for the J56 power jack are listed in Table 1.

Table 1. Power Jack J56 Specifications

Polarity	Positive Center
Inside Diameter	0.1" (2.5mm)
Outside Diameter	0.218" (5.5mm)
Current Capacity	Up to 1.7A

Other than using the AC adapter, the DC power may also be applied using a workbench power supply through the terminal block at TB1 (12_0VIN, GND). The workbench power supply voltage has to be between 10.8V and 13.2V for normal operation of switching power supply modules U14 and U15. If the 12V power source is outside the normal voltage range, the row of LEDs next to the ispPAC (U17) will all blink if the topmost lever of S1 is up. The 12V input voltage out of range LED blink warning can be disabled by pushing the topmost lever of S1 down. It is recommended that if you are using a power source that initiates the LED blink warning, that you first investigate the source of the out of tolerance voltage condition and correct it rather than disable the warning. For example, some small wall mount power supplies produce 14V or more while under lightly loaded conditions, if they produce too high of an input voltage, the 12V switching regulators could be damaged.

Power may also be supplied directly for each individual supply rail using test point connections. To enable this mode of operation, the appropriate fuses must be removed and S1 should be set as indicated in Table 3. All power sources must be regulated to the specifications in Table 2.

Table 2. Individual Control of Supplies

Supply	Test Points	Fuse	Requirement
3.3V	PP5	F2 (5A)	3.3V +/- 5%
2.5V	PP8	F6 (5A)	2.5V +/- 5%
1.5V	PP7	F5 (5A)	1.5V +/- 5%
1.2V	PP9	F4 (5A)	1.2V +/- 5%
VCC_CORE	PP6	F3 (5A)	1.2V +/- 5%
DDR3_VDD	PP1	F1 (10A)	1.5V +/- 5%
DDR3_VTT	PP2	—	0.75V +/- 5%
DRR3_VREF	PP3	—	0.75V +/- 5%

Table 3. S1 Switch Settings

Switch S1			
Topmost Lever	Middle Lever	Lowest Lever	Disable Selected Supply
UP	UP	UP	All regulators on, enable 12V blink warning
UP	UP	DOWN	DDR3
UP	DOWN	UP	2.5V
UP	DOWN	DOWN	1.5V
DOWN	UP	UP	All regulators on, disable 12V blink warning
DOWN	UP	DOWN	1.2V
DOWN	DOWN	UP	VCC_CORE
DOWN	DOWN	DOWN	Disable all regulators except 3.3V

The reference voltages for the DDR3 module sockets and LatticeECP3 can be set to a regulated 0.75V source by adding jumpers to J15, J16 and J19. With no jumpers on J15, J16 or J19, the DDR3 reference voltages can be individually set to adjustable voltages using the potentiometers R7, R8 and R12 to provide 0.75V +/- 0.22V adjustment range.

Power Voltage Sequencing, Monitoring, and Trimming

A Lattice ispPAC Power Manager II device, the ispPAC-POWR1220AT8, is used for sequencing, monitoring, and trimming various voltages on the board. When power is first applied, the ispPAC control outputs are tri-stated so transistors Q19, Q20, Q21, Q22 and Q23 are on, which disables the 2_5v, 1_5v, DDR3, VCC_CORE, and 1_2v voltage regulator outputs. The ispPAC device then turns on all supplies that are not disabled by the S1 switch setting.

Once the regulators are enabled, there are ten "Power Good" LEDs used to indicate the status of the monitored regulator voltages. If an individual monitored voltage is not in the normal voltage range, the corresponding power good LED will be OFF, otherwise that LED will stay ON. Table 4 shows the ten monitored voltages and the corresponding LEDs.

Table 4. Individual Monitoring of 12 Power Voltages

Voltage	LED	Power Good Voltage Range
1_2V	D27	1.2V +/- 5%
VCC_CORE	D26	1.2V +/- 5%
3_3V	D25	3.3V +/- 5%
2_5V	D24	2.5V +/- 5%
1_5V	D23	1.5V +/- 5%
DDR3_VDD	D22	1.5V +/- 5%
DDR3_VTT	D21	0.75V +/- 5%
DDR3_VREF	D20	0.75V +/- 5%
5_0V	D19	5.0V +/- 5%
VCCIO_1	D18	3.3V +5%, 1.2V - 5%
12_0V, 12_0VIN	ALL	12.0V +/- 10%

For the 12_0V and 12_0VIN supply voltages, all LEDs will indicate normally when the input power is 12.0v +/-10%. When the 12V input voltage is outside the normal range, all LEDs above will blink to warn that the 12V switching regulator modules (U14 and U15) are outside their normal operation range. As discussed above, the LED blink warning can be disabled by pushing down the topmost lever of S1.

Power Voltage Adjustment and Control

The ispPAC-POWR1220AT8 can also adjust the power supply voltages: 3_3V, 2_5V, 1_5V, 1_2V, VCC_CORE, and DDR3_VDD by +/- several percent from the nominal value using 6 of the built-in DAC trim outputs TRIM[1..8]. The ispPAC-POWR1220AT8 factory programming is set for open loop trim adjustment of the regulator voltages.

The ispPAC-POWR1220AT8 monitor inputs are aligned with the trim outputs should a user wish to experiment with the ispPAC-POWR1220AT8 closed loop trim compatibility. The ispPAC-POWR1220AT8 can also be set up to do an external closed loop trim by removing the two shorting resistors R292 and R293 and applying the external voltages to TP47 and TP48 while ensuring that externally applied voltages to the ispPAC-POWR1220AT8 do not exceed the 3_3v supply voltage. The trim outputs to control the external supplies are then available at TP29 and TP35. Additionally the 3_3v and 5_0v supplies can be enabled or disabled using the HVOUT1 and HVOUT 2 outputs from the PAC device when the jumpers on headers J49 and J61 are removed.

LatticeECP3 I/O Bank Voltage Setting

The jumper listed in Table 5 allows the user to select the bank 1 VCCIO voltage applied to the LatticeECP3 device. All other bank VCCIO voltages are hard wired as shown in Table 6. Certain restrictions for VCCIO1 apply depending on which features of the board are being used.

Table 5. VCCIO Selection Jumper

sysIO™ Bank	Jumper	Jumper on Pins
1	J41	1-3 -> 3.3V 2-4 -> 2.5V 3-5 -> 1.5V 4-6 -> 1.2V None -> External

Table 6. sysIO Bank Voltages

sysIO Bank	Bank Voltage
0	1.5V
1	(J41 selects)
2	2.5V
3	2.5V
SERDES	1.2V or 1.5V
6	1.5V
7	1.5V
8	3.3V

Depending on the optional devices installed, some sysIO™ banks may have restrictions. For J41 only select one bank voltage position at the jumper. For example, attaching more than one jumper to J41's 6 square pins could short supplies. You can also remove the jumper on J41 and apply an external voltage to pins 3 and 4 of J41. When applying an external voltage to J41, do not exceed the LatticeECP3 Family Data Sheet-specified absolute maximum rating for Output Supply Voltage VCCIO range of -0.5V to +3.75V, or damage to the device may occur.

Table 7. sysIO Bank Considerations

Bank	Setting
1	Selectable, LCD may require 3.3V.

The following tables detail the various I/O standards supported by the LatticeECP3 sysIO structures. More information can be found in TN1177, LatticeECP3 sysIO Usage Guide.

Table 8. Mixed Voltage I/O Support

	Input sysIO Standards					Output sysIO Standards				
VCCIO	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

For example, if VCCIO is 3.3V then signals from devices powered by 1.2V, 2.5V, or 3.3V can be input and the thresholds will be correct, assuming the user has selected the desired input level using ispLEVER® software. Output levels are tied directly to VCCIO.

Table 9. sysIO Standards Supported per Bank

Description	Top Side Banks 0-1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
Types of I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Single-Ended Standards Outputs	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL15 SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I HSTL18_I, II	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL15 SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I HSTL18 Class I, II	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL15 SSTL18 Class I, II SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I HSTL18 Class I, II	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL15 SSTL18 Class I, II SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I HSTL18 Class I, II
Differential Standards Outputs	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II LVDS[2] RSDS[2] Mini-LVDS[2] PPLVDS[2] (point-to-point) LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II, SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II, SSTL33D_I, II HSTL15D Class I HSTL18D Class I, II LVDS[2] RSDS[2] Mini-LVDS[2] PPLVDS[2] (point-to-point) LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]
Inputs	All Single-ended and Differential TRLVDS (Transition Reduced LVDS)	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Hot Socketing	Yes	Only on Bank 8	Yes	No
Equalization on Inputs	No	Yes	No	Yes
ISI Correction	For DDR3 memory	For DDR3 memory	For DDR3 memory	For DDR3 memory
On Chip Termination	No	On-Chip Parallel Termination On-Chip Differential Termination	No	On-Chip Parallel Termination On-Chip Differential Termination
PCI Support	PCI33 with or without clamp	PCI33 with clamp	PCI33 with clamp	PCI33 with clamp

1. These differential standards are implemented by using a complementary LVCMOS driver with the external resistor pack.
2. Available on 50% of the I/Os in the bank.

Prototype Areas

For general purpose I/O testing or monitoring, numerous test points are provided for direct access. Some test points are grouped together and arranged in a grid pattern according to their associated I/O bank and are labeled with the pin locations on the silkscreen of the board. Most test point I/Os are brought out to IDC connectors J54,

J55 and J57 with both source and end type termination resistors available for high-speed signal transmission over ribbon cables.

Differential Signal Connections

There are 17 pairs of SMA connectors and one HMZD connector that provide general purpose high-speed differential signal paths to the LatticeECP3. The SMA connectors are provided for SERDES, clocks and general purpose user-definable signals. The HMZD connector allows quick connection of 80 high-speed differentially paired signals to an external application PCB with low signal skew and good mechanical stability.

Table 10 details the I/O pins to which each SMA connector is wired.

Table 10. SMA Connectors

Location	LatticeECP3 I/O	Polarity	sysIO Bank	Description
J39	E19	P	1	PT76A/PT94A/PCLKT1_0
J45	E20	N	1	PT76B/PT94B/PCLKC1_0
J50	AA34	P	3	PR61E_A/PR79E_A/RLM1_GPLLT_FB_A
J42	AA33	N	3	PR61E_B/PR79E_B/RLM1_GPLLT_FB_B
J6	U5	P	7	PL43E_A/PL61E_A//LUM0_GPLLT_FB_A
J12	U4	N	7	PL43E_B/PL61E_B//LUM0_GPLLT_FB_B
J21	AH15 (from U8)	P	Quad B	PCSB_REFCLKP
J26	AH16 (from U8)	N	Quad B	PCSB_REFCLKN
J33	Y28 (from U8) U6 (from U8)	P	3 7	PR61E_C/PR79E_C/RLM1_GPLLT_IN_A PL43E_C/PL61E_C/LUM0_GPLLT_IN_A
J36	Y27 (from U8) U7 (from U8)	N	3 7	PR61E_D/PR79E_D/RLM1_GPLLT_IN_B PL43E_D/PL61E_D/LUM0_GPLLT_IN_B
J7	AL17	P	Quad B	PCSB_HDINP0
J13	AK17	N	Quad B	PCSB_HDINN0
J22	AL16	P	Quad B	PCSB_HDINP1
J27	AK16	N	Quad B	PCSB_HDINN1
J34	AP17	P	Quad B	PCSB_HDOUTP0
J37	AN17	N	Quad B	PCSB_HDOUTN0
J43	AP16	P	Quad B	PCSB_HDOUTP1
J51	AN16	N	Quad B	PCSB_HDOUTN1
J8	AL15	P	Quad B	PCSB_HDINP2
J14	AK15	N	Quad B	PCSB_HDINN2
J23	AL14	P	Quad B	PCSB_HDINP3
J28	AK14	N	Quad B	PCSB_HDINN3
J35	AP15	P	Quad B	PCSB_HDOUTP2
J38	AN15	N	Quad B	PCSB_HDOUTN2
J44	AP14	P	Quad B	PCSB_HDOUTP3
J52	AN14	N	Quad B	PCSB_HDOUTN3
J71	L26	P	2	NC/PR19A*
J72	M25	N	2	NC/PR19B*
J69	L32	P	2	NC/PR20A*
J70	L31	N	2	NC/PR20B*
J66	L34	P	2	NC/PR23A
J67	L33	N	2	NC/PR23B

Table 10. SMA Connectors (Continued)

Location	LatticeECP3 I/O	Polarity	sysIO Bank	Description
J47	K29	P	2	NC/PR25A*
J48	K30	N	2	NC/PR25B*

HMZD Connector

J58 is a high-speed HMZD header with 80 differential signal connections for interfacing the LatticeECP3 device to an external application PCB such a high-speed ADC/DAC. The signal path as been verified to operate at the 500 MT/s data rate. I/Os connected as LVDS inputs can be terminated to a 1.25V VTT voltage provided by U10 when header J31 pins 1 and 2 are shorted. When pins 2 and 3 of J31 are shorted, the VTT voltage is 0V. You can also apply external VTT voltages to pin 2 of J31. Differentially paired I/Os may also be used in the single-ended mode with some increase in SSO crosstalk. The connections for J58 are listed in Table 11.

Table 11. HMZD Connectors

J58 Pin	LatticeECP3 I/O	Polarity	sysIO Bank	Description
A1	AA31	P	3	PR65A/PR83A*
B1	AA30	N	3	PR65A/PR83B*
A2	AD33	P	3	NC/PR97A*
B2	AD34	N	3	NC/PR97B*
A3	AE30	P	3	PR74A/PR101A*
B3	AE29	N	3	PR74B/PR101B*
A4	AD26	P	3	NC/PR106A*
B4	AD25	N	3	NC/PR106B*
A5	AP33	P	3	PR83A/PR110A*
B5	AP32	N	3	PR83B/PR110B*
A6	K31	P	2	NC/PR32A
B6	K32	N	2	NC/PR32B
A7	T32	P	2	PR35A/PR53A
B7	T31	N	2	PR35B/PR53B
A8	R28	P	2	PR28A*/PR46A*
B8	R27	N	2	PR28B*/PR46B*
A9	R31	P	2	PR29A/PR47A*
B9	R30	N	2	PR29B/PR47B*
A10	N32	P	2	PR20A/PR38A*
B10	N31	N	2	PR20B/PR38B*
C1	W27	P	3	PR55A*/PR73A*
D1	W26	N	3	PR55B*/PR73B*
C2	Y26	P	3	PR61A*/PR79A*
D2	Y25	N	3	PR61B*/PR79B*
C3	AE34	P	3	NC/PR92A*
D3	AE33	N	3	NC/PR92B*
C4	AL30	P	3	PR91A*/PR118A*
D4	AM30	N	3	PR91B*/PR118B*
C5	AJ31	P	3	PR88A*/PR115A*
D5	AK31	N	3	PR88B*/PR115B*
C6	V29	P	3	PR52A*/PR70A*/VREF1_3

Table 11. HMZD Connectors (Continued)

J58 Pin	LatticeECP3 I/O	Polarity	sysIO Bank	Description
D6	W28	N	3	PR52B*/PR70B*/VREF2_3
C7	U32	P	2	PR41A/PR59A
D7	U31	N	2	PR41B/PR59B
C8	W34	P	3	PR47A/PR65A*
D8	W33	N	3	PR47B/PR65B*
C9	L30	N	2	NC/PR34B*
D9	M29	P	2	NC/PR34A*
C10	N26	P	2	PR19A*/PR37A*
D10	P26	N	2	PR19B*/PR37B*
E1	AA25	P	3	PR64A*/PR82A*
F1	AA26	N	3	PR64B*/PR82B*
E2	AA28	P	3	PR70A*/PR88A*
F2	AA27	N	3	PR70B*/PR88B*
E3	AD31	P	3	NC/PR91A*
F3	AD30	N	3	NC/PR91B*
E4	AC28	P	3	NC/PR100A*
F4	AB27	N	3	NC/PR100B*
E5	AM29	P	3	PR97A*/PR124A*
F5	AN29	N	3	PR97B*/PR124B*
E6	U28	P	3	PR46A*/PR64A*/PCLKT3_0
F6	V28	N	3	PR46B*/PR64B*/PCLKC3_0
E7	V31	P	3	PR44A/PR62A
F7	V30	N	3	PR44B/PR62B
E8	P28	P	2	PR25A*/PR43A*
F8	P27	N	2	PR25B*/PR43B*
E9	T29	P	2	PR34A*/PR52A*/VREF1_2
F9	T28	N	2	PR34B*/PR52B*/VREF2_2
E10	N34	P	2	PR23A/PR41A
F10	N33	N	2	PR23B/PR41B
G1	U33	N	2	PR43E_B/PR61E_B/RUM0_GPLLT_FB_B
H1	U34	P	2	PR43E_A/PR61E_A/RUM0_GPLLT_FB_A
G2	Y34	P	3	PR56A/PR74A*
H2	Y33	N	3	PR56B/PR74B*
G3	U26	P	2	PR43A*/PR61A*/PCLKT2_0
H3	U27	N	2	PR43A*/PR61B*/PCLKC2_0
G4	AH33	P	3	PR82A*/PR109A*
H4	AJ33	N	3	PR82B*/PR109B*
G5	AP31	P	3	PR92A/PR119A*
H5	AN31	N	3	PR92B/PR119B*
G6	W32	P	3	PR50A/PR68A
H6	W31	N	3	PR50B/PR68B
G7	R34	P	2	PR32A/PR50A
H7	R33	N	2	PR32B/PR50B

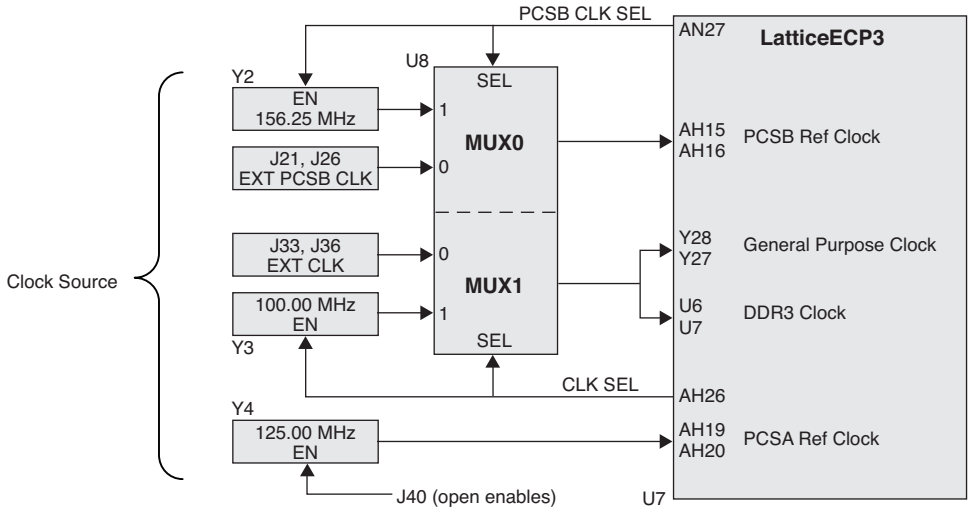
Table 11. HMZD Connectors (Continued)

J58 Pin	LatticeECP3 I/O	Polarity	sysIO Bank	Description
G8	T26	P	2	PR37A*/PR55A*/RUM0_GDLLT_IN_A
H8	T27	N	2	PR37B*/PR55B*/RUM0_GDLLT_IN_B
G9	N30	P	2	PR17A/PR35A
H9	N29	N	2	PR17B/PR35B
G10	P34	P	2	PR26A/PR44A
H10	P33	N	2	PR26B/PR44B

Crystal Oscillators and External Clock Sources

The evaluation board provides 5 dedicated clock sources available for use by a design loaded into the LatticeECP3: 3 crystal oscillators, and 2 pairs of external differential clocks applied through SMA connectors. The selection of internal or external clock sources is done with U8, a high-speed LVPECL multiplexer (MC100LV100VEL56) using the control signals CLK_SEL and PCSB_CLK_SEL. Figure 2 shows how the 5 dedicated clock sources connect to the LatticeECP3.

Figure 2. Dedicated Clock Sources



The CLK_SEL signal sourced from the LatticeECP3 pin AH26 controls U8 to select whether the internal or external clock source will drive the general-purpose and DDR3 clock inputs to the LatticeECP3 device. The PCSB_CLK_SEL signal sourced from the LatticeECP3 pin AN27 controls U8 to select whether the internal or external PCSB clock source will drive the SERDES PCSB reference clock input to the LatticeECP3 device. If either of the control signals CLK_SEL or PCSB_CLK_SEL are un-programmed, the default selections for the U8 mux are to forward the internal clocks Y2 and Y3 to the ECP3. Tables 12 and 13 detail the clock source selections.

Table 12. PSCB SERDES Clock Source Selection

U8 Mux0 Input				LatticeECP3 Input Clock			
Source		Description	LatticeECP3	I/O Pins	Bank	Usage	IO_Type
J21	+	EXT PCSB CLK	AN27 = 0 LVCMOS25	AH15, AH16	SERDES	Reference	CML 50 ohm
J26	–						
Y2 Oscillator		156.25 MHz	AN27 = 1 LVCMOS25				

Table 13. General-Purpose and DDR3 Clock Source Selection

U8 Mux1 Input				LatticeECP3 Input Clock			
Source		Description	LatticeECP3	I/O Pins	Bank	Usage	IO_Type
J33	+	EXT CLK	AH26 = 0 LVCMOS25	Y28, Y27	3	General	LVDS No term
J36	–						
Y3 Oscillator		100 MHz	AH26 = 1 LVCMOS25	U6, U7	7	DDR3	SSTL15D No term

The internal clock sources Y2 and Y3 are crystal oscillators with +/- 50 ppm accuracy that are individually enabled only while the U8 multiplexer is selecting them. The external clock sources are user supplied through SMA connectors at J21, J26, J33, and J36, after which they are AC coupled and 50 ohm terminated at the inputs of the U8 multiplexer. The external clock sources can be applied either single ended or differentially and should have an amplitude in the range of 0.15v to 1.0v p-p (max, into 50 ohm loads, 1 MHz to 1 GHz) for U8 to function normally.

Note that if U8 is set to select an external source when no external clock signal is attached, it is possible for residual crosstalk and thermal noise to be amplified by the U8 multiplexer, resulting in a relatively random clock signal, or no clock signal, to be output from the U8 multiplexer. For best performance, when the U8 multiplexer is selecting an internal clock source, the corresponding external de-selected clock source should be either shut off or disconnected for lowest output clock jitter from the U8 multiplexer.

The U8 multiplexer outputs drive the LatticeECP3 input I/O at pins Y28, Y27, U6, U7, AH15 and AH16. The Y28 and Y27 pins are the general-purpose differential clock source applied to bank 3. They should be set for LVDS input levels, and they do not require turning on the internal termination at the LatticeECP3. The U6 and U7 signals are used for the DDR3 clock in bank 7. They should be set for SSTL15D input type, and they do not require internal termination at the LatticeECP3. The general purpose clock and DDR3 clock signals are essentially the same clock signal from U8 applied to both banks 3 and 7, but with different IO_TYPE setting requirements. The AH15 and AH16 signals are the PCSB reference clock inputs and are terminated as CML 50 ohm loads. The crystal oscillator Y4 generates a 125 MHz clock signal with +/- 50 ppm accuracy that directly drives the PCSA reference clock inputs at AH19 and AH20. Y4 can be disabled by adding a jumper on J40.

SPI Serial Flash

SPI Serial Flash are available in three package styles. The device used on this board is a 16-pin, 64 Mbit, sufficient to store two bitstreams simultaneously in order to support SPIm mode.

Configuration/Programming Headers

Four programming headers are provided on the evaluation board, providing JTAG access to the LatticeECP3, MachXO, and ispPAC-POWR1220AT8 as well as sysCONFIG™ port access to the LatticeECP3. See Figure 3 and Table 14 for the locations and usage of the programming headers.

Figure 3. Configuration/Programming Headers

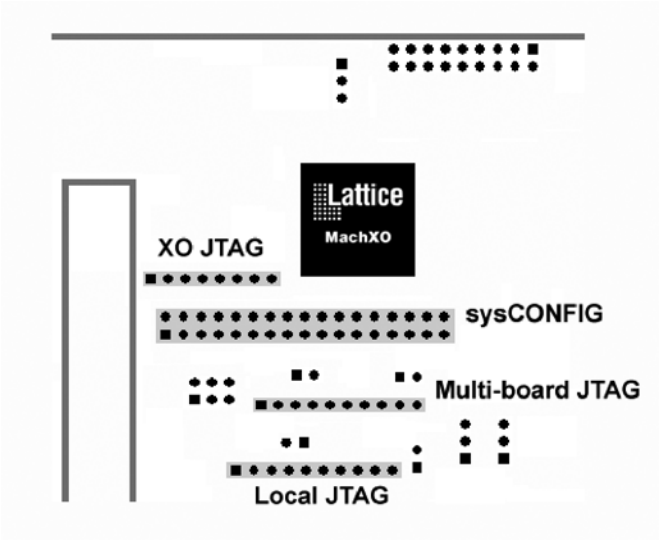


Table 14. Programming Header Access to Devices

Header	Function	Device Programmed
J10	Local JTAG	LatticeECP3, ispPAC
J11	Multi-board JTAG	External
J4	XO JTAG	MachXO
J5	sysCONFIG	LatticeECP3

The "Local JTAG" 1x10 header J10 is used for programming access to the LatticeECP3 and ispPAC-POWR1220AT8 devices. The "XO JTAG" 1x8 header J4 is used to program the MachXO device which is pre-programmed to create an on-board USB 2.0 download cable capability that can also program the LatticeECP3 and ispPAC-POWR1220AT8 devices. The JTAG ports for the LatticeECP3 and ispPAC-POWR1220AT8 devices can be configured as loop-through connectors to allow for easy daisy chaining of multiple boards connected to the "Multi-board" JTAG 1x10 header J11. With proper jumper selection (see the next section) standard IDC ribbon cable can be used without the need to swap any wires on the cable. The sysCONFIG 2x17 header J5 provides connections for 7 additional modes of configuring the LatticeECP3 device: Slave SPI, Single SPI, Multiple SPI, Burst Flash, Slave SCM, Slave PCM, and Master PCM. See TN1169 LatticeECP3 sysCONFIG Usage Guide for more information on the LatticeECP3 configuration modes. Figure 3 shows the 4 configuration headers with pin 1 on each header being the left-most (and lowest) pin on the connectors.

Lattice ispDOWNLOAD Cable

A Lattice parallel port or USB ispDOWNLOAD cable can be used with the LatticeECP3 I/O Protocol Board. When using the 1x8 cable adapter, connect pin 1 of the cable to pin 1 of the 1x10 Local JTAG header J10. J10 is the "Local JTAG" connection, a 1x10 100mil header that is provided for use with an external Lattice download cable with fly-wire style JTAG connections.

Important: *The board must be un-powered when connecting, disconnecting or reconnecting the ispDOWNLOAD Cable or USB cable. Always connect an ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP3 FPGA and render the board inoperable.*

Built-in USB 2.0 Download Cable

A standard USB cable is included that allows configuring the LatticeECP3 and ispPAC devices using the LatticeECP3 I/O Protocol Board built-in USB download cable feature. The built-in cable consists of a USB Type-B connector (J2), a USB microcontroller (U3), and a MachXO device (U5).

To use the built-in USB 2.0 download cable, simply connect a standard USB cable from J2 to your PC (with ispVM System installed and set to use the USB I/O port), set J20 as shown in Figure 4 and Table 15, and check that there are no cable connections on the Local JTAG connector J10. The USB Hub on the PC will detect the addition of the USB function making the built-in USB 2.0 download cable available for use with Lattice's ispVM System software.

Figure 4. Built-in USB 2.0 Enabled as Local JTAG Source at J2

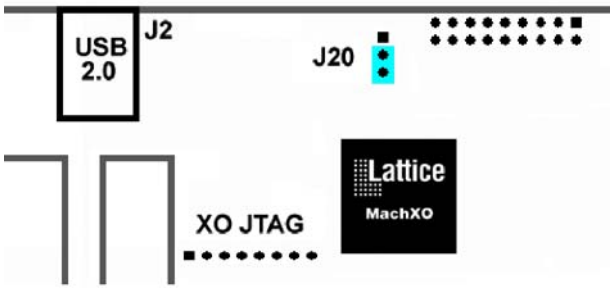


Table 15. Built-in USB vs. External Download Cable Selection

J20 Position		Local JTAG	Connector	Attach Download Cable
Shunt pins 1-2	Up	J10	1x10 header	Lattice ispDOWNLOAD
Shunt pins 2-3	Down	J2	USB Type B	Standard USB cable

Use of the built-in USB 2.0 download cable through J2 must be mutually exclusive to the use of an external download cable on the Local JTAG connector J10. When using an external download cable on J10 rather than the built in USB 2.0 download cable on J2, the jumper on J20 must be moved upwards to shunt pins 1-2, this tri-states the MachXO device I/O, preventing it from interfering with the external Lattice ispDOWNLOAD cable connected to J10.

LatticeECP3 Configuration Using JTAG

Two programming headers, J10 and J11, are provided on the evaluation board for access to the LatticeECP3 JTAG port and the ispPAC-POWR1220AT8 JTAG port. Note that in this discussion, the built-in USB 2.0 download cable can be enabled as described in the previous section to directly access the J10 signals. The pinouts for the J10 and J11 headers are provided in Table 16.

Table 16. JTAG Programming Headers

Pin	Local Programming		Multi-Board Programming	
	J10 Function	J11 Function	J10 Function	J11 Function
1	3_3V	Not used	3_3V	NC
2	TDO (from J9)	Not used	TDO (from J9)	TDO (to J9)
3	TDI	Not used	TDI	TDI (from J9)
4	PROGRAMN	Not used	PROGRAMN	PROGRAMN (from J18)
5	NC	Not used	NC	NC
6	TMS	Not used	TMS	TMS (buffered Local)
7	GND	Not used	GND	GND
8	TCK	Not used	TCK	TCK (buffered Local)

Table 16. JTAG Programming Headers (Continued)

Pin	Local Programming		Multi-Board Programming	
	J10 Function	J11 Function	J10 Function	J11 Function
9	DONE	Not used	DONE	DONE
10	INIT	Not used	INIT	INIT (from J24)

J9 is a 6-pin header that controls the functions of the local and multi-board programming headers as shown in Figure 5 and Table 17.

Figure 5. Selecting JTAG Configuration at J9

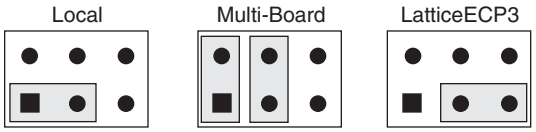


Table 17. Selecting JTAG Configuration at J9

J9 Position	J10 and J11 Usage
Shunt pins 1-3	Local JTAG
Shunt pins 1-2, 3-4	Multi-board JTAG
Shunt pins 3-5	LatticeECP3-Only JTAG

Typical use of the evaluation board is the LatticeECP3-only JTAG configuration where only the LatticeECP3 device is visible for programming in ispVM. The Multi-board setting allows daisy chaining additional JTAG devices external to the evaluation board.

The Local JTAG setting allows programming both the LatticeECP3 and ispPAC-POWR1220AT8 devices during the same configuration session in ispVM. While in the Local JTAG setting of J9, you can apply a jumper to header J17 to bypass the LatticeECP3 device to only program the ispPAC-POWR1220AT8 device as shown in Table 18.

Table 18. Local JTAG Device Programming

J17 Position	Local JTAG Programming
Shunt pins 1-2	ispPAC only
Open pins 1-2	LatticeECP3 and ispPAC

The header J59 provides a means to enable the ispPAC device in the JTAG chain. Likewise for J60 enabling the LatticeECP3 device in the JTAG chain. Being able to selectively enable either device is of use for cases where configuration headers J9 and J17 have set up an instance that both the ispPAC and LatticeECP3 are listening in parallel at the same point in the JTAG chain. In such an instance, the device that is not driving the remainder of the JTAG chain should be disabled so it will ignore the JTAG signals passing by its JTAG inputs and the device's configuration will remain intact.

The configuration procedures near the end of this user's guide describe how to properly set the evaluation board programming headers to easily download bitstreams into each of the Lattice devices on the evaluation board.

Configuration CFG Switches

The LatticeECP3 power-up configuration mode is controlled by the setting of SW5. Table 19 shows the how to set SW5 for the various configurations.

Table 19. CFG Configuration at SW5

CFG2 SW5-1	CFG1 SW5-2	CFG0 SW5-3	Configuration Mode
DOWN	DOWN	DOWN	SPI Flash
DOWN	UP	DOWN	SPIm
UP	DOWN	UP	Slave Serial
UP	UP	UP	Slave Parallel
X	X	X	ispJTAG™

Additional instructions and recommendations for programming this board are provided in the Configuring/Programming the Board section of this document.

Switches

There is one 8-position switch (SW4) and 2 push-button switches (PB1 and PB2) for implementing basic user-assigned input functions. Additionally, there are two 3-position switches (SW5 and S1) and 3 push-buttons (SW1, SW2, and SW3) for Power Manager and LatticeECP3 configuration.

Switches PB1, PB2, SW1, SW2, and SW3 are momentary switches. The pull-up resistors associated with these switches are wired to 3.3V. Pushing the switches down produces a low (0), otherwise it produces a high (1). The signals controlled by PB1, PB2, SW1, and SW2 are debounced by MAX6817 devices (U23 and U24) before connecting to an LatticeECP3 I/O pin. Table 20 shows the control relationship between the switches, LatticeECP3 I/O pins, and USB controller U3.

Table 20. Momentary Switches

	Connection	User Definable	Debounced
PB1	AM34 of LatticeECP3	Yes	Yes
PB2	AM33 of LatticeECP3	Yes	Yes
SW1	B34 of LatticeECP3 (PROGRAMN)	No	Yes
SW2	D33 of LatticeECP3 (GSRN)	Yes	Yes
SW3	Pin 9 of U3 (USB_RESETn)	No	No

SW4 on the lower side of the board is an 8-pin DIP switch with pull-up resistors to the DDR3_VDD (1.5V) supply. SW3 and S1 are 3-pin DIP switches with pull up resistors to 3.3V. A switch in the down position produces a low (0), the up position produces a high (1). Table 21 shows the SW4 connections to the LatticeECP3, Table 19 shows the S1 connections to ispPAC-POWR1220AT8 I/O pins, and Table 20 shows the SW3 connections to the LatticeECP3.

Table 21. 8-Position Switch SW4

Switch (Position#)	LatticeECP3 I/O	sysIO Bank
SW4 (position#1)	A9	0
SW4 (position#2)	A8	0
SW4 (position#3)	A6	0
SW4 (position#4)	B6	0
SW4 (position#5)	A7	0
SW4 (position#6)	B7	0
SW4 (position#7)	A5	0
SW4 (position#8)	A4	0

Table 22. 3-Position Switch S1

Switch (Position#)	POWR1220AT8 I/O Pin	Pin Name
S1 (position#1)	4	IN1
S1 (position#2)	6	IN2
S1 (position#3)	7	IN3

Table 23. 3-Position Switch SW3

Switch (Position#)	LatticeECP3 I/O	Pin Name	sysIO Bank
SW3 (position#1)	D32	CFG2	8
SW3 (position#2)	F30	CFG1	8
SW3 (position#3)	B33	CFG0	8

LEDs

There are eight user-definable LEDs located at the upper center of the board. These LEDs are each controlled by a separate general purpose I/O as defined in Table 24. The LEDs will light when their associated I/O is high and will have a current flowing through them of approximately 3 mA, the value of which is set by the NPN current source connected transistors (Q6, Q12, Q13, Q14, Q15, Q16, Q17, Q18) and resistors (R155, R162, R164, R177, R189, R193, R195, R199). The LEDs are off when the I/Os are set low.

Table 24. Connection Between LEDs and LatticeECP3

Signal	LED	LatticeECP3 IO	Bank
LED0	D6	C3	0
LED1	D9	C4	0
LED2	D10	D3	0
LED3	D12	C2	0
LED4	D14	B1	0
LED5	D11	B2	0
LED6	D8	E4	0
LED7	D7	D4	0

Table 25 describes the three LEDs associated with the dedicated programming pins.

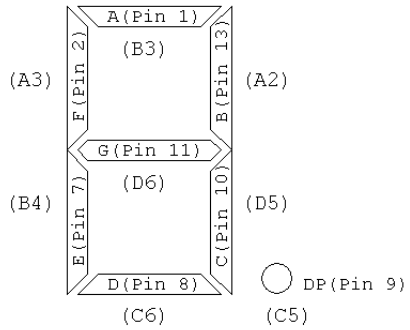
Table 25. Programming LEDs

LED	Pin	Color	Function
D4	PROGRAMN	Red	On when signal is low
D2	INIT	Red	On when initializing
D5	DONE	Green	On when config is complete
D3	GSRN	Red	On when signal is low
D1	TDI	Green	On when TDI is active

7-Segment Display

The 7-segment LED is controlled by LatticeECP3 bank 0 I/O pins. The connections of the segments are shown in Figure 6.

Figure 6. Seven Segment Display



The LED digit segments will light when their associated I/O is high and will have a current flowing through them of approximately 5 mA, the value of which is set by the NPN current source connected transistors (Q2, Q3, Q5, Q7, Q8, Q9, Q10, Q11) and resistors (R126, R133, R148, R150, R151, R152, R153, R154). The LED digit segments are off when the I/Os are set low.

LCD

The LCD module connector (J32) is a 2x9 header. This 18-pin header is compatible with some character LCD modules. Table 26 shows the pin function of the header and the connections to bank 1 of the LatticeECP3 FPGA. The bank 1 supply voltage (VCCIO_1) must be set using J41 to select the proper voltage level expected by the LCD module.

Table 26. LCD Header Connection

Pin #	Function	LatticeECP3 I/O	Pin #	Function	LatticeECP3 I/O
1	Anode	—	2	Cathode (GND)	—
3	VSS (GND)	—	4	VDD (5V)	—
5	VO	—	6	RS	D23
7	R/W	A23	8	E	K22
9	DB0	B23	10	DB1	K21
11	DB2	E22	12	DB3	A24
13	DB4	E23	14	DB5	B24
15	DB6	C23	16	DB7	G23
17	Anode	—	18	Cathode (GND)	—

The VR1 potentiometer is used to limit the current that flows through the backlight LED on the LCD module. The VR2 potentiometer is used to adjust the VO voltage that controls the LCD contrast.

When the following LCD modules are used, connect pins 1 through 16 to the backlight LCD module or connect pins 1 through 14 to the non-backlight LCD module.

Optrex:

- C-51505 Series: 20 characters x 2 lines

When the following LCD modules are used, connect pin 3 to 18 to the backlight LCD module or connect pin 3 to 16 to the non-backlight LCD module.

Lumex:

- LCM-S01601 Series: 16 characters x 1 line
- LCM-S00802 Series: 8 characters x 2 lines
- LCM-S01602 Series: 16 characters x 2 lines
- LCM-S02002 Series: 20 characters x 2 lines
- LCM-S02402 Series: 24 characters x 2 lines
- LCM-S04002 Series: 40 characters x 2 lines
- LCM-S02004 Series: 20 characters x 4 lines
- LCM-S02404 Series: 24 characters x 4 lines

Varitronix:

- MDLS-20189 Series: 20 characters x 1 line
- MDLS-20265 Series: 20 characters x 2 lines
- MDLS-24265 Series: 24 characters x 2 lines
- MDLS-40266 Series: 40 characters x 2 lines

Logic Analyzer Probe

Connector LA1 is configured for use with the Agilent 16760A Logic Analyzer probe. All the signal pins at LA1 are connected to the LatticeECP3 bank 1 I/Os, and to the test point header J54. The bank 1 supply voltage (VCCIO_1) must be set using J41 to select the proper voltage level expected by the logic analyzer. Series 33 ohm resistors are installed on the board to reduce reflection overshoot and undershoot for un-terminated receivers attached to J54. See Table 27 for the Logic Analyzer probe connections to the LatticeECP3 I/O pins.

Table 27. LA1 Logic Analyzer and J54 Test Points

LA1 Pin	J54 Pin	Signal	LatticeECP3 I/O
5	2	LA1	A17
6	3	LA2	B17
7	4	LA3	A18
8	5	LA4	B18
9	6	LA5	J18
10	7	LA6	H18
11	8	LA7	D18
12	9	LA8	E18
13	10	LA9	G19
14	11	LA10	H19
15	12	LA11	A19
16	13	LA12	B19
17	14	LA13	K20
18	15	LA14	L19
19	16	LA15	C19
20	17	LA16	D19
21	18	LA17	J19
22	19	LA18	K19
23	20	LA19	A20
24	21	LA20	B20
25	22	LA21	G20
26	23	LA22	G21
27	24	LA23	C20
28	25	LA24	D20
29	26	LA25	H20
30	27	LA26	J20
31	28	LA27	A22
32	29	LA28	B22
33	30	LA29	J22
34	31	LA30	J23
35	32	LA31	C22
36	33	LA32	D22
37	34	LA33	J21
38	35	LA34	H22

High-Speed Test Points

Additional high-speed test points are provided at the connectors shown in Table 28.

Table 28. Additional High-Speed Test Points

Connector	Pin	Signal	LatticeECP3 I/O	VCCIO	Type
J68	1	Y32	Y32	2.5	I/O
J63	1	C8	C8	1.5	I/O
J64	1	V5	V5	1.5	I/O
J65	1	K4	K4	1.5	I/O
J57	3	IDC0	H23	VCCIO1 (Set by J41)	I/O
	5	IDC1	D24		I/O
	7	IDC2	E24		I/O
	9	IDC3	K23		I/O
	11	IDC4	K24		I/O
	13	IDC5	A25		I/O
	15	IDC6	B25		I/O
	17	IDC7	C28		I/O
	19	IDC8	D28		I/O
	21	IDC9	C25		I/O
	23	IDC10	D25		I/O
	25	IDC11	G26		I/O
	27	IDC12	G25		I/O
	29	IDC13	B28		I/O
	31	IDC14	A28		I/O
	33	IDC15	A26		I/O
J55	33	TEST0	N27	2.5V	I/O
	31	TEST1	N28		I/O
	29	TEST2	AJ27		I/O
	27	TEST3	AK28		I/O
	25	TEST4	AJ28		I/O
	23	TEST5	AH27		I/O
	21	TEST6	R26		I/O
	19	TEST7	R25		I/O
	17	TEST8	T34		I
	15	TEST9	T33		I
	13	TEST10	T30		I/O
	11	TEST11	U30		I/O
	9	TEST12	AH28		I/O
	7	TEST13	AL29		I/O
	5	TEST14	AG26		I/O

High Current I/O

The High Current I/O connector J46 provides a means to evaluate multiple I/Os connected in parallel to produce a higher combined output I/O current exceeding that of a single I/O. The three series resistors R37, R38, and R157, are placed physically close to the LatticeECP3 pins and a 50 ohm signal trace connects the parallel side of the resistors to the SMA connector J46. For best results, the three output I/Os at pins H25, H26, and A31 should be set for the FAST setting and driven by the same signal within the LatticeECP3 internal routing.

The high current I/O output can also be used to implement a simple 3-bit DAC by replacing the 3 series resistors R37, R38, and R157 with higher scaled resistor values. Suggested values for the three resistors would be 487 ohm, 1.0K ohm, and 2K ohm. J46 will then output 8 monotonic voltage values between the VCCIO1 and GND potentials dependent on the output states of the signals at the LatticeECP3 I/Os located at H25, H26 and A31. For the DAC configuration just described, the fastest signal response will be had if the J46 output is driving a 50 ohm load. The largest output voltage range will occur when the J46 load is a high impedance. Be aware that simple DACs of this type can pass residual power supply noise (SSO) from other I/Os switching in the same bank. So if an application is noise-sensitive, either filter the DAC output at J46 or use an external DAC.

DDR3

The two 240-pin DIMM sockets provide a built-in 64-bit interface to standard 1.5V DDR3 SDRAM UDIMM memory modules. The required VREF and VTT voltages, as well as termination of each signal to VTT are provided. Performance has been verified at above the 800 MT/s data rate. See TN1180, LatticeECP3 High-Speed I/O Interface for further information about DDR3 design considerations and recommendations. The connections between the connector pins and LatticeECP3 balls are shown in Table 29.

Table 29. DDR3 Interface to DIMM Sockets

Description	LatticeECP3 I/O Pin	sysIO Bank	J1 & J3 Pin
DDR3_DQ0	AN3	6	3
DDR3_DQ1	AM3	6	4
DDR3_DQ2	AJ5	6	9
DDR3_DQ3	AJ6	6	10
DDR3_DQ4	AL5	6	122
DDR3_DQ5	AM5	6	123
DDR3_DQ6	AL4	6	128
DDR3_DQ7	AM4	6	129
DDR3_DM0	AP5	6	125
DDR3_DQS0_P	AM6	6	7
DDR3_DQS0_N	AN6	6	6
DDR3_DQ8	AN1	6	12
DDR3_DQ9	AN2	6	13
DDR3_DQ10	AD9	6	18
DDR3_DQ11	AD8	6	19
DDR3_DQ12	AP2	6	131
DDR3_DQ13	AP3	6	132
DDR3_DQ14	AL3	6	137
DDR3_DQ15	AK3	6	138
DDR3_DM1	AJ4	6	134
DDR3_DQS1_P	AJ2	6	16
DDR3_DQS1_N	AJ3	6	15
DDR3_DQ16	AA2	6	21
DDR3_DQ17	AA1	6	22
DDR3_DQ18	Y7	6	27
DDR3_DQ19	AA7	6	28
DDR3_DQ20	AA4	6	140
DDR3_DQ21	AA3	6	141
DDR3_DQ22	AB2	6	146
DDR3_DQ23	AB1	6	147

Table 29. DDR3 Interface to DIMM Sockets (Continued)

Description	LatticeECP3 I/O Pin	sysIO Bank	J1 & J3 Pin
DDR3_DM2	AA5	6	143
DDR3_DQS2_P	AA10	6	25
DDR3_DQS2_N	AB9	6	24
DDR3_DQ24	W2	6	30
DDR3_DQ25	W1	6	31
DDR3_DQ26	W8	6	36
DDR3_DQ27	W9	6	37
DDR3_DQ28	W4	6	149
DDR3_DQ29	W3	6	150
DDR3_DQ30	Y2	6	155
DDR3_DQ31	Y1	6	156
DDR3_DM3	Y8	6	152
DDR3_DQS3_P	W6	6	34
DDR3_DQS3_N	Y6	6	33
DDR3_DQ32	T6	7	81
DDR3_DQ33	T5	7	82
DDR3_DQ34	R8	7	87
DDR3_DQ35	T7	7	88
DDR3_DQ36	T4	7	200
DDR3_DQ37	T3	7	201
DDR3_DQ38	T2	7	206
DDR3_DQ39	T1	7	207
DDR3_DM4	U9	7	203
DDR3_DQS4_P	T9	7	85
DDR3_DQS4_N	T8	7	84
DDR3_DQ40	R7	7	90
DDR3_DQ41	R5	7	91
DDR3_DQ42	P9	7	96
DDR3_DQ43	P10	7	97
DDR3_DQ44	R2	7	209
DDR3_DQ45	R1	7	210
DDR3_DQ46	R4	7	215
DDR3_DQ47	R3	7	216
DDR3_DM5	R10	7	212
DDR3_DQS5_P	P7	7	94
DDR3_DQS5_N	P6	7	93
DDR3_DQ48	N3	7	99
DDR3_DQ49	M5	7	100
DDR3_DQ50	N5	7	105
DDR3_DQ51	N2	7	106
DDR3_DQ52	N1	7	218
DDR3_DQ53	P5	7	219
DDR3_DQ54	P4	7	224
DDR3_DQ55	N8	7	225