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LatticeECP3 Versa Evaluation Board

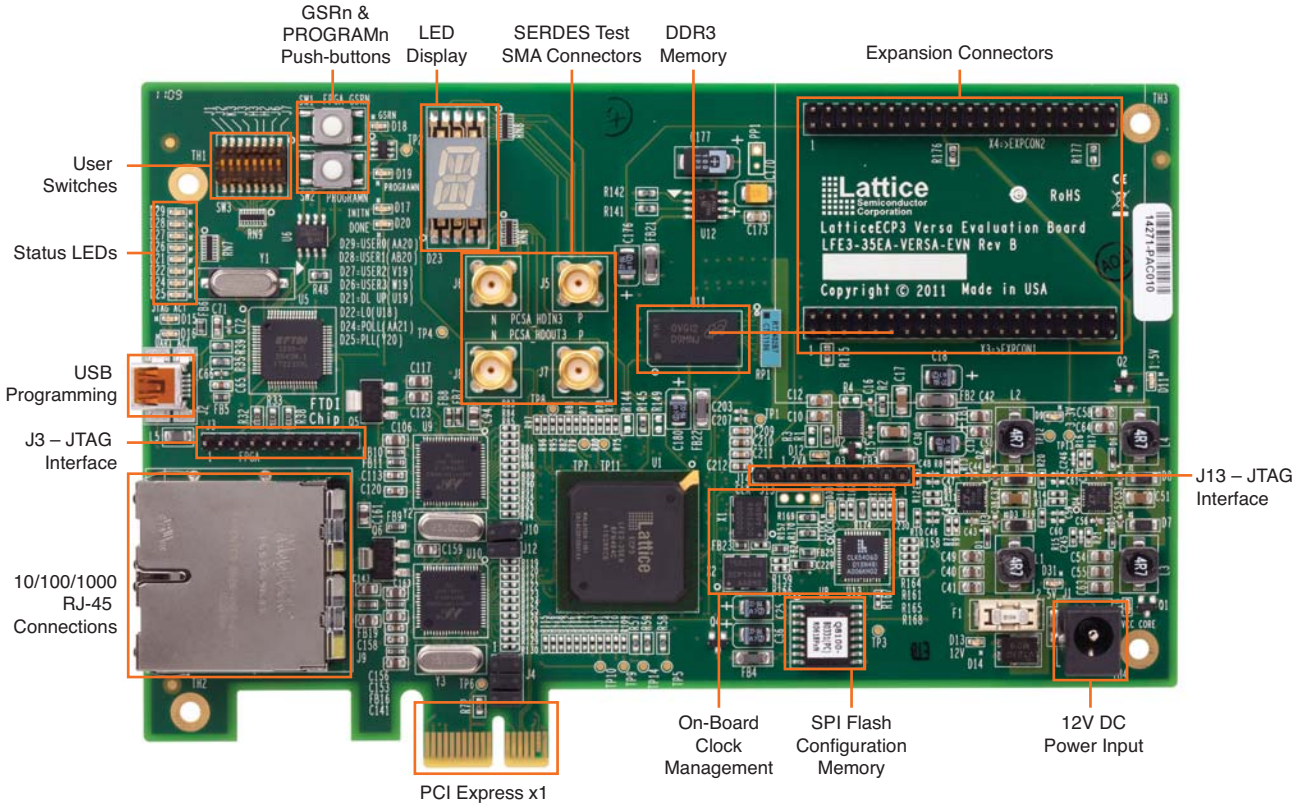
User's Guide

July 2013
Revision: EB62_01.6

Introduction

The LatticeECP3™ Versa Evaluation Board allows designers to investigate and experiment with the features of the LatticeECP3 Field-Programmable Gate Array. The features of the LatticeECP3 Versa Evaluation Board can assist engineers with rapid prototyping and testing of their specific designs. The LatticeECP3 Versa Evaluation Board is part of the LatticeECP3 Versa Development Kit. The guide is intended to be referenced in conjunction with demo user's guides to demonstrate the LatticeECP3 FPGA.

Figure 1. LatticeECP3 Versa Evaluation Board, Top Side



Features

- Half-length PCI Express form-factor
  - Allows demonstration of PCI Express x1 interconnection
- Electrical testing of one full-duplex SERDES channel via SMA connections
- USB-B connection for UART and device programming
- Two RJ45 interfaces to 10/100/1000 Ethernet to GMII
- On-board Boot Flash
  - 64M Serial SPI Flash
- DDR3-1333 memory components (64Mb/x16)
- Expansion mezzanine interconnection for prototyping
- 14-segment alpha-numeric display
- Switches, LEDs and displays for demo purposes
- ispVM™ programming support
- On-board reference clock sources

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics.

Caution: The LatticeECP3 Versa Evaluation Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the evaluation board.

LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V core supply. It can accommodate all pin-compatible LatticeECP3 devices in the 484-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP3 Family Data Sheet.

*Note: The connections referenced in this document refer to the **LFE3-35EA-8FN484C** device.*

Applying Power to the Board

The LatticeECP3 Versa Evaluation Board is ready to power on. The board can be supplied with power from a PCI Express host system or standalone with an external wall power module.

The 12V DC input power source is fused with a surface mounted fuse, as noted in Table 1.

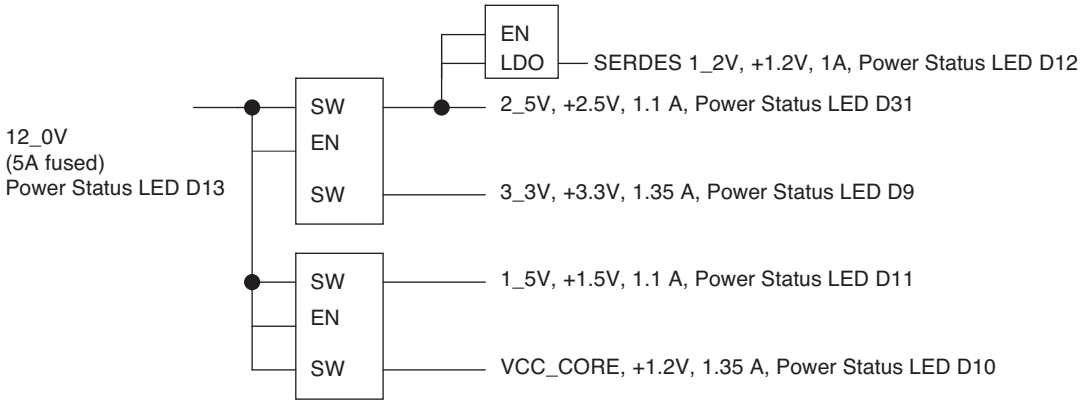
Table 1. Board Power Supply Fuses – (See Appendix B, Figure 12)

Fuse Designator	Description
F1	12V Input Supply Fuse

The board may be plugged into a host PC. Only plug the board into a PCI Express slot when the system is powered off. Once inserted, the PC can be safely powered on.

Using the evaluation board outside of a PC chassis supply requires the factory-supplied wall supply module. Use of other supplies is not suggested. GME Technology's GFP181DA-1215B-1 (or equivalent) is provided with the LatticeECP3 Versa Development Kit.

Figure 2. Power Distribution Scheme – (See Appendix B, Figure 12)



Programming/FPGA Configuration

The LatticeECP3 Versa Evaluation Board has a built-in download controller for programming the LatticeECP3 FPGA. The built-in module consists of a USB Type-B connector and a USB UART device. To use the built-in download cable, simply connect a standard USB cable (a USB-B to USB-A cable is included with the LatticeECP3 Versa Development Kit) from J2 to your PC (with ispVM System software installed). The USB hub on the PC will detect the addition of the USB function, making the built-in cable available for use with the ispVM System software. The USB cable is connected in parallel to J3.

Alternate ispVM Download Interface

J3 is a 1x10 100mil header that is provided for use with an external Lattice download cable (available separately). A USB download cable can be attached to the board using J3 to interface with the FPGA (U1).

Note: Resistors R38, R33, R32 and R36 need to be removed.

A separate header is provided to interface to a download cable for the ispClock™5406A clock device (U13). U13 is not interfaced to the built-in download interface. U13 is factory-programmed for use with the reference designs and should only be altered for customized designs.

A 10-pin JTAG connector is used in conjunction with the ispVM USB download cable to program and control the device. A separate 10-pin header (J14) is provided for programming U13.

Table 2. ispVM JTAG Connector Pinout (J3 and J14) – (See Appendix B, Figure 5)

Pin	Function	Color
1	PWR	Red
2	TDO	Brown
3	TDI	Orange
4	N/C	—
5	N/C	—
6	TMS	Purple
7	GND	Black
8	TCK	White
9	N/C	—
10	N/C	—

ispVM Requirements

Note: An ispDOWNLOAD™ cable is included with Lattice Diamond® design software. This cable is not needed for the typical use of this board since it includes the built-in download module and only requires the USB cable included with the board. Standalone ispVM download cables may be purchased separately from Lattice.

After initial board setup, use the following procedure to program the board. Instructions assume that ispVM software has been installed on a local PC.

Requirements:

- PC with ispVM System 18.0 (or later) programming software, installed with appropriate drivers (USB driver for USB cable, Windows 7/XP/2000/NT parallel port driver for ispDOWNLOAD cable).
  Note: An option to install these drivers is included as part of the ispVM System setup.
- ispDOWNLOAD cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.). Required only for alternative FPGA programming and ispClock5406A reprogramming.

Board Programming

Configuration Status Indicators

(see Appendix B, Figure 13)

Figure 3. LatticeECP3 Status LEDs and Push-button Controls

The LEDs indicate the configuration status of the LatticeECP3 FPGA.

- **D17 (red)** illuminated indicates that programming was aborted or reinitialized, driving the INITN output low.
- **D20 (green)** illuminated indicates the successful completion of configuration by releasing the open collector DONE output pin.
- **D19 (red)** illuminated indicates that PROGRAMN is low.
- **D18 (red)** illuminated indicates that GSRN is low.

PROGRAMN and GSRN

These push-button switches assert/de-assert the logic levels on PROGRAMN (SW2) and GSRN (SW1). Depressing the button drives a logic level "0" to the device.

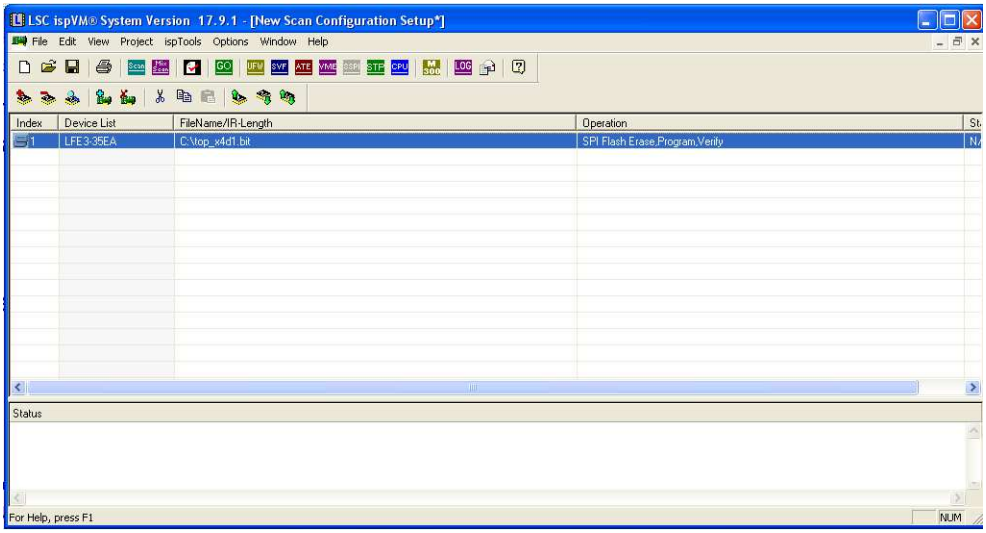
Programming Serial SPI Flash Memory

A serial SPI (16-pin TSSOP, 64M) Flash memory device (U8) is on-board for non-volatile configuration memory storage. A STMicro M25P64VMF16 device is populated on-board.

The Serial SPI Flash memory device can be configured easily via its JTAG port. This mode enables the FPGA to be programmed at power-up or assertion of PROGRAMN with a bitstream stored in the memory device.

1. Connect the LatticeECP3 Versa Evaluation Board.
2. In the dialog box, select **SPI Flash Programming Mode** in the Device Access Option pull-down menu.

Figure 4. Device Information Dialog Screen



3. The SPI Serial Flash Device dialog box will open. In this box, select **SPI Flash Erase, Program, Verify** in the Operation pull-down menu.

4. Select **SPI Serial Flash** in the Device Family pull-down menu, **STMicro** under the Vendor pull-down menu, **SPI-M2564** under the Device pull-down menu, and **16-lead SOIC** under the Package submenu.

Figure 5. Select Device Dialog Box

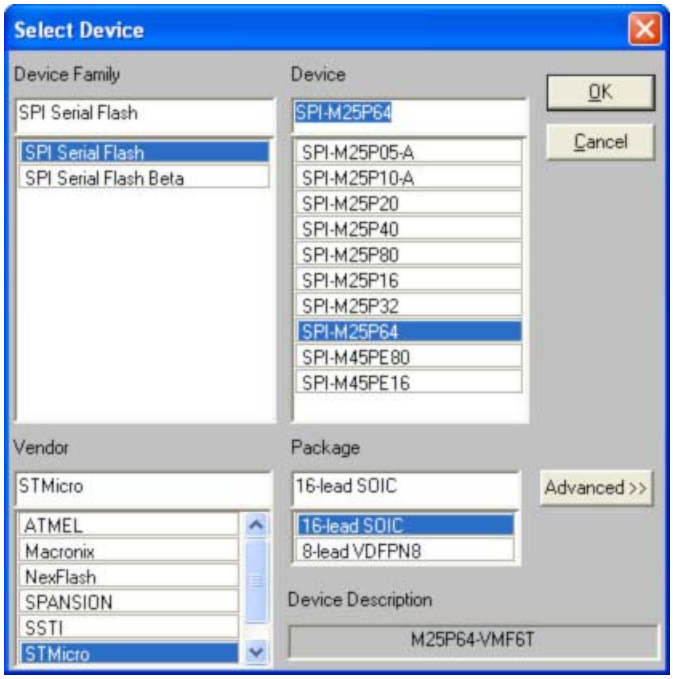
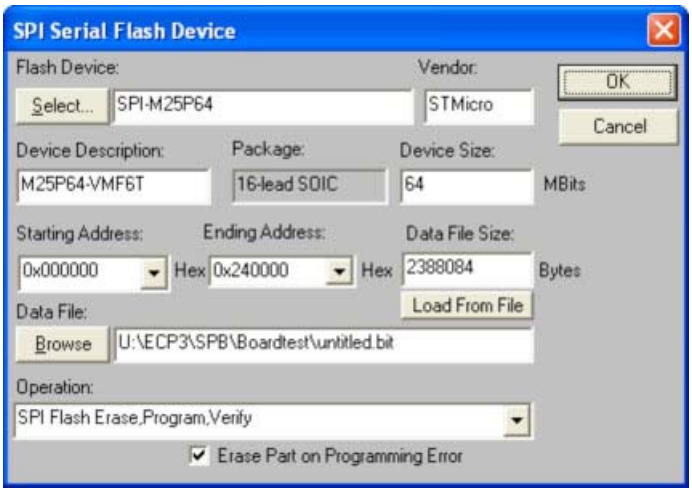


Figure 6. Sample SPI Serial Flash Device Dialog Box



5. Click **OK** in the SPI Serial Flash Device dialog box. Then click **OK** in the Select Device dialog box. You will return to the main configuration screen

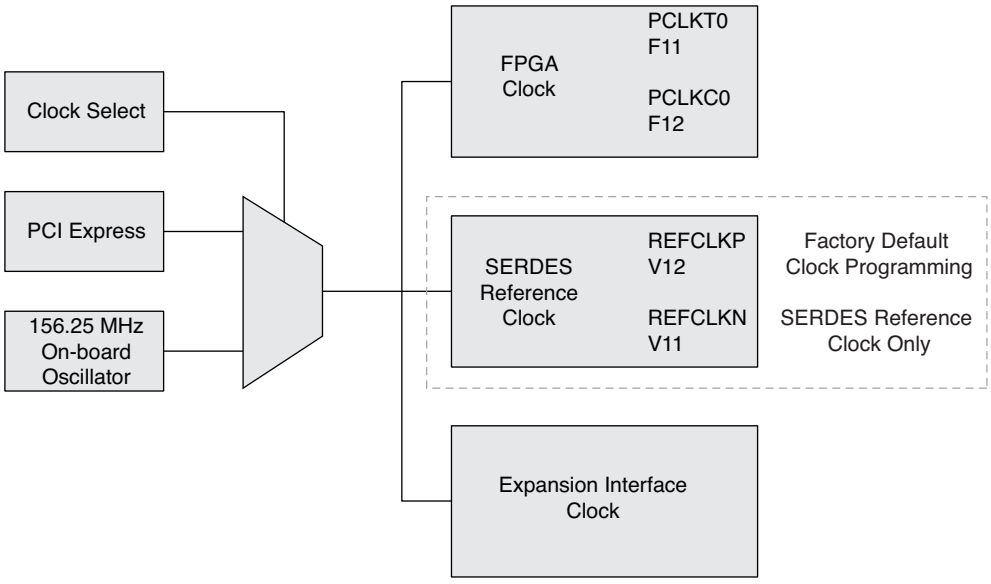
6. From the main programming window, select **Go** from the top toolbar. This will begin the SPI Serial Flash programming.

On-Board Clock Capabilities

(See Appendix B, Figure 19)

The LatticeECP3 Versa Evaluation Board allows for several clock source options. Some of these options are controlled via the ispClock5406A programmable clock manager device. The ispClock5406A enables the reference clock from the PCI Express interface to provide a reference clock to the SERDES. This is true only when the board is in a PCI Express host socket. When the board is not in a PCI Express host socket, the clock will be supplied by a 156.25 MHz clock on-board oscillator. Both clock inputs can be fanned out to the dedicated SERDES reference inputs, FPGA inputs, and to the expansion connectors. The factory default programming only connects the SERDES reference clock inputs. Factory-defined demonstration designs will control and manage the clock.

Figure 7. Clock Controller Scheme

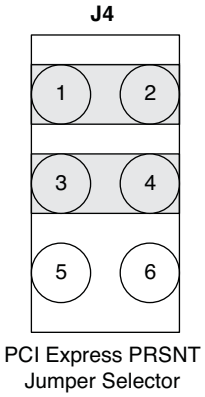


General Purpose Clock Source

An on-board 100MHz LVDS oscillator is provided for general purpose use. This clock source is connected to differential inputs L5 and K6 and must be used as LVDS inputs to the FPGA. This pin pair also provides optimal interface to the FPGA PLL for customized use.

The PCI Express add-in card specification requires add-in boards to include capabilities to tell the host of its presence. The LatticeECP3 Versa Evaluation Board allows this optional connection via a board jumper. The factory default will have two jumpers installed as shown below for the PRSNT connection to the PCI Express host.

Figure 8. PCI Express PRSNT Control Connection



PCI Express PRSNT
Jumper Selector

SERDES

The LatticeECP3 quad-based SERDES FPGA is utilized on the board for several purposes. The PCSA quad is provisioned to provide a single, full-duplex PCI Express channel. The high-speed signals are connected to the PCI Express edge connection.

Table 3. PCI Express Channel Interconnections

PETp0	HDINP0	Y15
PETn0	HDINN0	Y14
PERp0	HDOUTP0	AB15
PERn0	HDOUTN0	AB14

Table 4. SMA Test Interconnections

J5	HDINP3	Y8
J6	HDINN0	Y9
J7	HDOUTP3	AB8
J8	HDOUTN3	AB9

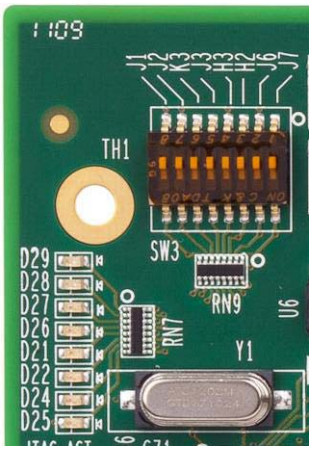
FPGA Test Pins

(see Appendix B, Figure 18)

General Purpose DIP Switches

General purpose FPGA pins are available for user applications. FPGA pins are connected to switch SW3, a SPST slide-actuated DIP switch. The switches are connected to logic level 0 when moved to the ON position. Switch position 1 is indicated with a dot. **These inputs are within a bank connected to 1.5V**. The user must program these inputs to be the LVCMOS15 type in the design.

Figure 9. LatticeECP3 Versa Evaluation Board LEDs and Switches



The designated pins are connected according to Table 5.

Table 5. FPGA Ball to DIP Switch Position

FPGA Ball Number	SW3 DIP Switch Position
J7	1
J6	2
H2	3
H3	4
J3	5
K3	6
J2	7
J1	8

General Purpose LEDs

(See Appendix B, Figure 18)

The LEDs provided on the LatticeECP3 Versa Evaluation Board are connected to general purpose FPGA I/Os. These LEDs provide status for user designs and must be included in the design. The LEDs illuminate when the FPGA output is driven LOW. Table 6 shows the LED and associated FPGA pins. These pins are within an I/O bank connected to 3.3V and the user should program these to be LVCMOS33 type outputs in the design.

Table 6. LED Definitions

LED Number	FPGA Ball Number	PCB Designator	LED Color
LED0	U19	D21	Green
LED1	U18	D22	Green
LED2	AA21	D24	Yellow
LED3	Y20	D25	Yellow
LED4	W19	D26	Red
LED5	V19	D27	Red
LED6	AA20	D29	Blue
LED7	AB20	D28	Blue

Alpha-numeric LED Display

(see Appendix A, Figure 18)

A 14-segment alpha-numeric display is provided on the board (D23). These LED segments are connected to general-purpose FPGA I/Os. The LEDs must be included in the FPGA design. The LEDs illuminate when the FPGA output is driven LOW. Table 7 shows the LED and associated FPGA pins. These pins are within an I/O bank connected to 3.3V and the user should program these to be LVCMOS33 outputs in the design.

Figure 10. 14-Segment Display

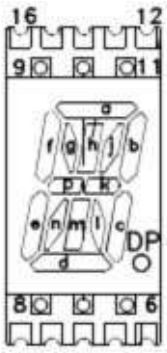


Table 7. Alpha-numeric LED Definitions

Display	fpBGA Ball Number	Display	fpBGA Ball Number
A	V6	J	AB3
B	U7	K	AB4
C	Y6	L	W4
D	Aa6	M	Y5
E	U8	N	AA4
F	T8	P	AA5
G	R9	DP	W5
H	T9		

DDR3 Memory Device

(see Appendix B, Figure 17)

- The LatticeECP3 Versa Evaluation Board is equipped with a SDRAM memory device (1.5V, 64Mb/x16, 96-ball FBGA, 667 MHz, DDR3-1333) such as the Micron MT41J64M16JT-15E:G device.
- The DDR3 memory includes a 16-bit wide memory controller interface.
- The board includes termination of data, address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP3 device.
- A 100 MHz on-board clock oscillator is available to provide a DDR3 reference clock.

Table 8. DDR3 Memory Controller Interconnections

NETNAME	484 fpBGA Ball Number
DQ0	E5
DQ1	E4
DQ2	D2
DQ3	D1
DQ4	C2
DQ5	B2
DQ6	G5
DQ7	G4
DQ8	G2
DQ9	F1
DQ10	H4
DQ11	E2
DQ12	J4
DQ13	B1
DQ14	C1
DQ15	G3
DQS0	F5
DQS0#	F4
DQS1	H5
DQS1#	H6
CEO	G8
RAS#	A6
CLKP	L5
CLKN	K6

NETNAME	484 fpBGA Ball Number
A0	C8
A1	C7
A2	B7
A3	D8
A4	F9
A5	E9
A6	A3
A7	D7
A8	A7
A9	B8
A10	C9
A11	C10
K_0	K4
K_0#	K5
CAS#	A4
BA0	B4
BA1	E6
BA2	D5
ODT	E7
CS0#	C6
WE#	D6
VREF	E1
DM0	E3
DM1	F3

Ethernet Interfaces

(see Appendix B, Figure 18)

Two Marvell 88E1119R Gigabit Ethernet transceiver devices (U17) are included on the board. This physical layer device supports 1000BASE-T, 100BASE-TX, and 10BASE-T applications via a standard media interface to a dual RJ45 connection. The RJ45 connection includes network magnetics providing the proper signal conditioning, electro-magnetic interference suppression and signal isolation. This connector includes two LEDs and the board includes four status LEDs from the Marvell device. The LEDs are register-programmed and detailed descriptions are available in the Marvell device data sheet.

Table 9. PHY Status Indicators

LED	Status Description
RJ45 (Yellow)	LED RX
RJ45 (Yellow)	LED TX

Each Marvell 88E1119R device communicates via a GMII interface to the LatticeECP3 device.

Table 10. FPGA GPIO to GMII Interfaces

Signal	PHY#1	PHY#2
RSTN	L3	R21
MDIO	L2	U16
MDC:	V4	Y18
RXC	L4	N19
RX_ER	M4	V20
RX_DV	M1	U15
RX_D0	M5	AB17
RX-D1	N1	AA17
RX_D2	N6	R19
RX_D3	P6	V21
RX_D4	T2	T17
RX_D5	R2	R18
RX_D6	P5	W21
RX_D7	P3	Y21
TXC	C12	M21
TX_EN	V3	V22
TX_D0	V1	W22
TX_D1	U1	R16
TX_D2	R3	P17
TX_D3	P1	Y22
TX_D4	N5	T21
TX_D5	N3	U22
TX_D6	N4	P20
TX_D7	N2	U20
GTXCLK	M2	M19
CRS	P4	P19
COL	R1	N18
COMA	R4[1]	T15[1]
125CLK	T3	R17

1. Each PHY device includes a header dedicated to the COMA connection to the device. The header is populated with a jumper that disables and places the PHY in a low power configuration. Headers J10 and J12 are used for this purpose. It is assigned to PHYs U9 and U10, respectively.

Table 11. Expansion Connections

x3 Expansion Connector		
Pin	**Signal**	**484-Ball fpBGA**
1	GND	GND
2	NC	NC
3	2.5V	2.5V
4	IO29	D17
5	IO30	J22
6	IO31	K22
7	IO32	L18
8	IO33	L19
9	IO34	L22
10	IO35	M22
11	IO36	K18
12	IO37	K17
13	IO38	H22
14	IO39	H21
15	IO40	G22
16	IO41	G21
17	IO42	J18
18	IO43	J17
19	IO44	F22
20	IO45	E22
21	5VIN	5VIN
22	GND	GND
23	2.5V	2.5V
24	GND	GND
25	3.3V	3.3V
26	GND	GND
27	3.3V	3.3V
28	GND	GND
29	OSC	U13 PIN27
30	GND	GND
31	CLKIN	E15
32	GND	GND
33	CLKOUT	D12
34	GND	GND
35	3.3V	3.3V
36	GND	GND
37	3.3V	3.3V
38	GND	GND
39	3.3V	3.3V
40	GND	GND

x4 Expansion Connector		
Pin	**Signal**	**484-Ball fpBGA**
1	HPE-RST#	J20
2	GND	GND
3	IO0	B11
4	IO1	B12
5	IO2	A12
6	IO3	A13
7	IO4	E12
8	IO5	E13
9	IO6	C13
10	IO7	C14
11	IO8	D13
12	IO9	D14
13	IO10	A14
14	IO11	B14
15	IO12	F13
16	IO13	F14
17	IO14	A15
18	IO15	B15
19	GND	GND
20	3.3V	3.3V
21	IO16	C15
22	GND	GND
23	IO17	D15
24	GND	GND
25	IO18	G15
26	GND	GND
27	IO19	G14
28	IO20	A16
29	IO21	B16
30	GND	GND
31	IO22	F15
32	IO23	F16
33	IO24	A17
34	GND	GND
35	IO25	B18
36	IO26	A18
37	IO27	A19
38	CARDSEL#	J19
39	IO28	D16
40	GND	GND

References

- DS1021, LatticeECP3 Family Data Sheet
- HB1009, LatticeECP3 Family Handbook
- QS013, LatticeECP3 Versa Evaluation Board Quick Start Guide
- UG46, PCI Express Demos for the LatticeECP3 Versa Evaluation Board
- UG45, DDR3 Demo for the LatticeECP3 Versa Evaluation Board
- UG44, SERDES Eye/Backplane Demo for the LatticeECP3 Versa Evaluation Board

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP3 Versa Evaluation Board	LFE3-35EA-VERSA-EVN	

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2011	01.0	Initial release.
August 2011	01.1	Updated LatticeECP3 Versa Evaluation Board, Top Side diagram.
		Corrected ispVM System software version number in the ispVM Requirements text section.
		Corrected ispVM JTAG Connector Pinout table caption information.
November 2011	01.2	Corrected error in the column headings of the Expansion Connections table.
February 2012	01.3	Updated document with new corporate logo.
February 2012	01.4	Expansion Connections table – Updated information for pins 31 and 33.
August 2012	01.5	Added alternate Abracon part numbers for Discera oscillators in Bill of Materials.
July 2013	01.6	Added note in the Alternate ispVM Download Interface section.
		Updated Technical Support Assistance information.

Appendix A. Schematics

Figure 11. Cover Page

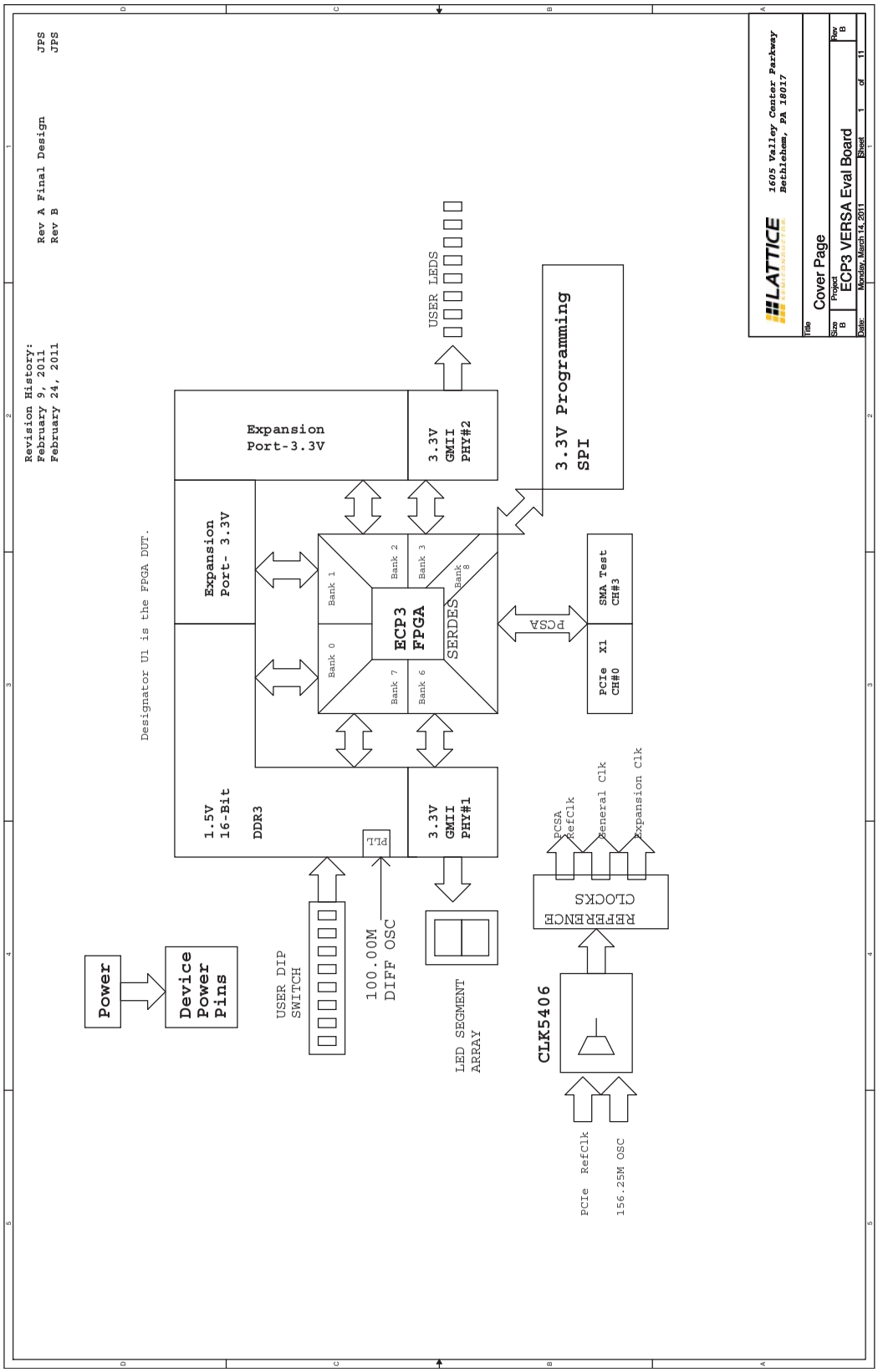


Figure 12. Power

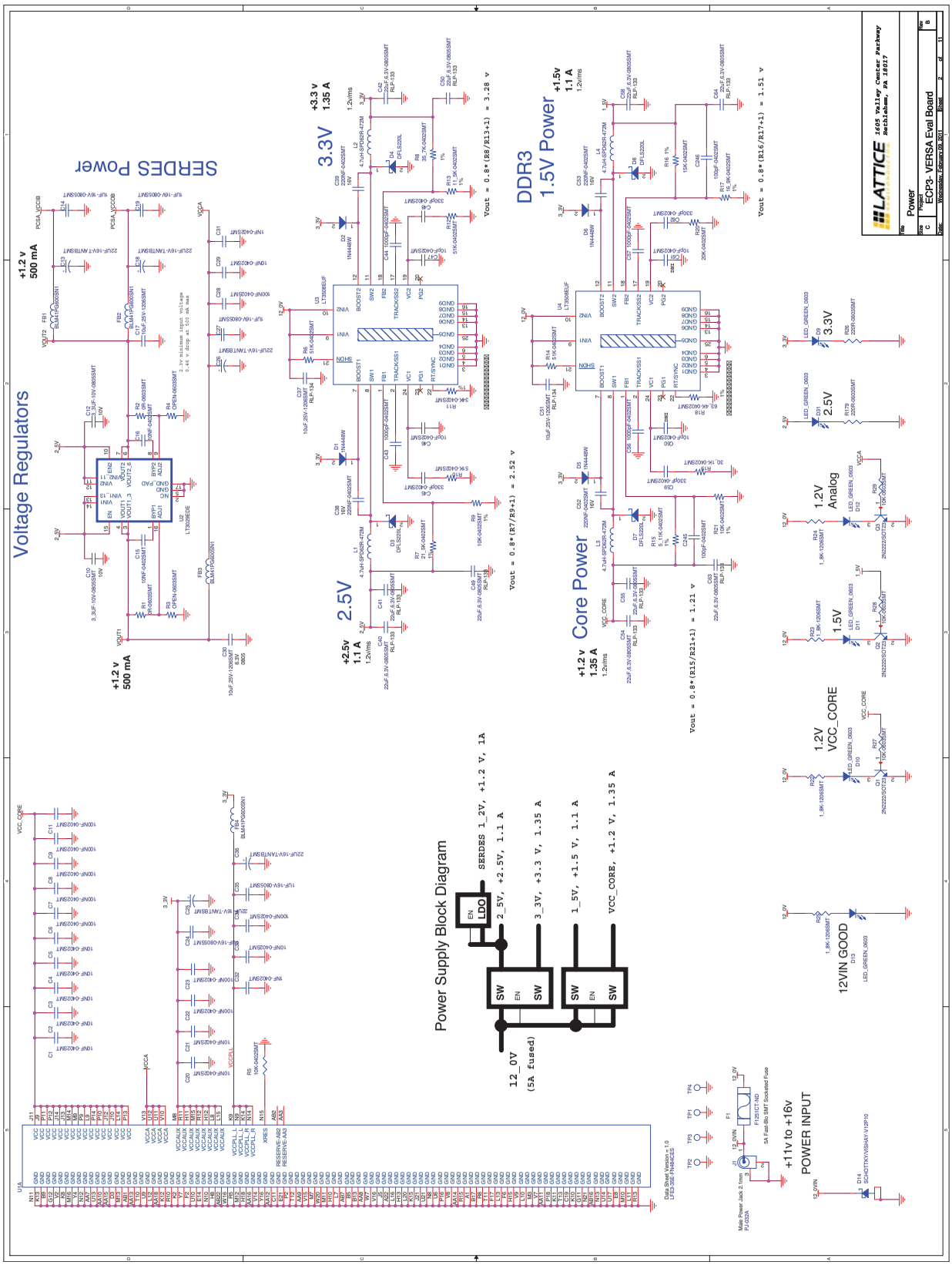


Figure 13. Programming

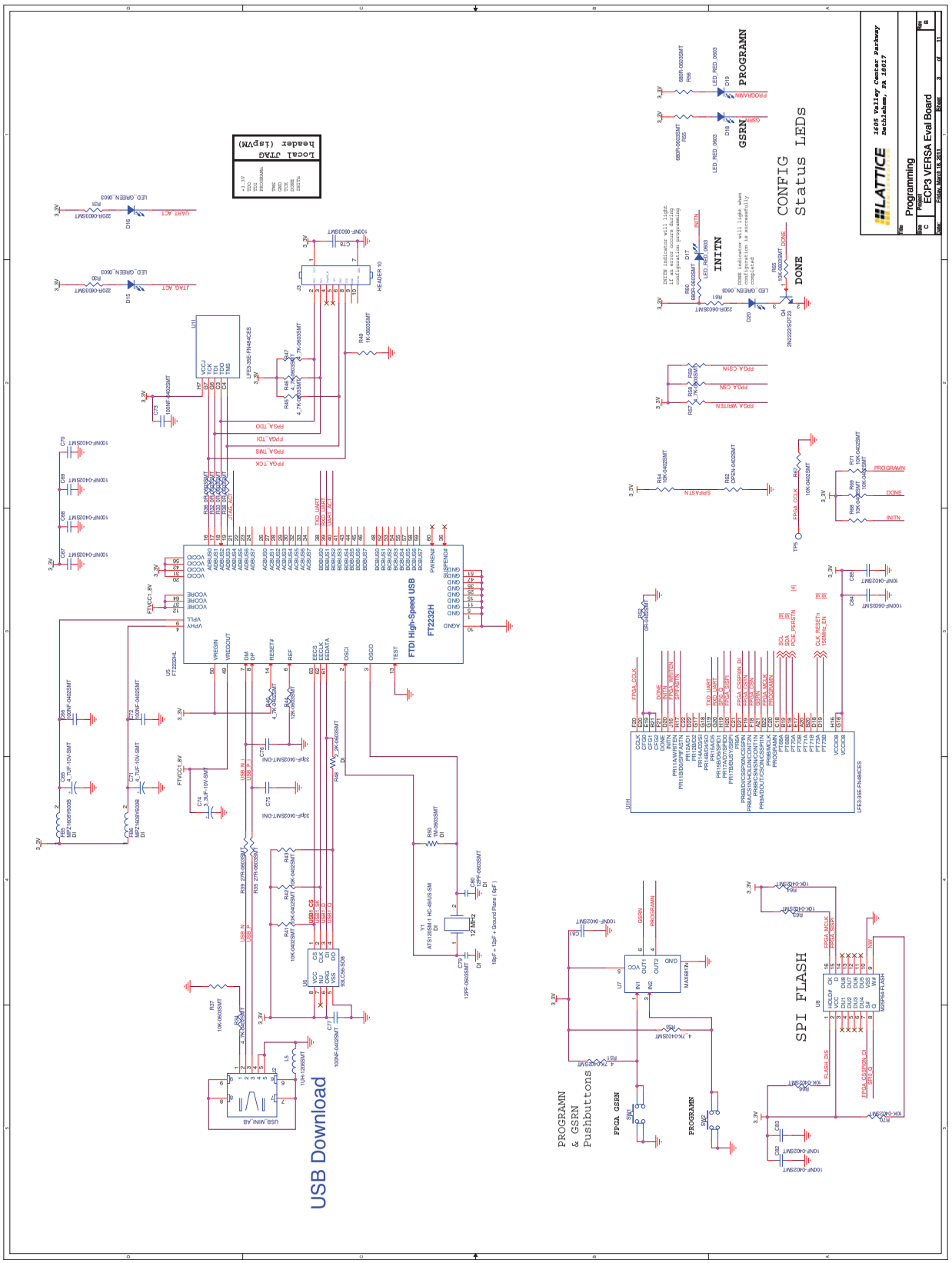


Figure 14. SERDES

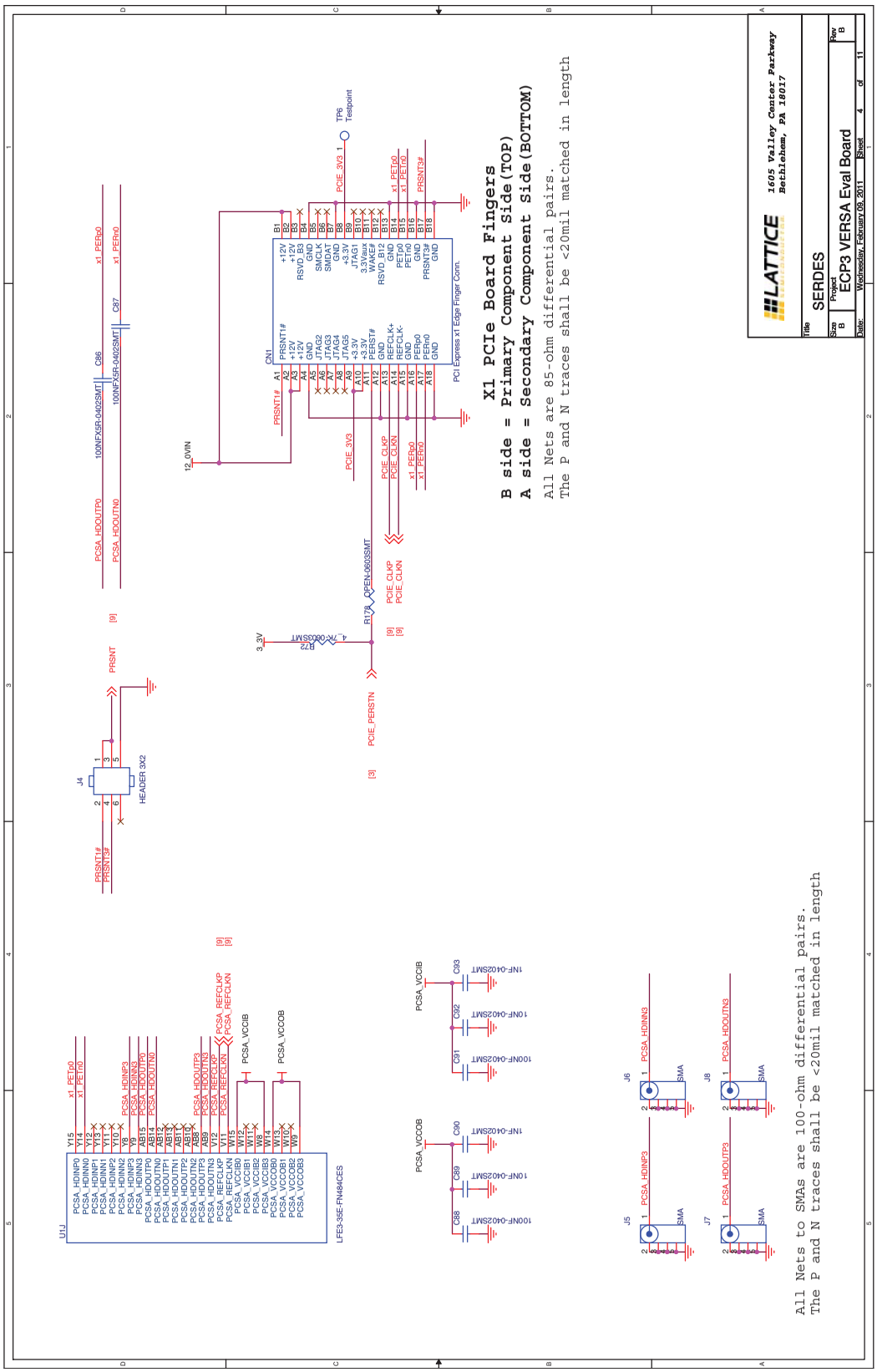


Figure 15. 10/100/1000-T PHY #1/RJ45

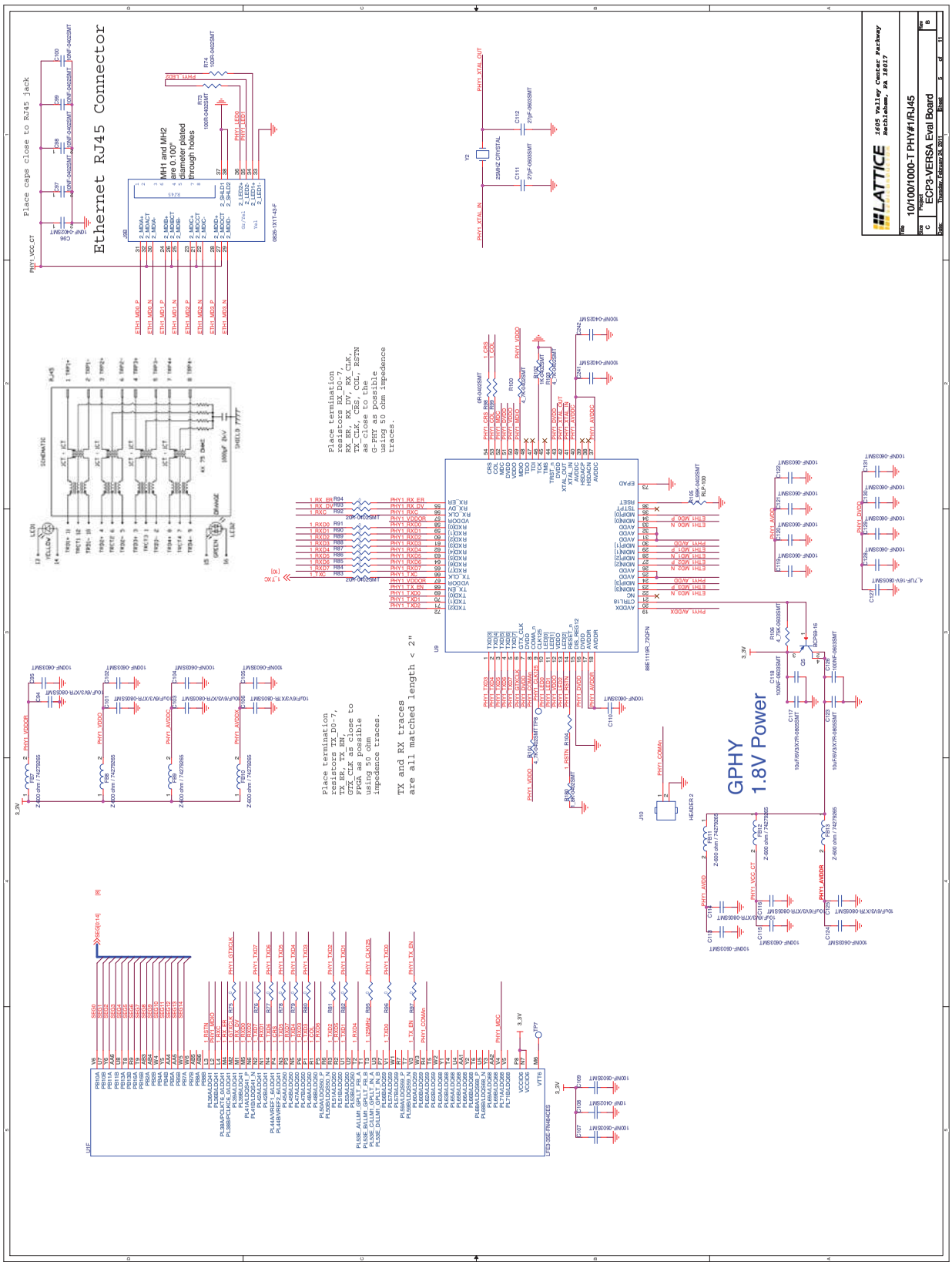


Figure 16. 10/100/1000-T PHY #2/RJ45

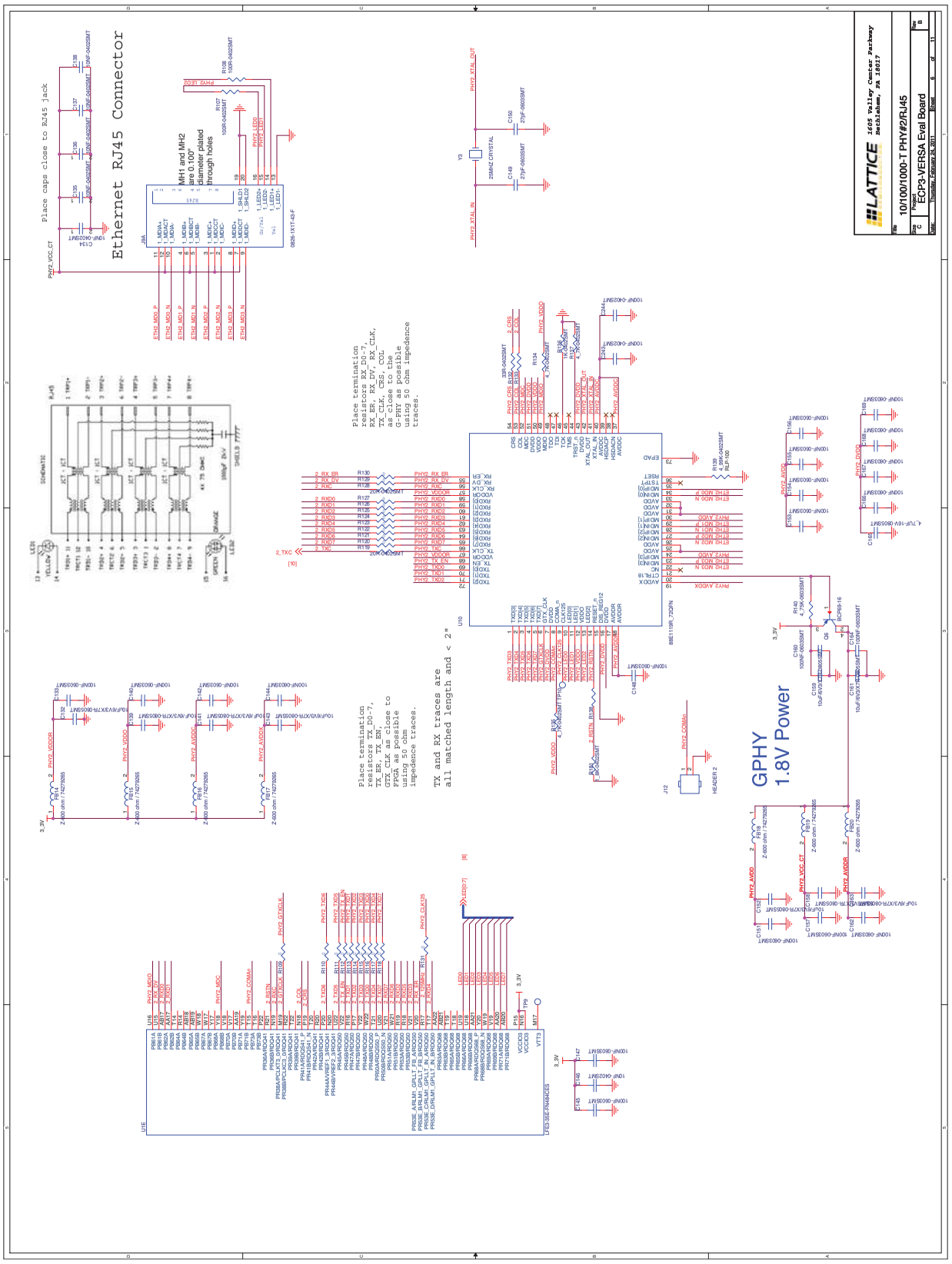


Figure 17. DDR3 Memory

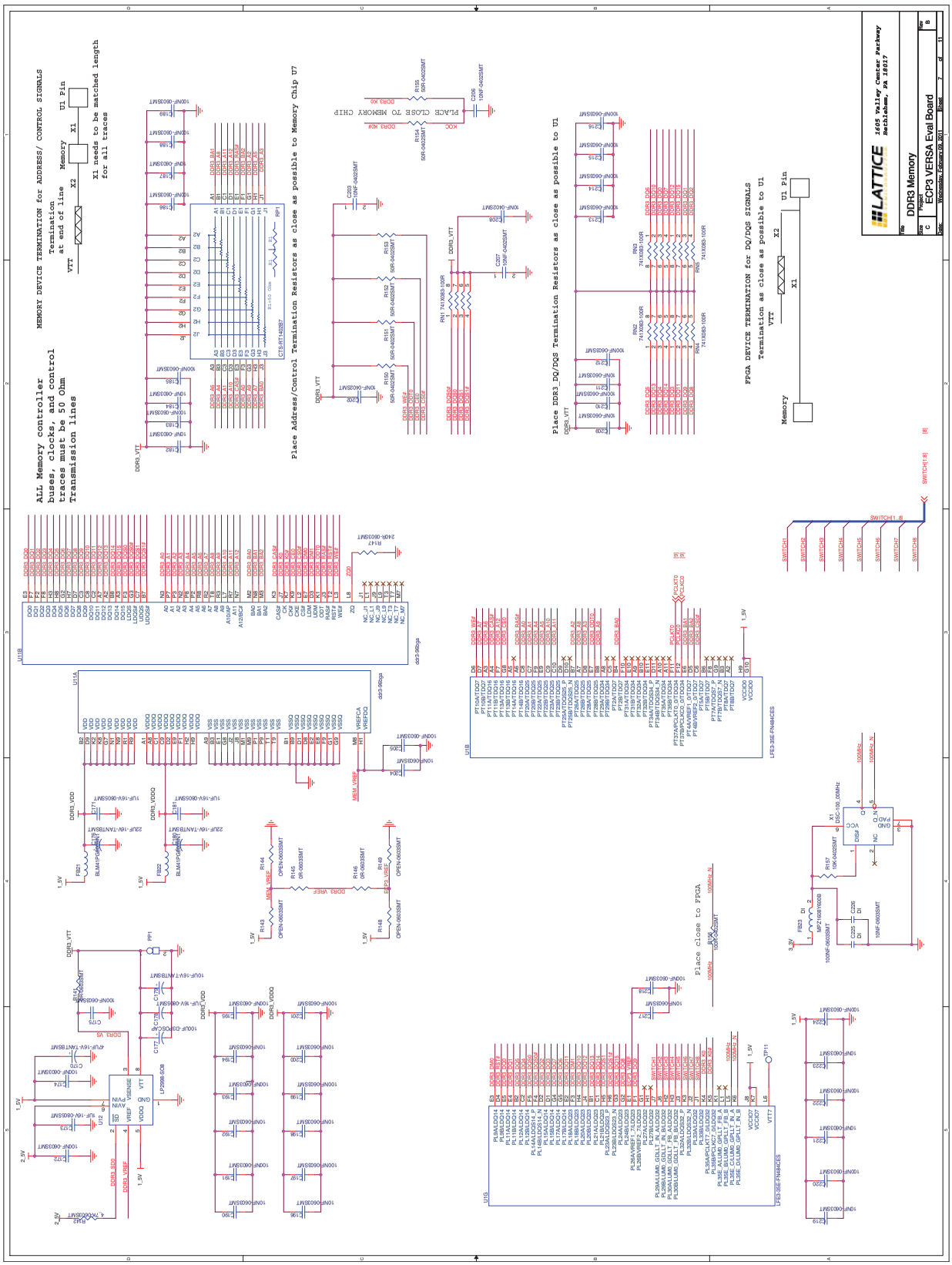


Figure 18. LEDs and Switches

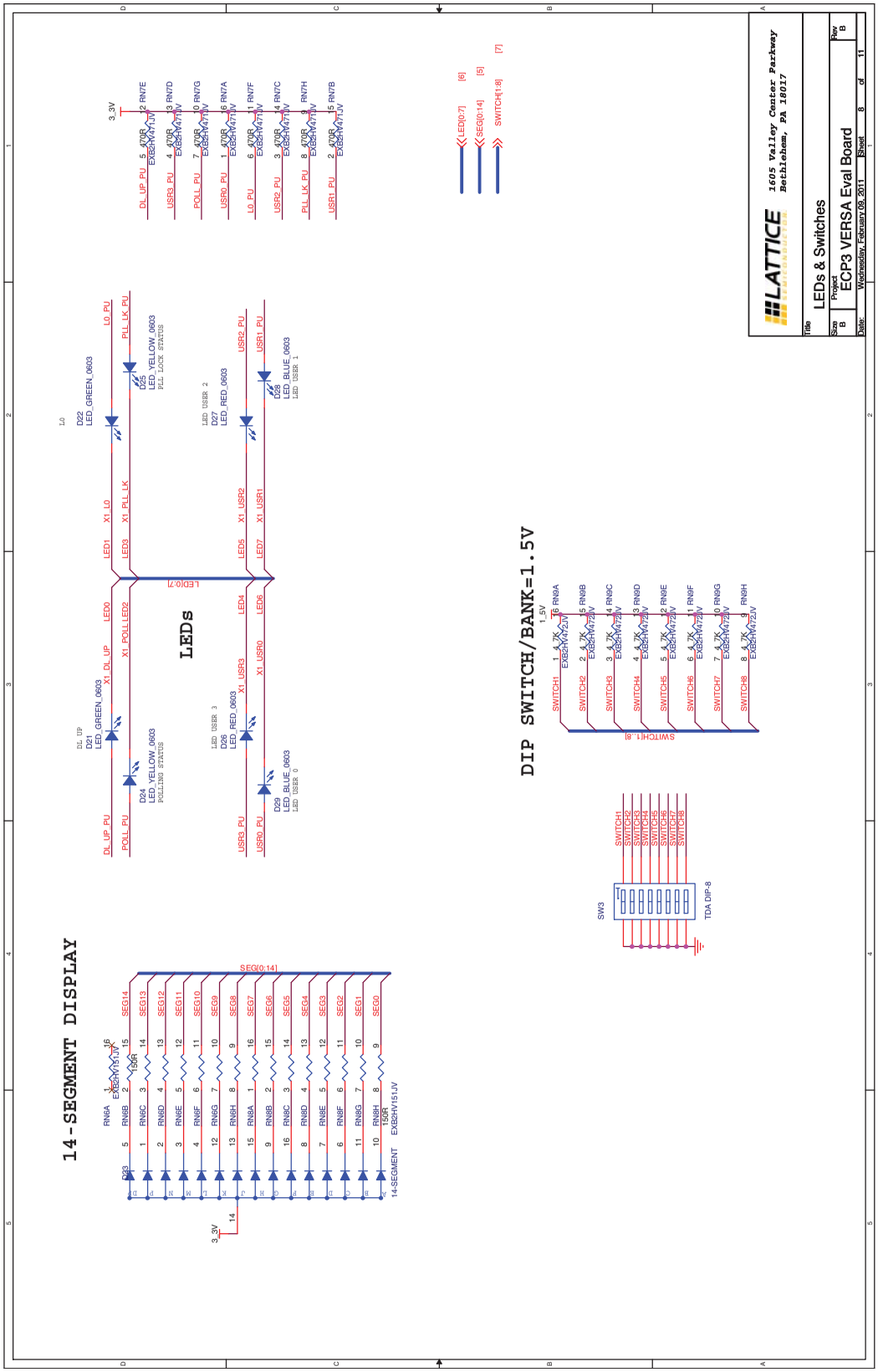


Figure 19. Reference Clock Generator

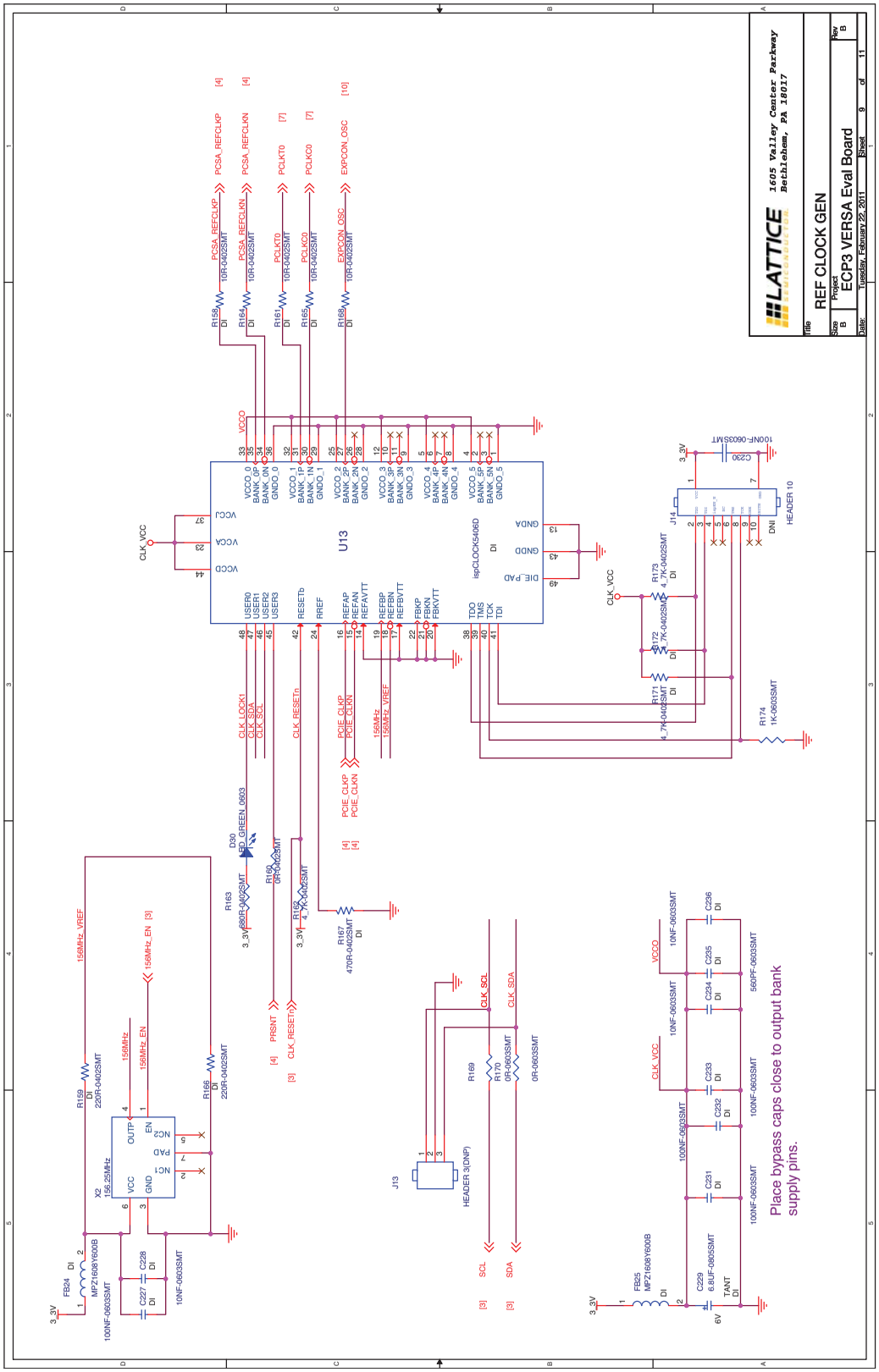


Figure 20. Expansion Connector