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LatticeECP3 PCI Express Solutions Board – Revision A

User's Guide

Introduction

As PCI Express applications have emerged, the LatticeECP3™ FPGA family has become a well-suited solution for many system designs. The features of the LatticeECP3 PCI Express Solutions Board can assist engineers with rapid-prototyping and testing their designs. The board is an enhanced form-factor of the PCI Express add-in card specification. It allows for full x1 form-factor compliance and x4 is available for demonstration purposes with some non-standard form-factor issues. The flexibility to use the same board to demonstrate both x1 and x4 configurations is accomplished by simply changing the mounting hardware. The board has several debugging and analyzing features for complete evaluation of the LatticeECP3 device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP3 FPGA.

This user's guide describes the LatticeECP3 PCI Express Solutions Board featuring the LatticeECP3 LFE3-95EA-FN672 FPGA. The stand-alone evaluation board provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces to demonstrate PCI Express capabilities using an add-on card form-factor. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 85-ohm for differential traces.

*Important: This document (including the schematics in the appendix) describes LatticeECP3 PCI Express Solutions Boards marked as **Rev A**. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo.*

Figure 1. LatticeECP3 PCI Express Solutions Board

Features

- PCI Express x1 and x4 edge connector interfaces

- Allows demonstration of PCI Express (x 1and x4) interfaces
  - x1 is form-factor compliant and will fit a standard PC-equipped PCI Express motherboard socket
  - x4 is non-compliant but will demonstrate x4 functionality by a simple change to the hardware

- Allows control of SERDES PCS registers using the Serial Client Interface (ORCAstra)

- On-board Boot Flash
  - Both Serial SPI Flash and Parallel Flash via MachXO™ programming bridge

- Shows interoperation with a high performance DDR2 memory component

- Includes driver based "run-time" device configuration capability via ORCAstra or PCI Express

- Switches, LEDs, displays for demo purposes

- Input connection for lab-power supply

- Power connections and power sources

- ispVM™ programming support

- On-board and external reference clock sources

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board.

Figure 2. PCI Express Solutions Board Outline Drawing, Top Side
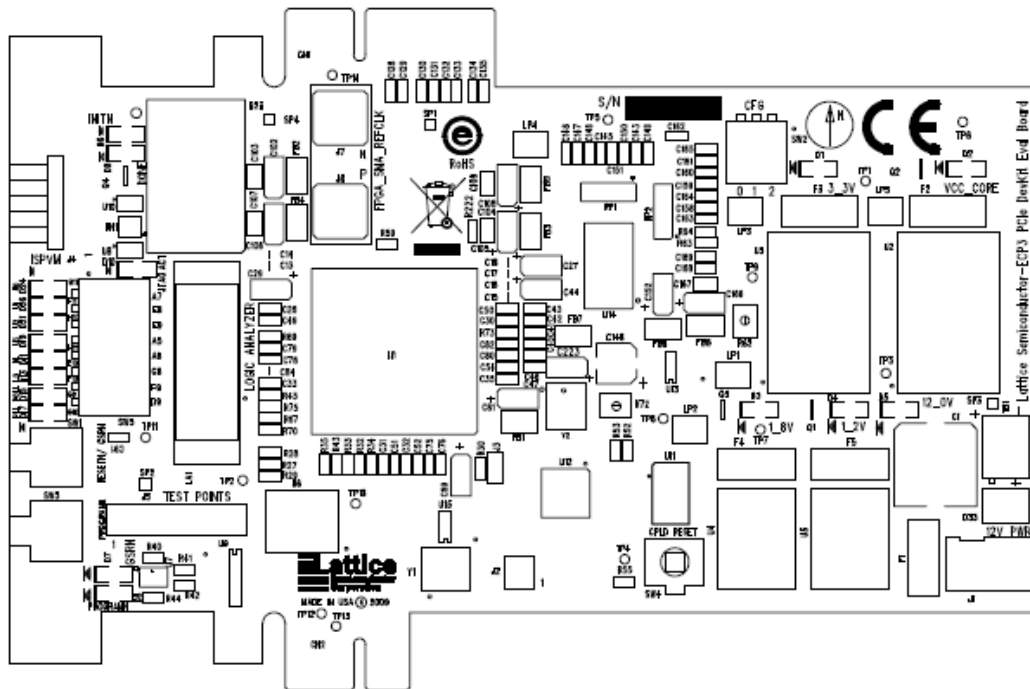
Figure 3. PCI Express Solutions Board Outline Drawing, Bottom Side
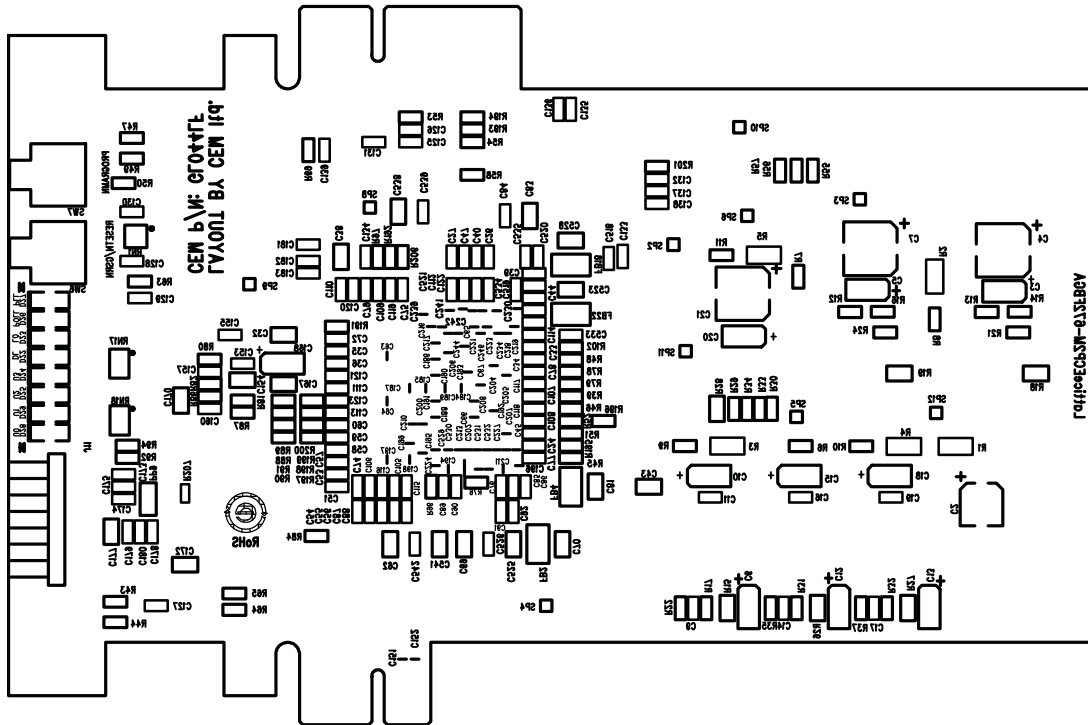
x1 and x4 PCI Express Support

PCI Express x1 and x4 is supported with the same PCB. This add-in PCB is designed to work in both types of motherboard slots. The PCB complies with the width and length dimensions of the PCI Express Card Electromechanical (CEM) Specification Revision 1.1. The only exclusion of the CEM specification is the component and back side of the add-in board may interfere with other boards in a fully-populated motherboard.

This board is easily interchanged from x1 to x4 configurations by removing the back-panel bracket and reinstalling it on the opposite side. This permits plug-in into PCI Express sockets on the motherboard and securing it in the chassis if desired. The back-panel bracket is shown below.

Figure 4. Back Panel Drawing
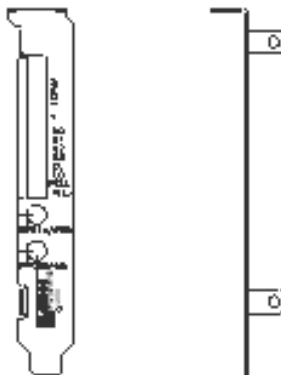
LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP3 devices in the 672-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP3 Family Data Sheet on the Lattice website at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFE3-95EA-FN672 device. Available I/Os and associated sysI/O™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeECP3 PCI Express Solutions Board is ready to power on. The board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a benchtop supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J1 and plug the wall-transformer into an AC wall-outlet.

Power Supplies

(see Appendix A, Figure 21)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a benchtop supply adjusted to provide a nominal +12V DC.

All input power sources and on-board power supplies are fused with surface-mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 1. Board Power Supply Fuses (see Appendix A, Figure 21)

F1	12V Fuse
F2	1.2V Core Fuse
F3	3.3V Fuse
F4	1.8V Fuse
F5	1.2V Analog Supply

Table 2. Board Power Supply Indicators (see Appendix A, Figure 21)

D1	3.3V Source Good Indicator
D2	1.2V VCC Core Source Good Indicator
D3	1.8V Source Good Indicator
D4	1.2V Analog Source Good Indicator
D5	12V Input Good Indicator

External power can be alternatively connected rather than the wall transformer power pack.

Table 3. External Board Supply Input Terminal (see Appendix A, Figure 21)

TB1	Screw terminal for +12V DC Pin1 (square PCB pad): +12V DC Pin2: Ground

PCI Express Power Interface

Power can be sourced to the board via the PCB edge-fingers (CN1 and CN2). This interface allows the user to provide power from a PCI Express Host board.

Programming/FPGA Configuration

(see Appendix A, Figure 23)

A programming header is provided on the evaluation board, providing access to the LatticeECP3 JTAG port.

ispVM Download Interface

J4 and J8 are 6-pin JTAG connectors used in conjunction with the ispVM USB download cable to program and control the device. These connectors are available through the back-panel bracket as needed for x1 or x4 PCI Express configurations. These connectors are used in conjunction with the ispVM programming cable and software to program the configuration memory or FPGA directly.

Table 4. Standard ispVM Programming Cable Configuration

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	TMS
Pin 5	GND
Pin 6	TCK

After initial board setup, use the following procedure to program the evaluation board. Instructions assume ispVM software has been installed on a local PC.

Connect the ispDOWNLOAD cable rainbow colored flywires to the connector J4.

Table 5. ispVM JTAG Connector (see Appendix A, Figure 21)

6 5 4 3 2 1
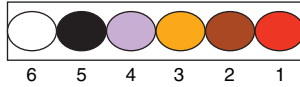
Note: A dot denotes PIN 1 on the both the
PCB or back-panel bracket.

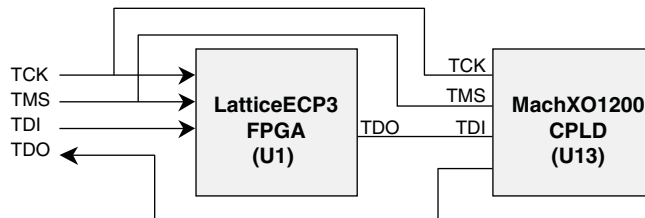| Pin	Function	Color
1	PWR	Red
2	TDO	Brown
3	TDI	Orange
4	TMS	Purple
5	GND	Black
6	TCK	White

Figure 5. ispVM Programming Cable Connector
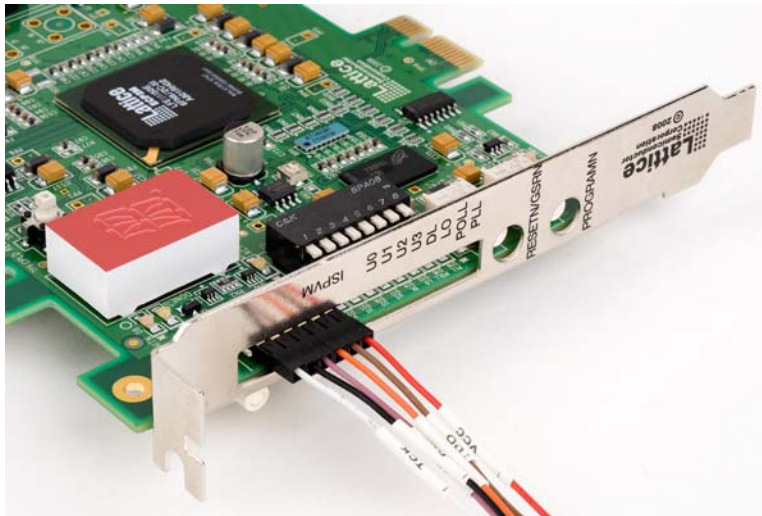
Programming the Daisy Chain

This board includes two Lattice Semiconductor programmable (U1=LFE3-95, U12=LCMXO1200) devices that can be programmed in a daisy chain.

Figure 6. JTAG Chain

Download Procedures

Requirements:

- PC with ispVM System v.17.7 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download
The LatticeECP3 device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

1. Connect the LatticeECP3 PCI Express Solutions Board to the appropriate power sources and power up board.

2. Connect the ispDOWNLOAD cable to the appropriate header. J4 is used for the 1x6 connection. J8 is used in the same manner for x4 configurations.

3. Start the ispVM System software.

4. Press the **SCAN** button located in the toolbar. The LatticeECP3 and the MachXO1200 devices should be automatically detected.

Figure 7. ispVM Main Window
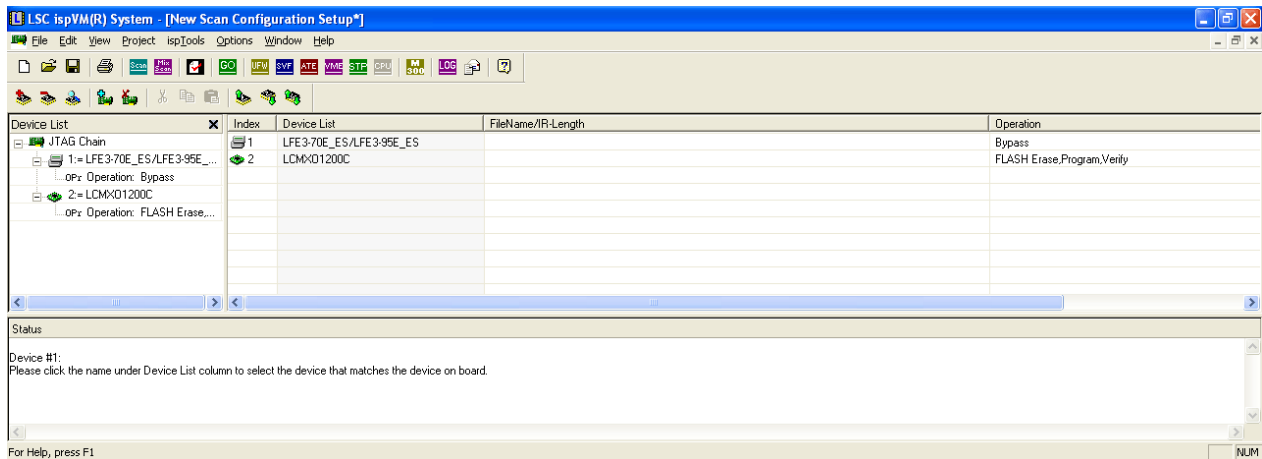
5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.

6. To program only the LatticeECP3-95, place the LCMXO1200C device into **BYPASS** and the LFE3-95 should be in **FAST PROGRAM** mode.

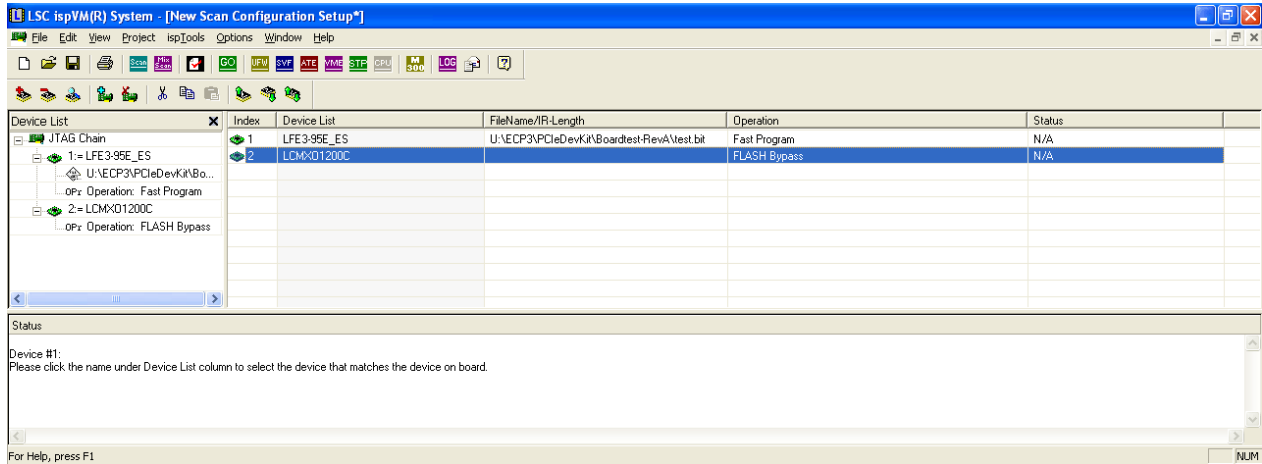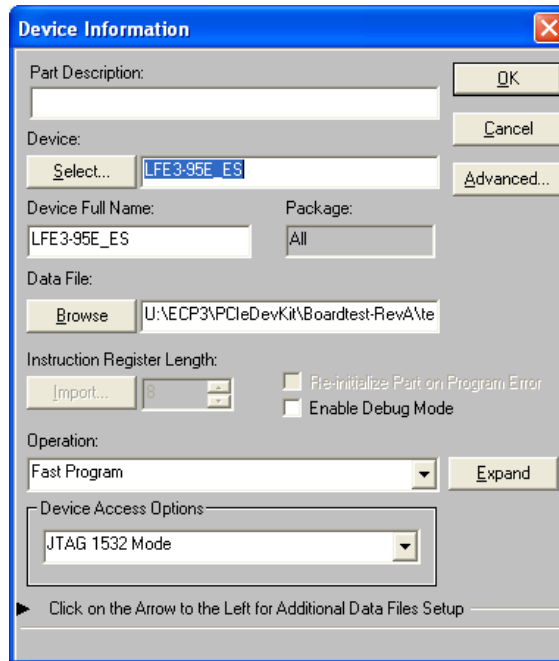*Figure 8. ispVM Fast Programming Mode*

Figure 9. ispVM Device Information Dialog Box

7. Add Data File.

8. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Configuration Status Indicators
(see Appendix A, Figure 23)

These LEDs indicate the status of configuration to the FPGA.

• D6 (red) illuminated, this indicates that the programming was aborted or reinitialized driving the INITN output low.

• D9 (green) is illuminated, this indicates the successful completion of configuration by releasing the open collector DONE output pin.

- D10 (green) will flash indicating TDI activity.

- D8 (red) illuminated, this indicates that PROGRAMN is low.

- D7 (red) illuminated, this indicates that GSRN is low.

PROGRAMN & GSRN
(see Appendix A, Figure 23)

- These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3 or SW7) and GSRN (SW1 or SW6). Depressing the button drives a logic level "0" to the device.

- These push-buttons are accessible from the back panel if the evaluation board is mounted in a PCI Express slot of a PC.

CFG [2:0]
(see Appendix A, Figure 23)

- The FPGA CFG pins are set on the board for a particular programming mode via the SW2 DIP switch.

- JTAG programming is independent of the MODE pins and is always available to the user.

- Pushing in (depressing) the switch is ON and sets the value to 0.

Table 6. CFG Mode Selections

CFG2	CFG1	CFG0	Configuration Mode
0 (ON)	0 (ON)	0 (ON)	SPI Flash
0 (ON)	1 (OFF)	0 (ON)	SPIm
1 (OFF)	0 (ON)	1 (OFF)	Slave Serial
1 (OFF)	1 (OFF)	1 (OFF)	Slave Parallel
X (don't care)	X (don't care)	X (don't care)	ispJTAG™

**On-Board Serial SPI Flash Memory**
(see Appendix A, Figure 23)

- One Serial SPI (16-pin tssop 64M) Flash memory device (U6) is on-board for non-volatile configuration memory storage. Either a STMicro M25P64VMF16 or Macronix MX25L6405 device is populated on-board.

- All CFG [2:0] need to be [000] depressed to read the Flash memory at power-up or after toggling the PRO-GRAMN pin.

- Install jumper across pins 2 and 4 on J2.

Programming Serial SPI Flash Memory
The Serial SPI Flash memory device can be configured easily via its JTAG port. This mode enables the FPGA to be programmed at power-up or assertion of PROGRAMN with a bitstream stored in the memory device.

1. Connect the LatticeECP3 PCI Express Solutions Board to the appropriate power sources and power-up board.

2. Connect the ispDOWNLOAD cable to the appropriate header. J4 is used with the cable.

3. Start the ispVM System software.

4. Press the **SCAN** button located in the toolbar. The LFE3-95 and the LCMXO1200C devices should be automatically detected.

Figure 10. Results of Scanning Board via ispVM
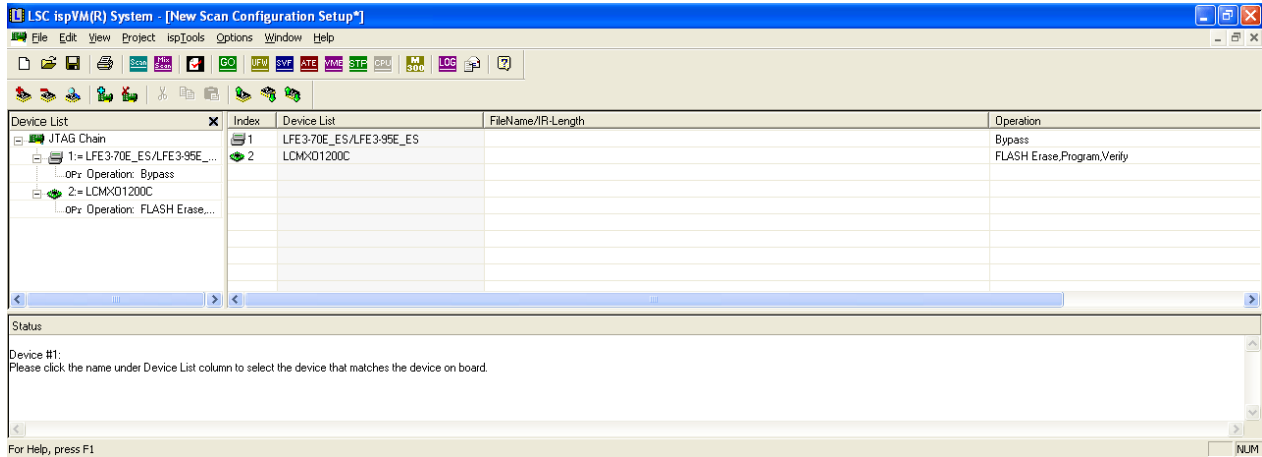
5. Double-click the **Operation** column for the LFE3-95 and the Device Dialog box shown below will open.

6. In the dialog box, select the **SPI Flash Programming** mode in the **Device Access Options** pull-down menu. This will open the SPI Serial Flash Dialog box.

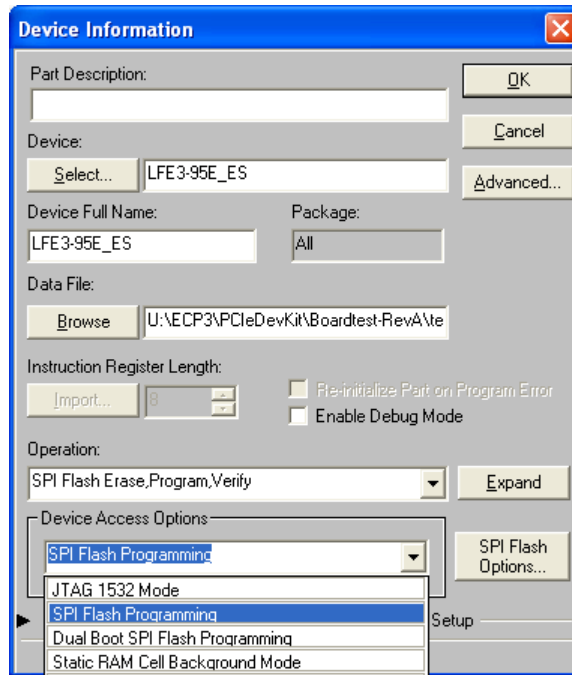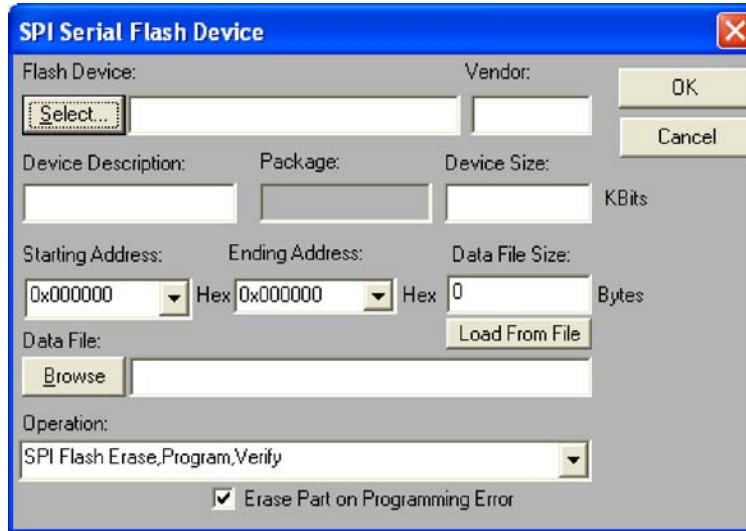*Figure 11. Device Information Dialog Screen*

Figure 12. SPI Serial Flash Dialog Screen

7. The SPI Serial Flash Device dialog box will open. In this box select **SPI Flash Erase, Program, Verify** in the **Operation** pull-down menu.

8. Select **SPI Serial Flash** in the **Device Family** pull-down menu, **STMicro** under the **Vendor** pull-down menu, **SPI-M2564** under the **Device** pull-down menu, and **16-lead SOIC** under the **Package** submenu.
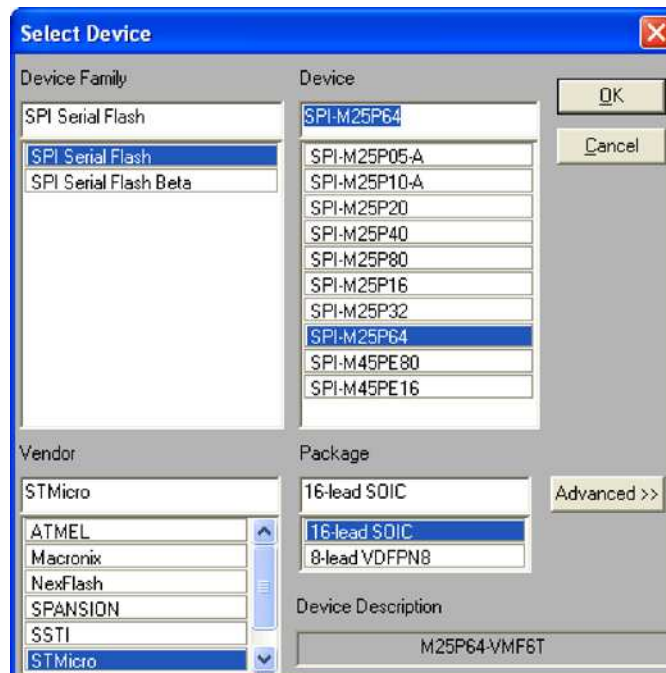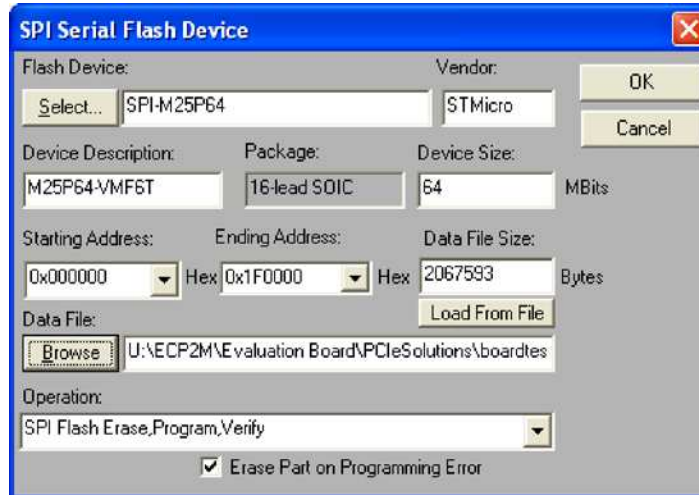
*Figure 13. Select Device Dialog Box*

*Figure 14. Sample SPI Serial Flash Device Dialog Box*

9. Click **OK** in the **SPI Flash Device** dialog box. Then click **OK** in the **Select Device** dialog box. You will then return to the main configuration screen. If you do not desire to load the LCMXO1200C device, this device should be placed in Flash Bypass mode by double-clicking the **Operation** column and selecting the **Bypass** operation shown below.

Figure 15. FLASH Bypass for LCMXO1200C Device
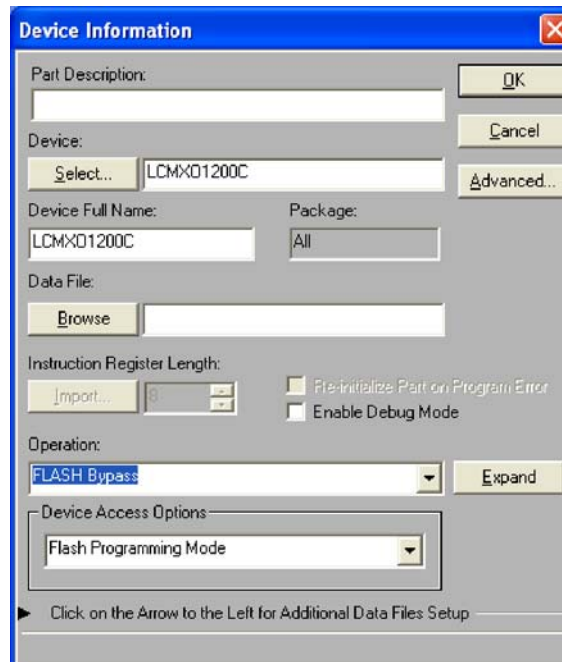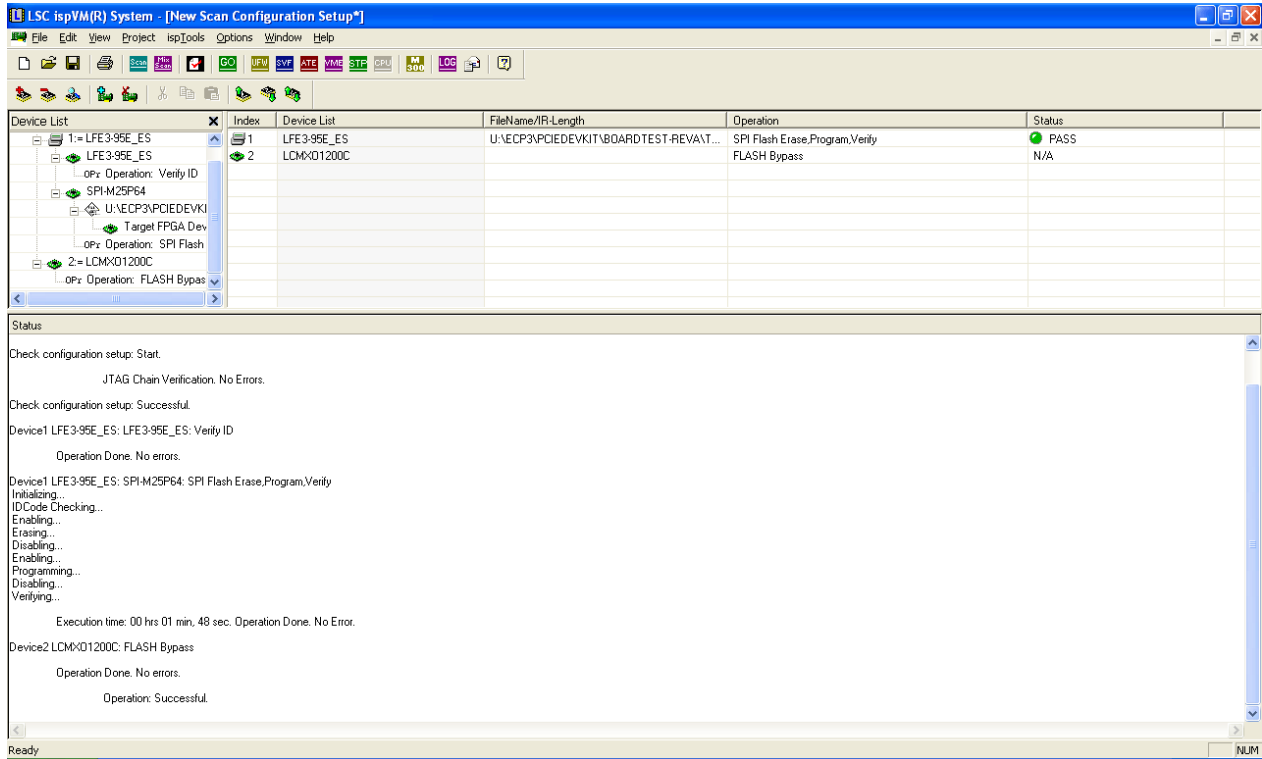
Figure 16. Programming Main Window
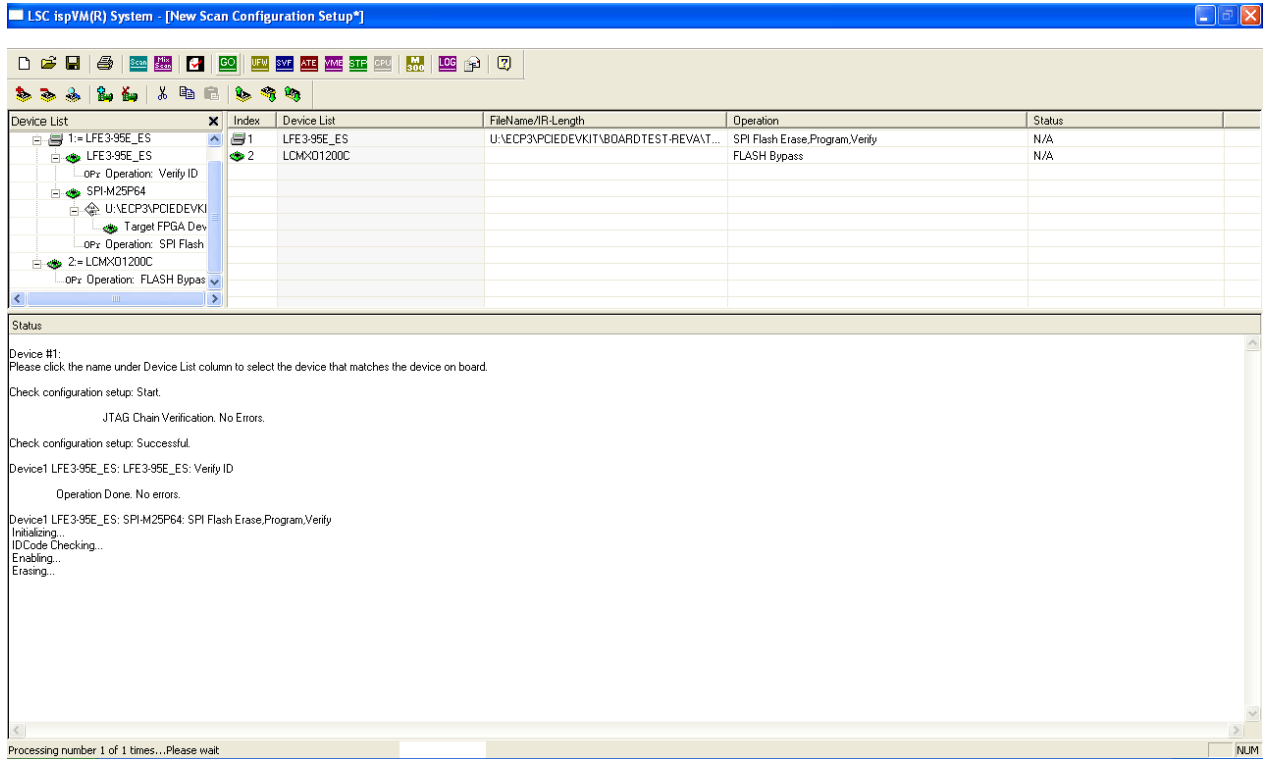
10. From the main programming window, select **GO** in the top toolbar. This will begin the SPI Serial Flash programming.

Figure 17. SPI Serial Flash Programming Status Window

Figure 18. Successful SPI Serial Flash Programming Session

On-Board Parallel SPI Flash Memory
(see Appendix A, Figure 24)

- A 16-bit parallel Flash device is also available. This board uses a Lattice MachXO CPLD device to act as a pro-gramming bridge from the Flash device.

- The CFG [2:0] need to be [111], all up.

- Lattice ispVM programming software can be used to program either the serial SPI Flash or the parallel Flash devices. Application note AN8077, *Parallel Flash Programming and FPGA Configuration,* addresses the use of the parallel Flash implementation. *Note: For parallel Flash loading, the board needs the appropriate connections of J2. J2 requires a jumper be installed between pins 1 and 3.*

User-Defined General Purpose Clock Oscillator

(see Appendix A, Figure 27, Y1)

A 100MHz oscillator is included on-board. It is fanned-out to several destinations on the board, as described in Table 7.

Table 7. 100MHz Clock Destinations

Clock Destination	PCB Designation	Destination Pin
CPLD	U12	A8
FPGA	U1	P21-PCLKT2_0
FPGA	U1	K3-LLUM0-GDLLT_IN
FPGA	U1	M4-PCLKT7_0

SERDES

(see Appendix A, Figure 25)

SERDES/FPGA Reference Clocks

The 50-ohm terminated SMA connectors are optionally provided to supply reference clocks directly to the LatticeECP3 device. Please contact the factory for information to populate the PCB with SMA connectors.

Table 8. SMA Inputs for External Clock Source

Connector	SERDES Signal	FPGA Pin
J6	FPGA_SMA_REFCLKP	V20
J7	FPGA_SMA_REFCLKN	W19

SERDES PCI Express Channels

(see Appendix A, Figure 25)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1 or CN2) that fit directly into a PCI Express host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

Table 9. x1 PCI Express Connections

CML Pin Name	FPGA Pin	PCIE	PCI Express Edge	Description
PCSA_HDOUTP_0	AF21	PERp0	A16	Integrated endpoint block transmit pair
PCSA_HDOUTN_0	AF20	PERn0	A17	
PCSA_HDINP_0	AD21	PETp0	B14	Integrated endpoint block receive pair
PCSA_HDINN_0	AD20	PETn0	B15	
PCSA_REFCLKP	AC17	PCIe_CLKp	A13	Integrated endpoint block differential clock pair
PCSA_REFCLKN	AC18	PCIe_CLKn	A14	
PCIE_PERSETN	U20	PERSTN	A11	Fundamental PCI Express reset

Table 10. x4 PCI Express Connections

CML Pin Name	FPGA Pin	PCIE	PCI Express Edge	Description
PCSB_HDOUTP_0	AF13	PERp0	A16	Integrated endpoint block transmit pair
PCSB_HDOUTN_0	AF12	PERn0	A17	
PCSB_HDINP_0	AD13	PETp0	B14	Integrated endpoint block receive pair
PCSB_HDINN_0	AD12	PETn0	B15	
PCSB_HDOUTP_1	AF10	PERp1	A21	Integrated endpoint block transmit pair
PCSB_HDOUTN_1	AF11	PERn1	A22	
PCSB_HDINP_1	AD10	PETp1	B19	Integrated endpoint block receive pair
PCSB_HDINN_1	AD11	PETn1	B20	

Table 10. x4 PCI Express Connections (Continued)

CML Pin Name	FPGA Pin	PCIE	PCI Express Edge	Description
PCSB_HDOUTP_2	AF9	PERp2	A25	Integrated endpoint block transmit pair
PCSB_HDOUTN_2	AF8	PERn2	A26	
PCSB_HDINP_2	AD9	PETp2	B23	Integrated endpoint block receive pair
PCSB_HDINN_2	AD8	PETn2	B24	
PCSB_HDOUTP_3	AF6	PERp3	A29	Integrated endpoint block transmit pair
PCSB_HDOUTN_3	AF7	PERn3	A30	
PCSB_HDINP_3	AD6	PETp3	B27	Integrated endpoint block receive pair
PCSB_HDINN_3	AD7	PETn3	B28	
PCSB_REFCLKP	AC9	PCIe_CLKp	A13	Integrated endpoint block differential clock pair
PCSB_REFCLKN	AC10	PCIe_CLKn	A14	
PCIE_PERSETN	U20	PERSTN	A11	Fundamental PCI Express reset

FPGA Test Pins
(see Appendix A, Figure 27)

General Purpose DIP Switch
(see Appendix A, Figure 27, SW5)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to a switch (SW5) which is an SPST side actuated DIP switch. The switch is physically located on the secondary side of the PCB along the back-panel edge. The switches are connected to a logic level 0 when depressed toward the board and a 1 when away from the board. The designated pins are connected according to Table 11.

Table 11. FPGA Test Pins (See Appendix A, Figure 26)

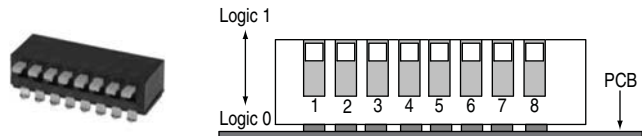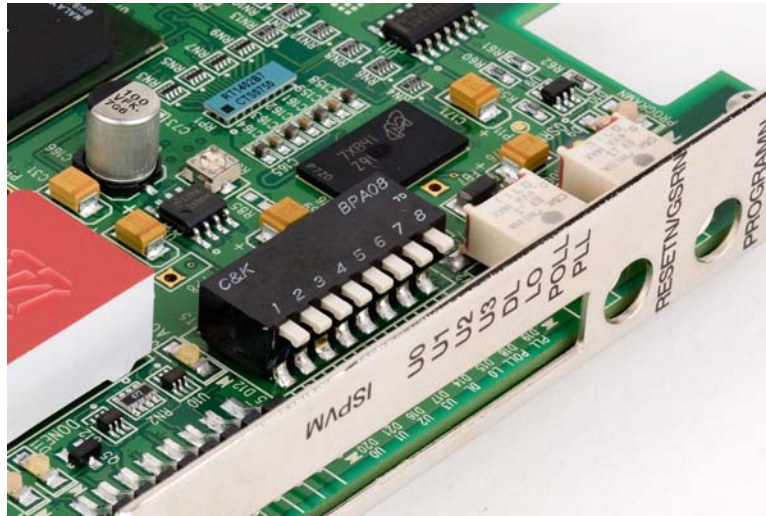| FPGA BGA	SW5 Switch Position
D9	1
F9	2
G8	3
A6	4
A5	5
E9	6
E8	7
A7	8

Figure 19. 8-position DIP Switch (SW5) on Secondary PCB Side

General Purpose LEDs
(see Appendix A, Figure 27)

LEDs are provided along the back panel edge of the PCB. These LEDs are connected to general-purpose FPGA I/Os. The LEDs are illuminated by the associated FPGA outputs being driven to a valid LOW level. The use of these LEDs is defined for PCI Express applications to observe the status of the PCI Express link during operation. The LEDs must be included in the FPGA design. These status LEDs are available in both x1 or x4 configurations. The back panel marking reflects PCI Express specific status.

Table 12. LED Definitions

PCI Express x1		PCI Express x4		
FPGA Pin#	PCB Designator	FPGA Pin#	PCB Designator	Description
H11	D19	C10	D20	User defined
H10	D21	A9	D22	User defined
F11	D26	A10	D27	User defined
G11	D24	B10	D25	User defined
D10	D11	D10	D12	Data link up active
F10	D13	A8	D14	L0 state active
G9	D15	B8	D16	Polling state inactive
G10	D17	C9	D18	PLL locked

General-Purpose Header
(see Appendix A, Figure 27, J5)

A 2x9 header (J5) provides a general-purpose connection to communicate with general purpose FPGA I/Os.

Table 13. General Purpose Header Connections

| Header Pin	FPGA Pin	Header Pin	FPGA Pin
1	GND	2	GND
3	C15	4	E15
5	B15	6	E14
7	C14	8	A20
9	D14	10	A19
11	B16	12	C17
13	C16	14	B17
15	F13	16	A18
17	F14	18	A17

17-Segment LED Display
(see Appendix A, Figure 27, D13)

General-purpose FPGA pins are connected to a 17-segment display according to Table 14. These pins can be driven low to illuminate the display segments.

Table 14. 17-Segment LED Display

| Segment	BGA
A	B7
B	F8
C	F7
D	A4
E	A3
F	H8
G	G7
H	C8
K	D8
M	B4
N	C5
P	C6
R	D6
S	C4
T	D5
U	C7
DP	B6
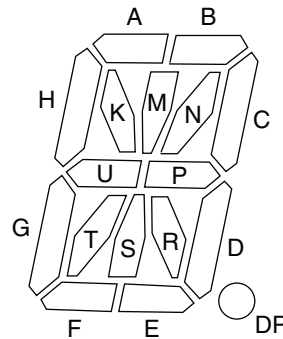
Logic Analyzer Probe
(see Appendix A, Figure 27, LA1)

An AMP/TYCO 767004 38-position .025 VERT SMD logic analyzer probe connection is provided for the user to utilize for test points. This connection provides 34 general I/O signals to be observed on a Logic Analyzer probe using Mictor connections such as the Agilent 5346A.

Table 15. Logic Analyzer To FPGA Pin Reference

Signal	FPGA Pin	Signal	FPGA Pin
LA1	AA25	LA2	Y24
LA3	W23	LA4	W22
LA5	AA26	LA6	AB26
LA7	W21	LA8	W20
LA9	AD26	LA10	AD25
LA11	AA24	LA12	AA23
LA13	AC26	LA14	AC25
LA15	Y19	LA16	Y20
LA17	AB24	LA18	AC24
LA19	Y22	LA20	AA22
LA21	AE25	LA22	AF24
LA23	AD24	LA24	AE24
LA25	AD23	LA26	AC23
LA27	AB20	LA28	AB21
LA29	AF23	LA30	AE23
LA31	W17	LA32	AB23
LA33	AB22	LA34	Y21
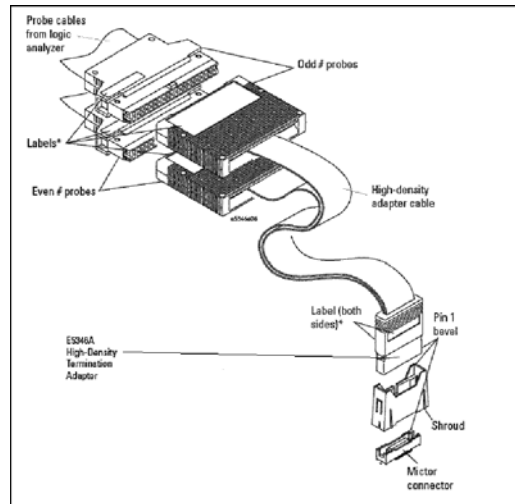
DDR2 Memory Devices
(see Appendix A, Figure 26, U14)

- The LatticeECP3 PCI Express Solutions Board is equipped with a 84-ball BGA DDR2 SDRAM memory device such as a Micron MT47H16M16BG-3 device.

- The DDR2 memory interfaces include a 16-bit wide device.

- The evaluation board includes termination of address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP3 device.

CPLD Device
(see Appendix A, Figure 24, U12)

The board includes a Lattice Semiconductor LCMXO-1200C CPLD. This device is used in conjunction with the parallel Flash device for loading the configuration memory of the FPGA. It is also used for general-purpose board management functions. It has several connections to the FPGA and other devices on the PCB. It includes an active high, push-button (SW4) if needed for a user design.

Generic user-defined interconnections are defined in Table 16.

Table 16. CPLD TO FPGA Interconnections

CPLD Pin	FPGA Pin
M1	B2
P13	B3
P10	D4
N7	E4
N8	C3
P11	D3
N13	G5
N1	G6
N3	E3
N4	F4
P1	H6
M12	J6
M2	C2
M3	D2
M4	K8
M6	J7

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP3 PCI Express Development Kit (Includes LatticeECP3 PCI Express Solutions Board)	LFE3-95EA-PCIE-DKN	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)

+1-503-268-8001 (Outside North America)

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
March 2010	01.0	Initial release.
December 2010	01.1	LED definitions table, L0 state changed from active to inactive.
		Download Procedures section, changed ispVM requirement from ispVM v.17.4 (or later) to ispVM v.17.7 (or later).
August 2012	01.2	Updated document with new corporate logo.
		Replaced Programming schematic.

Appendix A. Schematic

Figure 20. Cover Page

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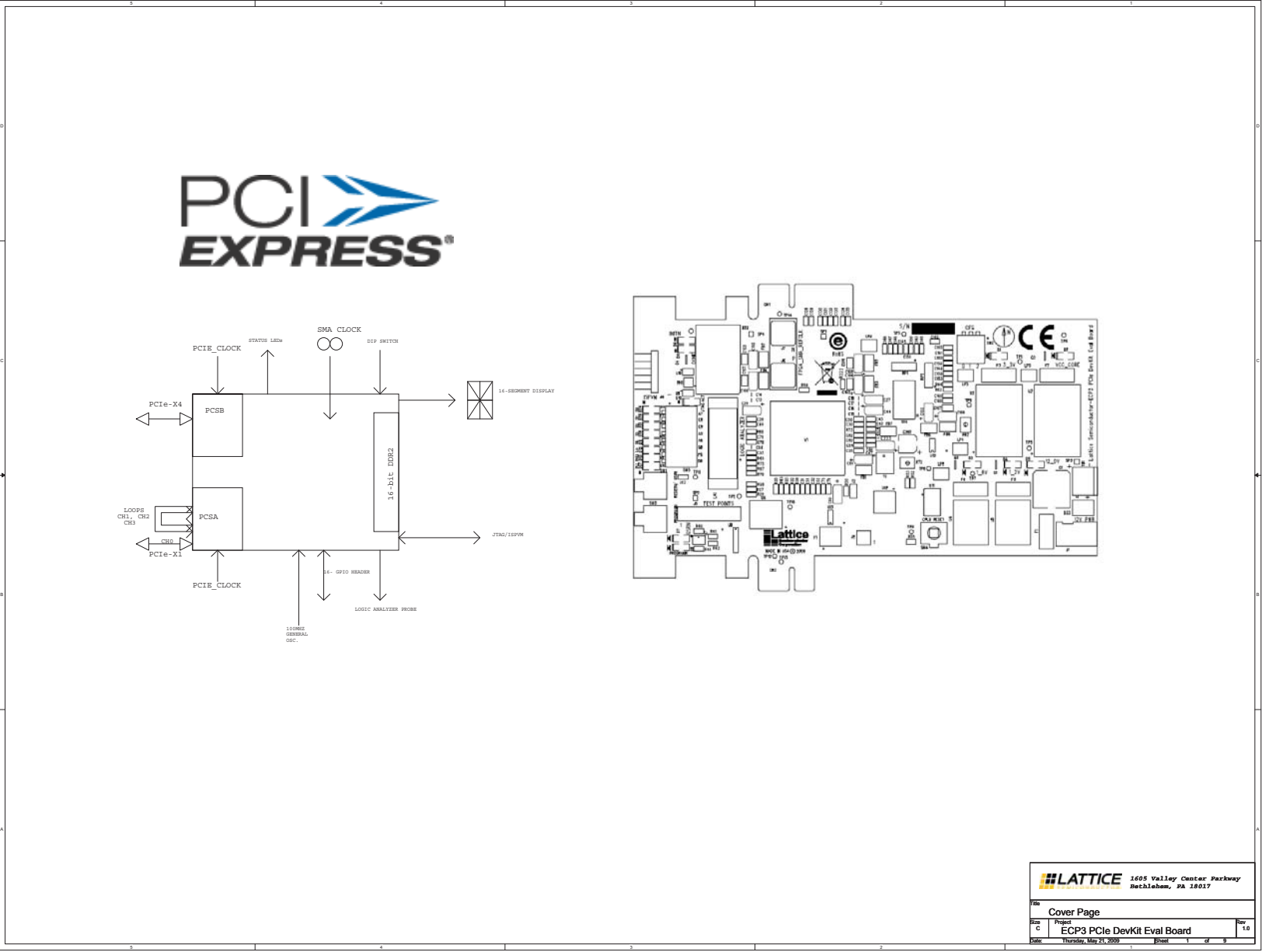
Figure 21. Power Generation

Figure 22. Power Supplies

Figure 23. Programming

CONFIG
Status LEDs

INITN indicator will light
if an error occurs during
configuration programming

DONE indicator will light when
configuration is successfully
completed

SPI FLASH

PROGRAMN
& GSRN
Pushbuttons

FPGA GSRN

PROGRAMN

SW1 and SW3 on Primary Side
SW6 and SW7 on Secondary Side

JTAG

This LED
indicates activity
on TDI.

FROM ISPVM CABLE

CONFIG
CFG Switches

CFG2	CFG1	CFG0	Configuration Mode
0 (ON)	0 (ON)	0 (ON)	SPI Flash
0 (ON)	1 (OFF)	0 (ON)	SPIm
1 (OFF)	0 (ON)	1 (OFF)	Slave Serial
1 (OFF)	1 (ON)	1 (OFF)	Slave Parallel
X	X	X	ispJTAG

1605 Valley Center Parkway
Bethlehem, PA 18017

Title: Progamming
Size: C
Project: ECP3 PCIe DevKit Eval Board
Rev: 1.0
Date: Thursday, August 09, 2012
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