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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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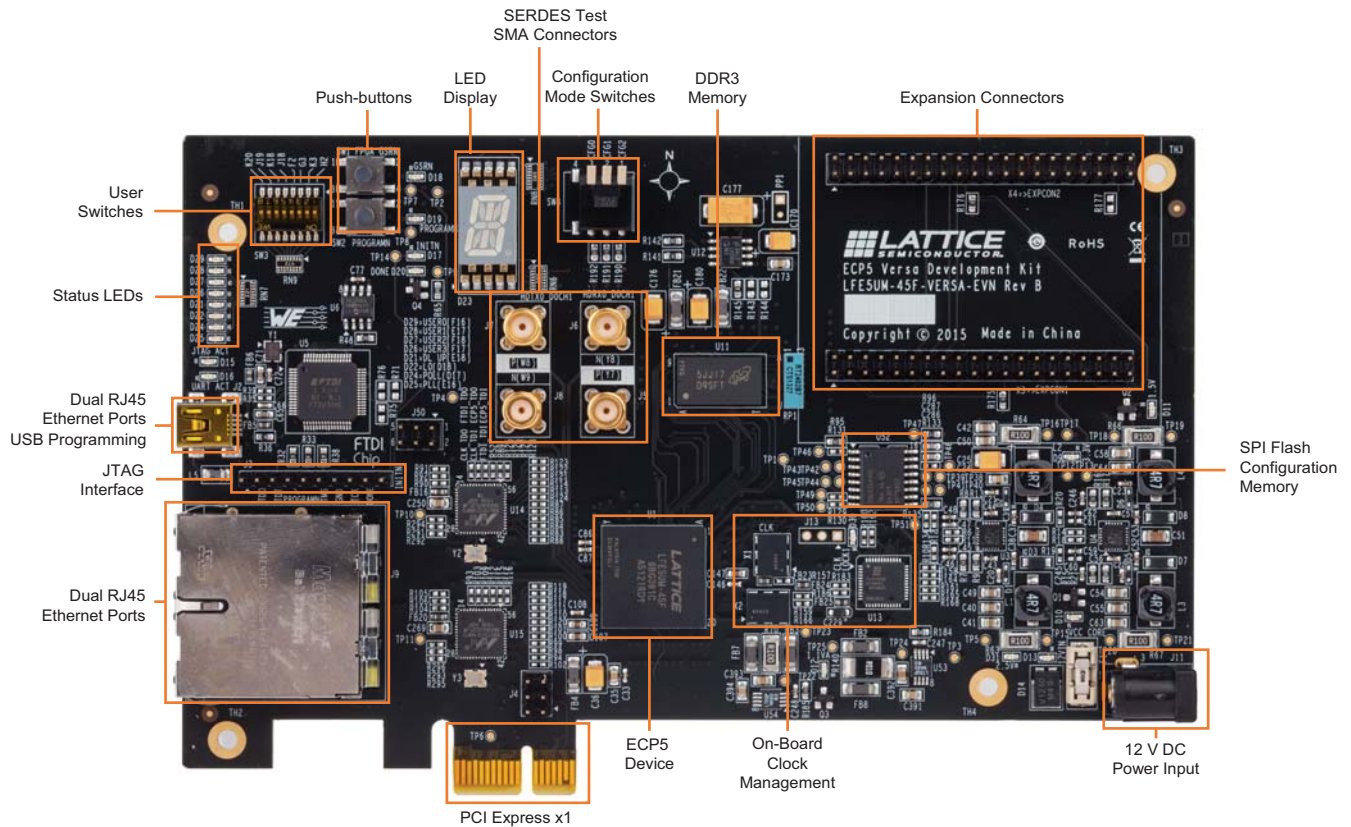
ECP5™ Versa Development Board User Guide

EB98 Version 2.1, November 2015

Introduction

The ECP5™ Versa Development Board allows designers to investigate and experiment with the features of the ECP5 Field-Programmable Gate Array. The features of the ECP5 Versa Development Board can assist engineers with rapid prototyping and testing of their specific designs. The ECP5 Versa Development Board is part of the ECP5 Versa Development Kit. The guide is intended to be referenced in conjunction with demo user guides to demonstrate the ECP5 FPGA.

Figure 1. ECP5 Versa Development Board, Top Side



Features

- Half-length PCI Express form-factor
 - Allows demonstration of PCI Express x1 interconnection
- Electrical testing of one full-duplex SERDES channel via SMA connections
- USB-B connection for UART and device programming
- Two RJ45 interfaces to 10/100/1000 Ethernet to RGMII
- On-board Boot Flash
 - 128M Serial SPI Flash
- DDR3-1866 memory components (64Mb/x16)
- Expansion mezzanine interconnection for prototyping
- 14-segment alpha-numeric display
- Switches, LEDs and displays for demo purposes
- Diamond® programming support
- On-board reference clock sources

The contents of this user guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics.

Caution: The ECP5 Versa Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the evaluation board.

ECP5 Device

This board features an ECP5 FPGA with a 1.1 V core supply. It can accommodate all pin-compatible ECP5 devices in the 381 ball caBGA package. A complete description of this device can be found in DS1044, [ECP5 Family Data Sheet](#).

*Note: The connections referenced in this document refer to the **LFE5UM-45F-8BG381C** device.*

Applying Power to the Board

The ECP5 Versa Development Board is ready to power on. The board can be supplied with power from a PCI Express host system or standalone with an external wall power module.

The 12 V DC input power source is fused with a surface mounted fuse, as noted in Table 1.

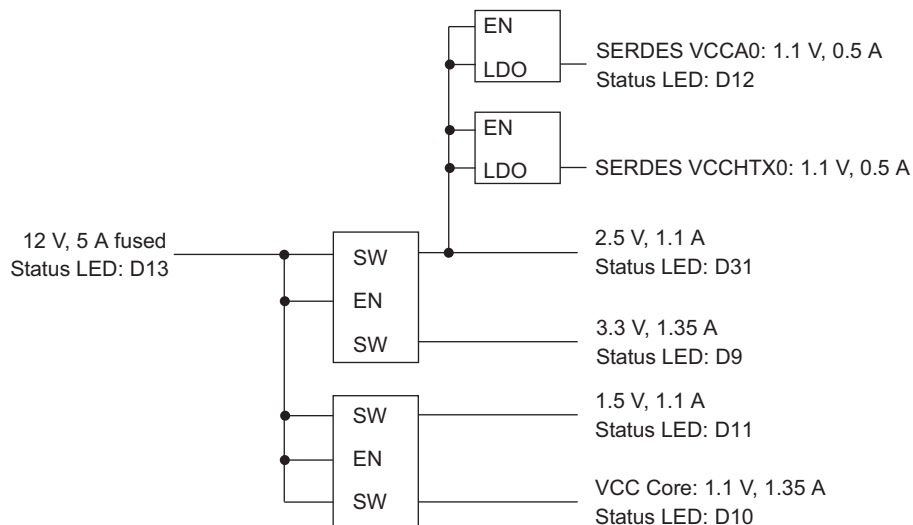
Table 1. Board Power Supply Fuses (See Appendix A, Sheet 2, Figure 11- Voltage Regulators)

Fuse Designator	Description
F1	12 V Input Supply Fuse

The board may be plugged into a host PC. Only plug the board into a PCI Express slot when the system is powered off. Once inserted, the PC can be safely powered on.

Using the evaluation board outside of a PC chassis supply requires the factory-supplied wall supply module. Use of other supplies is not suggested.

Figure 2. Power Distribution Scheme (See Appendix A, Sheet 2, Figure 11- Voltage Regulators)



Programming/FPGA Configuration

The ECP5 Versa Development Board has a built-in download controller for programming the ECP5 FPGA. The built-in module consists of a USB Type-B connector and a USB UART device. To use the built-in download cable, simply connect a standard USB cable (a USB-B to USB-A cable is included with the ECP5 Versa Development Kit) from J2 to your PC (with Diamond programming software installed). The USB hub on the PC will detect the addition of the USB function, making the built-in cable available for use with the Diamond programming software. The USB cable is connected in parallel to J3.

Alternate Programmer Download Interface

J3 is a 10 pin JTAG connector that is provided for use with an external Lattice download cable (available separately). A USB download cable can be attached to the board using J3 to interface with the FPGA (U1).

Note: Resistors R38, R33, R32 and R36 need to be removed for programming with J3.

The same interface can be used to access the ispClock 5406D clock device (U13) by reconfiguring the jumpers on J50 (See Appendix A, Sheet 3, Figure 12 - Programming). U13 is factory-programmed for use with the reference designs and should only be altered for customized designs.

Table 2. JTAG Connector Pinout (J3) (See Appendix A, Sheet 3, Figure 12 - Programming)

Pin	Function
1	PWR
2	TDO
3	TDI
4	PROGRAMn
5	N/C
6	TMS
7	GND
8	TCK
9	DONE
10	INITn

Diamond Programmer Requirements

Note: This board includes the built-in download module and only requires the USB cable included with the board. After initial board setup, use the following procedure to program the board. Instructions assume that Diamond Programmer software has been installed on a local PC.

Requirements:

- PC with Diamond Programmer 3.5.1 (or later) programming software, installed with appropriate drivers (USB driver for USB cable).

Note: An option to install these drivers is included as part of the Diamond Programmer setup.

Setting the Configuration Mode

The ECP5 device on the ECP5 Versa Development Board supports a variety of configuration modes, including 1149.1 JTAG and Master SPI. Refer to TN1260, [ECP5 sysCONFIG Usage Guide](#). On the PCB version Rev B, use the CFG Setting Dip Switch SW4 described in Table 3.

Table 3. CFG[2:0] Selection – Rev B

Configuration Mode	CFG[2:0]	SW4.3	SW4.2	SW4.1
1149.1 JTAG only	000	Down	Down	Down
Slave SPI	001	Down	Down	Up
Master SPI	010	Down	Up	Down
SCM (Slave_Serial)	101	Up	Down	Up
SCM (Slave_Parallel)	111	Up	Up	Up

Board Programming

Configuration Status Indicators

(See Appendix A, Sheet 3, Figure 12 - Programming)

Figure 3. ECP5 Status LEDs and Push-button Controls



The LEDs indicate the configuration status of the ECP5 FPGA.

- **D17 (red)** illuminated indicates that programming was aborted or reinitialized, driving the INITN output low.
- **D20 (green)** illuminated indicates the successful completion of configuration by releasing the open collector DONE output pin.
- **D19 (red)** illuminated indicates that PROGRAMN is low.
- **D18 (red)** illuminated indicates that GSRN is low.

PROGRAMN and GSRN

These push-button switches assert/de-assert the logic levels on PROGRAMN (SW2) and GSRN (SW1). Depressing the button drives a logic level “0” to the device.

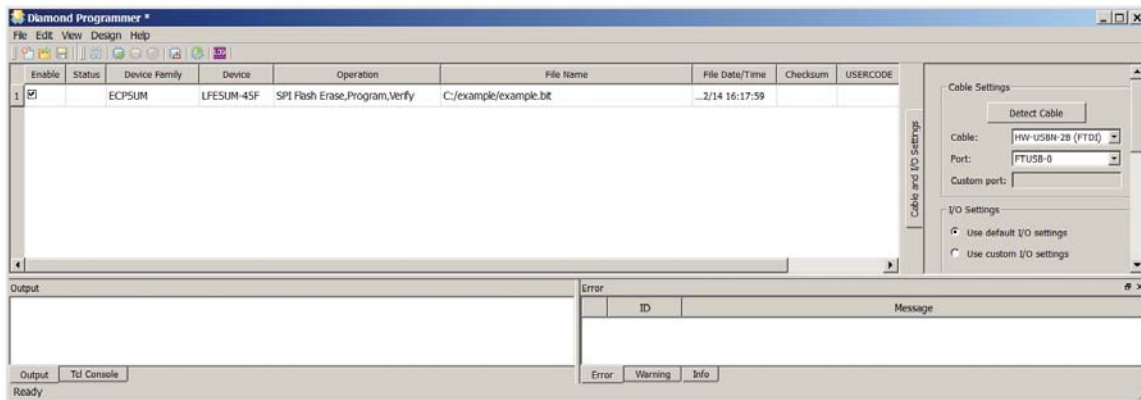
Programming Serial SPI Flash Memory

A serial SPI (16-pin TSSOP, 128M) Flash memory device (U52) is on-board for non-volatile configuration memory storage. A Micron N25Q128A device is populated on-board.

The Serial SPI Flash memory device can be configured easily via the ECP5 JTAG port. This mode enables the FPGA to be programmed at power-up or assertion of PROGRAMN with a bitstream stored in the memory device.

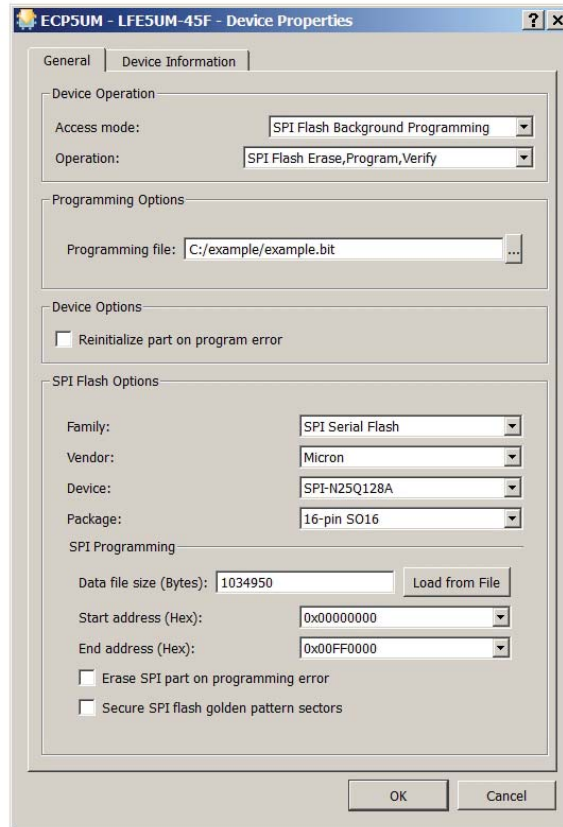
1. Connect the ECP5 Versa Development Board.
2. Scan the board or select the **LFE5UM-45F** device in the ECP5UM device family.
3. From the Edit pull down menu select **Device Properties**. Set the Access mode to **SPI Flash Background Programming** and Operation to **SPI Flash Erase, Program, Verify**.

Figure 4. Diamond Programmer Main Screen



4. Under the SPI Flash Options, select Family to **SPI Serial Flash**, Vendor to **Micron**, Device to **SPI-N25Q128A**, Package to **16-pin SO16**.

Figure 5. Device Properties Dialog Box



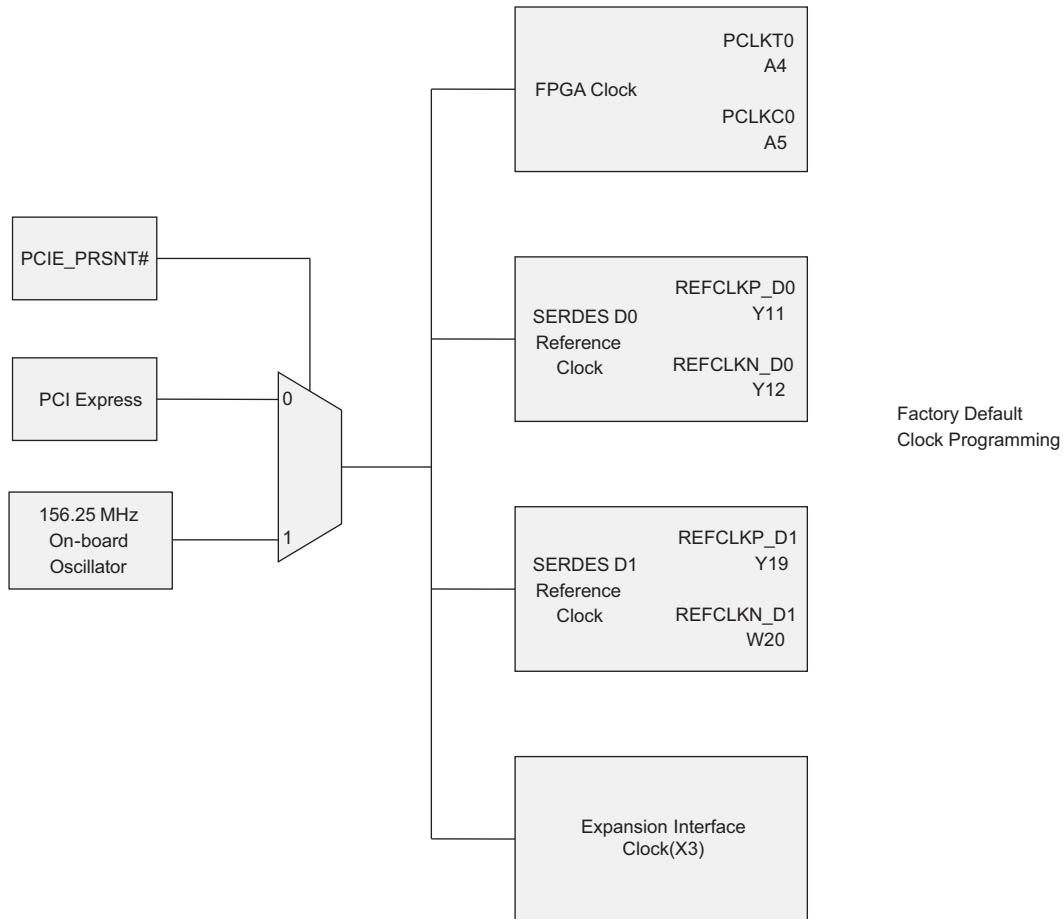
5. Click **OK** in the Device Properties dialog box. You will return to the main configuration screen.
6. Set J50 jumper to ECP5 programming (See Appendix A, sheet 3 "Programming")
7. From the main programming window, select **Program** from the top toolbar. This begins the SPI Serial Flash programming. Note that the SPI Flash Background Programming operation is only possible when the ECP5 device is either erased or the active design has the MASTER_SPI_PORT mode enabled. For more details see TN1260, [ECP5 sysCONFIG Usage Guide](#).

On-Board Clock Capabilities

(See Appendix A, Sheet 9, Figure 18 - Reference Clock Generator)

The ECP5 Versa Development Board allows for several clock source options. Some of these options are controlled via the ispClock5406D programmable clock manager device. The ispClock5406D enables the reference clock from the PCI Express interface to provide a reference clock to the SERDES. This is true only when the board is in a PCI Express host socket. When the board is not in a PCI Express host socket, the clock will be supplied by a 156.25 MHz clock on-board oscillator. Both clock inputs can be fanned out to the dedicated SERDES reference inputs, FPGA inputs, and to the expansion connectors. The factory default programming only connects the SERDES reference clock inputs. Factory-defined demonstration designs will control and manage the clock.

Figure 6. Clock Controller Scheme

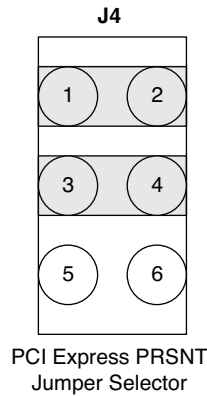


General Purpose Clock Source

An on-board 100 MHz LVDS oscillator is provided for general purpose use. This clock source is connected to differential inputs P3 and P4 and must be used as LVDS inputs to the FPGA. This pin pair also provides optimal interface to the FPGA PLL for customized use.

The PCI Express add-in card specification requires add-in boards to include capabilities to tell the host of its presence. The ECP5 Versa Development Board allows this optional connection via a board jumper. Using the board with a PCI Express host requires the setting shown in Figure 7 below.

Figure 7. PCI Express PRSNT Control Connection



SERDES

The ECP5 Dual Channel Unit (DCU) SERDES FPGA is utilized on the board for several purposes. DCU0, Channel 0 is provisioned to provide a single, full-duplex PCI Express channel. The high-speed signals are connected to the PCI Express edge connection. DCU0, Channel 1 is connected to the SMA connectors for external electrical demonstrations.

Table 4. PCI Express Channel Interconnections

Signal Name	SERDES Port	FPGA Ball Number
PETp0	HDRXP0_D0CH0	Y5
PETn0	HDRXN0_D0CH0	Y6
PERp0	HDTXP0_D0CH0	W4
PERn0	HDTXN0_D0CH0	W5

Table 5. SMA Test Interconnections

Connector	SERDES Port	FPGA Ball Number
J5	HDRXP0_D0CH1	Y7
J6	HDRXN0_D0CH1	Y8
J7	HDTXP0_D0CH1	W8
J8	HDTXN0_D0CH1	W9

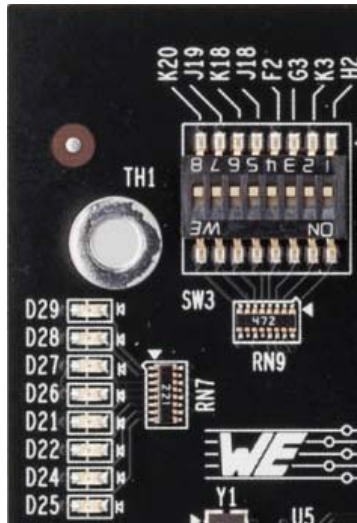
FPGA Test Pins

(See Appendix A, Sheet 8, Figure 17 - LEDs and Switches)

General Purpose DIP Switches

General purpose FPGA pins are available for user applications. FPGA pins are connected to switch SW3, a SPST slide-actuated DIP switch. The switches are connected to logic level 0 when moved to the ON position. Switch position 1 is indicated with an arrow. *Inputs 1-4 are within a 1.5 V bank and inputs 5-8 are within a 2.5 V bank.* The user must program inputs 1-4 to be the LVC MOS15 type and inputs 5-8 to be the LVC MOS25 type in the design. Figure 9 shows the switches. Note the silk marking associated with SW3-7 is incorrect in revision B, SW3-7 is mapped to K19, per Table 6.

Figure 8. ECP5 Versa Development Board LEDs and Switches



The designated pins are connected according to Table 6.

Table 6. FPGA Ball to DIP Switch Position

FPGA Ball Number	SW3 DIP Switch Position
H2	1
K3	2
G3	3
F2	4
J18	5
K18	6
K19	7
K20	8

General Purpose LEDs

(See Appendix A, Sheet 8, Figure 17 - LEDs and Switches)

The LEDs provided on the ECP5 Versa Development Board are connected to general purpose FPGA I/Os. These LEDs provide status for user designs and must be included in the design. The LEDs illuminate when the FPGA output is driven LOW. Table 7 shows the LED and associated FPGA pins. These pins are within an I/O bank connected to 2.5 V and the user should program these to be LVCMOS25 type outputs in the design.

Table 7. LED Definitions

LED Designator	FPGA Ball Number	LED Color
D25	E16	Yellow
D24	D17	Yellow
D22	D18	Green
D21	E18	Green
D26	F17	Red
D27	F18	Red
D28	E17	Red
D29	F16	Red

Alpha-numeric LED Display

(See Appendix A, Sheet 8, Figure 17 - LEDs and Switches)

A 14-segment alpha-numeric display is provided on the board (D23). These LED segments are connected to general-purpose FPGA I/Os. The LEDs must be included in the FPGA design. The LEDs illuminate when the FPGA output is driven LOW. Table 8 shows the LED and associated FPGA pins. These pins are within an I/O bank connected to 2.5 V and the user should program these to be LVCMOS25 outputs in the design.

Figure 9. 14-Segment Display

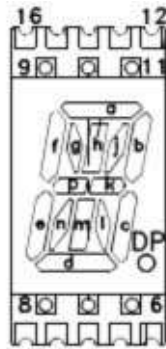


Table 8. Alpha-numeric LED Definitions

Display	FPGA Ball Number	Display	FPGA Ball Number
A	M20	J	N18
B	L18	K	P17
C	M19	L	N17
D	L16	M	P16
E	L17	N	R16
F	M18	P	R17
G	N16	DP	U1
H	M17		

DDR3 Memory Device

(See Appendix A, Sheet 7, Figure 16 - DDR3 Memory)

- The ECP5 Versa Development Board is equipped with an SDRAM memory device (1.5 V, 64 Mb/x16, 96-ball FBGA, 933 MHz, DDR3-1866) such as the Micron MT41K64M16TW-107:J device.
- The DDR3 memory includes a 16-bit wide memory controller interface.
- The board includes termination of data, address and command signals. It includes all power and external components needed to demonstrate the memory controller of the ECP5 device.
- A 100 MHz on-board clock oscillator is available to provide a DDR3 reference clock.

Table 9. DDR3 Memory Controller Interconnections

DDR3 Signal	FPGA Ball Number
DQ0	L5
DQ1	F1
DQ2	K4
DQ3	G1
DQ4	L4
DQ5	H1
DQ6	G2
DQ7	J3
DQ8	D1
DQ9	C1
DQ10	E2
DQ11	C2
DQ12	F3
DQ13	A2
DQ14	E1
DQ15	B1
DQS0	K2
DQS0#	J1
DQS1	H4
DQS1#	G5
CE0	N2
RAS#	P1
CLKP	P3
CLKN	P4
RST#	N4

DDR3 Signal	FPGA Ball Number
A0	P2
A1	C4
A2	E5
A3	F5
A4	B3
A5	F4
A6	B5
A7	E4
A8	C5
A9	E3
A10	D5
A11	B4
A12	C3
K_0	M4
K_0#	N5
CAS#	L1
BA0	P5
BA1	N3
BA2	M3
ODT	L2
CS0#	K1
WE#	M1
VREF	K5
DM0	J4
DM1	H5

Ethernet Interfaces

(See Appendix A, sheets 5 and 6 "10/100/1000-T PHY#x/RJ45")

Two Marvell 88E1512 Gigabit Ethernet transceiver devices (U14 and U15) are included on the board. These physical layer devices support 1000BASE-T, 100BASE-TX, and 10BASE-T applications via a standard media interface to a dual RJ45 connection. The RJ45 connection includes network magnetics providing the proper signal conditioning, electro-magnetic interference suppression and signal isolation. Each connector includes two LEDs which are controlled by the 88E1512 devices. Detailed descriptions are available in the Marvell device data sheet.

Table 10. PHY Status Indicators

LED	Status Description
RJ45 (Yellow)	Data RX/TX
RJ45 (Green/Orange)	Link State

Each Marvell 88E1512 device communicates via a RGMII interface to the ECP5 device.

Table 11. FPGA GPIO to RGMII Interfaces

Signal	Phy1	Phy2
CLK125	L19	J20
CLK125Pll	U16	C18
Config	T17	G20
Resetrn	U17	F20
TXCLK	P19	C20
TX_D0	N19	J17
TX_D1	N20	J16
TX_D2	P18	D19
TX_D3	P20	D20
TXCTRL	R20	E19
RXCLK	L20	J19
RX_D0	T20	G18
RX_D1	U20	G16
RX_D2	T19	H18
RX_D3	R18	H17
RXCTRL	U19	F19
MDIO	U18	H20
MDC	T18	G19

Table 12. Expansion Connections


X3 Expansion Connector		
Pin	Signal	FPGA Ball Number
1	GND	—
2	NC	—
3	2V5	—
4	IO29	B19
5	IO30	B12
6	IO31	B9
7	IO32	E6
8	IO33	D6
9	IO34	E7
10	IO35	D7
11	IO36	B11
12	IO37	B6
13	IO38	E9
14	IO39	D9
15	IO40	B8
16	IO41	C8
17	IO42	D8
18	IO43	E8
19	IO44	C7
20	IO45	C6
21	5VIN	—
22	GND	—
23	2V5	—
24	GND	—
25	3V3	—
26	GND	—
27	3V3	—
28	GND	—
29	OSC	—
30	GND	—
31	CLKIN	A10
32	GND	—
33	CLKOUT	E11
34	GND	—
35	3V3	—
36	GND	—
37	3V3	—
38	GND	—
39	3V3	—
40	GND	—

X4 Expansion Connector		
Pin	Signal	FPGA Ball Number
1	RESOUT#	A8
2	GND	—
3	IO0	A12
4	IO1	A13
5	IO2	B13
6	IO3	C13
7	IO4	D13
8	IO5	E13
9	IO6	A14
10	IO7	C14
11	IO8	D14
12	IO9	E14
13	IO10	D11
14	IO11	C10
15	IO12	A9
16	IO13	B10
17	IO14	D12
18	IO15	E12
19	GND	—
20	3V3	—
21	IO16	B15
22	GND	—
23	IO17	C15
24	GND	—
25	IO18	D15
26	GND	—
27	IO19	E15
28	IO20	A16
29	IO21	B16
30	GND	—
31	IO22	C16
32	IO23	D16
33	IO24	B17
34	GND	—
35	IO25	C17
36	IO26	A17
37	IO27	B18
38	CARDSEL#	A7
39	IO28	A18
40	GND	—

References

- DS1044, [ECP5 Family Data Sheet](#)
- UG98, [PCI Express Demos for the ECP5 Versa Development Board](#)
- UG97, [DDR3 Demo for the ECP5 Versa Development Board](#)
- UG93, [SERDES Eye Demo for the ECP5 Versa Development Board](#)
- UG92, [SEU \(Single Event Upset\) Demo for the ECP5 Versa Development Board](#)

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ECP5 Versa Development Board	LFE5UM-45F-VERSA-EVN	

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
November 2015	2.1	Updated Introduction section. Indicated Dual RJ45 Ethernet ports and corrected USB Programming callout in Figure 1, ECP5 Versa Development Board, Top Side.
		Updated General Purpose LEDs section. Revised FPGA ball numbers in Table 7, LED Definitions.
		Updated Appendix A. Schematics section. Revised LEDs signal map in Figure 17, LEDs and Switches.
		Updated Appendix B. Bill of Materials section. Revised description of item 111.
		Updated Setting the Configuration Mode section in Appendix C. Changed Figure 20, CFG[2:0] Setting Resistor Field – Revision A.
August 2015	2.0	Updated to support Rev B of development board.
July 2015	1.1	Added Setting the Configuration Mode section.
		Updated Technical Support Assistance section.
		Added ECP5 Versa Development Board Bill of Materials section.
March 2015	1.0	Initial release.

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Appendix A. Schematics

Figure 10. Board Block Design

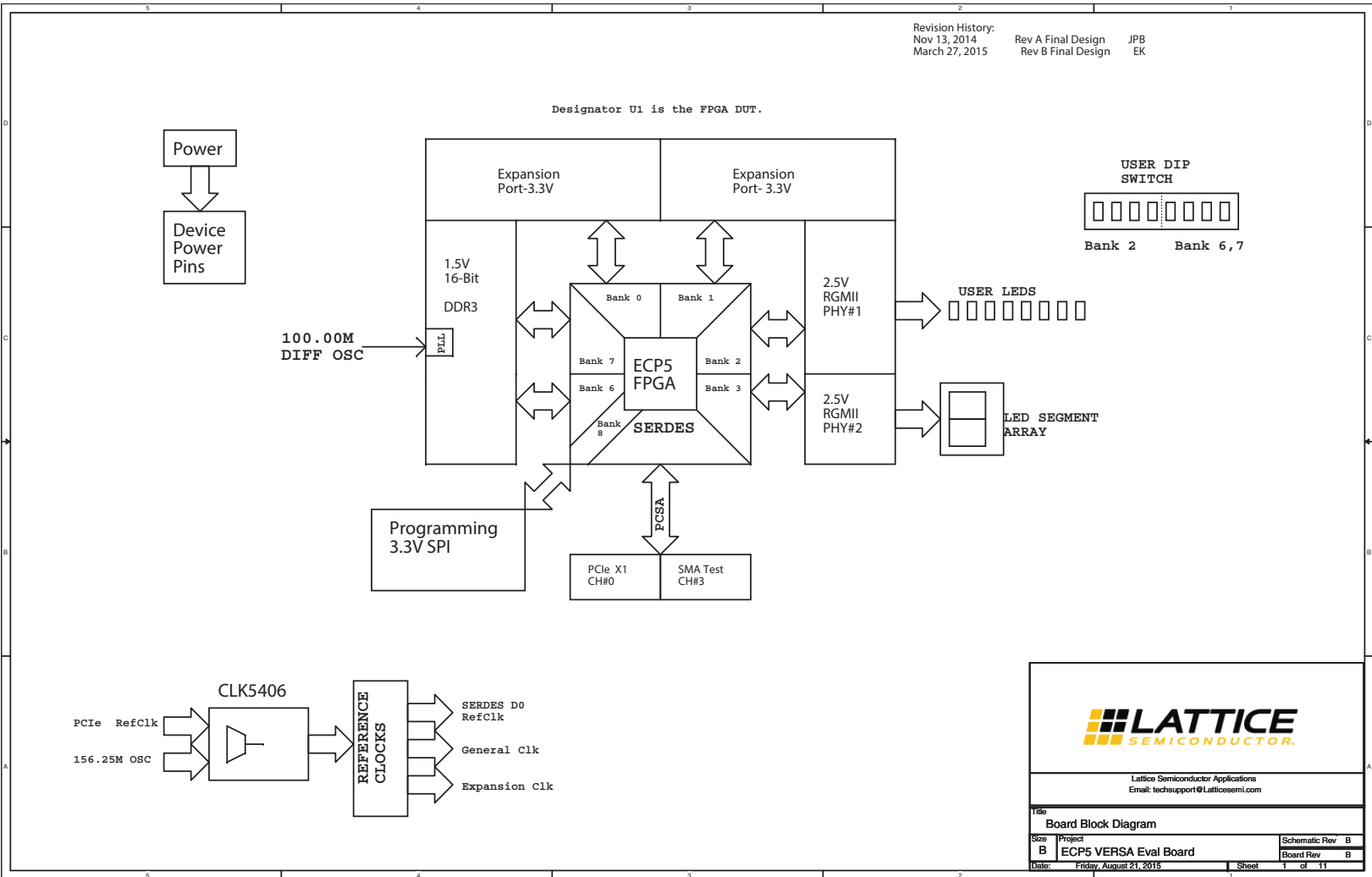
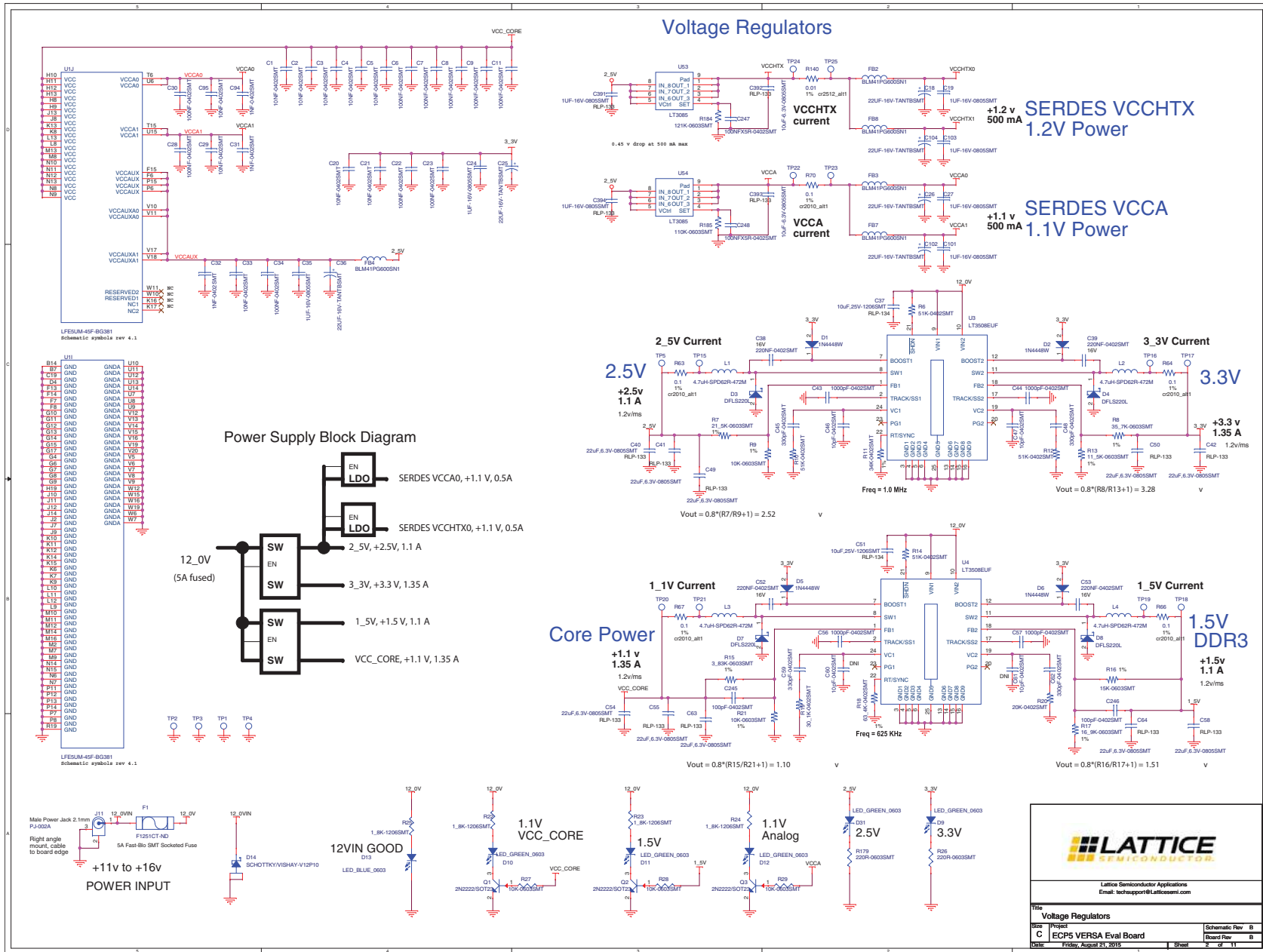


Figure 11. Voltage Regulators



LATTICE SEMICONDUCTOR

Lattice Semiconductor Applications
Email: techsupport@latticesemi.com

Title: Voltage Regulators			
Size: Project	Sheet: 1	Schematic Rev: B	Board Rev: B
C ECP5 VERSA Eval Board			
Date: 1/26/2011	Author: J. Smith	Sheet: 1	of 11

Figure 12. Programming

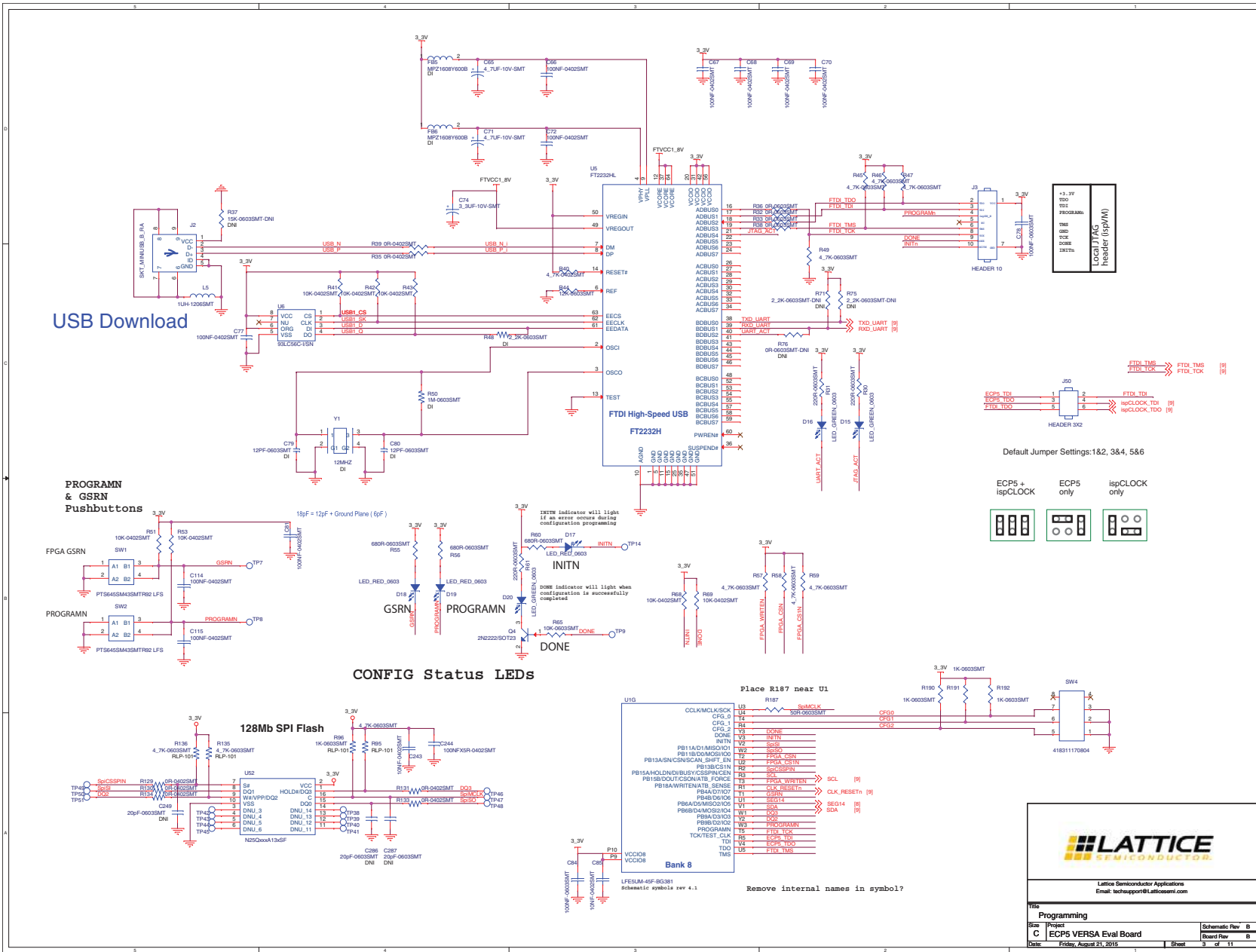


Figure 13. SERDES

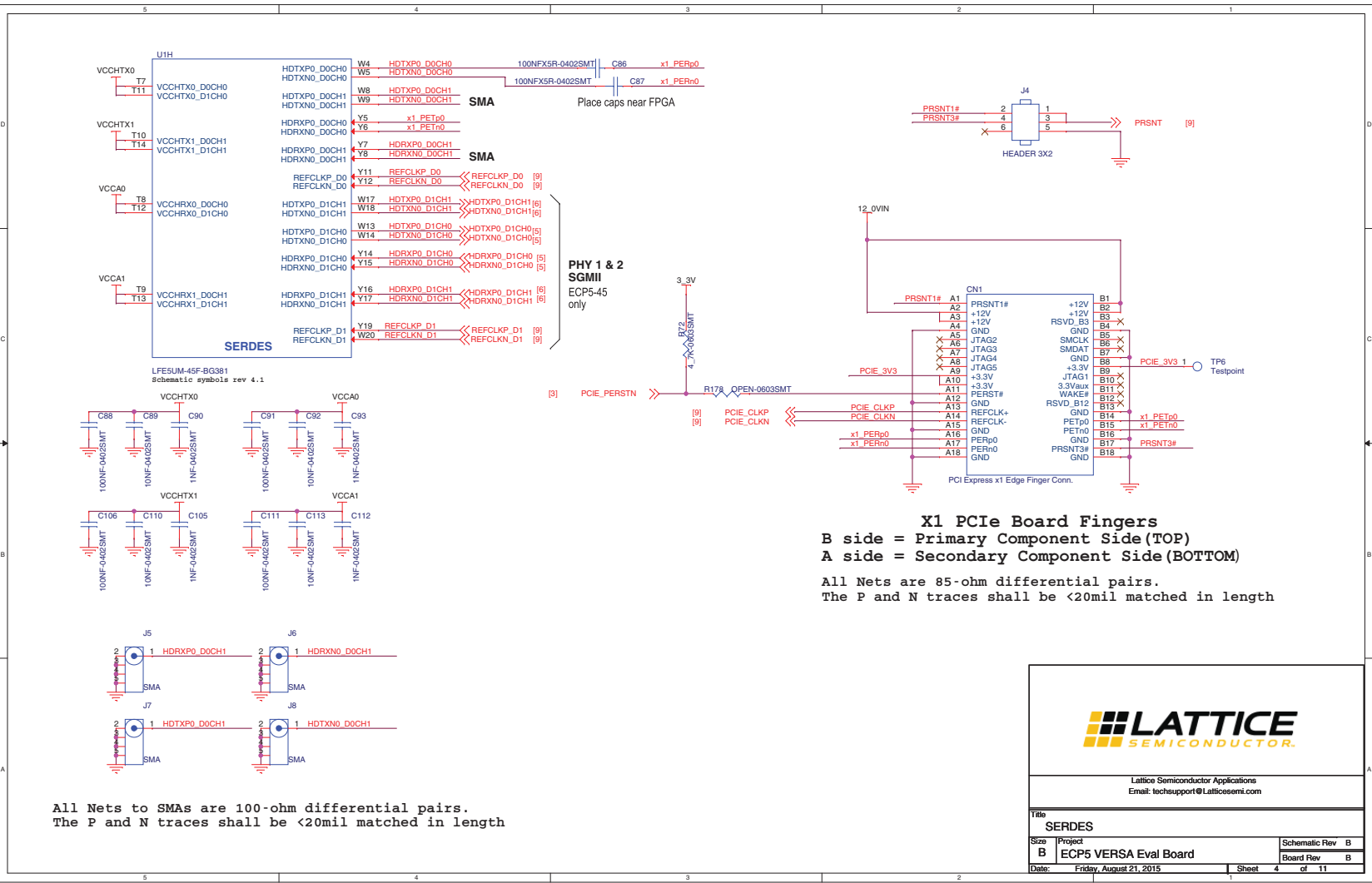


Figure 14. 10/100/1000-T PHY #1/RJ45

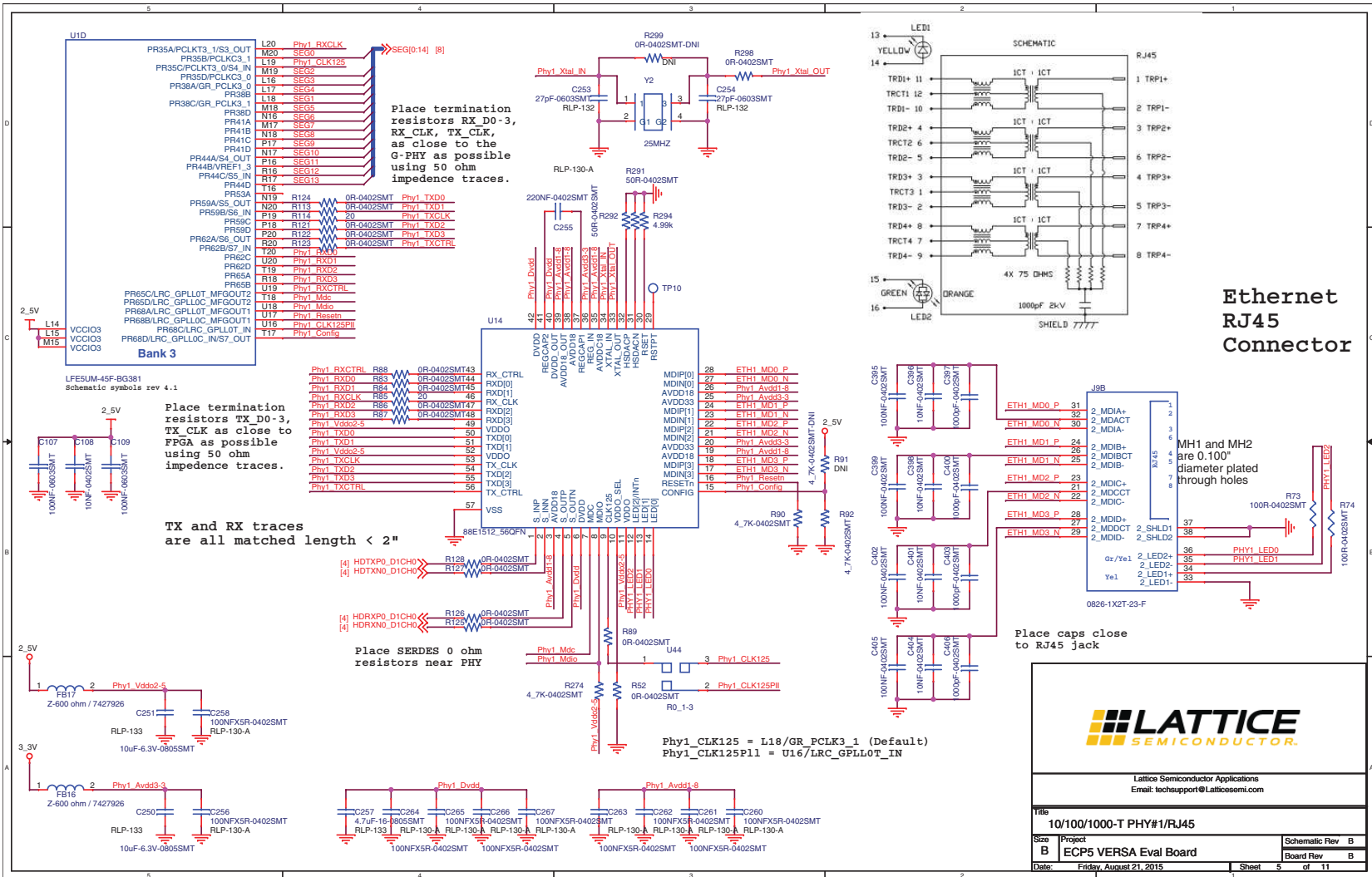


Figure 15. 10/100/1000-T PHY #2/RJ45

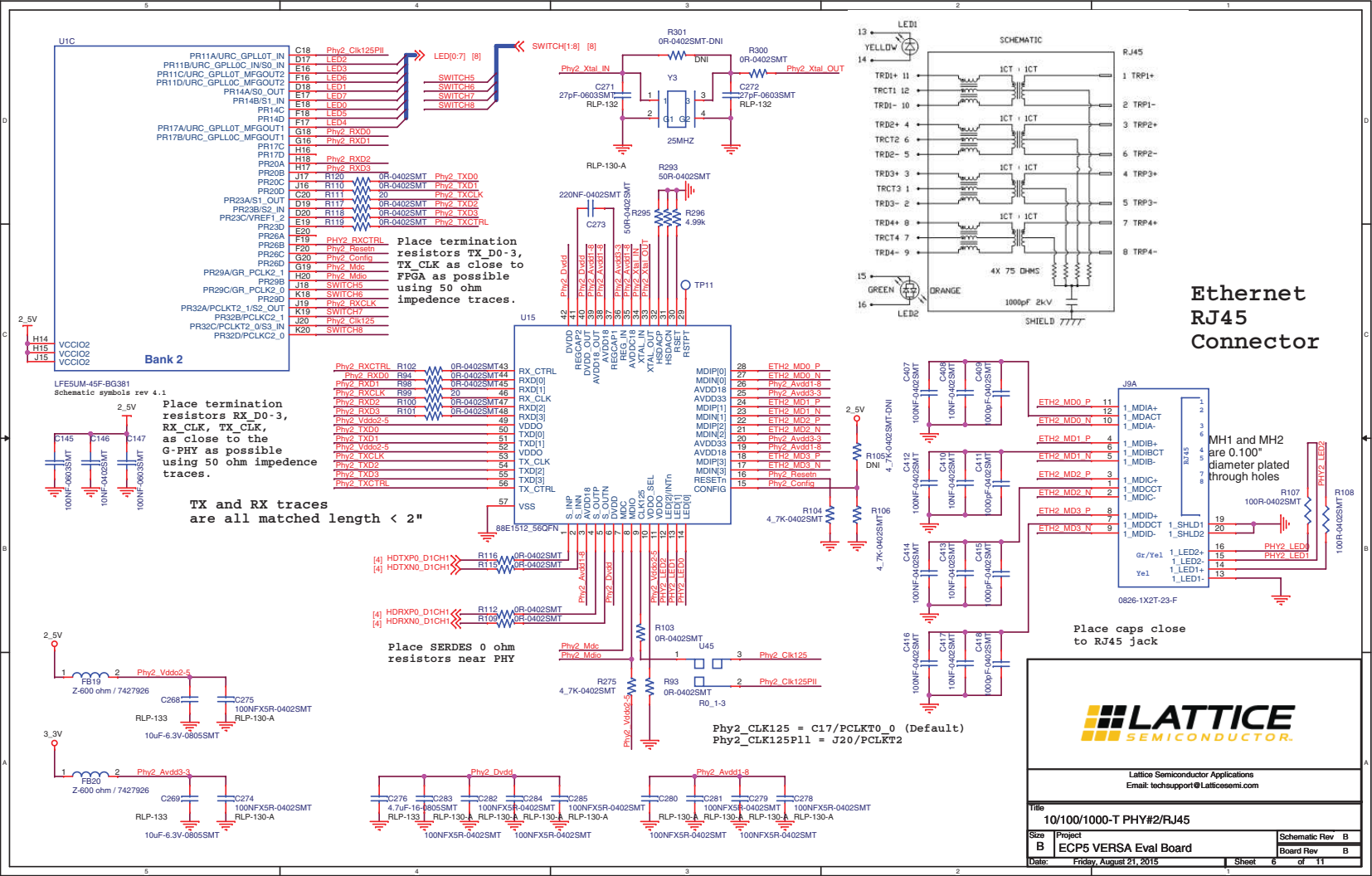


Figure 16. DDR3 Memory

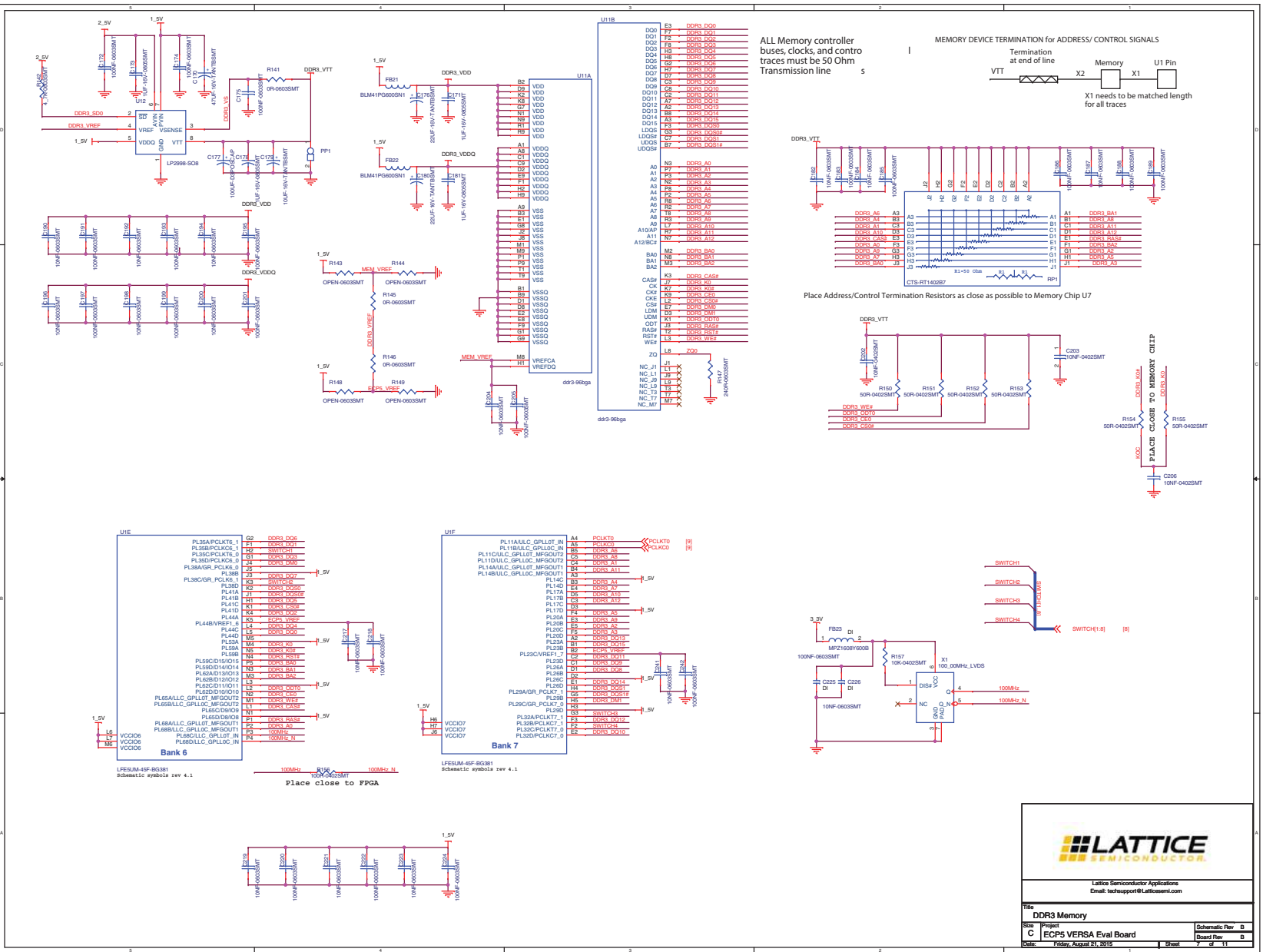


Figure 17. LEDs and Switches

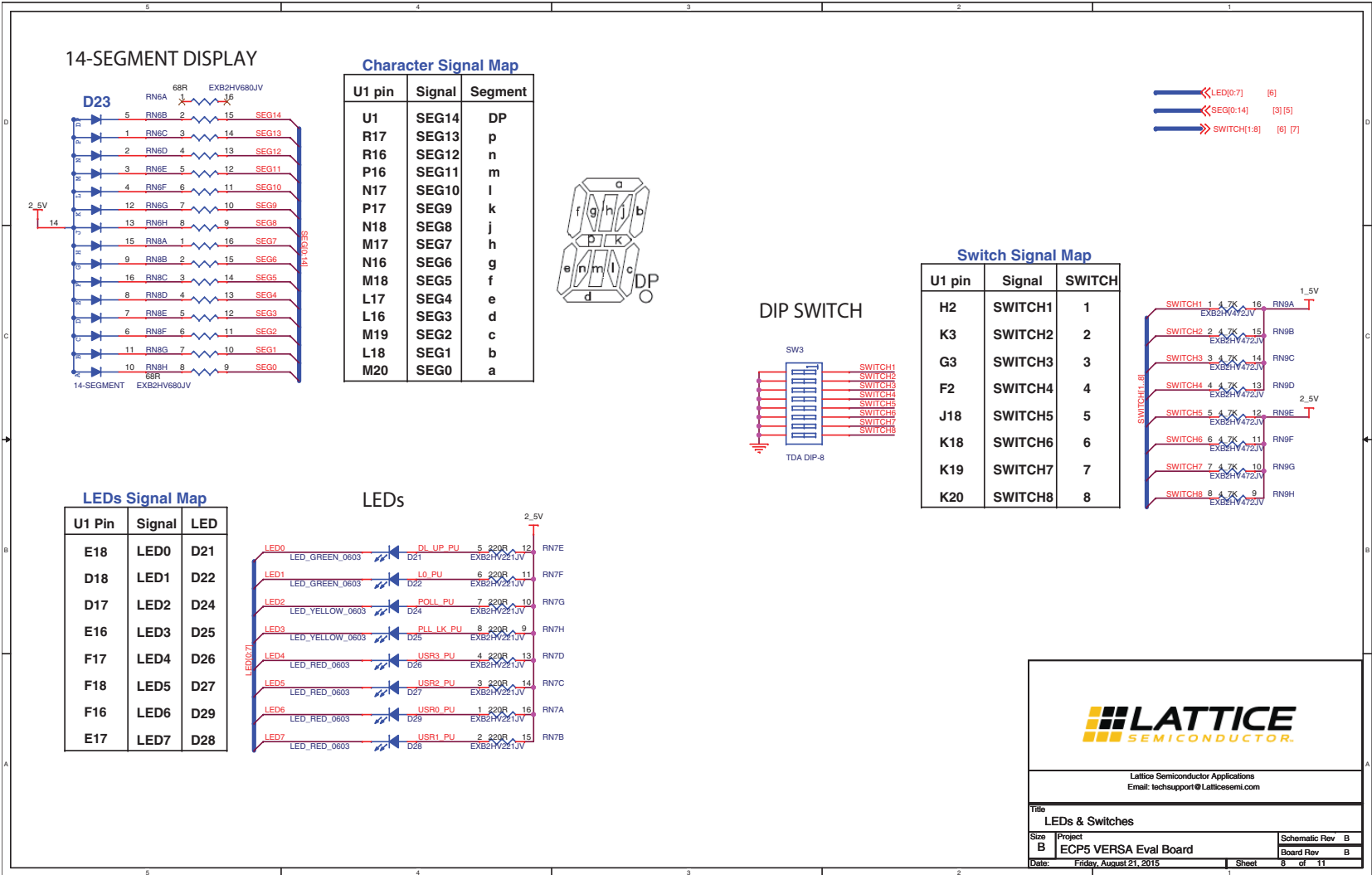


Figure 18. Reference Clock Generator

