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MPC5534 Microcontroller Data Sheet

by: Automotive and Industrial Solutions Group

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5534 microcontroller device. For functional characteristics, refer to the *MPC5534 Microcontroller Reference Manual*.

1 Overview

The MPC5534 microcontroller (MCU) is a member of the MPC5500 family of microcontrollers built on the Power Architecture® embedded technology. This family of parts has many new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement over the MPC500 family.

The host processor core of this device complies with the Power Architecture embedded category that is 100% user-mode compatible (including floating point library) with the original PowerPC instruction set. The embedded architecture enhancements improve the performance in embedded applications. The core also has additional instructions, including digital signal processing (DSP) instructions, beyond the original PowerPC instruction set.

Contents

1	Overview	1
2	Ordering Information	3
3	Electrical Characteristics	4
3.1	Maximum Ratings	4
3.2	Thermal Characteristics	5
3.3	Package	8
3.4	EMI Characteristics	8
3.5	ESD Characteristics	9
3.6	VRC and POR Electrical Specifications	9
3.7	Power-Up/Down Sequencing	10
3.8	DC Electrical Specifications	14
3.9	Oscillator and FMPLL Electrical Characteristics	20
3.10	eQADC Electrical Characteristics	22
3.11	H7Fb Flash Memory Electrical Characteristics	23
3.12	AC Specifications	24
3.13	AC Timing	26
4	Mechanicals	46
4.1	MPC5534 208 MAP BGA Pinout	46
4.2	MPC5534 324 PBGA Pinouts	47
4.3	MPC5534 208-Pin Package Dimensions	48
4.4	MPC5534 324-Pin Package Dimensions	50
5	Revision History for the MPC5534 Data Sheet	52
5.1	Changes Between Revisions 5.0 and 6.0	52
5.3	Changes Between Revisions 3.0 and 4.0	53

Overview

The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The host processor core of the MPC5534 also includes an instruction set enhancement allowing variable length encoding (VLE). This allows optional encoding of mixed 16- and 32-bit instructions. With this enhancement, it is possible to significantly reduce the code size footprint.

The MPC5534 has a single-level memory hierarchy consisting of 64-kilobytes (KB) on-chip SRAM and one megabyte (MB) of internal flash memory. Both the SRAM and the flash memory can hold instructions and data. The external bus interface (EBI) supports most standard memories used with the MPC5xx family.

The MPC5534 does not support arbitration with other masters on the external bus. The MPC5534 must be the only master on the external bus, or act as a slave-only device.

The complex input/output timer functions of the MPC5534 are performed by an enhanced time processor unit (eTPU) engine. The eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing: 24-bit timers, double-action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU is programmed using a high-level programming language.

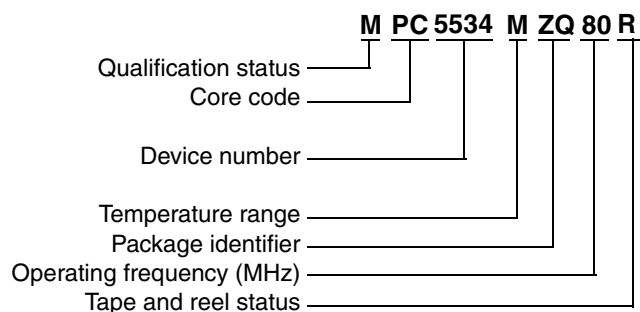
The less complex timer functions of the MPC5534 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs).

The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC) with a 5 V conversion range. The 324 package has 40-channels; the 208 package has 34 channels.

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer sub-block (IMUX) provides multiplexing of eQADC trigger sources and external interrupt signal multiplexing.

2 Ordering Information



Temperature Range
M = -40° C to 125° C

Package Identifier
VF = 208MAPBGA SnPb
VM = 208MAPBGA Pb-free
ZQ = 324PBGA SnPb
VZ = 324PBGA Pb-free

Operating Frequency
40 = 40 MHz
66 = 66 MHz
80 = 80 MHz

Tape and Reel Status
R = Tape and reel
(blank) = Trays

Qualification Status

P = Pre qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to [Table 1](#).

Figure 1. MPC5500 Family Part Number Example

Unless noted in this data sheet, all specifications apply from T_L to T_H .

Table 1. Orderable Part Numbers

Freescale Part Number	Package Description	Speed (MHz)		Operating Temperature ¹	
		Nominal	Max. ² (f_{MAX})	Min. (T_L)	Max. (T_H)
MPC5534MVZ80	MPC5534 324 package Lead-free (PbFree)	80	82	-40° C	125° C
MPC5534MVZ66		66	68		
MPC5534MVZ40		40	42		
MPC5534MVM80	MPC5534 208 package Lead-free (PbFree)	80	82	-40° C	125° C
MPC5534MVM66		66	68		
MPC5534MVM40		40	42		
MPC5534MZQ80	MPC5534 324 package Leaded (SnPb)	80	82	-40° C	125° C
MPC5534MZQ66		66	68		
MPC5534MZQ40		40	42		
MPC5534MVF80	MPC5534 208 package Leaded (SnPb)	80	82	-40° C	125° C
MPC5534MVF66		66	68		
MPC5534MVF40		40	42		

¹ The lowest ambient operating temperature is referenced by T_L ; the highest ambient operating temperature is referenced by T_H .

² Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 68 MHz parts allow for 66 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings ¹

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage ²	V_{DD}	-0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	-0.3	6.5	V
4	Flash read voltage	V_{FLASH}	-0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	-0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	-0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	-0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	-0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	-0.3	5.5	V
10	I/O supply voltage (fast I/O pads) ³	V_{DDE}	-0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) ³	V_{DDEH}	-0.3	6.5	V
12	DC input voltage ⁴ V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	-1.0 ⁵ -1.0 ⁵	6.5 ⁶ 4.6 ⁷	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	-0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} - V_{SSA}$	-0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} - V_{DDA}$	$-V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} - V_{RL}$	-0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} - V_{DDA}$	-5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} - V_{SSA}$	-0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} - V_{DDA}$	$-V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	-0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	-0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	-0.1	0.1	V
24	Maximum DC digital input current ⁸ (per pin, applies to all digital pins) ⁴	I_{MAXD}	-2	2	mA
25	Maximum DC analog input current ⁹ (per pin, applies to all analog pins)	I_{MAXA}	-3	3	mA
26	Maximum operating temperature range ¹⁰ Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	-55.0	150.0	°C

Table 2. Absolute Maximum Ratings ¹ (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
28	Maximum solder temperature ¹¹ Lead free (Pb-free) Leaded (SnPb)	T _{SDR}	— —	260.0 245.0	°C
29	Moisture sensitivity level ¹²	MSL	—	3	

¹ Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

² 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

³ All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

⁴ AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

⁵ Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on SINB during the internal power-on reset (POR) state.

⁶ Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

⁷ Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

⁸ Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

⁹ Total injection current for all analog input pins must not exceed 15 mA.

¹⁰ Lifetime operation at these specification limits is not guaranteed.

¹¹ Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

¹² Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

Table 3. MPC5534 Thermal Characteristic

Spec	MPC5534 Thermal Characteristic	Symbol	Package		Unit
			208 MAPBGA	324 PBGA	
1	Junction to ambient ^{1,2} , natural convection (one-layer board)	R _{θJA}	42	34	°C/W
2	Junction to ambient ^{1,3} , natural convection (four-layer board 2s2p)	R _{θJA}	26	23	°C/W
3	Junction to ambient (@200 ft./min., one-layer board)	R _{θJMA}	34	28	°C/W
4	Junction to ambient (@200 ft./min., four-layer board 2s2p)	R _{θJMA}	22	20	°C/W
5	Junction to board ⁴ (four-layer board 2s2p)	R _{θJB}	15	15	°C/W
6	Junction to case ⁵	R _{θJC}	8	10	°C/W
7	Junction to package top ⁶ , natural convection	Ψ _{JT}	2	2	°C/W

¹ Junction temperature is a function of: on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other board components, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board in a horizontal position.

³ Per JEDEC JESD51-6 with the board in a horizontal position.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

⁶ The thermal characterization parameter indicates the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package ($^{\circ}\text{C}$)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than $0.02 \text{ W}/\text{cm}^2$

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature ($^{\circ}\text{C}$)

T_B = board temperature at the package perimeter ($^{\circ}\text{C/W}$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^{\circ}\text{C/W}$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C/W}$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^{\circ}\text{C/W}$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^{\circ}\text{C/W}$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package ($^{\circ}\text{C}$)

Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C/W}$)

P_D = power dissipation in the package (W)

Electrical Characteristics

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Rd.
San Jose, CA., 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at <http://www.jedec.org>.

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, "Thermal Modeling of a PBGA for Air-Cooled Applications," Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.3 Package

The MPC5534 is available in packaged form. Read the package options in [Section 2, "Ordering Information."](#) Refer to [Section 4, "Mechanicals,"](#) for pinouts and package drawings.

3.4 EMI (Electromagnetic Interference) Characteristics

Table 4. EMI Testing Specifications ¹

Spec	Characteristic	Minimum	Typical	Maximum	Unit
1	Scan range	0.15	—	1000	MHz
2	Operating frequency	—	—	f _{MAX}	MHz
3	V _{DD} operating voltages	—	1.5	—	V
4	V _{DDSYN} , V _{RC33} , V _{DD33} , V _{FLASH} , V _{DDE} operating voltages	—	3.3	—	V
5	V _{PP} , V _{DDEH} , V _{DDA} operating voltages	—	5.0	—	V
6	Maximum amplitude	—	—	14 ² 32 ³	dBuV
7	Operating temperature	—	—	25	°C

¹ EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03. Qualification testing was performed on the MPC5554 and applied to the MPC5500 family as generic EMI performance data.

² Measured with the single-chip EMI program.

³ Measured with the expanded EMI program.

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings ^{1, 2}

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of pulses per pin:			
Positive pulses (HBM)	—	1	—
Negative pulses (HBM)	—	1	—
Interval of pulses	—	1	second

¹ All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.'

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. V_{RC} and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR ¹	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR ¹	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	\overline{RESET} pin supply (V_{DDEH6}) POR ^{1,2}	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on ^{3, 4}	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation ^{5, 6}	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by V_{RCCTL} at T_j :	−40° C 25° C 150° C	I_{VRCCTL} ⁷	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V

Table 6. V_{RC} and POR Electrical Specifications (continued)

Spec	Characteristic	Symbol	Min.	Max.	Units
9	Absolute value of slew rate on power supply pins	—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$) 6, 7, 8, 9	BETA ¹⁰	– 40° C	35	—
			25° C	40	—
			150° C	50	500

¹ The internal POR signals are V_{POR15} , V_{POR33} , and V_{POR5} . On power up, assert \overline{RESET} before the internal POR negates. \overline{RESET} must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert \overline{RESET} before any power supplies fall outside the operating conditions and until the internal POR asserts.

² V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5} .

³ Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

⁴ It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

⁵ At peak current for device.

⁶ Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 μ F phase compensation capacitor to ground. V_{DD} must have a 20 μ F (nominal) bulk capacitor (greater than 4 μ F over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 μ F, two 0.1 μ F, and one 1 μ F capacitors around the package on the V_{DD} supply signals.

⁷ I_{VRCCTL} is measured at the following conditions: $V_{DD} = 1.35$ V, $V_{RC33} = 3.1$ V, $V_{VRCCTL} = 2.2$ V.

⁸ Refer to Table 1 for the maximum operating frequency.

⁹ Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.

¹⁰ BETA represents the worst-case external transistor. It is measured on a per-part basis and calculated as $(I_{DD} \div I_{VRCCTL})$.

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the \overline{RESET} power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, “Power-Up Sequence (VRC33 Grounded),” and Section 3.7.3, “Power-Down Sequence (VRC33 Grounded).”

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, “Input Value of Pins During POR Dependent on VDD33.”

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by V_{RC33} . If V_{RC33} lags V_{DDSYN} by more than 100 mV, the increase in current consumed can drop V_{DD} low enough to assert the 1.5 V POR again. Oscillations are possible when the 1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices (up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH} .

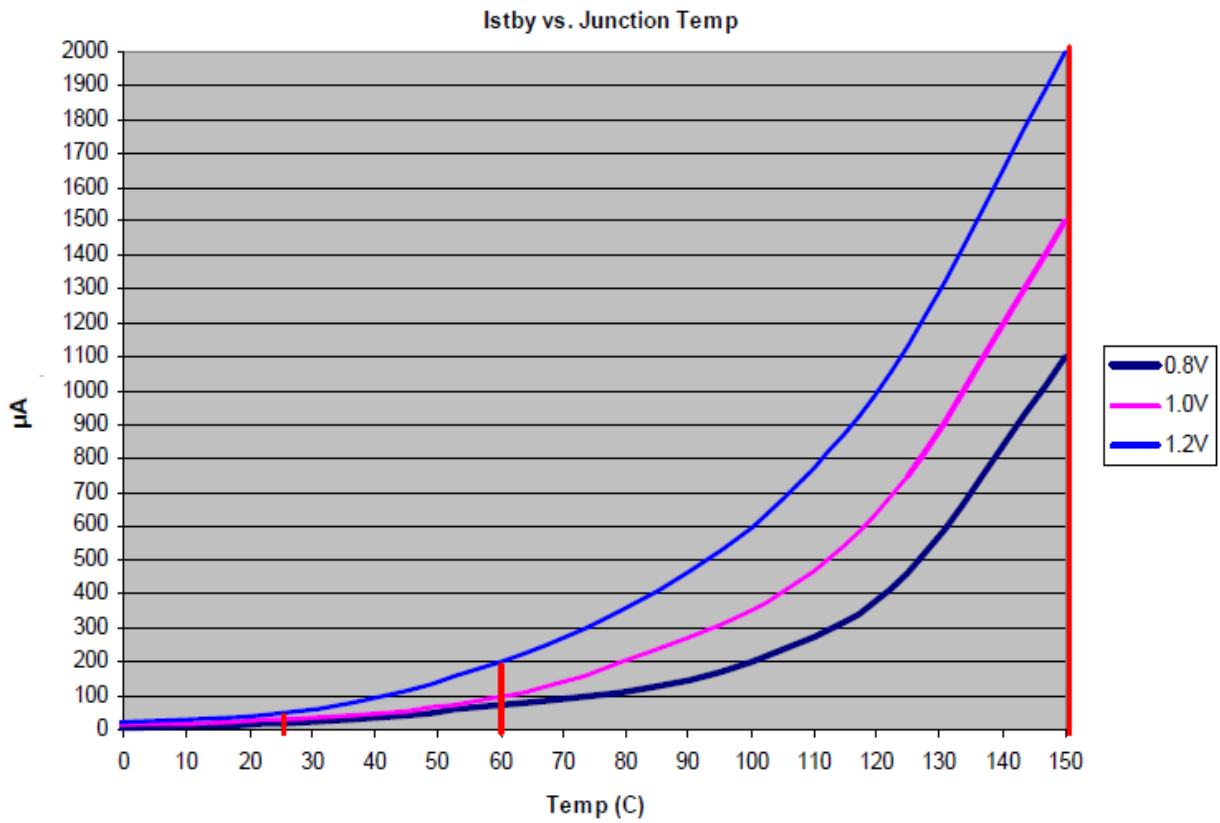
To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

During initial power ramp-up, when vstby is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until V_{DD} is applied. This current will not reoccur until V_{stby} is lowered below V_{stby} min specification.

Electrical Characteristics

Figure 2 shows an approximate interpolation of the I_{STBY} worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 2 are the actual I_{DD_STBY} specifications (27d) listed in Table 9

Figure 2. I_{STBY} Worst-case Specifications



3.7.1 Input Value of Pins During POR Dependent on V_{DD33}

When powering up the device, V_{DD33} must not lag the latest V_{DDSYN} or $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} or the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification applies during power up only. V_{DD33} has no lead or lag requirements when powering down.

3.7.2 Power-Up Sequence (V_{RC33} Grounded)

The 1.5 V V_{DD} power supply must rise to 1.35 V before the 3.3 V V_{DDSYN} power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

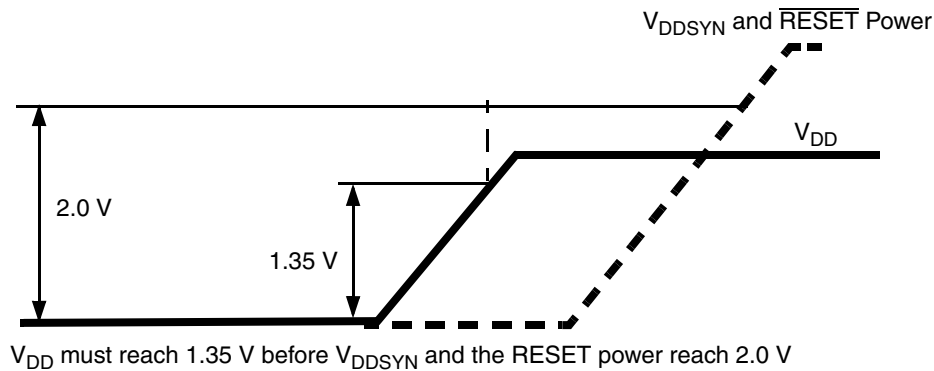


Figure 3. Power-Up Sequence (V_{RC33} Grounded)

3.7.3 Power-Down Sequence (V_{RC33} Grounded)

The only requirement for the power-down sequence with V_{RC33} grounded is if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

3.8 DC Electrical Specifications

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min	Max.	Unit
1	Core supply voltage (average DC RMS voltage)	V_{DD}	1.35	1.65	V
2	Input/output supply voltage (fast input/output) ¹	V_{DDE}	1.62	3.6	V
3	Input/output supply voltage (slow and medium input/output)	V_{DDEH}	3.0	5.25	V
4	3.3 V input/output buffer voltage	V_{DD33}	3.0	3.6	V
5	Voltage regulator control input voltage	V_{RC33}	3.0	3.6	V
6	Analog supply voltage ²	V_{DDA}	4.5	5.25	V
8	Flash programming voltage ³	V_{PP}	4.5	5.25	V
9	Flash read voltage	V_{FLASH}	3.0	3.6	V
10	SRAM standby voltage ⁴	V_{STBY}	0.8	1.2	V
11	Clock synthesizer operating voltage	V_{DDSYN}	3.0	3.6	V
12	Fast I/O input high voltage	V_{IH_F}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
13	Fast I/O input low voltage	V_{IL_F}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
14	Medium and slow I/O input high voltage	V_{IH_S}	$0.65 \times V_{DDEH}$	$V_{DDEH} + 0.3$	V
15	Medium and slow I/O input low voltage	V_{IL_S}	$V_{SS} - 0.3$	$0.35 \times V_{DDEH}$	V
16	Fast input hysteresis	V_{HYS_F}	$0.1 \times V_{DDE}$		V
17	Medium and slow I/O input hysteresis	V_{HYS_S}	$0.1 \times V_{DDEH}$		V
18	Analog input voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$	V
19	Fast output high voltage ($I_{OH_F} = -2.0$ mA)	V_{OH_F}	$0.8 \times V_{DDE}$	—	V
20	Slow and medium output high voltage $I_{OH_S} = -2.0$ mA $I_{OH_S} = -1.0$ mA	V_{OH_S}	$0.80 \times V_{DDEH}$ $0.85 \times V_{DDEH}$	—	V
21	Fast output low voltage ($I_{OL_F} = 2.0$ mA)	V_{OL_F}	—	$0.2 \times V_{DDE}$	V
22	Slow and medium output low voltage $I_{OL_S} = 2.0$ mA $I_{OL_S} = 1.0$ mA	V_{OL_S}	—	$0.20 \times V_{DDEH}$ $0.15 \times V_{DDEH}$	V
23	Load capacitance (fast I/O) ⁵ DSC (SIU_PCR[8:9]) = 0b00 = 0b01 = 0b10 = 0b11	C_L	— — — —	10 20 30 50	pF pF pF pF
24	Input capacitance (digital pins)	C_{IN}	—	7	pF
25	Input capacitance (analog pins)	C_{IN_A}	—	10	pF
26	Input capacitance: (Shared digital and analog pins AN[12]_MA[0]_SDS, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, and AN[15]_FCK)	C_{IN_M}	—	12	pF

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27a	Operating current 1.5 V supplies @ 82 MHz: ^{6, 7}				
	V_{DD} (including V_{DDF} max current) @ 1.65 V high use ^{8, 9, 10, 11, 12}	I_{DD}	—	250	mA
	V_{DD} (including V_{DDF} max current) @ 1.35 V high use ^{8, 9, 10, 11, 12}	I_{DD}	—	180	mA
27b	Operating current 1.5 V supplies @ 68 MHz: ^{13, 14}				
	V_{DD} (including V_{DDF} max current) @ 1.65 V high use ^{15, 16, 17}	I_{DD}	—	210	mA
	V_{DD} (including V_{DDF} max current) @ 1.35 V high use ^{15, 16, 17}	I_{DD}	—	160	mA
27c	Operating current 1.5 V supplies @ 42 MHz: ^{13, 14}				
	V_{DD} (including V_{DDF} max current) @ 1.65 V high use ^{15, 16, 17}	I_{DD}	—	130	mA
	V_{DD} (including V_{DDF} max current) @ 1.35 V high use ^{15, 16, 17}	I_{DD}	—	110	mA
27d	Refer to Figure 2 for an interpolation of this data. ¹⁸				
	I_{DD_STBY} @ 25° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	20	μA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	30	μA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	50	μA
	I_{DD_STBY} @ 60° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	70	μA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	100	μA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	200	μA
	I_{DD_STBY} @ 150° C (T_j)				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	1200	μA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	1500	μA
V_{STBY} @ 1.2 V	I_{DD_STBY}	—	2000	μA	
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} ¹⁹	I_{DD_33}	—	2 + (values derived from procedure of footnote ¹⁹)	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} ($V_{DDA0} + V_{DDA1}$)	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH} , V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA
30	Operating current V_{DDE} supplies: ²⁰				
	V_{DDEH1}	I_{DD1}	—	Refer to footnote ²⁰	mA
	V_{DDE2}	I_{DD2}	—		mA
	V_{DDE3}	I_{DD3}	—		mA
	V_{DDEH4}	I_{DD4}	—		mA
	V_{DDE5}	I_{DD5}	—		mA
	V_{DDEH6}	I_{DD6}	—		mA
	V_{DDE7}	I_{DD7}	—		mA
	V_{DDEH8}	I_{DD8}	—		mA
	V_{DDEH9}	I_{DD9}	—		mA

Electrical Characteristics

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
31	Fast I/O weak pullup current ²¹ 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V	I_{ACT_F}	10	110	μA
	20		130	μA	
	Fast I/O weak pulldown current ²¹ 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V		20	170	μA
	10		100	μA	
32	Slow and medium I/O weak pullup/down current ²¹ 3.0–3.6 V 4.5–5.5 V	I_{ACT_S}	20	130	μA
			10	170	μA
33	I/O input leakage current ²²	I_{INACT_D}	-2.5	2.5	μA
34	DC injection current (per pin)	I_{IC}	-2.0	2.0	mA
35	Analog input current, channel off ²³	I_{INACT_A}	-150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	-2.5	2.5	μA
36	V_{SS} to V_{SSA} differential voltage ²⁴	$V_{SS} - V_{SSA}$	-100	100	mV
37	Analog reference low voltage	V_{RL}	$V_{SSA} - 0.1$	$V_{SSA} + 0.1$	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	-100	100	mV
39	Analog reference high voltage	V_{RH}	$V_{DDA} - 0.1$	$V_{DDA} + 0.1$	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	-50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	-50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	-100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} - V_{DDSYN}$	-0.1	0.1 ²⁵	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	-2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L \text{ to } T_H)$	T_L	T_H	$^{\circ}C$
46	Slew rate on power-supply pins	—	—	50	V/ms

¹ V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

² $|V_{DDA0} - V_{DDA1}|$ must be < 0.1 V.

³ V_{PP} can drop to 3.0 V during read operations.

⁴ If standby operation is not required, connect V_{STBY} to ground.

⁵ Applies to CLKOUT, external bus pins, and Nexus pins.

⁶ Maximum average RMS DC current.

⁷ Figure 2 shows an illustration of the I_{DD_STBY} values interpolated for these temperature values.

⁸ Average current measured on Automotive benchmark.

⁹ Peak currents can be higher on specialized code.

¹⁰ High use current measured while running optimized SPE assembly code with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM.

- ¹¹ Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to [Table 11](#) for values to calculate power dissipation for specific operation.
- ¹² Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to [Table 10](#) for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
- ¹³ Maximum average RMS DC current.
- ¹⁴ [Figure 2](#) shows an illustration of the I_{DD_STBY} values interpolated for these temperature values.
- ¹⁵ Average current measured on automotive benchmark.
- ¹⁶ Peak currents can be higher on specialized code.
- ¹⁷ High use current measured while running optimized SPE assembly code with all channels of the eMIOS and eTPU running autonomously, plus the eDMA transferring data continuously from SRAM to SRAM.
- ¹⁸ [Figure 2](#) shows that the current specification relates to average standby operation after SRAM has been loaded with data. For power up current see [Section 3.7](#), “Power-Up/Down Sequencing”.
- ¹⁹ Power requirements for the V_{DD33} supply depend on the frequency of operation, load of all I/O pins, and the voltages on the I/O segments. Refer to [Table 11](#) for values to calculate the power dissipation for a specific operation.
- ²⁰ Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. Refer to [Table 10](#) for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
- ²¹ Absolute value of current, measured at V_{IL} and V_{IH} .
- ²² Weak pullup/down inactive. Measured at $V_{DDE} = 3.6$ V and $V_{DDEH} = 5.25$ V. Applies to pad types: pad_fc, pad_sh, and pad_mh.
- ²³ Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 °C to 12 °C, in the ambient temperature range of 50 °C to 125 °C. Applies to pad types: pad_a and pad_ae.
- ²⁴ V_{SSA} refers to both V_{SSA0} and V_{SSA1} . $|V_{SSA0} - V_{SSA1}|$ must be < 0.1 V.
- ²⁵ Up to 0.6 V during power up and power down.

3.8.1 I/O Pad Current Specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a segment. The output pin current can be calculated from Table 10 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 10.

Table 10. I/O Pad Average DC Current ($T_A = T_L$ to T_H)¹

Spec	Pad Type	Symbol	Frequency (MHz)	Load ² (pF)	Voltage (V)	Drive Select / Slew Rate Control Setting	Current (mA)
1	Slow	I_{DRV_SH}	25	50	5.25	11	8.0
2			10	50	5.25	01	3.2
3			2	50	5.25	00	0.7
4			2	200	5.25	00	2.4
5	Medium	I_{DRV_MH}	50	50	5.25	11	17.3
6			20	50	5.25	01	6.5
7			3.33	50	5.25	00	1.1
8			3.33	200	5.25	00	3.9
9	Fast	I_{DRV_FC}	66	10	3.6	00	2.8
10			66	20	3.6	01	5.2
11			66	30	3.6	10	8.5
12			66	50	3.6	11	11.0
13			66	10	1.98	00	1.6
14			66	20	1.98	01	2.9
15			66	30	1.98	10	4.2
16			66	50	1.98	11	6.7
17			56	10	3.6	00	2.4
18			56	20	3.6	01	4.4
19			56	30	3.6	10	7.2
20			56	50	3.6	11	9.3
21			56	10	1.98	00	1.3
22			56	20	1.98	01	2.5
23			56	30	1.98	10	3.5
24			56	50	1.98	11	5.7
25			40	10	3.6	00	1.7
26			40	20	3.6	01	3.1
27			40	30	3.6	10	5.1
28			40	50	3.6	11	6.6
29			40	10	1.98	00	1.0
30			40	20	1.98	01	1.8
31			40	30	1.98	10	2.5
32			40	50	1.98	11	4.0

¹ These values are estimates from simulation and are not tested. Currents apply to output pins only.

² All loads are lumped.

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply depends on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H)¹

Spec	Pad Type	Symbol	Frequency (MHz)	Load ² (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

¹ These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

² All loads are lumped.

3.9 Oscillator and FMPLL Electrical Characteristics

Table 12. FMPLL Electrical Specifications
 ($V_{DDSYN} = 3.0\text{--}3.6\text{ V}$; $V_{SS} = V_{SSSYN} = 0.0\text{ V}$; $T_A = T_L\text{ to }T_H$)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	PLL reference frequency range: ¹ Crystal reference External reference Dual controller (1:1 mode)	$f_{ref_crystal}$ f_{ref_ext} $f_{ref_1:1}$	8 8 24	20 20 $f_{sys} \div 2$	MHz
2	System frequency ²	f_{sys}	$f_{ICO(MIN)} \div 2^{RFD}$	f_{MAX} ³	MHz
3	System clock period	t_{CYC}	—	$1 \div f_{sys}$	ns
4	Loss of reference frequency ⁴	f_{LOR}	100	1000	kHz
5	Self-clocked mode (SCM) frequency ⁵	f_{SCM}	7.4	17.5	MHz
6	EXTAL input high voltage crystal mode ⁶ All other modes [dual controller (1:1), bypass, external reference]	V_{IHEXT}	$V_{XTAL} + 0.4\text{ V}$	—	V
		V_{IHEXT}	$(V_{DDE5} \div 2) + 0.4\text{ V}$	—	V
7	EXTAL input low voltage crystal mode ⁷ All other modes [dual controller (1:1), bypass, external reference]	V_{ILEXT}	—	$V_{XTAL} - 0.4\text{ V}$	V
		V_{ILEXT}	—	$(V_{DDE5} \div 2) - 0.4\text{ V}$	V
8	XTAL current ⁸	I_{XTAL}	0.8	3	mA
9	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
10	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
11	Crystal manufacturer's recommended capacitive load	C_L	Refer to crystal specification	Refer to crystal specification	pF
12	Discrete load capacitance to connect to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L) - C_{S_EXTAL} - C_{PCB_EXTAL}$ ⁹	pF
13	Discrete load capacitance to connect to XTAL	C_{L_XTAL}	—	$(2 \times C_L) - C_{S_XTAL} - C_{PCB_XTAL}$ ⁹	pF
14	PLL lock time ¹⁰	t_{pll}	—	750	μs
15	Dual controller (1:1) clock skew (between CLKOUT and EXTAL) ^{11, 12}	t_{skew}	-2	2	ns
16	Duty cycle of reference	t_{DC}	40	60	%
17	Frequency unLOCK range	f_{UL}	-4.0	4.0	% f_{sys}
18	Frequency LOCK range	f_{LCK}	-2.0	2.0	% f_{sys}

Table 12. FMPLL Electrical Specifications (continued) $(V_{DDSYN} = 3.0\text{--}3.6\text{ V}; V_{SS} = V_{SSSYN} = 0.0\text{ V}; T_A = T_L \text{ to } T_H)$

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: ^{13, 14} Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	— —	5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit ¹⁵ (do not exceed f_{SYS} maximum)	C_{MOD}	0.8	2.4	% f_{SYS}
21	ICO frequency $f_{ICO} = [f_{ref_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ ¹⁶ $f_{ICO} = [f_{ref_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ICO}	48	80 ¹⁷	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 ¹⁸	MHz

¹ Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within $\pm 5\%$ of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

² All internal registers retain data at 0 Hz.

³ Up to the maximum frequency rating of the device (refer to [Table 1](#)).

⁴ Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

⁵ The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR} . SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

⁶ Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). $(V_{extal} - V_{xtal})$ must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

⁷ Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). $(V_{xtal} - V_{extal})$ must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

⁸ I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

⁹ C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

¹⁰ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

¹¹ PLL is operating in 1:1 PLL mode.

¹² $V_{DDE} = 3.0\text{--}3.6\text{ V}$.

¹³ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

¹⁴ Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

¹⁵ Modulation depth selected must not result in f_{SYS} value greater than the f_{SYS} maximum specified value.

¹⁶ $f_{SYS} = f_{ICO} \div (2^{RFD})$.

¹⁷ The ICO frequency can be higher than the maximum allowable system frequency. For this case, set the FMPLL synthesizer control register reduced frequency divider (FMPLL_SYNCR[RFD]) to divide-by-two (RFD = 0b001). Therefore, for a 40 MHz maximum device (system frequency), program the FMPLL to generate 80 MHz at the ICO output and then divide-by-two the RFD to provide the 40 MHz clock.

¹⁸ Maximum value for dual controller (1:1) mode is $(f_{MAX} \div 2)$ with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	ADC clock (ADCLK) frequency ¹	F_{ADCLK}	1	12	MHz
2	Conversion cycles Differential Single ended	CC	13 + 2 (15) 14 + 2 (16)	13 + 128 (141) 14 + 128 (142)	ADCLK cycles
3	Stop mode recovery time ²	T_{SR}	10	—	μ s
4	Resolution ³	—	1.25	—	mV
5	INL: 6 MHz ADC clock	INL6	-4	4	Counts ³
6	INL: 12 MHz ADC clock	INL12	-8	8	Counts
7	DNL: 6 MHz ADC clock	DNL6	-3 ⁴	3 ⁴	Counts
8	DNL: 12 MHz ADC clock	DNL12	-6 ⁴	6 ⁴	Counts
9	Offset error with calibration	OFFWC	-4 ⁵	4 ⁵	Counts
10	Full-scale gain error with calibration	GAINWC	-8 ⁶	8 ⁶	Counts
11	Disruptive input injection current ^{7, 8, 9, 10}	I_{INJ}	-1	1	mA
12	Incremental error due to injection current. All channels are $10\text{ k}\Omega < R_s < 100\text{ k}\Omega$ Channel under test has $R_s = 10\text{ k}\Omega$, $I_{INJ} = I_{INJMAX}, I_{INJMIN}$	E_{INJ}	-4	4	Counts
13	Total unadjusted error (TUE) for single ended conversions with calibration ^{11, 12, 13, 14, 15}	TUE	-4	4	Counts

¹ Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

² Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

³ At $V_{RH} - V_{RL} = 5.12\text{ V}$, one least significant bit (LSB) = 1.25, mV = one count.

⁴ Guaranteed 10-bit mono tonicity.

⁵ The absolute value of the offset error without calibration ≤ 100 counts.

⁶ The absolute value of the full scale gain error without calibration ≤ 120 counts.

⁷ Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than V_{RH} , and 0x000 for values less than V_{RL} . This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

⁸ Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

⁹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5\text{ V}$ and $V_{NEGCLAMP} = -0.3\text{ V}$, then use the larger of the calculated values.

¹⁰ This condition applies to two adjacent pads on the internal pad.

¹¹ The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

¹² TUE does not apply to differential conversions.

¹³ Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: $-16\text{ counts} < \text{TUE} < 16\text{ counts}$.

¹⁴ TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

¹⁵ Depending on the input impedance, the analog input leakage current (Table 9. DC Electrical Specifications, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

3.11 H7Fb Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications ($T_A = T_L$ to T_H)

Spec	Flash Program Characteristic	Symbol	Min.	Typical ¹	Initial Max. ²	Max. ³	Unit
3	Doubleword (64 bits) program time ⁴	$T_{dwprogram}$	—	10	—	500	μ s
4	Page program time ⁴	$T_{pprogram}$	—	22	44 ⁵	500	μ s
7	16 KB block pre-program and erase time	$T_{16kpperase}$	—	325	525	5000	ms
9	48 KB block pre-program and erase time	$T_{48kpperase}$	—	435	525	5000	ms
10	64 KB block pre-program and erase time	$T_{64kpperase}$	—	525	675	5000	ms
8	128 KB block pre-program and erase time	$T_{128kpperase}$	—	675	1800	7500	ms
11	Minimum operating frequency for program and erase operations ⁶	—	25	—	—	—	MHz

¹ Typical program and erase times are calculated at 25 °C operating temperature using nominal supply values.

² Initial factory condition: ≤ 100 program/erase cycles, 25 °C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

³ The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

⁴ Actual hardware programming times. This does not include software overhead.

⁵ Page size is 128 bits (4 words).

⁶ The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min.	Typical ¹	Unit
1a	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
1b	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	P/E	1000	100,000	cycles
2	Data retention Blocks with 0–1,000 P/E cycles Blocks with 1,001–100,000 P/E cycles	Retention	20 5	— —	years

¹ Typical endurance is evaluated at 25° C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 Typical Endurance for Nonvolatile Memory.

Electrical Characteristics

Table 16 shows the FLASH_BIU settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 16. FLASH_BIU Settings vs. Frequency of Operation¹

Target Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN ²	IPFEN ²	PFLIM ³	BFEN ²
Up to and including 27 MHz ^{4, 5}	0b000	0b000	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Up to and including 52 MHz ⁶	0b001	0b001	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Up to and including 77 MHz ⁷	0b010	0b010	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Up to and including 82 MHz ⁸	0b011 ⁹	0b011 ⁹	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Reset values:	0b111	0b111	0b11	0b0	0b0	0b000	0b0

¹ Illegal combinations exist. Use entries from the same row in this table.

² For maximum flash performance, set to 0b1.

³ For maximum flash performance, set to 0b010.

⁴ 27 MHz parts allow for 25 MHz system clock + 2% frequency modulation (FM).

⁵ The APC, RWSC, and WWSC combination requires setting the PRD bit to 1 in the flash MCR register.

⁶ 52 MHz parts allow for 50 MHz system clock + 2% FM.

⁷ 77 MHz parts allow for 75 MHz system clock + 2% FM.

⁸ 82 MHz parts allow for 80 MHz system clock + 2% FM.

⁹ For frequencies up to and including 80 MHz, if VDD is within ±5% of 1.5 V, then APC = RWSC = 0b010 is a valid setting.

3.12 AC Specifications

3.12.1 Pad AC Specifications

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V)¹

Spec	Pad	SRC / DSC (binary)	Out Delay (ns) ^{2, 3, 4}	Rise / Fall (ns) ^{4, 5}	Load Drive (pF)
1	Slow high voltage (SH)	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200

Table 17. Pad AC Specifications ($V_{DDEH} = 5.0\text{ V}$, $V_{DDE} = 1.8\text{ V}$)¹ (continued)

Spec	Pad	SRC / DSC (binary)	Out Delay ^{2, 3, 4} (ns)	Rise / Fall ^{4, 5} (ns)	Load Drive (pF)
2	Medium high voltage (MH)	11	16	8	50
			43	30	200
		01	34	15	50
			61	35	200
		00	192	100	50
			239	125	200
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
				—	—
4	Pullup/down (3.6 V max)	—	—	9000	50
5	Pullup/down (5.5 V max)	—	—	—	50

¹ These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: $V_{DD} = 1.35\text{--}1.65\text{ V}$; $V_{DDE} = 1.62\text{--}1.98\text{ V}$; $V_{DDEH} = 4.5\text{--}5.25\text{ V}$; V_{DD33} and $V_{DDSYN} = 3.0\text{--}3.6\text{ V}$; and $T_A = T_L$ to T_H .

² This parameter is supplied for reference and is guaranteed by design (not tested).

³ The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

⁴ The output delay and rise and fall are measured to 20% or 80% of the respective signal.

⁵ This parameter is guaranteed by characterization rather than 100% tested.

Table 18. Derated Pad AC Specifications ($V_{DDEH} = 3.3\text{ V}$, $V_{DDE} = 3.3\text{ V}$)¹

Spec	Pad	SRC/DSC (binary)	Out Delay ^{2, 3, 4} (ns)	Rise / Fall ^{3, 5} (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium high voltage (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200