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# LatticeXP™ Advanced Evaluation Board

## User's Guide

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## Introduction

Traditional SRAM-based FPGA solutions require additional non-volatile memory components be placed onto the printed circuit board (PCB), consuming additional resources and adding cost to the PCB solution. Alternatives to the SRAM-based FPGA include fuse based FPGAs or ASIC devices. While these solutions provide a non-volatile solution, they cannot be re-programmed.

The LatticeXP is a non-volatile, re-programmable FPGA solution, including both SRAM-based FPGA cells for easy reconfiguration and Flash-based memory for non-volatility, all in one efficient package.

The LatticeXP Advanced Evaluation Board is designed to help the user examine key features of the LatticeXP device and to aid in the development of custom designs. It is a ready-made, proven platform that includes a variety of industry-standard memory and communication interfaces.

Please check the Lattice web site for updates to this user's guide at: www.latticesemi.com/boards. Please note the revision number on the front of this document.

## Features

- Single board solution for evaluation of the LatticeXP FPGA
- LatticeXP FPGA in a 388-ball fpBGA package
- DDR SODIMM socket and DDR power generation
- FCRAM interface and memory
- 10/100/1000 Mbps Ethernet PHY to an RJ45 connector
- PCI plated finger connections
- Seven-segment LED
- Eight LEDs for visual feedback
- Eight-position switch input
- 1149.1 JTAG programming/boundary scan interface
- Built-in power supply operating from 5V external supply (AC adapter included)
- Selectable CORE voltage for the LatticeXP
- Selectable voltages for all eight I/O banks
- Built in oscillator for reference clocks
- SMA connectors to LatticeXP clock input and general purpose I/O pins
- 100mil center-center test point grid

## General Description

The heart of the LatticeXP Advanced Evaluation board is the LatticeXP FPGA. Around this core device are several industry standard interfaces and protocol devices.

The LatticeXP is manufactured to operate with multiple 1.2V to 5V voltage ranges. The LFXP10E device requires a core voltage supply at 1.2V and an auxiliary I/O supply at 3.3V. The LFXP10C device requires a core voltage supply at 1.5V-3.3V, and an auxiliary 3.3V supply. The LatticeXP Advanced Evaluation Board provides four supply voltages, all sourced from a 5V external source. The board provides fixed 1.2V, 2.5V and 3.3V power rails, and a single adjustable voltage that ranges from 1.2V to 3.3V. It is possible to use external power supplies to override the fixed output levels, if it is required. The voltage supplied to the LatticeXP core is selectable using shunts.

Once a correct set of supply voltages has been applied to the LatticeXP FPGA, the device is ready for programming. The LatticeXP FPGA is typically programmed and verified from the 1149.1 JTAG interface. A JTAG download cable can be connected onto either a 1x10 SIP header or a 2x5 DIP header. The LatticeXP is typically programmed using the Lattice ispVM® System software. The ispVM System software can be downloaded from the Lattice web site at www.latticesemi.com/software. ispVM System 15.2 or later should be used to program the LatticeXP device. The ispVM System software can be used to program either the SRAM memory or the Flash cells. The internal Flash memory on the LatticeXP device can be reprogrammed in the background while the FPGA is operating.

LatticeXP devices can also be programmed using either serial or parallel interfaces. The parallel interface permits either the SRAM or the Flash PROM memories to be programmed in the same manner as the JTAG port. The slave serial and master serial modes available on the LatticeXP only program the SRAM memory. The LatticeXP Advanced board does not support these alternate programming modes directly. Test points are provided on the board for connecting to the serial programming points. The parallel programming interface is inaccessible since it is connected to provide the FCRAM memory function.

Once programmed, the LatticeXP device has access to several interfaces designed to highlight FPGA features. The LatticeXP directly interfaces to a set of switches, LEDs, a seven segment display, a prototype grid, a FCRAM chip, Double-data-rate DRAM, a set of SMA connectors, a PCI bus and an Ethernet PHY device.

One of the key interfaces supported directly in the LatticeXP FPGA is easy support for DDR DRAM memories. The evaluation board provides a DDR SODIMM socket for inserting SODIMM DDR modules. The LatticeXP directly controls the address and memory strobes and connects to a 16-bit data bus. The data bus requires data qualification strobes (DQS) also be present. The LatticeXP FPGA series has an internal hardware assist for managing the DQS signals. These signals are connected to the DDR SODIMM. The DDR interface is capable of running at 167MHz (333 DDR).

The FCRAM interface also uses the LatticeXP DQS hardware assist. The LatticeXP Advanced Evaluation board provides a single FCRAM device, providing an eight-bit data bus. Data rates to between the FCRAM and the LatticeXP are equivalent to the DDR interface.

The evaluation board also provides a 3.3V 33MHz, 32-bit PCI interface. The board is designed to only be inserted into 3.3V PCI backplanes. It is not recommended to install the board into a 5V backplane. The LatticeXP FPGA is not directly 5V tolerant. In order for the device to be placed into a 5V system the PCI I/O clamp diodes must be enabled, and series current limiting resistors need to be on each 5V I/O.

The evaluation board includes a 10/100/1000 Ethernet PHY device (National Semiconductor DP83865). All of the necessary support components are provided to connect to a 10/100/1000 Base-T network. The physical side of the PHY connects to an RJ45 connector with built-in isolation magnetics and a 3KV capacitor. The Media Independent Interface (MII) is connected to the LatticeXP FPGA. The LatticeXP must be programmed with a Media Access Controller (MAC) before Ethernet traffic can be routed across the interface.

Additional features of the LatticeXP Advanced Evaluation board are described in detail in the following section.

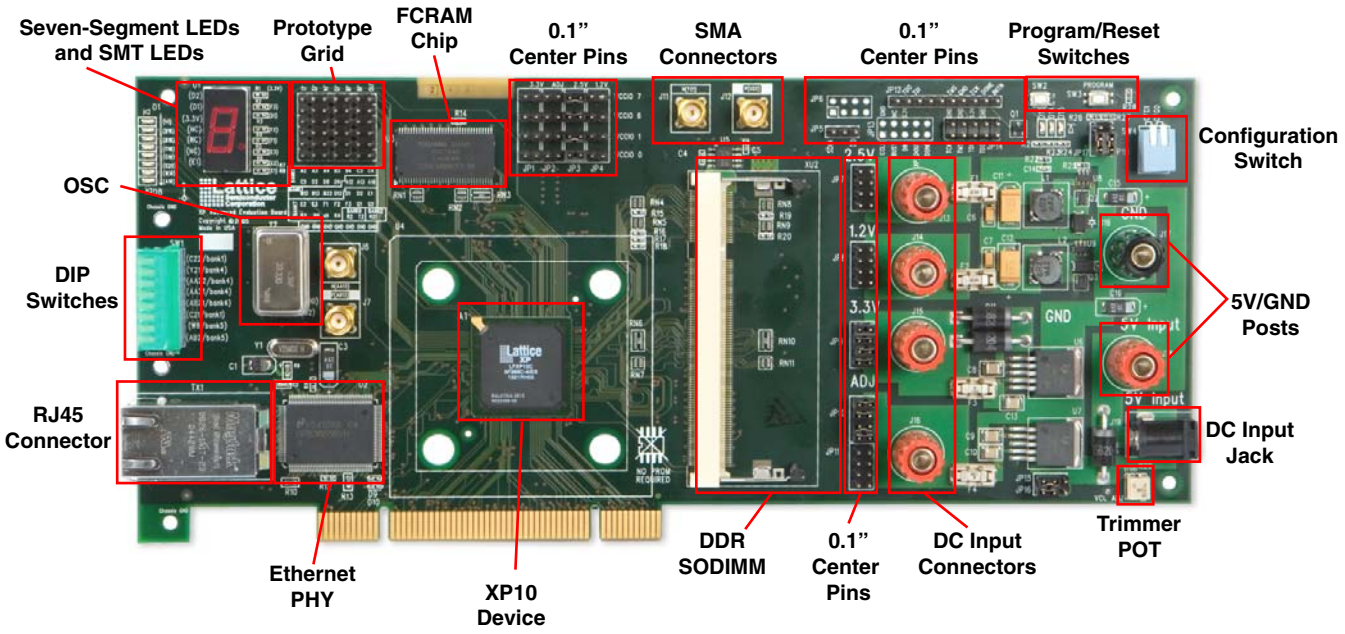
## Additional Resources

Additional resources related to this board can be downloaded from the web at www.latticesemi.com/boards. Click on the appropriate evaluation board, then see the blue "Resources" box on the right of the screen for items such as: updated documentation, software, sample designs, IP evaluation bitstreams, and more.

## LatticeXP Advanced Evaluation Board Functional Description

The LatticeXP Advanced Evaluation Board is comprised of several primary functional blocks as shown in Figure 1. In the descriptions below, locations of components and board features will be described relative to a compass symbol placed adjacent to the Lattice logo. For example, the seven-segment LED is on the northwest corner of the board, and the trimmer potentiometer is on the southeast corner of the board.

*Figure 1. LatticeXP Advanced Evaluation Board Functional Blocks*




## Power Supply

The LatticeXP Advanced Evaluation Board provides three locations to apply power. On the east side of the board are a pair of banana jacks (J18 and J17), and a coaxial DC connector (J19), which receive power from either a bench power supply or a brick style power supply. The third method for powering the board is to place it in a PCI host. Do not provide a supply voltage from the other DC input sources when the board is plugged into a PCI host backplane. In order to power the board, a DC source between 5V and 5.5V must be applied to the DC input jack or the 5V/GND banana connectors. Alternately 3.3V must be supplied from the PCI interface.

The 5V DC input voltage is converted by DC-DC converters and switching power supplies to provide 3.3V, 2.5V, 1.2V, and an adjustable DC source. The output from these supplies travels through surface mounted fuse holders. Fuses are supplied and prevent over-current conditions from damaging the power supply circuitry.

Each of the DC converters can be enabled and disabled independently. Jumpers JP15-18 control the conversion system.

*Table 1. Power Supply Enable/Disable*

| Jumper Number | Supply Rail Enabled/Disabled | Function |
|---|---|---|
| JP15 | $V_{ADJ}$ | 1-2: Disable<br>2-3: Enable |
| JP16 | 3.3V | 1-2: Disable<br>2-3: Enable |
| JP17 | 2.5V | 1-2: Disable<br>2-3: Enable |
| JP18 | 1.2V | 1-2: Disable<br>2-3: Enable |

More banana jack inputs are located immediately next to (west of) the fuse blocks. These inputs provide an alternate means for applying DC voltage levels to the board. To apply voltages not supplied by the on-board power circuitry, simply remove the appropriate fuse from the fuse holder, then connect an alternate DC supply to the banana jack associated with that fuse.

***Table 2. Power Supply Fuses***

| Fuse Number | Supply Rail Enabled/Disabled | Banana Jack Input |
|---|---|---|
| F1 | 2.5V | J6 |
| F2 | 1.2V | J7 |
| F3 | 3.3V | J8 |
| F4 | $V_{ADJ}$ | J9 |

A set of 2x4 100mil headers (JP7-JP11) are located next to (west of) the banana jacks (J13-J16). All but one of these headers control the LatticeXP core voltage setting. JP10 connects to the Ethernet PHY (U2) and does not connect to the core voltage of the LatticeXP device. JP10 is connected to $V_{ADJ}$ on one side and to the PHY core supply on the other. When using the PHY, $V_{ADJ}$ must be set to 1.8V. Do not remove power from the Ethernet PHY core. Doing so may damage the Ethernet PHY.

The remaining jumper blocks must have only one supply rail connected to the LatticeXP core voltage. The jumpers placed on the jumper block must run in an east-west orientation. The jumper blocks assign the core voltage as follows:

***Table 3. LatticeXP Core Voltage Selection***

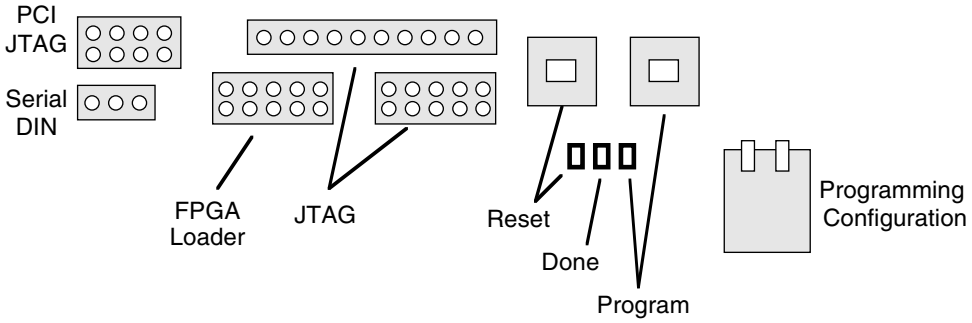
| Jumper Block | Voltage Supplied to the LatticeXP Core |
|---|---|
| JP7 | 2.5V |
| JP8 | 1.2V 'E' series LatticeXP only |
| JP9 | 3.3V |
| JP11 | $V_{ADJ}$ |

R29 is a trimmer potentiometer which controls the output level of the $V_{ADJ}$ section of the power supply. R29 is located in the southeast corner of the board. The $V_{ADJ}$ can be set between 1.2V and 3.3V.

## Programmability

Components and logic related to programming the LatticeXP FPGA are located in the northeast corner of the board. These include a set of switches, jumpers, push buttons and header blocks that modify how the LatticeXP programs itself when power is applied.

***Figure 2. Programming Interface***




**SW4 Configuration**

SW4 directs the LatticeXP to a programming data source used to configure the on-chip SRAM. SW4 is located on the east side of the board. Table 4 shows the mode for each switch setting.

***Table 4. LatticeXP Programming Configuration***

| SW4 Setting CFG1:CFG0 | Mode |
|---|---|
| Up:up | Self-download mode<br>CPU Flash programming |
| Up:down | Slave parallel programming |
| Down:up | Master serial programming |
| Down:down | Slave serial programming |

SW4 is typically set with both switches up. The LatticeXP loads configuration data from the on-chip internal Flash memory.

The LatticeXP Advanced Evaluation board does not support the Slave Parallel programming mode since the data bus and controls for this mode are dual-use pins, connected to the FCRAM interface.

Slave and Master Serial programming modes are also available. The serial mode interface is available using JP5 (Serial DIN) and JP13 (FPGA Loader). See the LatticeXP Evaluation Board schematic at the end of this document for further details concerning the connectivity for the serial mode I/Os.

***Table 5. LatticeXP Serial DIN Header Settings***

| Serial DIN Header | Action |
|---|---|
| 1:2 | JP13 DIN to XP DIN |
| 2:3 | Reserved |
| Open | XP DIN available for general purpose I/O |

**Push-buttons and Status LEDs**

There are two push-buttons and three LEDs in the northeast corner of the evaluation board (see Figure 2). The Program push-button asserts the PROGRAM pin on the LatticeXP device, erasing the SRAM and causing the LatticeXP to begin a programming sequence. Pushing the button also illuminates a yellow LED, giving confirmation the switch has been closed.

The other push-button acts as a RESET input to the LatticeXP. The LatticeXP does not have a dedicated RESET input. RESET must be assigned an I/O when the device is programmed. This is done by instantiating the Global Reset macro in the HDL source. A red LED is illuminated whenever the RESET button is pushed.

The third LED is connected through a small amount of control circuitry to the LatticeXP DONE I/O. DONE is driven high when the LatticeXP is successfully programmed. When DONE is driven high, this green LED turns on. This LED is active when the LatticeXP is programmed using the JTAG header. When a JTAG programming sequence is initiated, the LatticeXP I/Os are tristated. The tristated I/Os float high, which mimics the open-drain high assertion of DONE following a successful programming sequence. At the completion of a JTAG programming sequence, the DONE LED will stay illuminated if the programming sequence succeeded. It will turn off if the sequence did not succeed.

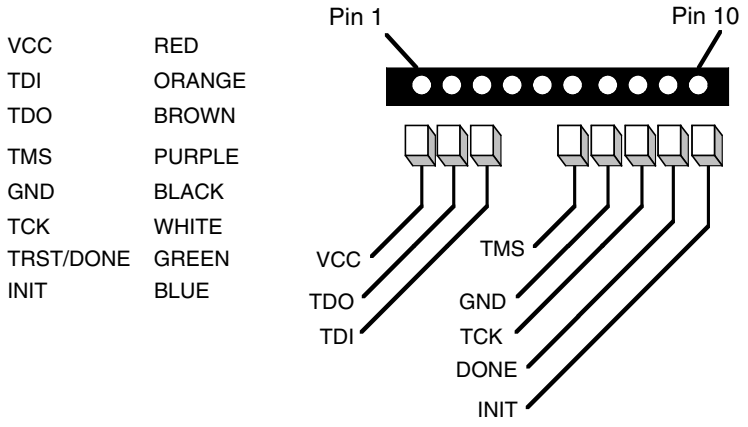
**Programming Headers**

The LatticeXP Advanced Evaluation Board provides two JTAG headers for programming the LatticeXP device. These headers are wired in parallel, and only differ in form factor. JP12 is a 1x10 100mil header, and JP14 is a 2x5 100mil header. Either can be used with a Lattice USB or parallel port download cable. The download cable used with ispVM System software may have either fly-wire JTAG wires, or the JTAG wires in a captive header. Figure 3 shows how the fly-wire JTAG wires are connected to the 1x10 header.

***Important Note:*** *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG*

*pins. Failure to follow these procedures can in result in damage to the LatticeXP FPGA device and render the board inoperable.*

***Figure 3. JTAG Fly-wire Connections***




The 2x5 programming header only connects the four basic JTAG signals, and the VCC source. The silkscreen provided on the board shows the connection points for each wire. All of the remaining fly-wires are left unconnected.

Regardless of which header is used, the ispVM System software is used to control the download cable. Configure the ispVM software to use the cable type connected to the evaluation board (parallel port or USB). Select the bitstream to download, and the memory space to which the data will be written (SRAM or FLASH). See the ispVM System Help for more information.

***Table 6. Programming Interface Connection Summary***

| Function | LatticeXP Pin Location | JP 13 Pin | JP 6 Pin | JP 12 Pin | JP 14 Pin | Note |
|---|---|---|---|---|---|---|
| BUSY | C11 | JP13 (3) | | | | |
| CCLK | G4 | JP13 (1) | | | | |
| DONE | B1 | JP13 (9) | | JP12 (9) | | D14 (Green LED) |
| INITN | Y2 | JP13 (8) | | JP12 (10) | | |
| PROGRAMN | F4 | JP13 (10) | | | | D15 (Yellow LED) |
| TCK | D18 | | JP6 (8) | JP12 (8) | JP14 (1) | |
| TDI | D20 | | JP6 (4) | JP12 (3) | JP14 (5) | |
| TDO | F19 | | JP6 (2) | JP12 (2) | JP14 (7) | |
| TMS | D19 | | JP6 (6) | JP12 (6) | JP14 (3) | |

***Table 7. Supplemental Programming Interface Connection Summary***

| Schematic Name | LatticeXP Pin Location | JP 5 Pin |
|---|---|---|
| CFG0 | C1 | |
| CFG1 | B2 | |
| D0 | D10 | |
| DIN_2_D0 | C13 | JP5 (3) |
| DIN_2_SDIN | A7 | JP5 (1) |

*Important: Use only ispVM System version 15.2 or later to program the LatticeXP device.*

## LatticeXP and Support Interfaces

The LatticeXP Advanced Evaluation Board includes advanced interfaces such as DDR, PCI, FCRAM and Ethernet. These are complex either by the nature of the signaling interface, or by the internal programming required to operate them. Lattice provides bitstreams which can be used to evaluate the performance of the LatticeXP FPGA on several of these interfaces. Lattice also provides precompiled intellectual property cores for controlling the FCRAM, DDR, PCI and the Ethernet. These precompiled intellectual property cores can be used to design and simulate an integrated solution. An intellectual property license is required to generate customized programming bitstreams. Visit the Lattice web site at www.latticesemi.com/boards to find the latest available evaluation bitstreams for these interfaces.

The LatticeXP Advanced Evaluation Board uses the following conventions.

- Devices are numbered in a consistent fashion. Each device starts at reference designator '1' in the northwest corner of the board (i.e. R1, C1, U1, L1, etc.). The component number increases by one in a columnar fashion (i.e. southward). When the south edge of the board is reached, the count resumes slightly east, and at the north side of the board. Thus the highest numbered components will always be in the southeast corner of the board. This same numbering sequence is applied to the reverse side of the printed circuit board.
- Adjacent to the switch inputs, LED outputs, SMA connectors and test points is the alphanumeric position of the pin on the LatticeXP FPGA. For example, next to the DIP oscillators (pin 10 in the silkscreen) is the designator (A10). This indicates XU2 pin 10 is connected to the LatticeXP A10 pin.
- SMA connectors have a solid white rectangular area near them denoting the positive side of a matched pair. The negative side of a matched pair has a white outline rectangle area.

For detailed information concerning the pin connections for these interfaces, see the appropriate connection summary tables in the following pages, and the LatticeXP Advanced Evaluation Board schematics in Appendix A.

### VCCIO Power

The LatticeXP provides eight banks for configuring different input/output voltages and different input/output protocols. The LatticeXP Advanced Evaluation board permits four of these I/O banks to be statically configured based on the requirements of the design. VCCIO bank 2/3 is fixed to 2.5V. These two banks interface to the DDR SODIMM socket. The DDR memory only operates at 2.5V, so making these two banks I/O voltage adjustable is not very useful. Banks 4/5 are set to 3.3V, which configures the I/O correctly for the PCI bus. Banks 0,1, 6, and 7 can be configured to different I/O voltage levels. VCCIO power selection is made using the header in the north-central section of the board (see Figure 4).

***Figure 4. VCCIO Voltage Selection Header***

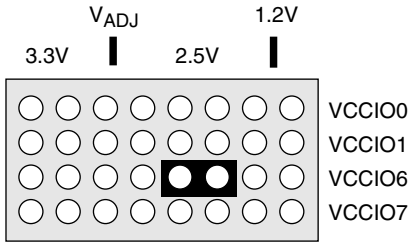



Figure 4 shows how VCCIO6 would be configured to use a 2.5V supply for the output buffer drive level.

### Prototype Grid

The board provides a small 100mil center-center prototype area just to the west of the VCCIO power selection jumpers. This area is connected to FPGA I/Os primarily in banks 0, 1, 6 and 7. The silkscreen near the prototype grid provides a map describing the FPGA alphanumeric grid number and bank of the I/O.

Please note that some of the bank 7 I/Os are connected in parallel with the seven-segment LED. Also, H21 is one of the PLL input pins, so an additional clock frequency can be injected into the FPGA from the prototype area. Refer to Table 8 for a complete description of the prototype area connections.

***Table 8. Prototype Area Connection Summary***

| Board Location | LatticeXP Pin Location | Schematic Name | Note |
|---|---|---|---|
| J1 (1) | A2 | TP_A2 | |
| J1 (2) | C5 | TP_C5 | |
| J1 (3) | B12 | TP_B12 | |
| J1 (4) | E2 | SSEG_D | Also seven-segment display |
| J1 (5) | G3 | TP_G3 | |
| J2 (1) | A3 | TP_A3 | |
| J2 (2) | D3 | TP_D3 | |
| J2 (3) | B13 | TP_B13 | |
| J2 (4) | E3 | SSEG_DP | Also seven-segment display |
| J2 (5) | H4 | TP_H4 | |
| J4 (1) | A4 | TP_A4 | |
| J4 (2) | D8 | TP_D8 | |
| J4 (3) | B22 | TP_B22 | |
| J4 (4) | F1 | SSEG_C | Also seven-segment display |
| J4 (5) | J4 | TP_J4 | |
| J5 (1) | B3 | TP_B3 | Also DIN_2_SDIN |
| J5 (2) | D9 | TP_D9 | |
| J5 (3) | D12 | TP_D12 | Also DIN_2_D0 |
| J5 (4) | F2 | SSEG_G | Also seven-segment display |
| J5 (5) | K4 | TP_K4 | |
| J8 (1) | B4 | TP_B4 | |
| J8 (2) | A12 | TP_A12 | |
| J8 (3) | D1 | SSEG_F | Also seven-segment display |
| J8 (4) | F3 | SSEG_B | Also seven-segment display |
| J8 (5) | R2 | TP_R2 | |
| J9 (1) | C3 | TP_C3 | |
| J9 (2) | A13 | TP_A13 | |
| J9 (3) | D2 | SSEG_A | Also seven-segment display |
| J9 (4) | G1 | TP_G1 | |
| J9 (5) | T2 | TP_T2 | |
| J10 (1) | C4 | TP_C4 | |
| J10 (2) | A18 | TP_A18 | |
| J10 (3) | E1 | SSEG_E | Also seven-segment display |
| J10 (4) | G2 | TP_G2 | |
| J10 (5) | H21 | TP_H21 | Also PLL input |

**LED Displays**

In the northwest corner of the board are two different types of LEDs. Eight chip-style LEDs are connected to I/O pins dedicated to driving the LEDs. The silkscreen indicates the alphanumeric location of the driving I/O. These locations are also indicated in Table 9. The LEDs illuminate when the corresponding I/O is driven to $V_{OL.}$

*Table 9. LED Connection Summary*

| LED Number | LatticeXP Pin Location | Schematic Name |
|---|---|---|
| D1 | H1 | TP_H1 |
| D2 | B16 | TP_B16 |
| D3 | B18 | TP_B18 |
| D4 | C18 | TP_C18 |
| D5 | C19 | TP_C19 |
| D6 | C20 | TP_C20 |
| D7 | W16 | TP_W16 |
| D8 | A16 | TP_A16 |

A seven-segment LED is located in the northwest corner of the board. Unlike the chip LEDs, the I/Os driving the seven-segment display are not dedicated. These LED segments are also connected to the prototype grid. Illuminating one of the LED segments works in the same way as the chip LEDs. Each segment, when driven toward $V_{OL,}$ will illuminate. Refer to Table 10 for a complete description of the seven-segment display connections.

*Table 10. Seven-segment Display Connection Summary*

| Display Segment | LatticeXP Pin Location | Alternate Header Connection | Schematic Name |
|---|---|---|---|
| SSEG_A | D2 | J9 (3) | TP_D2 |
| SSEG_B | F3 | J8 (4) | TP_F3 |
| SSEG_C | F1 | J4 (4) | TP_F1 |
| SSEG_D | E2 | J1 (4) | TP_E2 |
| SSEG_DP | E3 | J2 (4) | TP_E3 |
| SSEG_E | E1 | J10 (3) | TP_E1 |
| SSEG_F | D1 | J8 (3) | TP_D1 |
| SSEG_G | F2 | J5 (4) | TP_F2 |

**Switches**

A set of eight simple toggle switches is located at the west edge of the board. The silkscreen indicates the alphanumeric location of the I/O on the FPGA. When in the up position, the switch is pulled to 3.3V through a 10K resistor. When in the down position, the switch is tied to ground. Refer to Table 11 for a complete description of the switch connections.

*Table 11. Switch Connection Summary*

| Board Location | LatticeXP Pin Location | Schematic Name |
|---|---|---|
| SW1_1 | C22 | TP_C22 |
| SW1_2 | Y21 | TP_Y21 |
| SW1_3 | AA22 | TP_AA22 |
| SW1_4 | AA21 | TP_AA21 |
| SW1_5 | AB21 | TP_AB21 |
| SW1_6 | C21 | TP_C21 |
| SW1_7 | W8 | TP_W8 |
| SW1_8 | AB2 | TP_AB2 |

**Oscillator and Clock Inputs**

FPGA designs are nearly always created with logic synchronous to some reference frequency. The FPGA has four PLLs and multiple primary clock inputs. Some of these clock inputs are dedicated to a particular interface on the evaluation board. There are several ways to input reference clock frequencies.

LatticeXP pins U22 and T21 are connected to SMA connectors. These two SMAs are connected to the positive and negative pairs of one of the four PLLs provided by the FPGA. The characteristic impedance of the traces is 50 ohms.

Two additional SMA connectors provide a matched pair (positive and negative) of traces to one of the Primary Clock inputs. This pair of traces enter the FPGA at pins AB13 (positive) and AA13 (negative). The characteristic impedance of the traces is 50 ohms.

***Table 12. SMA Connection Summary***

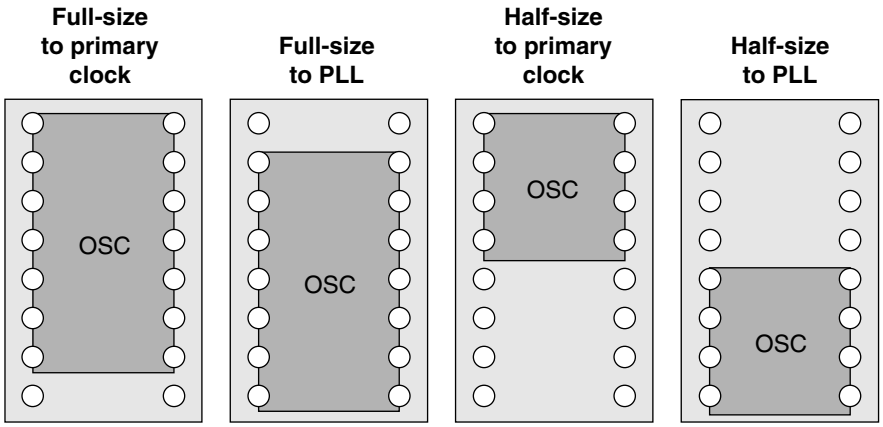
| Board Location | LatticeXP Pin Location | Schematic Name |
|---|---|---|
| J6 SMA | AA13 | PRI_CLK_N |
| J7 SMA | AB13 | PRI_CLK_P |
| J11 SMA | U22 | SMA_U22 |
| J12 SMA | T21 | SMA_T21 |

The PLL input and the Primary Clock are also programmable as general purpose I/Os. This permits these I/Os to be evaluated in operation over coaxial cables.

The board also provides a 14-pin 3.3V clock oscillator device. The oscillator is in a 16-pin DIP socket. Using a socket permits the use of an arbitrary input clock frequency and the use of oscillators with different accuracy and jitter characteristics.

The oscillator socket is also wired to permit the use of either full-size or half-size DIP oscillators. Figure 5 shows the configuration options available.

***Figure 5. Oscillator Input Options***




The socket is wired such that pins 10 and 13 are connected to the same Primary Clock input (pin A10). Pin 9 is connected to a PLL input (pin J2) in bank 7 on the FPGA.

The last location provided on the board for supplying external clock frequencies lies in the prototype area. FPGA pin H21 is the positive side of one of the four PLL inputs. An arbitrary clock frequency can be supplied to the FPGA from J10 pin 5 in the prototype grid.

**10/100/1000 Ethernet PHY**

In the southwest corner of the board is a National Semiconductor Gigabit Ethernet PHY (DP83865). The LatticeXP FPGA interacts with the PHY over a Media Independent Interface (MII). The PHY is connected to an RJ45 header on the Media Dependent Interface (MDI). The RJ45 connector has built-in magnetics and spark-gap capacitor. The PHY is available on the board in order to demonstrate the Lattice Ethernet Media Access (MAC) IP core. However, it is also possible to use the PHY to evaluate a custom MAC solution. Refer to the schematic and the National Semiconductor DP83865 Data Sheet for detailed information about the operation of the Ethernet PHY interface on this device. Refer to Table 13 for a description of the ethernet PHY connections.

***Table 13. 10/100/1000 Ethernet PHY Connection Summary***

| Schematic Name | LatticeXP Pin Location |
|---|---|
| ETH_CLK_TO_MAC | L4 |
| ETH_COL | W1 |
| ETH_CRS | W2 |
| ETH_EGP0 | J1 |
| ETH_EGP2 | K2 |
| ETH_EGP4 | K3 |
| ETH_EGP5 | J3 |
| ETH_EGP6 | K1 |
| ETH_EGP7 | L2 |
| ETH_GTX_CLK | N4 |
| ETH_MAC_CLK_EN | L3 |
| ETH_MDC | M1 |
| ETH_MDIO | L1 |
| ETH_RESET_N | Y1 |
| ETH_RX_CLK | P1 |
| ETH_RX_D0 | T3 |
| ETH_RX_D1 | N2 |
| ETH_RX_D2 | U4 |
| ETH_RX_D3 | U3 |
| ETH_RX_D4 | U2 |
| ETH_RX_D5 | P2 |
| ETH_RX_D6 | V4 |
| ETH_RX_D7 | V3 |
| ETH_RX_DV | V2 |
| ETH_RX_ER | V1 |
| ETH_TX_CLK | H2 |
| ETH_TX_D0 | M4 |
| ETH_TX_D1 | N3 |
| ETH_TX_D2 | R1 |
| ETH_TX_D3 | P4 |
| ETH_TX_D4 | P3 |
| ETH_TX_D5 | M3 |
| ETH_TX_D6 | T1 |
| ETH_TX_D7 | R4 |
| ETH_TX_EN | R3 |
| ETH_TX_ER | T4 |

**Required Board Modification**

The LatticeXP Advanced Evaluation Board uses the National Semiconductor DP83865 GigaPhyter Ethernet PHY to provide network access. Lattice has discovered that the circuit placed on the XP Advanced board prevents correct operation upon applying power to the board.

In order for the Ethernet PHY to operate it is mandatory to modify the evaluation board. The tuned crystal oscillator circuit providing the 25MHz input clock to the GigaPhyter device is incorrect. A parallel termination resistor, R54, was placed according to guidelines published by National Semiconductor. The value selected for the termination resistor has been determined to be incorrect. The resistor attenuates the clock preventing the tuned circuit from providing sufficient output swing to the DP83865. This termination resistor is optional. R54 must be removed for the DP83865 to operate.

**Putting the PHY into GMII Mode**

Lattice has also determined the PHY device will power up in RGMII mode and the TX_CLK and RX_CLK signals will not oscillate. The PHY needs to be put into GMII mode. The DP83865 enters GMII mode in one of two ways. The first is by writing to the AUX_CTRL register using the MDIO interface. The second is by applying a pull-down resistor to the RGMII_EN[1] configuration pin. The configuration pin is read at power up, placing the DP83865 into GMII mode.

To make the DP83865 enter GMII mode at power up tie the DP83865 side of R71 to ground through a current limiting resistor. This rework is not mandatory. You can use MDIO transactions to write into the DP83865's registers, putting it into GMII mode. Using MDIO write the Auxiliary Control Register (AUX_CTRL) address 0x12, bits 13:12. The register description is as follows:

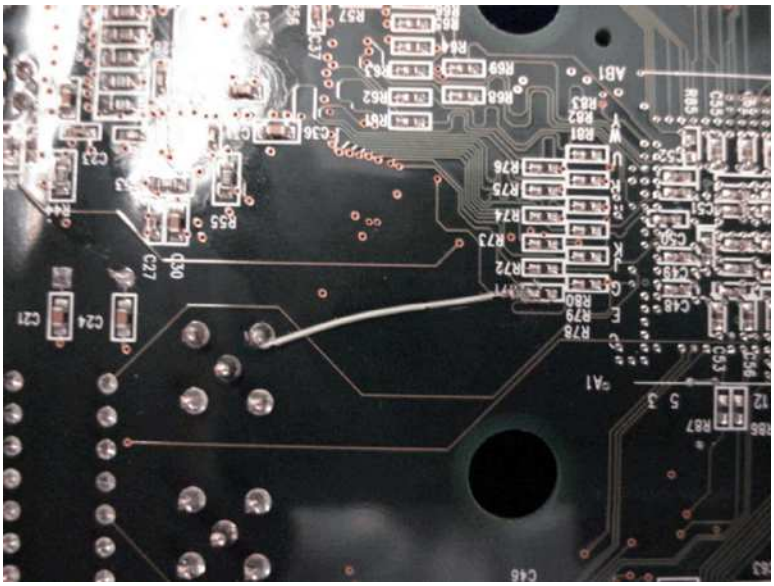
RGMII ENABLE: These two bits control RGMII mode or MII/GMII mode.
RGMII_EN[1:0]
11 = RGMII - 3COM mode
10 = RGMII - HP mode
01 = GMII mode
00 = GMII mode

Lattice has tested putting a current-limiting pull-down resistor on the board. This will pull the TX_CLK / RGMII_SEL[1] bit to a '0' on power-up, putting the device automatically into GMII mode. This is based on the data sheet:

| RGMII_SEL1 | RGMII_SEL0 | MAC Interface |
|---|---|---|
| 0 | 0 | GMII |
| 0 | 1 | GMII |
| 1 | 0 | RGMII – HP |
| 1 | 1 | RGMII – 3COM |

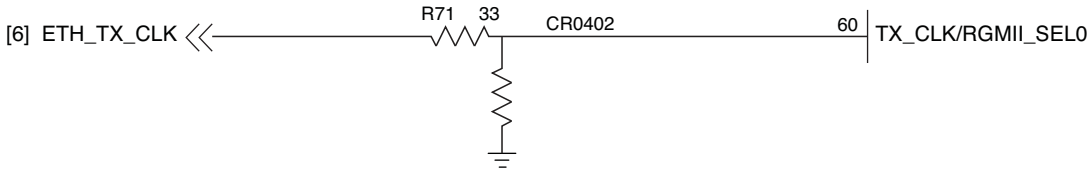
In this example, a current limiting resistor of 2.2K was used. You can see the picture below of the fix. A resistor was soldered to R71 and a wire was soldered to the ground terminal of SMA J7.

***Figure 6. Board Fix, R71 to GND***



From the Ethernet PHY schematic in EB13, LatticeXP Advanced Evaluation Board User's Guide, the fix would look like the figure below.

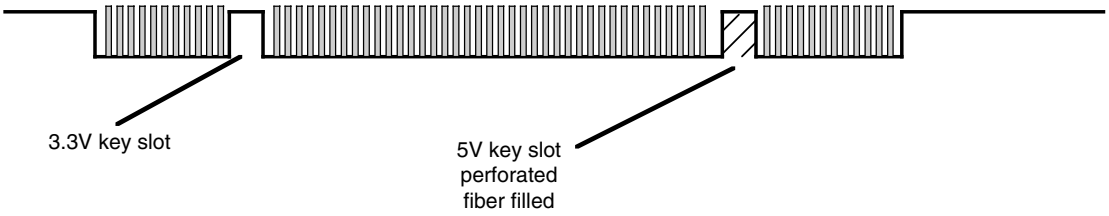
***Figure 7. Schematic Diagram of R71 Fix***




**PCI Interface**

The LatticeXP Advanced Evaluation Board includes a PCI bus interface. The PCI interface is capable of 33MHz operation, and provides a 32-bit data bus path. The board is designed to plug into 3.3V PCI systems exclusively since the LatticeXP I/O pins are not 5V tolerant. Figure 8 shows the PCI plated fingers and the notches used to prevent insertion into the wrong kind of backplane. Visit the Lattice web site at www.latticesemi.com/boards to download a test evaluation package for the PCI interface. Refer to Table 14 for a description of the PCI connections.

***Figure 8. PCI Backplane Keys***




By default, the board is fabricated with the 5V cutout filled. In order to allow the board to be inserted into all PCI backplanes the 5V cutout is fabricated to permit it to be cut away. If the 5V cutout fiberglass is removed, Lattice does not take responsibility for damage to the FPGA, the evaluation board or the system the evaluation board is inserted into, should it occur.

The PCI traces are routed to the bottom (banks 4 and 5) of the LatticeXP FPGA. The pins on the top and bottom of the FPGA have PCI clamp diodes integrated into the I/O pins. The PCI clock, however, is routed to one of the PLL input pins. The PLL input pins reside on the left and right sides of the FPGA. The left and right side of the device do not have clamp diodes. To compensate for this, the board includes space to install PCI clamp diodes, if desired. Visit the Lattice web site at www.latticesemi.com/boards to download a test evaluation package for the PCI interface. Refer to Table 14 for a description of the PCI connections.

***Table 14. PCI Connection Summary***

| Schematic Name | LatticeXP Pin Location |
|---|---|
| PCI_ACK64_N | AA20 |
| PCI_AD0 | AB18 |
| PCI_AD1 | AA18 |
| PCI_AD10 | AB15 |
| PCI_AD11 | AA15 |
| PCI_AD12 | W13 |
| PCI_AD13 | W12 |
| PCI_AD14 | AB14 |
| PCI_AD15 | AA14 |
| PCI_AD16 | AA12 |
| PCI_AD17 | AA10 |
| PCI_AD18 | Y8 |
| PCI_AD19 | AB8 |
| PCI_AD2 | Y18 |
| PCI_AD20 | AA8 |
| PCI_AD21 | Y7 |
| PCI_AD22 | AB7 |
| PCI_AD23 | AA7 |
| PCI_AD24 | Y10 |
| PCI_AD25 | Y9 |
| PCI_AD26 | AB6 |
| PCI_AD27 | AA6 |
| PCI_AD28 | AB5 |
| PCI_AD29 | AA5 |
| PCI_AD3 | AB17 |
| PCI_AD30 | AB4 |
| PCI_AD31 | W9 |
| PCI_AD4 | Y14 |
| PCI_AD5 | Y13 |
| PCI_AD6 | AA17 |
| PCI_AD7 | Y17 |
| PCI_AD8 | AB16 |
| PCI_AD9 | AA16 |
| PCI_CBE0_N | AA19 |
| PCI_CBE1_N | Y20 |
| PCI_CBE2_N | W14 |
| PCI_CBE3_N | W15 |
| PCI_CLK | U1 |

*Table 14. PCI Connection Summary (Continued)*

| Schematic Name | LatticeXP Pin Location |
|---|---|
| PCI_DEVSEL_N | AB10 |
| PCI_FRAME_N | AB11 |
| PCI_GNT_N | AB3 |
| PCI_IDSEL | AB19 |
| PCI_INTA_N | W6 |
| PCI_INTB_N | Y6 |
| PCI_INTC_N | Y4 |
| PCI_INTD_N | Y5 |
| PCI_IRDY_N | Y11 |
| PCI_LOCK_N | AA9 |
| PCI_PAR | W11 |
| PCI_PERR_N | W10 |
| PCI_PRSNT1_N | AB12 |
| PCI_PRSNT2_N | Y19 |
| PCI_REQ64_N | AB20 |
| PCI_REQ_N | AA3 |
| PCI_RST_N | AA4 |
| PCI_SERR_N | AB9 |
| PCI_STOP_N | AA11 |
| PCI_TRDY_N | Y12 |

**Double Data Rate SDRAM**

The evaluation board includes a SODIMM DDR SDRAM socket. The LatticeXP is well suited to interfacing to DDR SDRAM memories. The LatticeXP FPGA family has dedicated I/O pins for controlling the Data Qualification Strobe (DQS) pin implemented in DDR. The DQS pin is used to signal valid data is present on the data bus. The FPGA provides a dedicated DQS I/O pin for each eight data bits on the DDR bus. Each DQS I/O spans 13 other LatticeXP I/O pins. Thus the eight data bits can be assigned to a wide range of FPGA pins. The high number of I/O pins available improves the likelihood of successfully routing the data bus on a PCB.

A standard SODIMM socket provides 64 data bits. The LatticeXP Advanced Evaluation Board only connects to 16 data bus bits. This subset is chosen to provide a demonstration of the DDR capabilities of the LatticeXP while still permitting other interfaces to be showcased. All of the remaining DDR control signals, including the serial data bus, are connected to the LatticeXP FPGA. The DDR memory interface operates up to a 166MHz clock rate.

The DDR specifies a fairly rigid set of requirements with respect to the reference and termination voltages. In order to meet these requirements the evaluation board uses a National Semiconductor LP2995 DDR power management chip. The LP2995 accepts a 2.5V input and provides a regulated $V_{REF}$ and $V_{TT}$ supply for the SODIMM socket. Visit the Lattice web site at www.latticesemi.com/boards to download a test evaluation package for the DDR SDRAM interface. Refer to Table 15 for a description of the DDR SDRAM connections.

*Table 15. DDR SDRAM Connection Summary*

| Schematic Name | LatticeXP Pin Location |
|---|---|
| DDR_A0 | R19 |
| DDR_A1 | R21 |
| DDR_A10 | T22 |
| DDR_A11 | M19 |
| DDR_A12 | M22 |

*Table 15. DDR SDRAM Connection Summary (Continued)*

| Schematic Name | LatticeXP Pin Location |
|---|---|
| DDR_A2 | P19 |
| DDR_A3 | R22 |
| DDR_A4 | P22 |
| DDR_A5 | P20 |
| DDR_A6 | N19 |
| DDR_A7 | P21 |
| DDR_A8 | M20 |
| DDR_A9 | N21 |
| DDR_BA0 | V22 |
| DDR_BA1 | T19 |
| DDR_CAS_N | T20 |
| DDR_CK0 | H19 |
| DDR_CK0_N | G19 |
| DDR_CKE0 | J20 |
| DDR_CKE1 | J19 |
| DDR_DM0 | D22 |
| DDR_DM1 | K21 |
| DDR_DQ0 | F21 |
| DDR_DQ1 | E22 |
| DDR_DQ10 | K22 |
| DDR_DQ11 | L22 |
| DDR_DQ12 | J21 |
| DDR_DQ13 | K19 |
| DDR_DQ14 | L19 |
| DDR_DQ15 | L20 |
| DDR_DQ2 | F22 |
| DDR_DQ3 | G22 |
| DDR_DQ4 | D21 |
| DDR_DQ5 | E21 |
| DDR_DQ6 | F20 |
| DDR_DQ7 | H20 |
| DDR_DQ8 | H22 |
| DDR_DQ9 | J22 |
| DDR_DQS0 | G21 |
| DDR_DQS1 | K20 |
| DDR_RAS_N | U19 |
| DDR_S0_N | W22 |
| DDR_S1_N | U20 |
| DDR_SA0 | V21 |
| DDR_SA1 | W21 |
| DDR_SA2 | Y22 |
| DDR_SCL | V19 |
| DDR_SDA | V20 |
| DDR_WE_N | U21 |

**FCRAM Interface**

The LatticeXP FPGA is connected to a single eight-bit FCRAM device. The LatticeXP Advanced Evaluation Board always has a quantity of scratch RAM since the FCRAM memory, unlike the DDR memory, cannot be removed. With the addition of an FCRAM memory controller into the FPGA, the FCRAM memory can be used to store data.

Operation of the FCRAM memory is similar, but not identical to, the DDR memory interface. Like DDR, FCRAM memories depend on a DQS to qualify when data is valid on the bus. This means the DQS hardware built into the LatticeXP can be used to improve data transfer reliability in the same way it is used in DDR.

Visit the Lattice web site at www.latticesemi.com/boards to download a test evaluation package for the FCRAM interface. Refer to Table 16 for a description of the FCRAM connections.

***Table 16. FCRAM Connection Summary***

| Schematic Name | LatticeXP Pin Location |
|---|---|
| FCRAM_PD_N | B6 |
| FC_A0 | A21 |
| FC_A1 | A20 |
| FC_A10 | B14 |
| FC_A11 | C14 |
| FC_A12 | D14 |
| FC_A13 | D13 |
| FC_A14 | C12 |
| FC_A2 | B20 |
| FC_A3 | A19 |
| FC_A4 | B19 |
| FC_A5 | B17 |
| FC_A6 | A15 |
| FC_A7 | B15 |
| FC_A8 | D15 |
| FC_A9 | A14 |
| FC_BA0 | B7 |
| FC_BA1 | C6 |
| FC_CLK | C9 |
| FC_CLK_N | C10 |
| FC_CS_N | B5 |
| FC_DQ0 | C7 |
| FC_DQ1 | B8 |
| FC_DQ2 | C8 |
| FC_DQ3 | A9 |
| FC_DQ4 | D11 |
| FC_DQ5 | B10 |
| FC_DQ6 | A11 |
| FC_DQ7 | B11 |
| FC_DQS | B9 |
| FC_FN | A5 |

## Ordering Information

| Description | Ordering Part Number | China RoHS Environment-Friendly Use Period (EFUP) |
|---|---|---|
| LatticeXP10C Evaluation Board - Advanced | LFXP10C-H-EV |  |

## Technical Support Assistance

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| July 2005 | 01.0 | Initial release. |
| March 2007 | 01.1 | Added Ordering Information section. |
| April 2007 | 01.2 | Added important information for proper connection of ispDOWNLOAD (Programming) Cables. |
| September 2009 | 01.3 | |

# Appendix A. Schematics

***Figure 9. 32-Bit PCI***

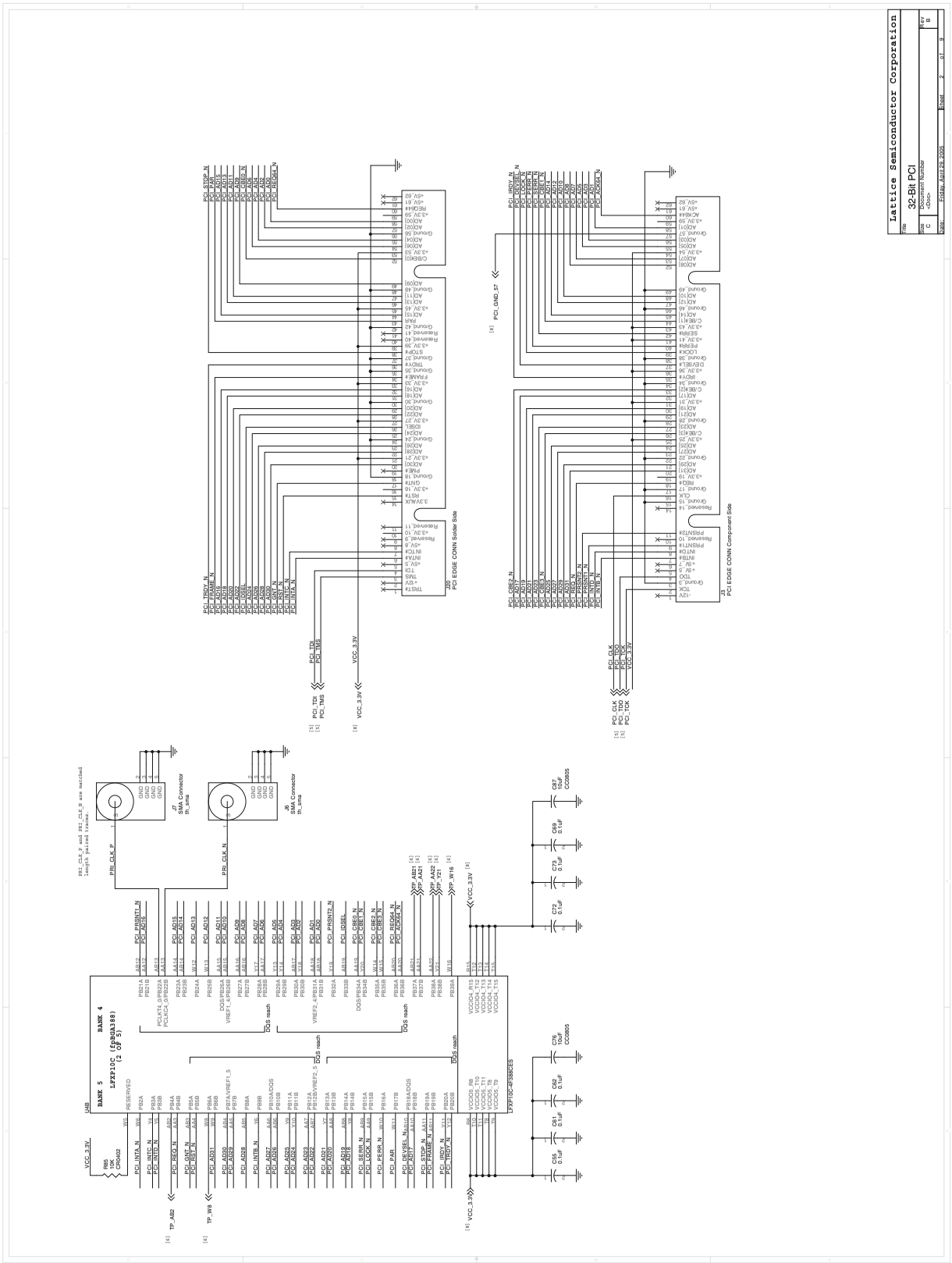

***Figure 10. DDR SDRAM***

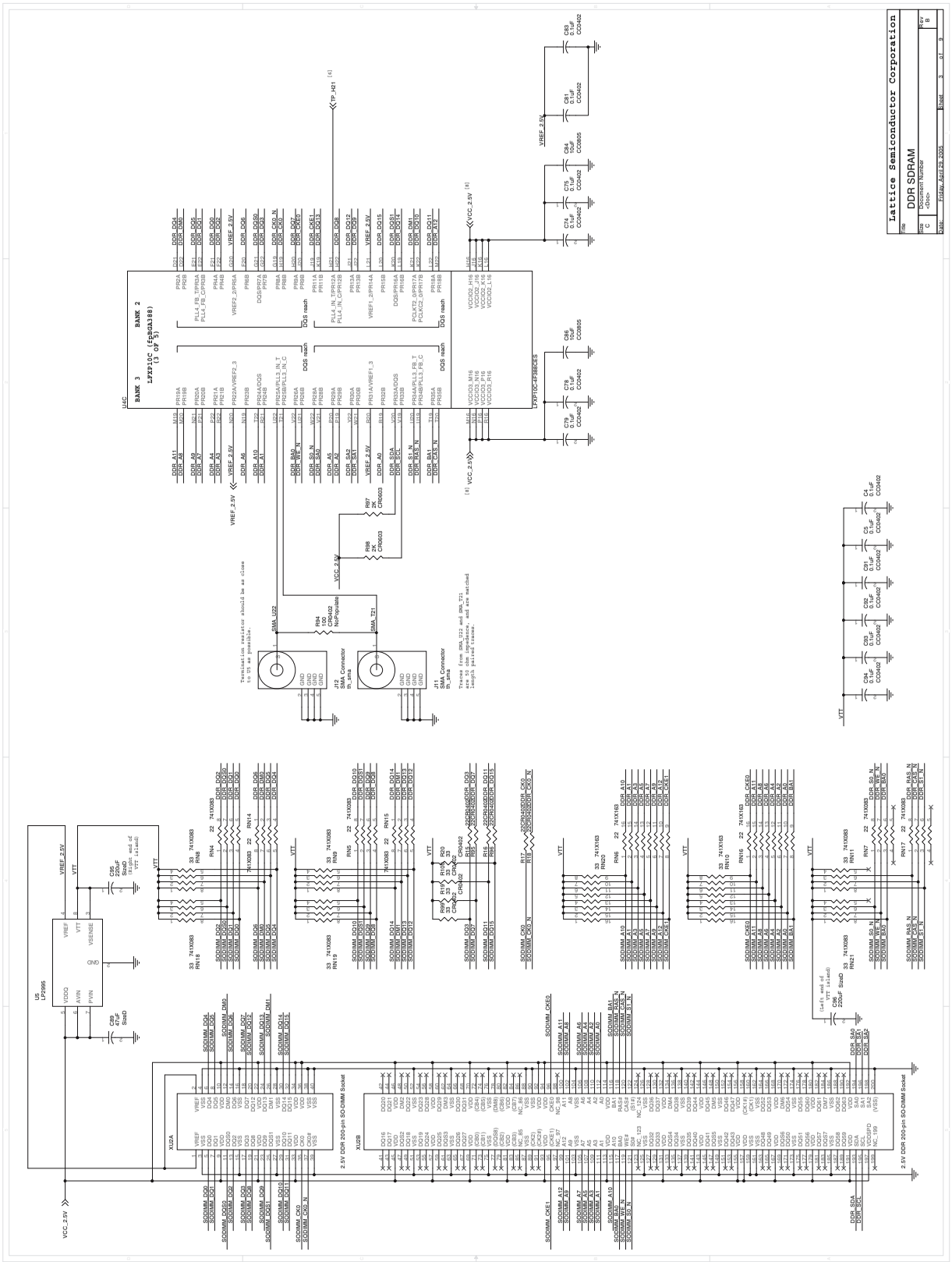

***Figure 11. FCRAM***

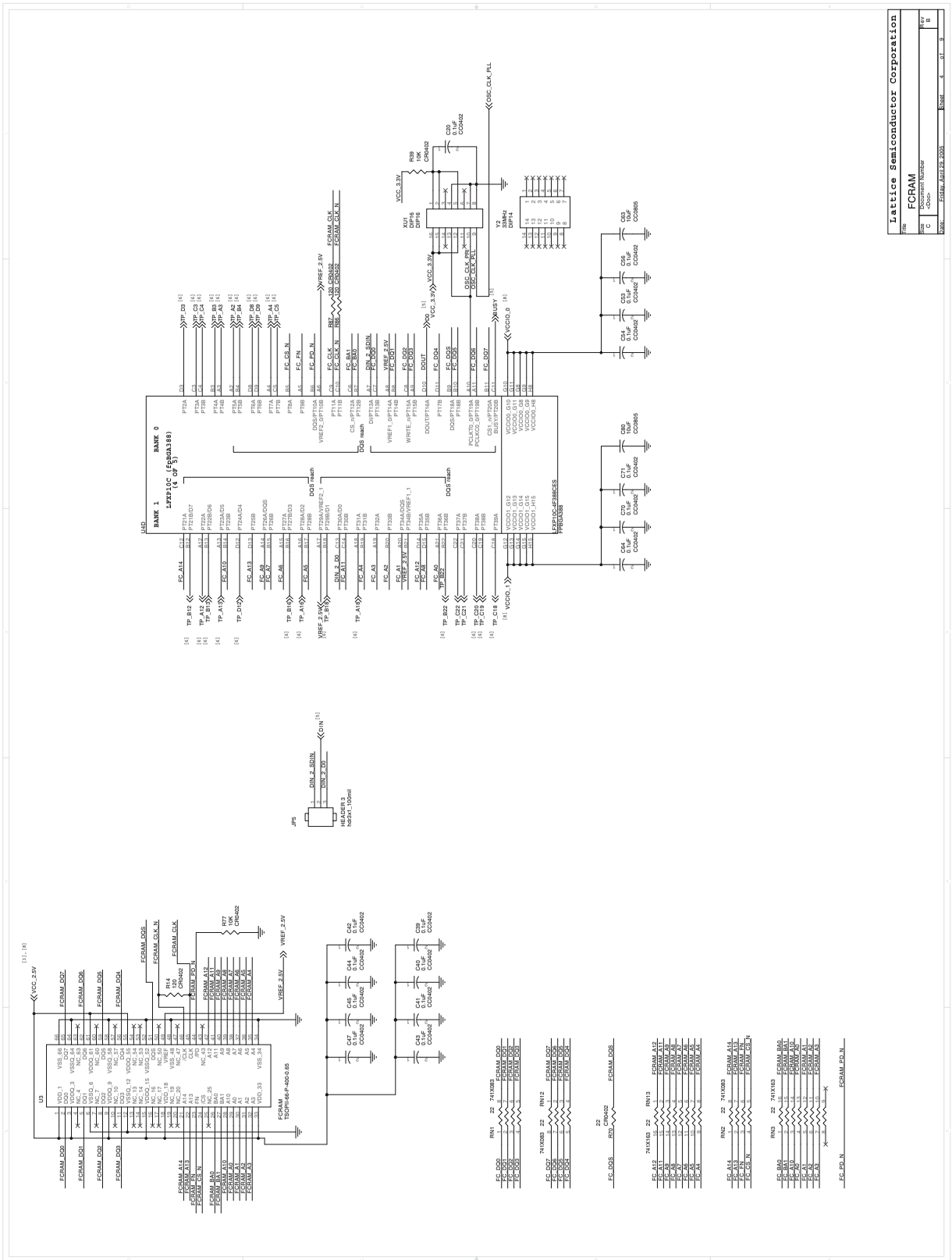

***Figure 12. JTAG and FPGA Programming***

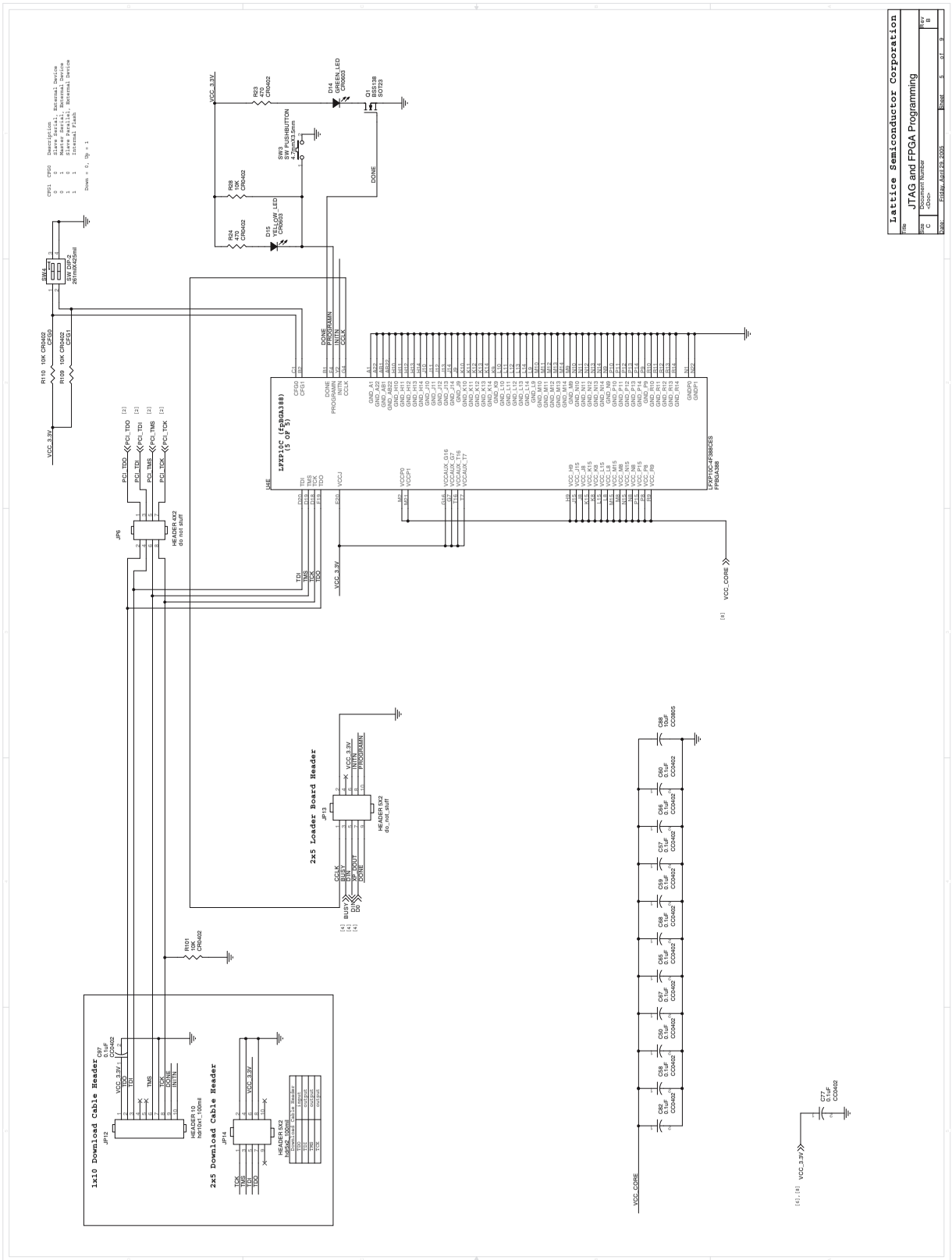

***Figure 13. Ethernet PHY***