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LatticeXP™ Standard Evaluation Board

User's Guide

June 2008
EB12_02.4

Introduction

The LatticeXP Standard Evaluation Board provides a convenient platform to evaluate, test and debug user designs. The board consists of a LatticeXP-10 FPGA in a 256 fpBGA package, power input jacks, a clock oscillator (33MHz) and I/O connections. The LatticeXP I/Os are connected to a rich variety of interfaces including switches (momentary and ON/OFF), LEDs, SMA pads, RJ45, 0.10" headers and PCB test points.

The information in this document pertains to boards marked as 'Rev. A' and 'Rev. B'. This marking is located on the front of the board, beneath the Lattice logo. Any information that only applies to either the 'Rev. A' or 'Rev.B' board will be explicitly stated as such.

Features

Included

- LatticeXP FPGA: LFXP10C-5F256C or LFXP10E-5F256C
- On-board power supply (rev. B only)
- Prototyping area
- 188 user I/Os, grouped in eight I/O banks
- Independent voltage control for core, I/O and clock voltages
- 33MHz on-board oscillator
- Status LEDs, input switches
- Lattice ispDOWNLOAD cable
- AC adapter (rev. B only)

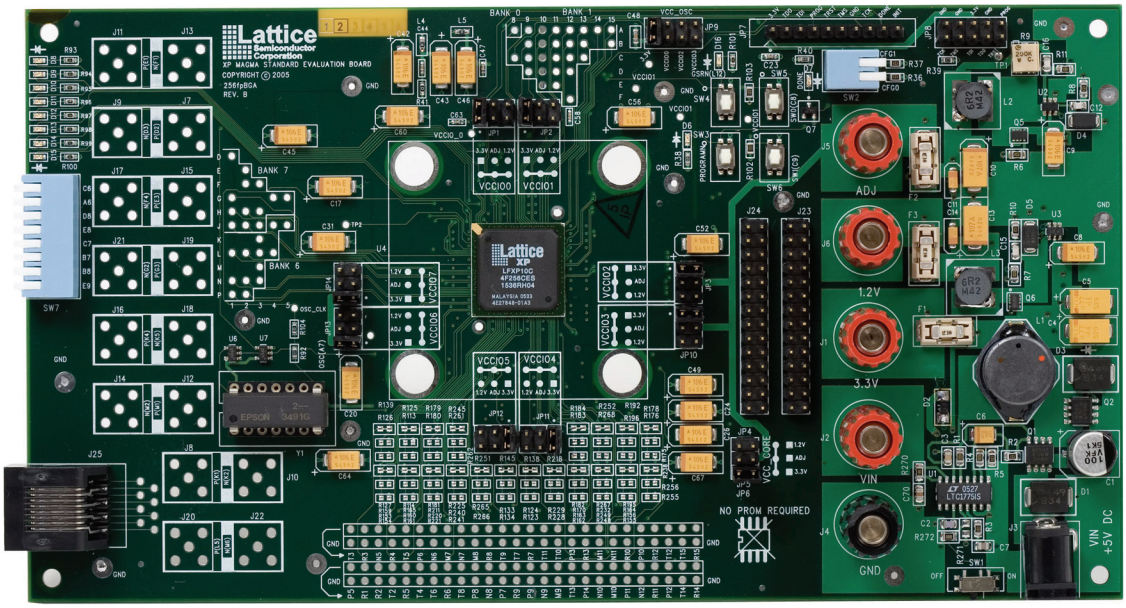
Optional

- Optional SMA connectors (up to 16) for high-speed clock and data interfacing. The board includes pads for these connectors. The SMA connectors must be procured and installed separately by the user.

Software Support

- To target your HDL design to the LatticeXP device, use the ispLEVER® design software. You can learn more about ispLEVER on the Lattice web site at: www.latticesemi.com/software.
- To download your program to the LatticeXP device, use the ispVM® System software. ispVM System can be downloaded from the Lattice web site at: www.latticesemi.com/ispvm.
- ispTRACY™ in-system logic analysis support (ispTRACY is included with the ispLEVER design software)

Figure 1. LatticeXP Standard Evaluation Board



Electrical, Mechanical and Environmental Specifications

The nominal board dimensions are 7 inches by 3.9 inches. The environmental specifications are as follows:

- Operating temperature: 0ºC to 55ºC
- Storage temperature: -40ºC to 75ºC
- Humidity: < 95% without condensation
- VDC input (+/- 10%) up to 4A

Additional Resources

Additional resources related to this board can be downloaded from the web at www.latticesemi.com/boards. Click on the appropriate evaluation board, then follow the appropriate links for items such as updated documentation, software, sample designs, IP evaluation bitstreams, and more.

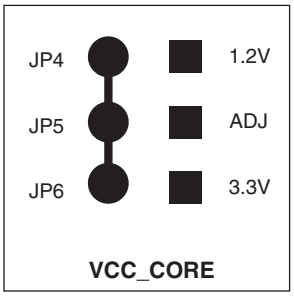
LatticeXP Device

This board features a LatticeXP FPGA with either a 3.3V or a 1.2V DC core. The board is populated with a LatticeXP-10 device in plastic 256-ball fpBGA (1mm pitch) package. Density migration is possible for Lattice XP devices in the 256 fpBGA package. A complete description of this device can be found in the LatticeXP Family Data Sheet on the Lattice web site at www.latticesemi.com.

Device Core and I/O Voltage

Boards shipping with a 3.3V DC core device will allow operation of the core between 1.8V and 3.3V DC. Jumpers (JP4, JP5 and JP6) are available to switch between 3.3V, 1.2V and an adjustable supply between the other two voltages. Boards shipping with a 1.2V core device will not have headers installed for core voltage selection. JP4 will be shorted on the board. Figure 2 shows the core voltage selection jumpers.

Figure 2. Core Voltage Select Jumpers



The LatticeXP device has eight sysIO™ buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (VCCIO) and two voltage reference resources, VREF1 and VREF2, that allow each bank to be completely independent from the others.

Please refer to the LatticeXP Family Data Sheet for additional information about supported I/O standards. This data sheet can be downloaded from www.latticesemi.com.

The LatticeXP Standard Evaluation Board provides individual control of each I/O bank capable of supporting VCCIO between 1.2V and 3.3V. The board provides jumper blocks which allow the end user to select 1.2V, 3.3V or an adjustable voltage between these two voltages. Figure 3 shows a typical layout for a VCCIO select jumper block. Table 1 details the VCCIO bank selection connectors.

Figure 3. VCCIO Jumper Block

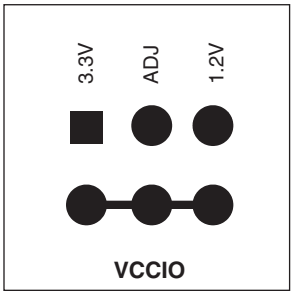


Table 1. VCCIO Connectors

VCCIO Bank	Connector Number
VCCIO0	JP1
VCCIO1	JP2
VCCIO2	JP3
VCCIO3	JP10
VCCIO4	JP11
VCCIO5	JP12
VCCIO6	JP13
VCCIO7	JP14

Device Clocks

The LatticeXP Standard Evaluation Board provides a variety of ways to input clock signals to the LatticeXP device. These include an on-board crystal oscillator, SMA connectors and 0.1" header pins. Clock inputs connect to pri-

mary clock inputs and device PLL inputs. Clock outputs connect to PLL outputs and external feedback pins. Table describes the clock connections to the LatticeXP device.

Table 2. Lattice XP-10 Clock Pins and Connections

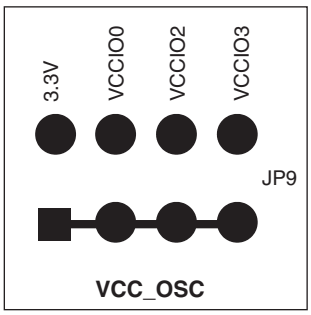
XP-10 Pin Number	XP Pin Label	PCB Connection[1]	On-Board OSC. Resistor[2]	Buffered (Y/N)[3]
N16	RLM0_PLLT_IN_A	J23-15	R89	Y
M16	RLM0_PLLC_IN_A	J23-16	N/A	N
L13	RLM0_PLLT_OUT_A	J23-9	N/A	N
M14	RLM0_PLLC_OUT_A	J23-10	N/A	N
N15	RLM0_PLLT_FB_A	J23-17	N/A	N
P15	RLM0_PLLC_FB_A	J23-18	N/A	N
F16	RUM0_PLLT_IN_A	J24-7	R90	Y
G16	RUM0_PLLC_IN_A	J24-8	N/A	N
F13	RUM0_PLLT_OUT_A	J24-17	N/A	N
G12	RUM0_PLLC_OUT_A	J24-18	N/A	N
C15	RUM0_PLLT_FB_A	J24-3	N/A	N
D15	RUM0_PLLC_FB_A	J-24-4	N/A	N
M1	LLM0_PLLT_IN_A	SMA J12	N/A	N
M2	LLM0_PLLC_IN_A	SMA J14	N/A	N
K4	LLM0_PLLT_OUT_A	SMA J16	N/A	N
K5	LLM0_PLLC_OUT_A	SMA J18	N/A	N
L5	LLM0_PLLT_FB_A	SMA J20	N/A	N
M6	LLM0_PLLC_FB_A	SMA J22	N/A	N
G3	LUM0_PLLT_IN_A	SMA J19	N/A	N
G2	LUM0_PLLC_IN_A	SMA J21	N/A	N
E3	LUM0_PLLT_OUT_A	SMA J15	N/A	N
F4	LUM0_PLLC_OUT_A	SMA J17	N/A	N
D2	LUM0_PLLT_FB_A	SMA J7	N/A	N
D3	LUM0_PLLC_FB_A	SMA J9	N/A	N
A7	PCLKT0_0	OSC	R104	N
A8	PCLKC0_0	Test Point	N/A	N
H16	PCLKT2_0	J24-9	N/A	N
J16	PCLKC2_0	J24-10	N/A	N
T10	PCLKT4_0	Test Pad	N/A	N
T11	PCLKC4_0	Test Pad	N/A	N
K1	PCLKT6_0	SMA J8	N/A	N
K2	PCLKC6_0	SMA J10	N/A	N

1. Check the schematic pages for termination resistors connected to these pins.
2. 0_ resistor connecting to on-board oscillator.
3. Indicates a non-inverting buffer between the oscillator and pin.

The oscillator socket accepts both full-size and half-size oscillators and can route to different clock inputs, depending on installation of several 0Ω resistors. The oscillator has a 22Ω series termination resistor at the oscillator output. These inputs correspond with PCLKT0, RLM0_PLLT_IN_A and RUM0_PLLT_IN_A. The oscillator supply voltage is changeable, via the VCC_OSC header, located at JP9. The onboard oscillator operates at 3.3V. It is possible to power this socket from the following supplies: 3.3V, VCCIO0, VCCIO2 or VCCIO3, depending on the I/O bank being used and the operating conditions for the chosen oscillator.

Figure 4 shows the layout and connections for JP9. There is also an optional 10K pull-up (R91) connect to pins 1 and 4 of the oscillator socket, in the event a oscillator with enable is required. The oscillator is also connected to J24-26, for use as a clock input to a logic analyzer.

Figure 4. VCC_OSC Jumper Block



Device I/O Banks 0 and 1

I/O banks 0 and 1 represent general purpose I/O banks, which connect to a combination of test pads, switches, LEDs and an RJ45 connector. The switches consist of two user defined push-button switches and an 8-position DIP switch. Both types of switches are pulled up to the associated VCCIO voltage with 10KΩ resistors and connected to GND when activated (pushed or levered in the down position). LEDs are active (lit) when the device I/O is low. The RJ-45 connector is connected using paired I/O connections. Table 3 details the I/O banks 0 and 1 connections. Unlisted pins in banks 0 and 1are connected to test pads on the board.

Table 3. Banks 0 and 1 I/O Connections

I/O Bank	XP-10 Pin Number	Connection
0	C5	LED D8
0	F5	LED D9
0	B1	LED D10
0	A2	LED D11
0	B2	LED D12
0	B3	LED D13
0	A3	LED D14
0	D5	LED D15
0	D6	RJ-45 J25-1
0	E6	RJ-45 J25-2
0	B6	RJ-45 J25-3
0	A4	RJ-45 J25-4
0	B5	RJ-45 J25-5
0	A5	RJ-45 J25-6
0	D7	RJ-45 J25-7
0	E7	RJ-45 J25-8
0	C6	Switch SW7 1
0	A6	Switch SW7 2
0	D8	Switch SW7 3
0	E8	Switch SW7 4
0	C7	Switch SW7 5
0	B7	Switch SW7 6
0	B8	Switch SW7 7
0	E9	Switch SW7 8
1	C8	Pushbutton SW0
1	C9	Pushbutton SW1

Device I/O Banks 2 and 3

I/O banks 2 and 3 contain general purpose I/Os with LVDS transmit/receive pairs. These I/O pairs are connected to two 0.1" headers suitable for connecting to a logic analyzer or ribbon cable. Table 4 details the I/O banks 2 and 3 connections.

Table 4. Banks 2 and 3 I/O Connections

I/O Bank	LatticeXP-10 Pin Number		Connection	
	Positive	Negative[1]	Positive	Negative[1]
2	C15	D15	J24-3	J24-4
2	E14	F14	J24-1	J24-2
2	E15	F15	J24-19	J24-20
2	C16	B16	J24-5	J24-6
2	F13	G12	J24-17	J24-18
2	F16	G16	J24-7	J24-8
2	G14	G15	J24-13	J24-14
2	H14	H15	J24-21	J24-22
2	H12	H13	J24-15	J24-16
2	H16	J16	J24-9	J24-10
2	G13		J24-25	
3	J14	J15	J23-1	J23-2
3	K16	L16	J23-3	J23-4
3	K13	K12	J23-13	J23-14
3	K15	K14	J23-5	J23-6
3	N16	M16	J23-15	J23-16
3	L14	L15	J23-7	J23-8
3	L13	M14	J23-9	J23-10
3	N14	M15	J23-21	J23-22
3	R16	P16	J23-19	J23-20
3	N15	P15	J23-17	J23-18
3	L12		SW4	

1. Blank cell indicated pin with no negative paired pin.

Each I/O pair is connected to a resistor termination network, and the trace lengths are matched. Figure 5 shows the termination network for these differential pairs. These resistors are not installed, and the series resistors use a trace between the resistor pads. This trace can be cut to allow the installation of a series termination resistor. The series resistors are 0805 size and the parallel resistors are 0603 size. Figure 5 shows this trace in relation to the resistor pads.

Figure 5. Differential I/O Termination Network

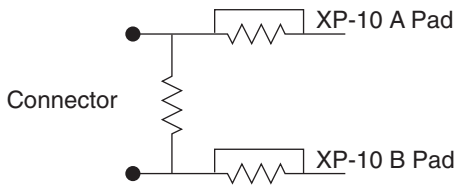
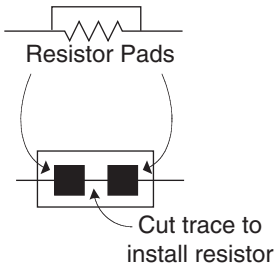


Figure 6. Close-up of Series/Passthrough



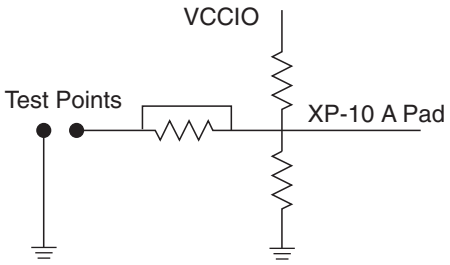
Device I/O Banks 4 and 5

I/O banks 4 and 5 consist of general purpose I/O pins. These pins connect to test pads on the board. The test pads are paired with a ground pad, which are spaced on 0.1" centers. In addition to the test pads, these I/O banks are connected to a pull-up, pull-down and series resistor network. The resistor network is not populated. The series resistors are 0805 size, and the pull-up/pull-down resistors are 0603 size. Figure 7 shows the schematic for the individual I/O termination network.

Table 5. Banks 4 and 5 I/O Connections

Position	Pin Number	GND Row	Pin Number	GND Row
1	T3	GND	P5	GND
2	R3	GND	R1	GND
3	N5	GND	R2	GND
4	R4	GND	T2	GND
5	T5	GND	R5	GND
6	P6	GND	T4	GND
7	N6	GND	T6	GND
8	M7	GND	R6	GND
9	N7	GND	T8	GND
10	M8	GND	P8	GND
11	R8	GND	N8	GND
12	T9	GND	P7	GND
13	T7	GND	R9	GND
14	R7	GND	P9	GND
15	T11	GND	N9	GND
16	T10	GND	M9	GND
17	P13	GND	T13	GND
18	R13	GND	P14	GND
19	M11	GND	N10	GND
20	N11	GND	M10	GND
21	R10	GND	P11	GND
22	P10	GND	N12	GND
23	R12	GND	R11	GND
24	T12	GND	P12	GND
25	T15	GND	T14	GND
26	R15	GND	R14	GND

Figure 7. Banks 4 and 5 I/O Termination Network



Device I/O Banks 6 and 7

I/O banks 6 and 7 contain general purpose I/Os with LVDS transmit/receive pairs. The I/O pairs in these banks have been routed to test pads on the PCB and eight pairs have been routed to SMA connectors. Table 6 details the I/O bank 6 and 7 SMA connections. Unlisted pins are connected to test pads on the board.

Table 6. Bank 6 and 7 I/O Connections

I/O Bank	LatticeXP-10 Pin Number		SMA Connection	
	Positive	Negative[1]	Positive	Negative[1]
6	K1	K2	J8	J10
6	M1	M2	J12	J14
6	K4	K5	J16	J18
6	L5	M6	J20	J22
7	D2	D3	J7	J9
7	E1	F1	J11	J13
7	E3	F4	J15	J17
7	G3	G2	J19	J21

Pairs routed to SMA connectors are connected with series and parallel termination resistors, similar to the network shown in Figure 5 (see Bank 2 and 3 description). The SMA connectors are not included with the LatticeXP-Standard board, and must be procured and installed separately. AMP SMA connector 221780-1 or similar is recommended.

Programming Headers

Two programming headers are provided on the evaluation board, providing access to the LatticeXP JTAG port. Both 1x10 and 2x5 formats are available for compatibility with all Lattice ispDOWNLOAD® cables. The pinouts for the headers are provided in Tables 6 and 7.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeXP FPGA device and render the board inoperable.*

Table 7. JTAG Programming Headers Function JP8 (2x5)

JTAG Programming Function	JP8 Pin Number (2x5)
TCK	1
GND	2
TMS	3
GND	4
TDI	5
VCC (3.3V)	6
TDO	7
GND	8
TRST	9
PROGRAM	10

Table 8. JTAG Programming Headers Function JP7 (1x10)

JTAG Programming Function	JP7 Pin Number (1x10)
VCC (3.3V)	1
TDO	2
TDI	3
PROGRAM	4
TRST	5
TMS	6
GND	7
TCK	8
DONE	9
INIT	10

Power Supply

Power can be supplied to the LatticeXP Standard Evaluation Board via the banana jacks (J1, 2, 5, 6 – all PCB revisions), or a coaxial DC connector (J3 – Rev. B PCB only), which receive power from either a bench power supply or a brick style power supply.

[Rev. B Only] The output from the DC system is controlled by switch SW1. This is a small surface mount switch that enables and disables the LTC1775 DC-DC conversion chip. The output voltages from the power supply are enabled when the switch is in the left position.

[Rev. B Only] The 5.0V to 28.0V DC input voltage (input to either J2 or J3) is converted by DC-DC converters and switching power supplies to provide 3.3V, 1.2V, and an adjustable DC source on the board. The output from these

supplies travels through surface mounted fuse holders. Fuses are supplied and prevent over-current conditions from damaging the components on the board (vendor: Littlefuse, make: Nano SMF Very Fast Acting, 1.5A or 3A).

Both Rev. A and Rev. B boards may be supplied with DC voltage through the banana plug connector. On both boards, J4 is the GROUND connection point, J1 is the +3.3V input, J6 is the +1.2V input and J5 is the input for the Adjustable rail. J2 connects to the VIN input of the on-board power supply of the Rev. B board. J2 is unconnected on the Rev. A board. To directly connect power to the banana jacks on the Rev. B board, the SMT fuses must be removed. SMT fuses are not installed on Rev. A boards.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeXP10C Evaluation Board - Standard (upper voltage)	LFXP10C-L-EV	
LatticeXP10C Evaluation Board - Standard (lower voltage)	LFXP10E-L-EV	
ispLEVER Base with LatticeXP10 Standard Development Kit	LS-XP10-BASE-PC-N	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
August 2006	02.1	Changes to I/O Bank column of Bank 6 and 7 I/O Connections table.
March 2007	02.2	Added Ordering Information section.
April 2007	02.3	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.
June 2008	02.4	Updated schematic.

Appendix A. Schematic

Figure 8. LatticeXP Evaluation Board

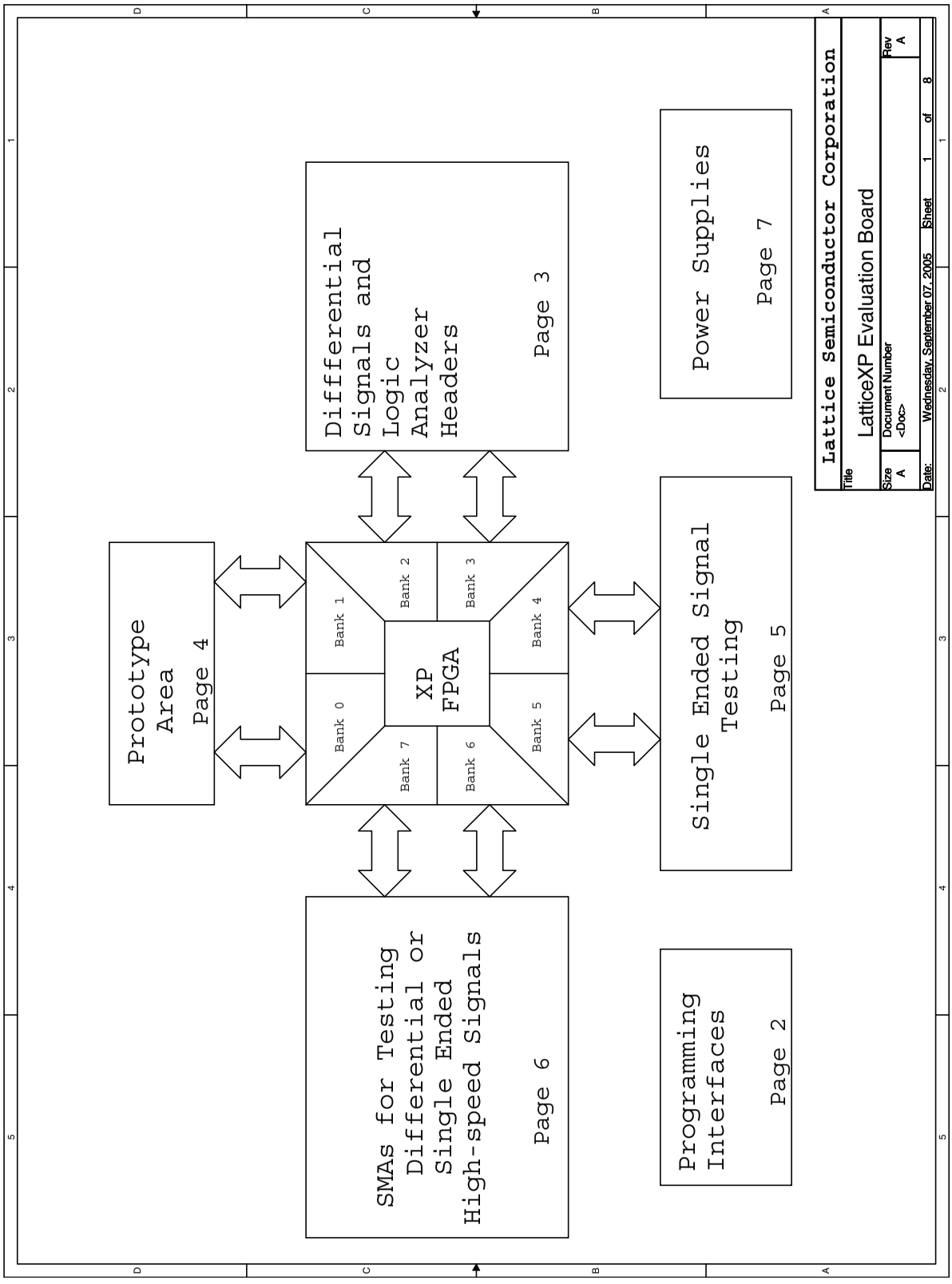


Figure 9. JTAG and FPGA Programming

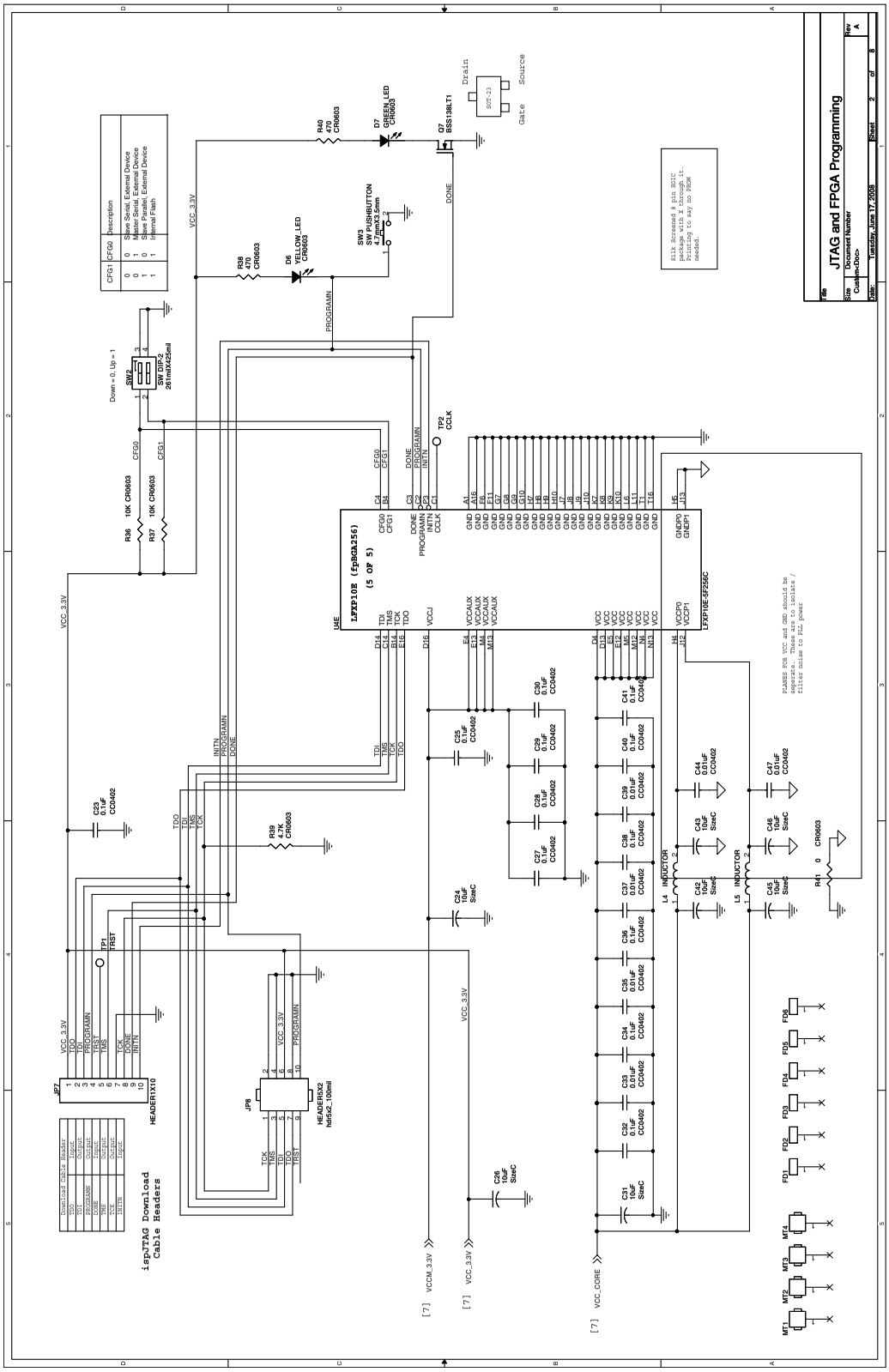


Figure 10. Banks 3 and 4

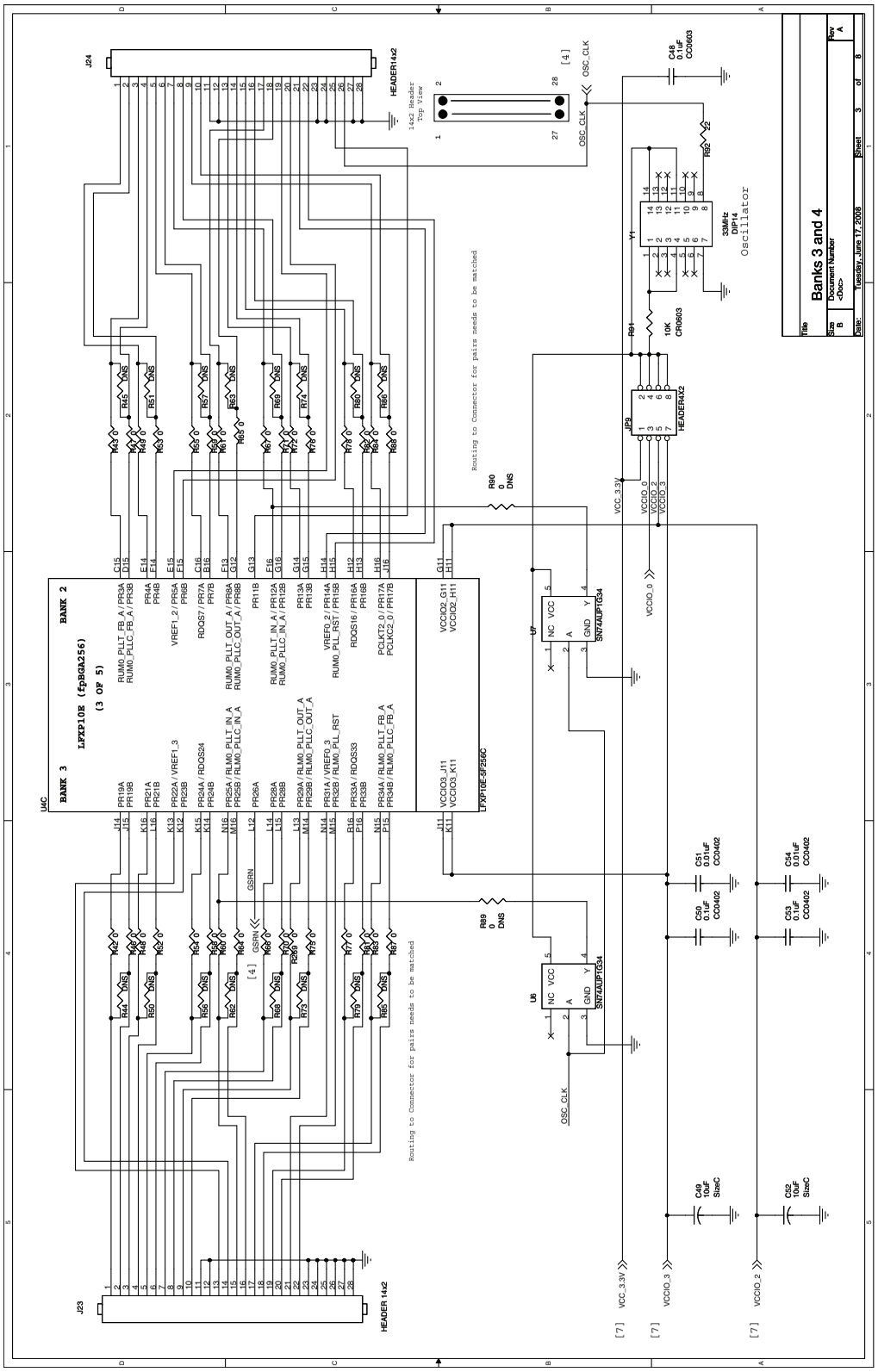


Figure 11. Banks 0 and 1

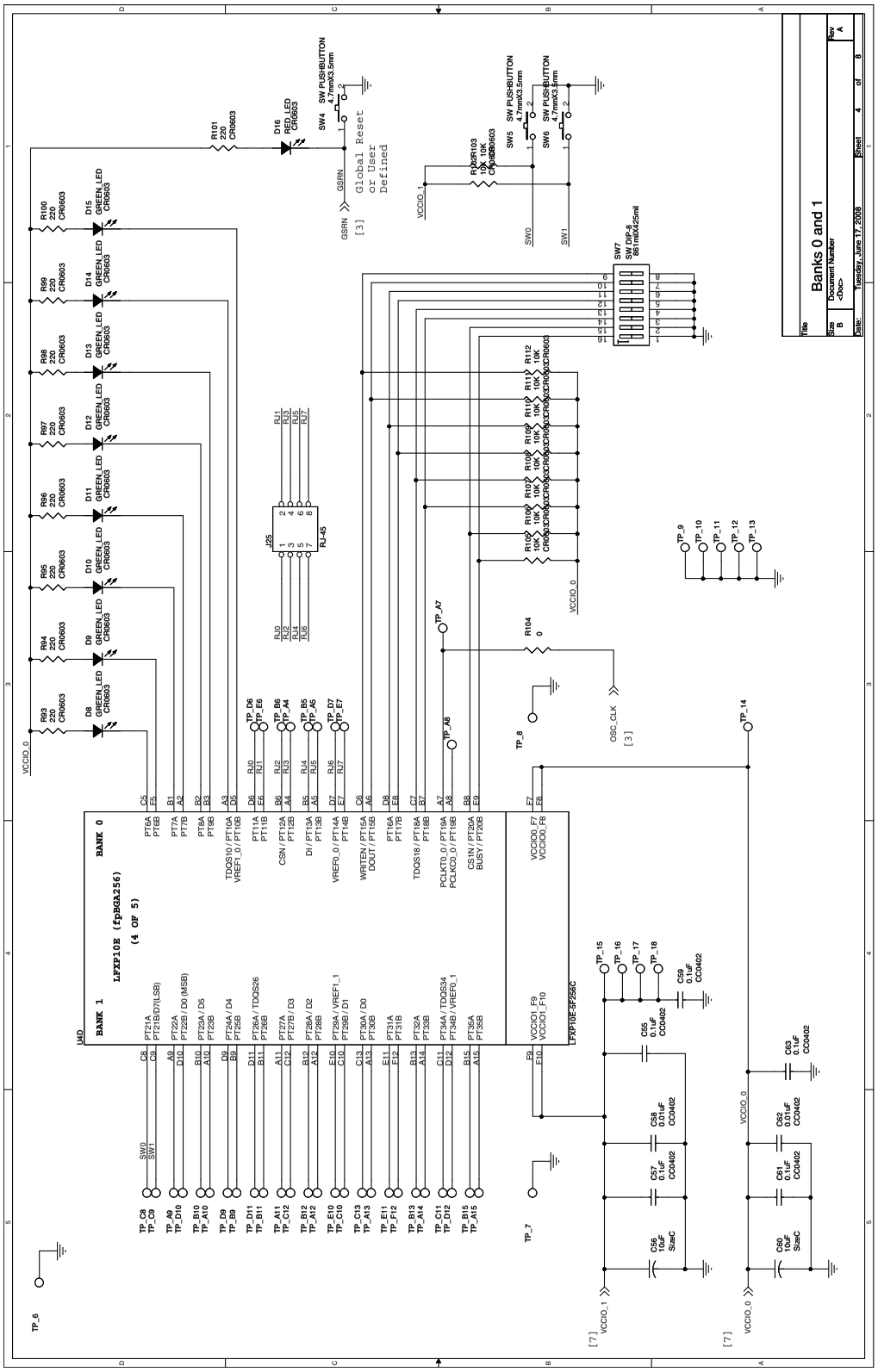


Figure 12. Banks 4 and 5

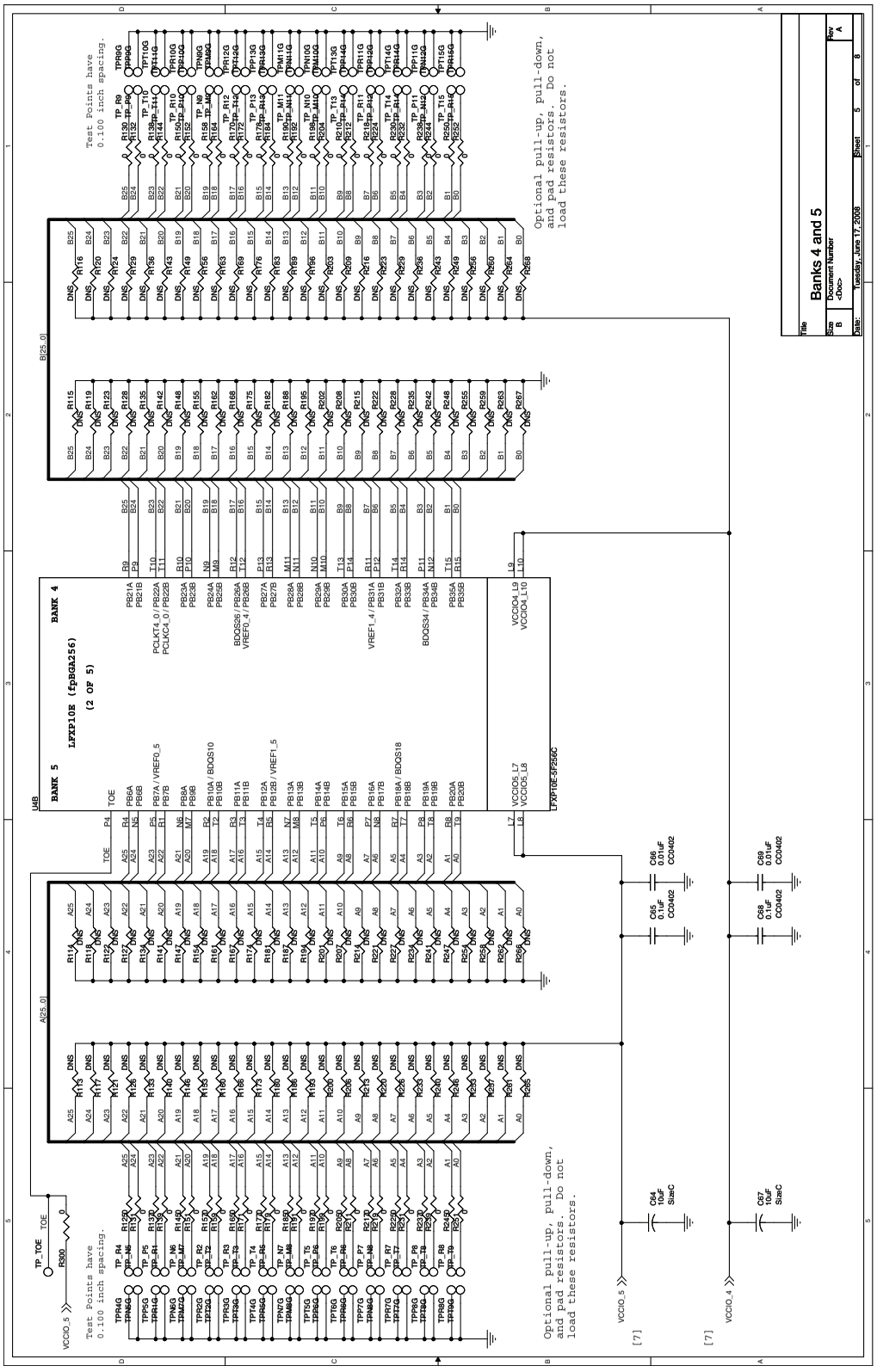


Figure 13. Banks 6 and 7

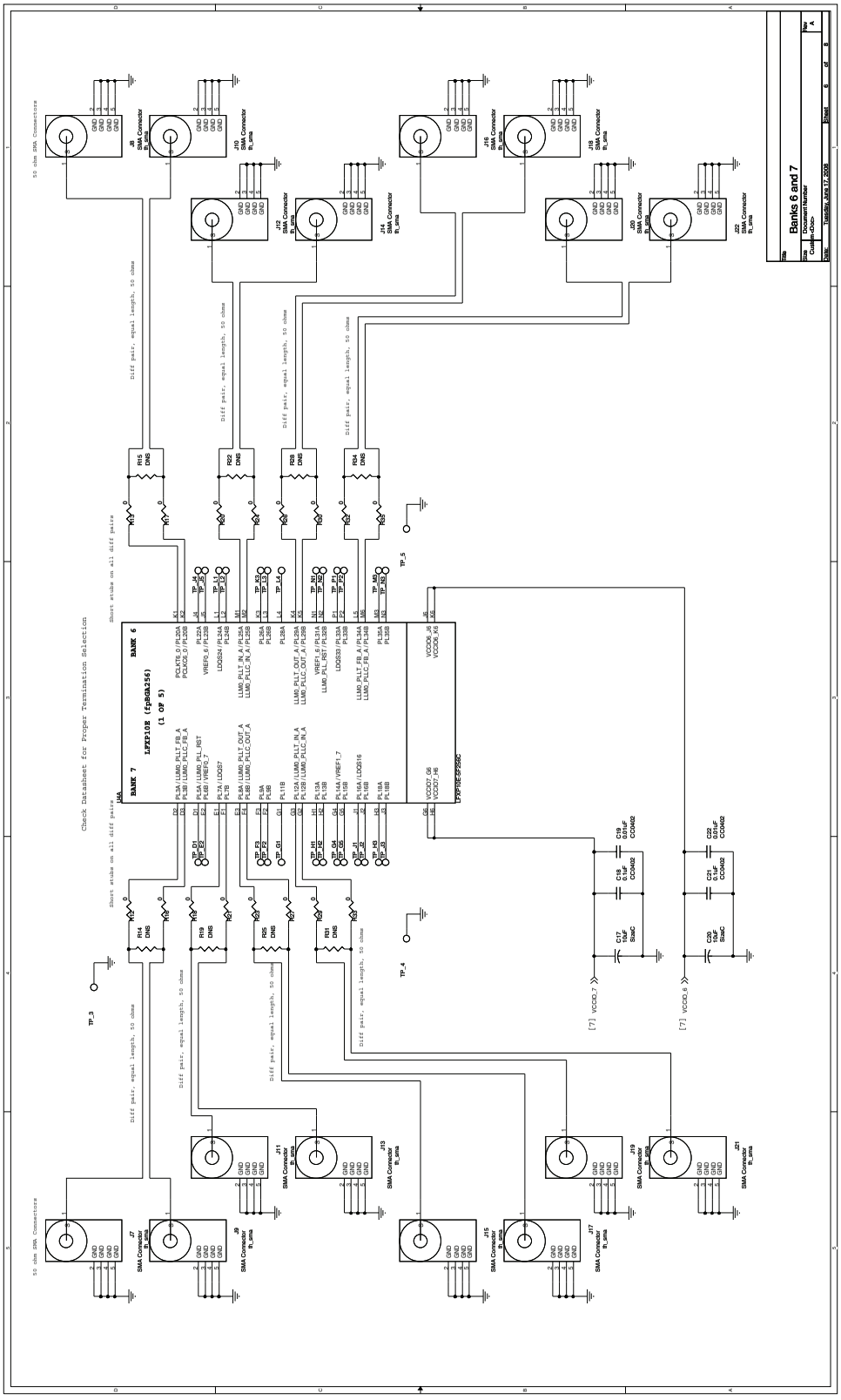


Figure 14. Power

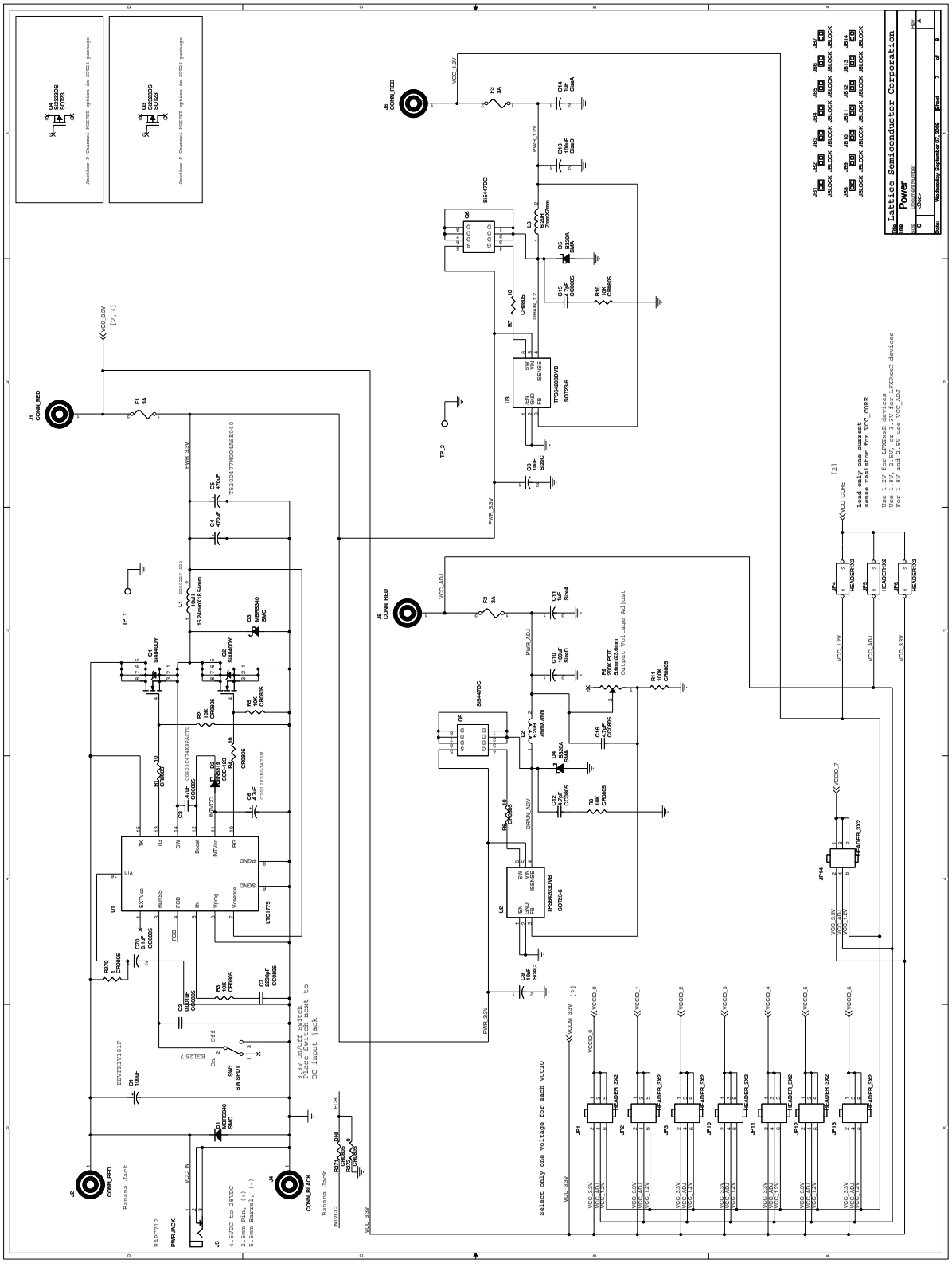


Figure 15. Mechanical Drawing