Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LatticeXP2 Advanced Evaluation Board

User's Guide

March 2011
Revision: EB30_01.5

Introduction

The LatticeXP2™ Advanced Evaluation Board provides a convenient platform to evaluate, test and debug user designs and IP cores targeted for the LatticeXP2-17 FPGA. The board features of a LatticeXP2-17 FPGA in a 484 fpBGA package. The LatticeXP2 I/Os are connected to a rich variety of both generic and application-specific interfaces described later in this document.

Important: This document (including the schematics in the appendix) describes LatticeXP2 Advanced Evaluation Boards marked as Rev B. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo.

The LatticeXP2 is a second-generation non-volatile FPGA device. It combines a Look-up Table (LUT) based FPGA fabric with Flash non-volatile cells in a flexiFLASH™ architecture. The flexiFLASH approach provides benefits such as instant-on, small footprint, on chip storage with FlashBAK™ embedded block memories and Serial TAG memory and design security. The LatticeXP2 also support live updates with TransFR™, 128-bit AES encryption and dual-boot technologies. The LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O and enhanced sysDSP™ blocks.

For a full description of the LatticeXP2 FPGA, see the Lattice website for data sheets, technical notes, technology summaries and more: www.latticesemi.com.

Some common uses for the LatticeXP2 Advanced Evaluation Board include:

- Video and other DSP processing
- An analog-to-digital, and digital-to-analog mixed signal source/sink
- A single-board computer system
- A platform for evaluating the Input/Output (I/O) characteristics of the FPGA
- A platform for evaluation and development with Lattice IP cores

Features

Key features of the LatticeXP2 Advanced Evaluation Board include:

- SPI Serial Flash device included for low-cost, non-volatile configuration storage
- One 32-bit DDR2 SO-DIMM module connector
- 32-bit PCI connector
- Both a Tri-speed (10/100/1000 Mbit) Ethernet PHY that includes RJ-45, magnetics and spark gap, as well as a directly wired RJ-45 connector
- RS-232 interface chip and 9-pin D-sub connector
- PS/2 Mouse connector
- USB 1.1 transceiver and USB type-A and type-B connectors
- USB download of LatticeXP2 and power manager bitstreams
- Video TX and RX MDR connectors
- Quad 12-bit ADC and Quad 12-bit DAC
- Two 8-pin DIP switches
- Discrete LEDs and 7-segment LED
- CompactFlash connector for type I and type II CompactFlash cards
- LCD module connector

- Prototyping areas with access to 14 I/O pins
- Selectable I/O bank voltages
- Four pairs of SMA connectors for high speed differential signals
- Oscillator socket for both half-size and full-size oscillators
- 3.3V, 2.5V, 1.8V, 1.2V and ADJ (adjustable voltage) powers generated from a single 5V to 28V power source
- ispPAC®-POWR1220AT8 Power Manager II device for monitoring the 3.3V, 2.5V, 1.8V, 1.2V, ADJ voltages and DDR Vref, Vtt voltages
- ispVM® System programming support

General Description

The heart of the board is the LatticeXP2 non-volatile FPGA. The board also provides several different interconnections and support devices that permit it to be used for a variety of purposes. The PCI connector, DDR2 socket, and Tri-speed Ethernet PHY are useful for applications using Lattice IP cores.

A number of connectors are useful for general purpose of the LatticeXP2 I/O capability. These include the SMA connectors, RS-232, Video Tx/Rx MDR connectors, and the various generic prototype access points.

The CompactFlash connector is also useful for expansion purposes. It provides the ability to add storage, or communication capabilities to the board.

Other features on the board help in evaluating the capabilities and performance of the LatticeXP2. The A/D, D/A, and digital potentiometer are helpful for some basic mixed signal applications. The SMA connectors permit the evaluation of high-speed differential signals, and protocols. The SPI memory showcases the failsafe capabilities of the LatticeXP2.

The board also acts as a showcase for the ispPAC-POWR1220 power manager. The ispPAC-POWR1220 is a programmable device useful for safely managing the power supply system on the board. While the LatticeXP2 device has no specific power-sequencing requirements, the ispPAC-POWR1220 device can be used to sequence and monitor voltages.

Additional Resources

Additional resources for the LatticeXP2 Advanced Evaluation Board, such as updates to this document, sample programs and links to demos can be found on the Lattice web site. Go to www.latticesemi.com/boards, and navigate to the appropriate page for this board.

Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the board can be damaged by improper handling.

The devices on the evaluation board contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static sensitive to conditions that exceed their designed in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation board when it is removed from the static shielding bag. If you will not be using the board for a

while, it's best to put it back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the board when it is not in use.

When reaching for the board, it is recommended that you first touch the outside threaded portion of one of the gold SMA connectors. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: to minimize the possibility of ESD damage, the first and last electrical connection to the board, should always be from test equipment chassis ground to GND on the board (black banana jack).

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the GND on the board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged, should be the chassis GND connection to eval board GND. If you have signal sources that are floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board while it's not in a static shielding bag, please keep one finger on the threaded portion of one of the gold SMA connectors. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

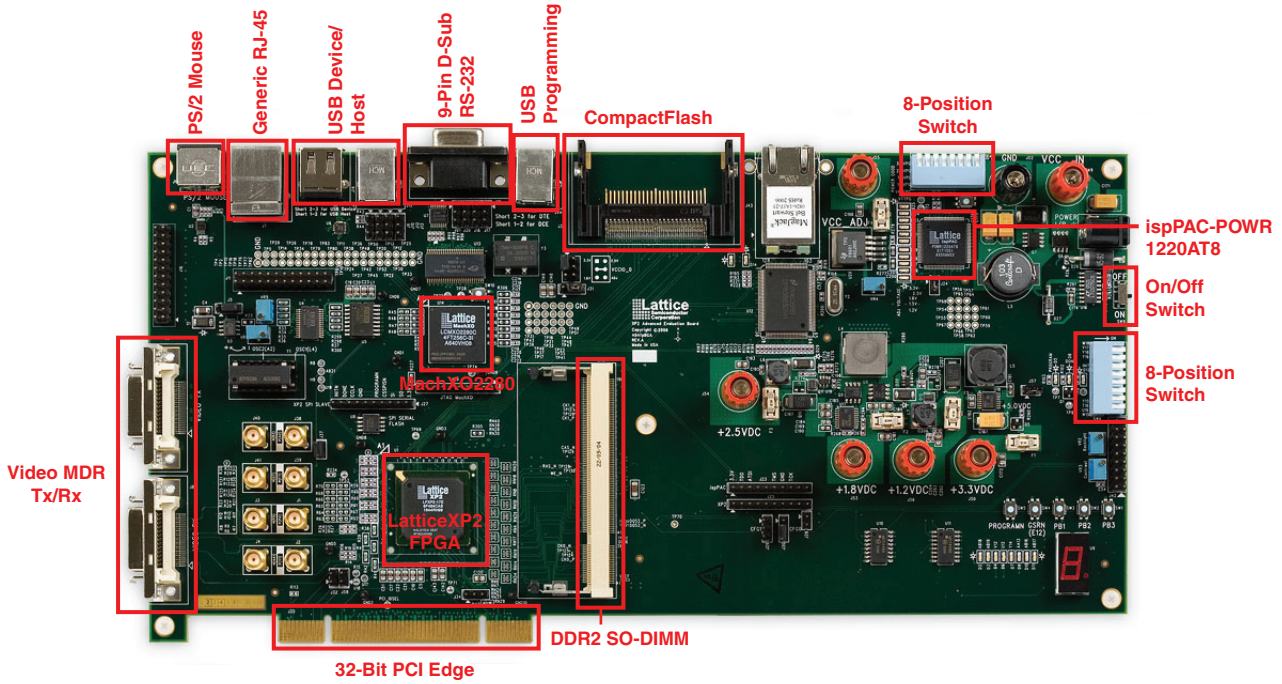
Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 12 inches by 6 inches. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: <95% without condensation
- 5V to 28V DC (20 watts max.)

Functional Description

Figure 1. LatticeXP2 Advanced Evaluation Board



LatticeXP2 Device

This board features a LatticeXP2 FPGA with a 1.2V DC core in a 484-ball fpBGA package. The default device is the LatticeXP2-17. Any other LatticeXP2 density in this package can be accommodated. A complete description of this device can be found on the Lattice web site at www.latticesemi.com.

Power Setup

The board is supplied by a single 5.0V to 28.0V DC power supply. On-board regulators will provide the necessary supply voltages. The on-board regulators supply 3.3V, 2.5V, 1.8V, 1.2V, and an adjustable voltage (VCC_ADJ). The adjustable voltage is set by the potentiometer VR1 and can be set to a value between 1.22V and 3.25V. The DC power may be applied through the power jack at J54 using an AC adapter with a 5.0V to 28.0V DC output range. Requirements for the power jack are listed in Table 1. The on/off switch (SW9) can be used as a convenience to disable power jack J54. Be sure that SW9 is in the "on" position for normal operation.

The DC power may also be applied using a workbench power supply through the banana jacks at J53 (VCC_IN) and J51 (GND). The workbench power supply voltage has to be between 5.0V and 28.0V.

Table 1. Power Jack J54 Specifications

Polarity	Positive Center
Inside Diameter	0.1" (2.5mm)
Outside Diameter	0.218" (5.5mm)
Current Capacity	Up to 4A

Power may also be supplied directly for each individual supply rail using banana jack connectors. To enable this mode of operation, the appropriate fuses must be removed. All power sources must be regulated to the specifications in Table 2. No special power sequencing is required for the evaluation board.

Table 2. Individual Control of Supplies

Supply	Jack	Fuse	Requirement
3.3V	J50	F5 (3.0A)	+/- 5%
2.5V	J41	F1 (3.0A)	+/- 5%
1.8V	J47	F3 (10.0A)	+/- 5%
1.2V	J48	F4 (3.0A)	+/- 5%
VCC_ADJ	J46	F2 (1.5A)	User-defined

Power Voltage Monitoring

A Lattice's ispPAC Power Manager II device, ispPAC-POWR1220AT8, is used for monitoring various voltages on the board. There are six LEDs used to indicate the status of the monitoring voltages. If the monitoring voltage is not in the +/- 5% voltage window, the corresponding LED will be flashing, otherwise the LED will stay ON. Table 3 shows these six voltages and the corresponding LEDs.

Table 3. Individual Monitoring of Six Power Voltages

Voltage	LED	Monitoring Voltage Range
3.3V	D5	3.3V +/- 5%
2.5V	D6	2.5V +/- 5%
1.8V	D7	1.8V +/- 5%
1.2V	D8	1.2V +/- 5%
Vref	D9	0.9V +/- 5%
Vtt	D10	0.9V +/- 5%

For the VCC_ADJ adjustable voltage, the ispPAC-POWR1220AT8 will detect the voltage rail and show the status using five LEDs. Each of these five LEDs indicates a particular voltage range. If the VCC_ADJ is in one of the voltage ranges, the corresponding LED will be turned ON and the other LEDs will be turned OFF, otherwise these five LEDs will be turned ON and then OFF sequentially so that you will see a light keep moving between the LEDs. The five LEDs and corresponding voltages are listed in Table 4.

Table 4. Monitoring of VCC_ADJ Power Voltages

LED	Indicating Voltage Range
D11	3.3V +/- 5%
D12	2.5V +/- 5%
D13	1.8V +/- 5%
D14	1.5V +/- 5%
D15	1.2V +/- 5%

LatticeXP2 I/O Bank Voltage Setting

The jumpers listed in Table 5 allow the user to select the voltage (V_{CCIO}) applied to each of the eight I/O banks of the LatticeXP2 device. Certain restrictions apply depending on which features of the board are being used.

Table 5. V_{CCIO} Selection Jumper

sysIO™ Bank	Jumper	Jumper on Pins
0	J34	1-3 -> VCC_3.3V 2-4 -> VCC_2.5V 3-5 -> VCC_1.8V 4-6 -> VCC_ADJ
6	J37	
1		VCC_2.5V
2		VCC_1.8V
3		VCC_1.8V
4		VCC_3.3V
5		VCC_3.3V
7		VCC_3.3V

Depending on the optional devices installed, some sysIO banks may have restrictions. For each of J34 and J37 only select one bank voltage position at that jumper. For example, attaching more than one jumper to J34's 6 square pins will short supplies.

Table 6. sysIO Bank Considerations

Bank	Setting
0	Selectable. CompactFlash requires 3.3V.
1	Cannot be changed
2	
3	
4	
5	
6	Selectable. Video TX/RX requires 2.5V.
7	Cannot be changed

The following tables detail the various I/O standards supported by the LatticeXP2 sysIO structures. More information can be found in technical note TN1136, LatticeXP2 sysIO Usage Guide.

Table 7. Mixed Voltage I/O Support

V_{CCIO}	Input sysIO Standards					Output sysIO Standards				
	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

For example, if V_{CCIO} is 3.3V then signals from devices powered by 1.2V, 2.5V, or 3.3V can be input and the thresholds will be correct, assuming the user has selected the desired input level using ispLEVER® software. Output levels are tied directly to V_{CCIO}.

Table 8. sysIO Standards Supported per Bank

Description	Top Side, Banks 0-1	Right Side, Banks 2-3	Bottom Side, Banks 4-5	Left Side, Banks 6-7
Types of I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Output standards supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I HSTL18_I, II SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I HSTL18 Class I, II SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I, II HSTL18D Class I, II PCI33 LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I HSTL18 Class I, II SSTL18D Class I, II SSTL25D Class I, II, SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II, SSTL33D_I, II HSTL15D Class I HSTL18D Class I, II PCI33 LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]
Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
PCI Support	PCI33 no clamp	PCI33 no clamp	PCI33 with clamp	PCI33 no clamp
LVDS Output Buffers		LVDS (3.5mA) Buffers[2]		LVDS (3.5mA) Buffers[2]

1. These differential standards are implemented by using complementary LVCMOS drivers and external resistors.
2. Available on 50% of the I/Os in the bank.

Prototype Areas

For general purpose I/O testing or monitoring, numerous test points are provided for direct access. Some test points are grouped together and arranged in a grid pattern according to their associated I/O bank and are labeled with the pin locations on the silkscreen of the board. Other test point I/Os are brought out to IDC connectors J1 and J10 with both source and end termination resistors available for high speed parallel signal transmission over ribbon cable.

Differential Signal Connections

There are four pairs of SMA connectors and one RJ-45 connector connected directly to the LatticeXP2 differential I/O pairs.

The eight SMA connectors are provided for clocks or general purpose, user-definable signals. The center pin is wired to an I/O pin and the outer case is soldered to ground. Table 9 details to which I/O pin each SMA connector is wired.

Table 9. SMA Connectors

Location	LatticeXP2 I/O	Polarity	sysIO Bank	Description
J12[1]	A2*	Pair#0 P	0	PT4A/ULC_GPLLT_IN_A
J6	B3	Pair#0 N	0	PT4B/ULC_GPLLC_IN_A
J13	F7	Pair#1 P	0	PT5A/ULC_GPLLT_FB_A
J7	G7	Pair#1 N	0	PT5B/ULC_GPLLC_FB_A
J14	P4	Pair#2 P	6	PL37A
J8	P5	Pair#2 N	6	PL37B
J15	Y1	Pair#3 P	6	PL35A
J9	AA1	Pair#3 N	6	PL35B

1. The SMA connector on J12 is shared with the on-board oscillator. When this SMA connector is used, the jumper on J17 needs to be removed.

RJ-45 Connectors

There are two RJ-45 connectors, J5 and J43, on the evaluation board. J5 is a simple RJ-45 female connector provided for general-purpose differential interfacing to the LatticeXP2 device, while J43 is a full featured Ethernet PHY connection with internal magnetics and spark gap. The connections for J5 are listed in Table 10. J43 is described in more detail in the Ethernet section later in this user guide.

Table 10. J5 RJ-45 Connections

J1 Pin	LatticeXP2 I/O	Polarity	SysIO Bank	Description
1	P2	Pair#0 P	6	PL32A
2	P3	Pair#0 N	6	PL32B
3	T1	Pair#1 P	6	PL30A/LDQS30
6	U1	Pair#1 N	6	PL30B
4	M4	Pair#2 P	6	PL28A
5	M5	Pair#2 N	6	PL28B
7	R5	Pair#3 P	6	PL40A
8	P6	Pair#3 N	6	PL40B

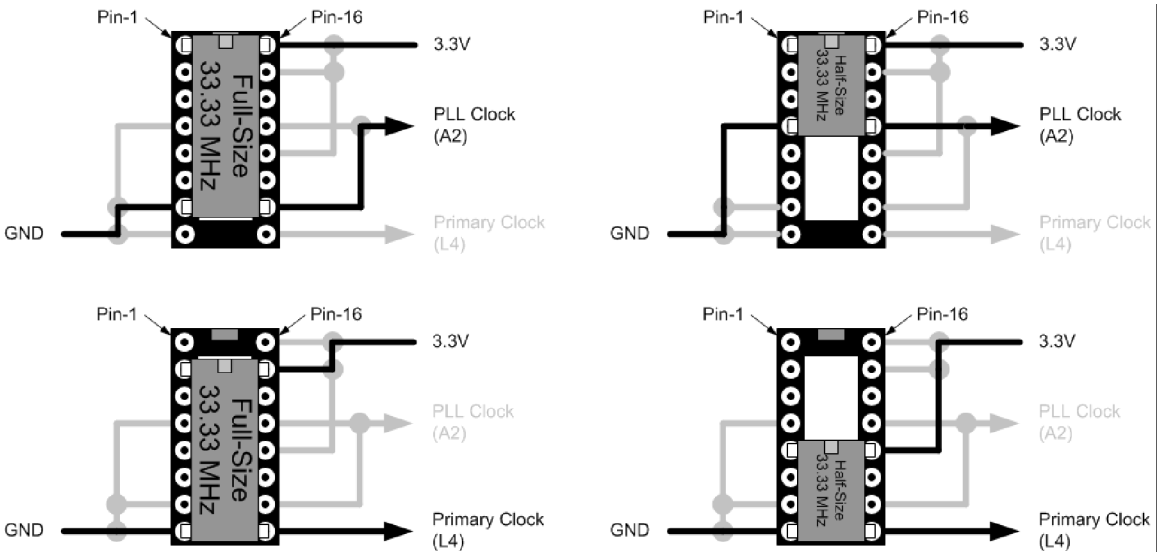
Oscillator

The 3.3V oscillator socket (Y1) accepts both full-size and half-size oscillators and can route to different clock inputs, depending on its position within the socket (see Figure 2). The board is shipped with an EPSON programmable oscillator programmed to 33.33MHz.

The 16-pin socket will allow connection to PLL clock pin A2 when the top of the oscillator is aligned to socket pins 1 and 16. Note that the SMA connector J12 is shared with the on-board oscillator. When installing the oscillator to connect the clock to PLL clock pin A2, the SMA connector J12 cannot be used and the jumper on J17 needs to be installed.

When the bottom of the oscillator is aligned to socket pins 8 and 9, the clock is provided to primary clock pin L4.

Figure 2. On-board Oscillator



SPI Serial Flash

SPI Serial Flash are available in three package styles. The device used this board is an 8-pin, 16-Mbit, sufficient to store two bitstreams simultaneously in order to support SPIm mode.

Configuration/Programming Headers

Four programming headers are provided on the evaluation board, providing access to the LatticeXP2, MachXO™, and ispPAC-POWR1220AT8 and LatticeXP2 SPI Slave JTAG ports. The JTAG connectors J25, J32, J39 and J40 are 1x10 headers. The JTAG ports for the LatticeXP2 and ispPAC-POWR1220AT8 devices can be configured as loop-through connectors to allow for easy daisy chaining of multiple boards. With proper jumper selection (see the next section) standard IDC ribbon cable can be used without the need to swap any wires on the cable.

The pinouts for these headers are provided in the following tables.

A USB ispDOWNLOAD® cable is included with each LatticeXP2 Advanced Evaluation Board. When using the 1x8 cable adapter, connect pin 1 of the cable to pin 1 of the 1x10 JTAG header.

Important Note: The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable or USB cable. Always connect an ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeXP2 FPGA and render the board inoperable.

LatticeXP2 Configuration

Two programming headers, J39 and J40, are provided on the evaluation board, providing access to the LatticeXP2 JTAG port and the ispPAC-POWR1220AT8 JTAG port. The pinouts for the headers are provided in Table 11.

Table 11. JTAG Programming Headers

Pin	Separate Programming		Chained Programming	
	Jumper on J49 (None on J45)		Jumper on J45 (None on J49)	
	J39 Function	J40 Function	J39 Function	J40 Function
1	Vcc (3.3V)	Vcc (3.3V)	Vcc (3.3V)	Not used
2	TDO of ispPAC-POWR1220AT8	TDO of LatticeXP2	TDO of ispPAC-POWR1220AT8	Not used
3	TDI of ispPAC-POWR1220AT8	TDI of LatticeXP2	TDI of LatticeXP2	Not used
4	NC	NC	NC	Not used
5	NC	NC	NC	Not used
6	TMS of both chips	TMS of both chips	TMS of both chips	Not used
7	GND	GND	GND	Not used
8	TCK of ispPAC-POWR1220AT8	TCK of LatticeXP2	TCK of both chips	Not used
9	NC	DONE of LatticeXP2	NC	Not used
10	NC	INITN of LatticeXP2	NC	Not used

J49 and J45 control the functions of the two programming headers. When a jumper is installed on J49, the programming header J39 is connected to the JTAG port of ispPAC-POWR1220AT8 and is used for programming the ispPAC-POWR1220AT8 only; the programming header J40 is connected to the JTAG port of LatticeXP2 and is used for programming the LatticeXP2 only.

When the jumper is moved from J49 to J45, the JTAG ports of the LatticeXP2 and ispPAC-POWR1220AT8 are chained together. In this case, the programming header J40 is connected to the JTAG port of the LatticeXP2 first and then chained with the JTAG port of ispPAC-POWR1220AT8. The programming header J39 should not be used when the JTAG ports are chained together. During chained programming, the ispPAC-POWR1220AT8 device will set the HVOUT1 signal (pin 86 of U17) tri-state until programming completes, so the enable for the 3.3V power for the LatticeXP2 device will be interrupted during programming unless a jumper is installed at J52. After chained programming of the ispPAC-POWR1220AT8, the jumper at J52 can be removed.

Additional instructions and recommendations for programming this board are provided in the Configuring/Programming the Board section of this document.

Switches

There are two 8-position switches and six push-button switches for implementing basic static input functions.

Switches SW3, SW4, SW5, SW6, SW7 and SW10 are momentary switches. The pull-up resistors associated with these switches are wired to 3.3V. Pushing the switches down produces a low (0), otherwise it produces a high (1). The signals controlled by SW4, SW5, SW6, SW7 and SW10 are debounced by an MC14490 (U15) before connecting to an LatticeXP2 I/O pin. Table 12 shows the control relationship between the switches, LatticeXP2 and ispPAC-POWR1220AT8 I/O pins.

Table 12. Momentary Switches

Switch	Connection	User-Definable	Debounced
SW3	Pin 97 of ispPAC-POWR1220AT8*	Yes[1]	No
SW4	J6 of LatticeXP2 (PROGRAMN)	No	Yes
SW5	E12 of LatticeXP2 (GSRN)	Yes	Yes
SW6	W18 of LatticeXP2	Yes	Yes
SW7	W17 of LatticeXP2	Yes	Yes
SW10	U7 of LatticeXP2	Yes	Yes

1. SW3 signal is also connected (wire-AND) to position#1 of SW2. Therefore, when position#1 of SW2 is in the down position, SW3 signal (POWR1220AT8 pin 97) will be low even when SW3 is not being pushed.

SW2 and SW8 on the right side and the upper side of the board are 8-pin DIP switches. The pull-up resistors associated with these switches are wired to 3.3V. A switch in the down position produces a low (0), the up position produces a high (1). All signals of SW8 are debounced before connecting to LatticeXP2 I/O pins. Table 13 shows the SW8 connections to the LatticeXP2 and Table 14 shows the SW2 connections to ispPAC-POWR1220AT8 I/O pins.

Table 13. 8-Position Switch SW8

Switch (Position#)	LatticeXP2 I/O	sysIO Bank
SW8 (position #1)	W15	4
SW8 (position #2)	U16	4
SW8 (position #3)	T16	4
SW8 (position #4)	Y15	4
SW8 (position #5)	Y16	4
SW8 (position #6)	Y18	4
SW8 (position #7)	Y17	4
SW8 (position #8)	W18	4

Table 14. 8-Position Switch SW2

Switch (Position#)	POWR1220AT8 I/O Pin	Pin Name
SW2 (position #1)	97	IN1
SW2 (position #2)	1	IN2
SW2 (position #3)	2	IN3
SW2 (position #4)	4	IN4
SW2 (position #5)	6	IN5
SW2 (position #6)	7	IN6
SW2 (position #7)	89	VPS0
SW2 (position #8)	90	VPS1

LEDs

The eight user-definable LEDs are provided on the lower right side of the board. These LEDs are each wired to a separate general purpose I/O as defined in the Table 15. The current limiting resistors associated with these LEDs are wired to 3.3V but it is safe to use any FPGA I/O voltage. The LED will light when its associated I/O pin is driven low.

Table 15. Connection between LEDs and LatticeXP2

LED	LatticeXP2 I/O	Bank	LED	LatticeXP2 I/O	Bank
D17	AB18	4	D21	Y14	4
D18	AB19	4	D22	AA13	4
D19	V12	4	D24	AB16	4
D20	U12	4	D25	AB17	4

Table 16 describes the three LEDs associated with the dedicated programming pins.

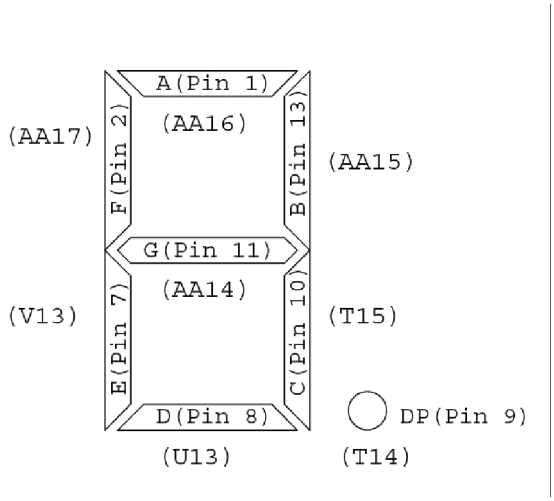
Table 16. Programming LEDs

LED	Pin	Color	Function
D27	PROGRAMN	Yellow	On when signal is low
D29	INIT	Red	On when initializing
D28	DONE	Green	On when config is complete

Seven Segment Display

The 7-segment LED located near the eight LEDs is controlled by LatticeXP2 Bank 4 I/O pins. The connections of the segments are shown in Figure 3.

Figure 3. 7-Segment Display



LCD

The LCD module connector (J55) is a 2x9 header. This 18-pin header is compatible with quite a few character LCD modules. Table 17 shows the pin function of the header and the connections to the bank 0 of the LatticeXP2 FPGA.

Table 17. LCD Header Connection

Pin #	Function	LatticeXP2 I/O	Pin #	Function	LatticeXP2 I/O
1	Anode	—	2	Cathode (GND)	—
3	VSS(GND)	—	4	VDD (5V)	—
5	VO	—	6	RS	U14
7	R/W	AA20	8	E	AA21
9	DB0	AB20	10	DB1	AA22
11	DB2	V14	12	DB3	Y21
13	DB4	W14	14	DB5	Y22
15	DB6	U15	16	DB7	V15
17	Anode	—	18	Cathode (GND)	—

The VR4 potentiometer is used to limit the current that flows through the backlight LED on the LCD module. The VR5 potentiometer is used to adjust the VO voltage that controls the LCD contrast.

When the following LCD modules are used, connect pin 1 to 16 to the backlight LCD module or connect pin 1 to 14 to the non-backlight LCD module:

Optrex:

- C-51505 Series: 20 characters x 2 lines

When the following LCD modules are used, connect pin 3 to 18 to the backlight LCD module or connect pin 3 to 16 to the non-backlight LCD module.

Lumex:

- LCM-S01601 Series: 16 characters x 1 line
- LCM-S00802 Series: 8 characters x 2 lines
- LCM-S01602 Series: 16 characters x 2 lines
- LCM-S02002 Series: 20 characters x 2 lines
- LCM-S02402 Series: 24 characters x 2 lines
- LCM-S04002 Series: 40 characters x 2 lines
- LCM-S02004 Series: 20 characters x 4 lines
- LCM-S02404 Series: 24 characters x 4 lines

Varitronix:

- MDLS-20189 Series: 20 characters x 1 line
- MDLS-20265 Series: 20 characters x 2 lines
- MDLS-24265 Series: 24 characters x 2 lines
- MDLS-40266 Series: 40 characters x 2 lines

Video TX and RX MDR Connectors

The video TX (J2) and RX (J3) MDR connectors accept 7:1 LVDS 2.5v differential video signals. The connections between the connector pins and LatticeXP2 I/O are shown in Tables 18 and 19. All the pins are connected to Bank 6 I/Os. The Bank 6 supply voltage (VCCIO_6) must be set to select 2.5V for proper LVDS 2.5V signal levels.

Table 18. Video TX MDR Connections

Pin #	Function	LatticeXP2 I/O	Pin #	Function	LatticeXP2 I/O
1	—	—	14	TX_OUT0_N	Y4
2	GND	—	15	TX_OUT0_P	AA3
3	—	—	16	—	—
4	TX_OUT1_N	U5	17	GND	—
5	TX_OUT1_P	U4	18	—	—
6	TX_OUT2_N	V3	19	GND	—
7	TX_OUT2_P	U2	20	—	—
8	—	—	21	—	—
9	—	—	22	TX_CLKOUT_N	T2
10	GND	—	23	TX_CLKOUT_P	R2
11	—	—	24	—	—
12	TX_OUT3_N	R4	25	GND	—
13	TX_OUT3_P	R3	26	—	—

Table 19. Video RX MDR Connections

Pin #	Function	LatticeXP2 I/O	Pin #	Function	LatticeXP2 I/O
1	—	—	14	RX_IN3_P	Y3
2	GND	—	15	RX_IN3_N	W3
3	—	—	16	—	—
4	RX_CLKIN_P	P1	17	GND	—
5	RX_CLKIN_N	R1	18	—	—
6	—	—	19	—	—
7	—	—	20	RX_IN2_P	R7
8	GND	—	21	RX_IN2_N	R6
9	—	—	22	RX_IN1_P	T3
10	GND	—	23	RX_IN1_N	U3
11	—	—	24	—	—
12	RX_IN0_P	T6	25	GND	—
13	RX_IN0_N	T7	26	—	—

CompactFlash

The CompactFlash connector (J38) on the board accepts both type-I and type-II CompactFlash cards. The connections between the connector pins and LatticeXP2 balls are shown in Table 20. All the pins are connected to Bank 1 I/Os.

Table 20. CompactFlash Connection

Pin #	Function	LatticeXP2 I/O	Pin #	Function	LatticeXP2 I/O
1	GND	—	26	CD1	A8
2	D3	A14	27	D11	B8
3	D4	B13	28	D12	A7
4	D5	F12	29	D13	F9
5	D6	F11	30	D14	E9
6	D7	C12	31	D15	C8
7	CE1/CS0	E11	32	CE2/CS1	D8
8	A10	A13	33	VS1	B7
9	OE/ATASEL	B12	34	IORD	B6
10	A9	A12	35	IOWR	A6
11	A8	B11	36	WE	A5
12	A7	G9	37	READY/IREQ/INTRQ	J7
13	VCC	—	38	VCC	—
14	A6	G8	39	CSEL	H7
15	A5	C11	40	VS2	C7
16	A4	D11	41	RESET	C6
17	A3	A11	42	WAIT/IORDY	A4
18	A2	A10	43	INPACK/DMARQ	A3
19	A1	B10	44	REG/DMACK	C4
20	A0	B9	45	BVD2/SPKR/DASP	C5
21	D0	E10	46	BVD1/STSCHG/PDIAG	E8
22	D1	F10	47	D8	F8
23	D2	C9	48	D9	D5

Table 20. CompactFlash Connection (Continued)

Pin #	Function	LatticeXP2 I/O	Pin #	Function	LatticeXP2 I/O
24	WP/IOIS16/IOCS16	D9	49	D10	D6
25	CD2	A9	50	GND	—

USB 1.1

For implementing the USB interface, the LatticeXP2 board contains a USB 1.1 transceiver MAX3454EETE (or NCN2500MNR2 from On Semiconductor), a type-A connector and a type-B USB connector. Note there is a third USB connector, which is used for the built-in USB download cable, described later in this document.

Table 21. Header Settings for Configuring USB Interface as USB Host

Header/Connector	Jumper Position	Description
J21	Pin 1 and 2	Drive USB transceiver ENUM pin to GND to disconnect the internal 1.5K resistor between Vtrm and D+ or D-.
J22 (D+)	Pin 1 and 2	Pull D+ signal low through an external 15K resistor.
J23 (D-)	Pin 1 and 2	Pull D- signal low through an external 15K resistor.
J24	Pin 1 and 2	Provide 5V power to the external USB device.
J16 (USB type A)	—	Type A is used while implementing USB host.
J20 (USB type B)	—	This connector is not used in this configuration.

Table 22. Header Settings for Configuring USB Interface as USB Device

Header/Connector	Jumper Position	Description
J21	Pin 2 and 3	Drive USB transceiver ENUM pin to 3.3V to connect the internal 1.5K resistor between Vtrm and D+ or D-.
J22 (D+)	Pin 2 and 3	Disconnect D+ signal from the external 15K pull-down.
J23 (D-)	Pin 2 and 3	Disconnect D- signal from the external 15K pull-down.
J24	Pin 2 and 3	No 5V power is provided when implementing USB device.
J16 (USB type A)	—	This connector is not used in this configuration.
J20 (USB type B)	—	Type A is used while implementing USB host.

The connections between the USB 1.1 transceiver MAX3454EETE (or NCN2500MNR2 from On Semiconductor) and the LatticeXP2 FPGA are shown in Table .

Table 23. Connections Between USB 1.1 Transceiver and LatticeXP2

Pin #	MAX3454EETE	NCN2500MNR2	LatticeXP2 I/O	Description
1	SPD	DSPD	D4	Connect to LatticeXP2 bank 7 I/O
2	RCV	RCV	E3	Connect to LatticeXP2 bank 7 I/O
3	VP	VP	C1	Connect to LatticeXP2 bank 7 I/O
4	VM	VM	D1	Connect to LatticeXP2 bank 7 I/O
5	NC	EN_Vobus#	—	Connect to 3.3V
6	GND	GND	—	Connect to GND
7	SUS	SPND	E1	Connect to LatticeXP2 bank 7 I/O
8	NC	NC	—	No connect
9	OE#	OE#	D3	Connect to LatticeXP2 bank 7 I/O
10	D-	D-	—	Connect to USB connectors through 33 Ohm resistor
11	D+	D+	—	Connect to USB connectors through 33 Ohm resistor
12	Vtrm	Vreg	—	Connect to GND though a capacitor

Table 23. Connections Between USB 1.1 Transceiver and LatticeXP2 (Continued)

Pin #	MAX3454EETE	NCN2500MNR2	LatticeXP2 I/O	Description
13	ENUM	Vobus	—	Connect to J21 pin 2
14	Vbus	Vusb	—	Connect to USB connectors
15	VL	Vcc	—	Connect to 3.3V
16	NC	EN_RPU	—	Connect to J21 pin 2

PS/2 Mouse

The PS/2 mouse connector (JP1) on this board connects the clock and data through the PCA9306 level translator to the LatticeXP2. The clock and data are connected as described in Table 24.

Table 24. Connections Between PS/2 Mouse Connector and LatticeXP2

JP1 Pin #	Signal	LatticeXP2 I/O	Description
1	DATA	V5	PS/2 data signal, open drain
5	CLOCK	V4	PS/2 clock signal, open drain

RS-232

The RS-232 interface on this board includes a RS-232 interface chip (MAX3232), a 9-pin D-sub female connector and four headers. This RS-232 interface can be configured to DCE or DTE by changing the jumper settings of J27, J28, J29 and J30 headers. These headers are used to connect the MAX3232 to the D-sub connector. Installing jumpers on Pin 1 and Pin 2 of these headers configures the RS-232 to DCE. Installing jumpers on Pin 2 and Pin 3 of these headers configures the RS-232 to DTE. The connections and functions of the signals between MAX3232 and LatticeXP2 stay the same for DCE and DTE configurations. These are listed in Table 25.

Table 25. Connections Between MAX3232 and LatticeXP2

Signal Name	MAX3232 Pin	LatticeXP2 I/O	LatticeXP2 Bank	LatticeXP2 I/O Type
/CTS	9 (R2OUT)	C3	7	Input
RXD	12 (R1OUT)	B2	7	Input
TXD	11 (T1IN)	B1	7	Output
/RTS	10 (T2IN)	C2	7	Output

DDR2

The 200-pin SODIMM socket provides a built-in 32-bit interface to standard 1.8V DDR2 SDRAM memory modules (PC2-5300). Lattice recommends the Kingston KVR533D284/512. However, other memories conforming to this standard will also work. The required V_{REF} and V_{TT} voltages, as well as termination of each signal to V_{TT} are provided. Performance has been verified at above the 533Mbps data rate. Write mode dynamic ODT at the memory modules is fully supported, while read mode ODT at the controller (FPGA) is approximated with external terminations optimized for best performance. The connections between the connector pins and LatticeXP2 balls are shown in Table 26.

Table 26. DDR2 Interface to SODIMM Socket

Description	LatticeXP2 I/O	sysIO Bank	J36
DDR2_DQ0	R21	3	5
DDR2_DQ1	R20	3	7
DDR2_DQ2	N17	3	17
DDR2_DQ3	N16	3	19
DDR2_DQ4	P19	3	4
DDR2_DQ5	R19	3	6

Table 26. DDR2 Interface to SODIMM Socket (Continued)

Description	LatticeXP2 I/O	sysIO Bank	J36
DDR2_DQ6	T21	3	14
DDR2_DQ7	T20	3	16
DDR2_DM0	P16	3	10
DDR2_DQS0_P	T22	3	13
DDR2_DQS0_N	U22	3	11
DDR2_DQ8	K21	3	23
DDR2_DQ9	L21	3	25
DDR2_DQ10	M19	3	35
DDR2_DQ11	M20	3	37
DDR2_DQ12	M17	3	20
DDR2_DQ13	M16	3	22
DDR2_DQ14	M21	3	36
DDR2_DQ15	N21	3	38
DDR2_DM1	P21	3	26
DDR2_DQS1_P	M22	3	31
DDR2_DQS1_N	N22	3	29
DDR2_DQ16	G21	2	43
DDR2_DQ17	F22	2	45
DDR2_DQ18	J17	2	55
DDR2_DQ19	K17	2	57
DDR2_DQ20	K18	2	44
DDR2_DQ21	L17	2	46
DDR2_DQ22	H22	2	56
DDR2_DQ23	G22	2	58
DDR2_DM2	J16	2	52
DDR2_DQS2_P	H21	2	51
DDR2_DQS2_N	J21	2	49
DDR2_DQ24	H20	2	61
DDR2_DQ25	G20	2	63
DDR2_DQ26	E19	2	73
DDR2_DQ27	F19	2	75
DDR2_DQ28	J20	2	62
DDR2_DQ29	H19	2	64
DDR2_DQ30	C22	2	74
DDR2_DQ31	B22	2	76
DDR2_DM3	H17	2	67
DDR2_DQS3_P	D22	2	70
DDR2_DQS3_N	E22	2	68
DDR2_A0	R18	3	102
DDR2_A1	R17	3	101
DDR2_A2	U21	3	100
DDR2_A3	V22	3	99
DDR2_A4	U20	3	98
DDR2_A5	V20	3	97

Table 26. DDR2 Interface to SODIMM Socket (Continued)

Description	LatticeXP2 I/O	sysIO Bank	J36
DDR2_A6	R16	3	94
DDR2_A7	T17	3	92
DDR2_A8	Y20	3	93
DDR2_A9	Y19	3	91
DDR2_A10	W22	3	105
DDR2_A11	G15	2	90
DDR2_A12	G16	2	89
DDR2_A13	F17	2	116
DDR_BA0	P20	3	107
DDR_BA1	P22	3	106
DDR_BA2	F18	2	85
DDR2_CK0_P	G17	2	30
DDR2_CK0_N	H18	2	32
DDR2_CK1_P	B21	2	164
DDR2_CK1_N	C21	2	166
DDR2_CKE0	J19	2	79
DDR2_CKE1	C20	2	80
DDR2_S0_N	J18	2	110
DDR2_S1_N	H16	2	115
DDR2_RAS_N	K16	2	108
DDR2_CAS_N	L18	2	113
DDR2_WE_N	L19	2	109
DDR2_ODT0	P18	3	114
DDR2_ODT1	N18	3	119
DDR2_SDA	AA2	0	195
DDR2_SCL	Y2	0	197

Ethernet PHY

In the upper middle portion of the board is U11, a National Semiconductor Gigabit Ethernet PHY (DP83865). The LatticeXP2 FPGA interacts with the PHY over a Media Independent Interface (MII). The PHY is connected to an RJ45 connector J43 on the Media Dependent Interface (MDI). The RJ45 connector J43 has built in magnetics and spark-gap capacitor.

The PHY is available on the board in order to demonstrate the Lattice Ethernet Media Access (MAC) IP core. However, it is also possible to use the PHY to evaluate a custom MAC solution.

Refer to the schematic and the National Semiconductor DP83865 Data Sheet for detailed information about the operation of the Ethernet PHY interface on this device. Refer to Table 27 for a description of the Ethernet PHY connections.

Table 27. 10/100/1000 Ethernet PHY Connection Summary

Description	LatticeXP2 I/O	sysIO Bank
ETH_CLK_TO_MAC	G11	1
ETH_COL	A17	1
ETH_CRS	B16	1
ETH_EGP0	(low, install R91 to pull high)	--
ETH_EGP2	G13	1
ETH_EGP4	G14	1
ETH_EGP5	D12	1
ETH_EGP6	B14	1
ETH_EGP7	A15	1
ETH_GTX_CLK	D15	1
ETH_MAC_CLK_EN	G10	1
ETH_MDC	E15	1
ETH_MDIO	E14	1
ETH_RESET_N	A16	1
ETH_RX_CLK	B15	1
ETH_RX_D0	F14	1
ETH_RX_D1	D14	1
ETH_RX_D2	C16	1
ETH_RX_D3	C17	1
ETH_RX_D4	B17	1
ETH_RX_D5	A18	1
ETH_RX_D6	F13	1
ETH_RX_D7	G12	1
ETH_RX_DV	C14	1
ETH_RX_ER	E13	1
ETH_TX_CLK	C15	1
ETH_TX_D0	D17	1
ETH_TX_D1	E18	1
ETH_TX_D2	C18	1
ETH_TX_D3	C19	1
ETH_TX_D4	A20	1
ETH_TX_D5	D19	1
ETH_TX_D6	D17	1
ETH_TX_D7	D18	1
ETH_TX_EN	A19	1
ETH_TX_ER	A21	1

PCI Connection

The 124-pin PCI connector installed at the bottom-left corner of the board is used for 32-bit PCI. With this PCI connector, PCI IP and proper LatticeXP2 FPGA design, the LatticeXP2 Advanced Evaluation board can be used in a PCI slot on a PC motherboard. There are two sides to the PCI connector, component side (J11) and solder side (J56). Refer to Tables 28 and 29 for a description of the PCI connections where the I/O direction is referenced to the LatticeXP2 Advanced Evaluation Board.

Table 28. PCI Connector Component Side

J11 Pin#	Signal	I/O	Description	LatticeXP2 Connection
1	12V	Vcc	12V voltage supply pin	—
2	TCK	-	PCI JTAG TCK signal	—
3	GND	Vss	System ground	GND
4	TDO	-	JTAG TDO signal	—
5	5V	Vcc	5V voltage supply pin	—
6	5V	Vcc	5V voltage supply pin	—
7	INTB#	O	PCI INTB# signal	—
8	INTD#	O	PCI INTD# signal	—
9	PRSNT1#	O	PCI PRSNT1# signal	—
10	Reserved	-	Reserved	—
11	PRSNT2#	O	PCI PRSNT2# signal	—
14	Reserved	-	Reserved	—
15	GND	Vss	System ground	GND
16	CLK	I	PCI system clock	AB14
17	GND	Vss	System ground	GND
18	REQ#	O	PCI arbitration request signal	W5
19	+VIO	Vio	VIO voltage supply pin	—
20	AD[31]	I/O	PCI address and bit 31	Y5
21	AD[29]	I/O	PCI address and data bit 29	Y6
22	GND	Vss	System ground	GND
23	AD[27]	I/O	PCI address and data bit 27	AB6
24	AD[25]	I/O	PCI address and data bit 25	AA7
25	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
26	C/BE#[3]	I/O	PCI bus command, byte enable, bit 3	Y8
27	AD[23]	I/O	PCI address and data bit 23	W4
28	GND	Vss	System ground	GND
29	AD[21]	I/O	PCI address and data bit 21	W6
30	AD[19]	I/O	PCI address and data bit 19	U8
31	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
32	AD[17]	I/O	PCI address and data bit 17	W8
33	C/BE#[2]	I/O	PCI bus command, byte enable, bit 2	V9
34	GND	Vss	System ground	GND
35	IRDY#	I/O	PCI initiator ready signal	T10
36	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
37	DEVSEL#	I/O	PCI device select	T9
38	GND	Vss	System ground	GND
39	LOCK#	I/O	PCI lock signal	-
40	PERR#	I/O	PCI parity error signal	V10
41	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
42	SERR#	I/O	PCI system error signal	V11
43	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
44	C/BE#[1]	I/O	PCI bus command, byte enable, bit 1	T12
45	AD[14]	I/O	PCI address and data bit 14	T13
46	GND	Vss	System ground	GND

Table 28. PCI Connector Component Side (Continued)

J11 Pin#	Signal	I/O	Description	LatticeXP2 Connection
47	AD[12]	I/O	PCI address and data bit 12	AA9
48	AD[10]	I/O	PCI address and data bit 10	Y9
49	M66EN	O	PCI 66 MHz enable	—
52	AD[8]	I/O	PCI address and data bit 8	AB11
53	AD[7]	I/O	PCI address and data bit 7	AA11
54	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
55	AD[5]	I/O	PCI address and data bit 5	AB12
56	AD[3]	I/O	PCI address and data bit 3	AB13
57	GND	Vss	System ground	GND
58	AD[1]	I/O	PCI address and data bit 1	Y12
59	+VIO	Vio	VIO voltage supply pin	—
60	ACK64#	I/O	PCI 64-bit acknowledge pin	—
61	+5V	Vcc	5V voltage supply pin	—
62	+5V	Vcc	5V voltage supply pin	—

Table 29. PCI Connector Solder Side

J56 Pin#	Signal	I/O	Description	LatticeXP2 Connection
1	TRST#	I	PCI JTAG TRST# signal	—
2	+12V	Vcc	12V voltage supply pin	—
3	TMS	I	PCI JTAG TMS signal	—
4	TDI	I	JTAG TDI signal	—
5	+5V	Vcc	5V voltage supply pin	—
6	INTA#	O	PCI INTA# signal	AB2
7	INTC#	O	PCI INTC# signal	—
8	+5V	Vcc	5V voltage supply pin	—
9	Reserved	—	Reserved	—
10	VIO	Vio	VIO voltage supply pin	—
11	Reserved	—	Reserved	—
14	+3.3V AUX	Vcca	3.3V auxiliary voltage supply	—
15	RST#	I	PCI system reset	AB3
16	VIO	Vio	VIO voltage supply pin	—
17	GNT#	I	PCI arbitration grant	AB4
18	GND	Vss	System ground	GND
19	PME#	—		—
20	AD[30]	I/O	PCI address and data bit 30	AB5
21	+3.3V	Vcc	3.3V voltage supply	+3.3V
22	AD[28]	I/O	PCI address and data bit 28	AA6
23	AD[26]	I/O	PCI address and data bit 26	Y7
24	GND	Vss	System ground	GND
25	AD[24]	I/O	PCI address and data bit 24	AB7
26	IDSEL	I	PCI interface control, ID select	AA8
27	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
28	AD[22]	I/O	PCI address and data bit 22	V6
29	AD[20]	I/O	PCI address and data bit 20	U6

Table 29. PCI Connector Solder Side (Continued)

J56 Pin#	Signal	I/O	Description	LatticeXP2 Connection
30	GND	Vss	System ground	GND
31	AD[18]	I/O	PCI address and data bit 18	V8
32	AD[16]	I/O	PCI address and data bit 16	U9
33	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
34	FRAME#	I/O	PCI interface control FRAME# signal	W9
35	GND	Vss	System ground	GND
36	TRDY#	I/O	PCI interface control TRDY# signal	T8
37	GND	Vss	System ground	GND
38	STOP#	I/O	PCI interface control STOP# signal	T11
39	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
40	Reserved	—	Reserved	—
41	Reserved	—	Reserved	—
42	GND	Vss	System ground	GND
43	PAR	I/O	PCI address and data PAR signal	U10
44	AD[15]	I/O	PCI address and data bit 15	U11
45	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
46	AD[13]	I/O	PCI address and data bit 13	AB8
47	AD[11]	I/O	PCI address and data bit 11	AB9
48	GND	Vss	System ground	GND
49	AD[9]	I/O	PCI address and data bit 9	AB10
52	C/BE#[0]	I/O	PCI bus command, byte enable, bit 0	AA10
53	+3.3V	Vcc	3.3V voltage supply pin	+3.3V
54	AD[6]	I/O	PCI address and data bit 6	Y11
55	AD[4]	I/O	PCI address and data bit 4	W11
56	GND	Vss	System ground	GND
57	AD[2]	I/O	PCI address and data bit 2	AB15
58	AD[0]	I/O	PCI address and data bit 0	AA12
59	+VIO	Vio	VIO voltage supply pin	—
60	REQ64#	I/O	PCI 64-bit request transfer pin	—
61	+5V	Vcc	5V voltage supply pin	—
62	+5V	Vcc	5V voltage supply pin	—

4-Input ADC

U3 is the quad ADC (Analog to Digital Converter) ADS7842 IC. The four analog inputs AIN0 to AIN3 are RC filtered versions of the external analog signals applied at J10. The full scale values for the ADC inputs will match that of the AREF signal described below. AIN3 is also tied to VR1 to allow user adjustment of a set DC value based on the AREF signal described below. The connections between the ADC pins and LatticeXP2 balls are shown in Table 30.

Table 30. ADC Connections

Description	LatticeXP2 I/O	sysIO Bank
D0	H3	7
D1	H4	7
D2	G3	7
D3	G2	7
D4	H1	7
D5	H2	7
D6	G6	7
D7	H6	7
D8	H5	7
D9	J5	7
D10	J1	7
D11	J2	7
A0	F3	7
A1	E5	7
CLK	F2	7
BUSYN	F1	7
WRN	G1	7
CSN	F5	7
RDN	F4	7

4-Output DAC

U5 is the quad DAC (Digital to Analog Converter) DAC7617 IC. The four analog outputs, AOUT0 to AOUT3, are available at connector J10. The full scale values for the DAC outputs will match that of the AREF signal described below. The connections between the DAC pins and LatticeXP2 balls are shown in Table 31.

Table 31. DAC Connections

Description	LatticeXP2 I/O	sysIO Bank
RSTN	K1	7
LOADREGN	K2	7
LDACN	J4	7
CSN	M1	7
CLK	M2	7
SDI	L3	7

The AREF signal is used by both the ADC and DAC as the full scale voltage reference. The AREF signal can be selected from three different sources: a low drift band gap voltage provided at U2, the power supply voltage VCC_3.3v, or an externally applied voltage at jumper J4 pin 2. J4 allows selection of which voltage will be the source of the AREF signal as shown in Table 32.

Table 32. DAC and ADC Full Scale Reference Selection (AREF)

J4 Jumper Position	AREF Source	ADC and DAC Usage
1-2	VCC_3.3v	Full scale values track 3.3v power
2-3	Band gap reference	Full scale values track low drift reference
open	J4 pin 2	Full scale values track external voltage

USB Download

The evaluation board has a USB download cable built in. The built-in cable consists of a USB Type-B connector (J33), a USB microcontroller, and a MachXO device.

To use the built-in download cable, simply connect a standard USB cable from J33 to your PC (with ispVM System software installed). The USB hub on the PC will detect the addition of the USB function making the built-in cable available for use with Lattice's ispVM System software. J35 must have a jumper shunted from pins 2-3 to enable the built-in download cable.

The built-in USB cable is connected in parallel to J39 and J40. J39 and J40 are 1x10 100mil headers that are provided for use with an external Lattice download cable. A Lattice parallel port or USB download cable can be attached to the board using J39 or J40.

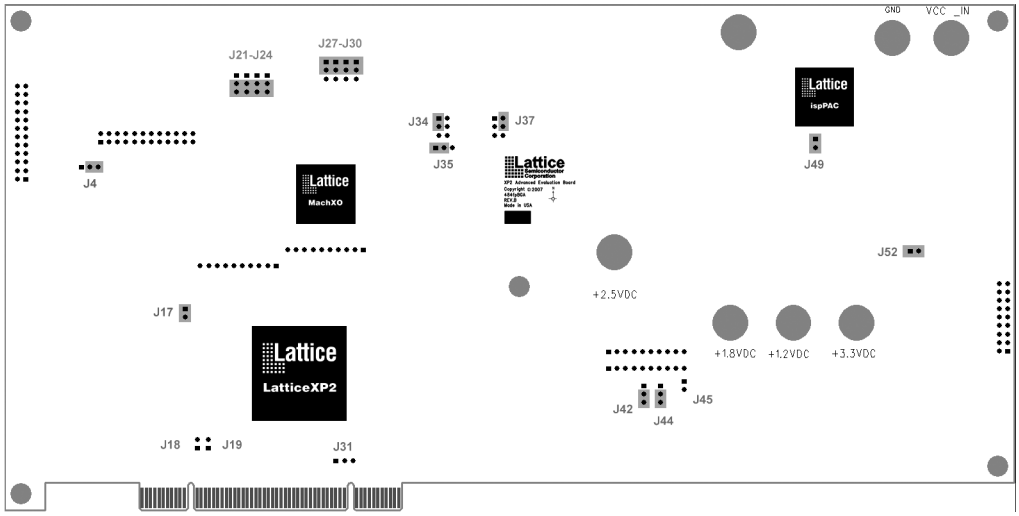
Use of the built-in cable must be mutually exclusive to the use of an external download cable. When using an external download cable, the jumper on J35 must be moved to shunt pins 1 and 2. This tri-states the MachXO device, preventing it from interfering with the external download cable.

Important Note: The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable or USB cable. Always connect an ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeXP2 FPGA and render the board inoperable.

Default Jumper Settings

The evaluation board is shipped with default jumper positions as shown in Figure 4. Some jumper settings are required for bitstream downloading and display functionality.

Figure 4. Default Jumper Settings



Configuring/Programming the Board

Requirements:

- PC with Lattice's ispVM System version 17.0 (or later) programming software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). *Note: An option to install these drivers is included as part of the ispVM System setup.*
- Standard USB cable, or any ispDOWNLOAD or Lattice USB Cable (pDS4102-DL2x, HW7265-DL3x, HW-USB-2x, etc.).

The following device programming sections provide procedures for programming the on-board SPI Flash using either a standard USB cable, or an ispDOWNLOAD cable (parallel or USB). If you would like to program the LatticeXP2 SRAM or Flash directly instead, then the procedures are slightly different in that you will select those rather than SPI Flash programming at Step 7, Figure 6 in the first procedure below, and much the same for the second configuration procedure.

For a complete discussion of the LatticeXP2's configuration and programming options, refer to technical note TN1141, LatticeXP2 sysCONFIG Usage Guide.

LatticeXP2 SRAM Configuration Using SPI Flash and a Standard USB Cable at J33

The LatticeXP2 SRAM can be configured easily via the on-board SPI Flash using the USB Download port at J33 and ispVM. The LatticeXP2 device is SRAM-based, so it must remain powered on to retain its configuration when programming the SRAM. The on-board SPI Flash retains its programmed bitstreams when power is off, and can quickly load programmed bitstreams into the LatticeXP2 device when power is applied.

1. Attach a ground connection from the test equipment chassis ground to the black GND terminal J51.
2. Check that the jumpers are installed as shown in Figure 4. Now move the J35 jumper from the left-side two pins to be on the right-side two pins.
3. Connect the LatticeXP2 Evaluation Board to an external 5V supply.
4. Push the SW1 USB Download reset button located just above the MachXO device (U9). Connect a standard USB cable from your PC's USB connector to the USB download connector J33 on the LatticeXP2 Advanced Evaluation Board.
5. Start the ispVM System software, then select **Options > Cable and I/O Port Setup...**, then check that the Cable Type is set to **USB**.

   *Note: If you receive a Windows notification about installing a USB driver, then in ispVM System select **ISPTOOLS** and **INSTALL/UNINSTALL LSC USB/PARALLEL PORT DRIVER...**, then select the **LSC WINDOWS USB DRIVER**, and push the **INSTALL** button. Now push the **SW1 USB Download reset button** located just above the MachXO device (U9). Windows should recognize the USB cable to the LatticeXP2 Advanced Evaluation Board.*
6. Press the **SCAN** button located in the toolbar. The LatticeXP2 device will be automatically detected. The resulting screen will be similar to Figure 5. If offered multiple LatticeXP2 device types, select the LFXP2-17E.

Figure 5. ispVM System Interface

7. Left-click on the **LFXP2-17E** device line and if offered other selections, select the **LFXP2-17E**, and leave that line selected. Now, in the ispVM main menu select **Edit > EDIT_DEVICE** and a Device Information window will